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### Understanding [Embedded - FPGAs \(Field Programmable Gate Array\)](#)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

### Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

#### Details

|                                |                                                                                                                                     |
|--------------------------------|-------------------------------------------------------------------------------------------------------------------------------------|
| Product Status                 | Obsolete                                                                                                                            |
| Number of LABs/CLBs            | 128300                                                                                                                              |
| Number of Logic Elements/Cells | 340000                                                                                                                              |
| Total RAM Bits                 | 19456000                                                                                                                            |
| Number of I/O                  | 696                                                                                                                                 |
| Number of Gates                | -                                                                                                                                   |
| Voltage - Supply               | 0.82V ~ 0.88V                                                                                                                       |
| Mounting Type                  | Surface Mount                                                                                                                       |
| Operating Temperature          | 0°C ~ 85°C (TJ)                                                                                                                     |
| Package / Case                 | 1517-BBGA, FCBGA                                                                                                                    |
| Supplier Device Package        | 1517-FBGA (40x40)                                                                                                                   |
| Purchase URL                   | <a href="https://www.e-xfl.com/product-detail/intel/5sgxea3k1f40c2l">https://www.e-xfl.com/product-detail/intel/5sgxea3k1f40c2l</a> |

**Table 7. Recommended Transceiver Power Supply Operating Conditions for Stratix V GX, GS, and GT Devices (Part 2 of 2)**

| Symbol                 | Description                                                  | Devices    | Minimum <sup>(4)</sup> | Typical | Maximum <sup>(4)</sup> | Unit |
|------------------------|--------------------------------------------------------------|------------|------------------------|---------|------------------------|------|
| $V_{CCR\_GXBR}$<br>(2) | Receiver analog power supply (right side)                    | GX, GS, GT | 0.82                   | 0.85    | 0.88                   | V    |
|                        |                                                              |            | 0.87                   | 0.90    | 0.93                   |      |
|                        |                                                              |            | 0.97                   | 1.0     | 1.03                   |      |
|                        |                                                              |            | 1.03                   | 1.05    | 1.07                   |      |
| $V_{CCR\_GTBR}$        | Receiver analog power supply for GT channels (right side)    | GT         | 1.02                   | 1.05    | 1.08                   | V    |
| $V_{CCT\_GXBL}$<br>(2) | Transmitter analog power supply (left side)                  | GX, GS, GT | 0.82                   | 0.85    | 0.88                   | V    |
|                        |                                                              |            | 0.87                   | 0.90    | 0.93                   |      |
|                        |                                                              |            | 0.97                   | 1.0     | 1.03                   |      |
|                        |                                                              |            | 1.03                   | 1.05    | 1.07                   |      |
| $V_{CCT\_GXBR}$<br>(2) | Transmitter analog power supply (right side)                 | GX, GS, GT | 0.82                   | 0.85    | 0.88                   | V    |
|                        |                                                              |            | 0.87                   | 0.90    | 0.93                   |      |
|                        |                                                              |            | 0.97                   | 1.0     | 1.03                   |      |
|                        |                                                              |            | 1.03                   | 1.05    | 1.07                   |      |
| $V_{CCT\_GTBR}$        | Transmitter analog power supply for GT channels (right side) | GT         | 1.02                   | 1.05    | 1.08                   | V    |
| $V_{CCL\_GTBR}$        | Transmitter clock network power supply                       | GT         | 1.02                   | 1.05    | 1.08                   | V    |
| $V_{CCH\_GXBL}$        | Transmitter output buffer power supply (left side)           | GX, GS, GT | 1.425                  | 1.5     | 1.575                  | V    |
| $V_{CCH\_GXBR}$        | Transmitter output buffer power supply (right side)          | GX, GS, GT | 1.425                  | 1.5     | 1.575                  | V    |

**Notes to Table 7:**

- (1) This supply must be connected to 3.0 V if the CMU PLL, receiver CDR, or both, are configured at a base data rate > 6.5 Gbps. Up to 6.5 Gbps, you can connect this supply to either 3.0 V or 2.5 V.
- (2) Refer to Table 8 to select the correct power supply level for your design.
- (3) When using ATX PLLs, the supply must be 3.0 V.
- (4) This value describes the budget for the DC (static) power supply tolerance and does not include the dynamic tolerance requirements. Refer to the PDN tool for the additional budget for the dynamic tolerance requirements.

### I/O Pin Leakage Current

Table 9 lists the Stratix V I/O pin leakage current specifications.

**Table 9. I/O Pin Leakage Current for Stratix V Devices <sup>(1)</sup>**

| Symbol   | Description        | Conditions                          | Min | Typ | Max | Unit          |
|----------|--------------------|-------------------------------------|-----|-----|-----|---------------|
| $I_I$    | Input pin          | $V_I = 0 \text{ V to } V_{CCIOMAX}$ | -30 | —   | 30  | $\mu\text{A}$ |
| $I_{OZ}$ | Tri-stated I/O pin | $V_O = 0 \text{ V to } V_{CCIOMAX}$ | -30 | —   | 30  | $\mu\text{A}$ |

**Note to Table 9:**

(1) If  $V_O = V_{CCIO}$  to  $V_{CCIOMAX}$ , 100  $\mu\text{A}$  of leakage current per I/O is expected.

### Bus Hold Specifications

Table 10 lists the Stratix V device family bus hold specifications.

**Table 10. Bus Hold Parameters for Stratix V Devices**

| Parameter               | Symbol            | Conditions                                     | V <sub>CCIO</sub> |      |       |      |       |      |       |      |       |      | Unit |
|-------------------------|-------------------|------------------------------------------------|-------------------|------|-------|------|-------|------|-------|------|-------|------|------|
|                         |                   |                                                | 1.2 V             |      | 1.5 V |      | 1.8 V |      | 2.5 V |      | 3.0 V |      |      |
|                         |                   |                                                | Min               | Max  | Min   | Max  | Min   | Max  | Min   | Max  | Min   | Max  |      |
| Low sustaining current  | I <sub>SUSL</sub> | V <sub>IN</sub> > V <sub>IL</sub><br>(maximum) | 22.5              | —    | 25.0  | —    | 30.0  | —    | 50.0  | —    | 70.0  | —    | μA   |
| High sustaining current | I <sub>SUSH</sub> | V <sub>IN</sub> < V <sub>IH</sub><br>(minimum) | −22.5             | —    | −25.0 | —    | −30.0 | —    | −50.0 | —    | −70.0 | —    | μA   |
| Low overdrive current   | I <sub>ODL</sub>  | 0V < V <sub>IN</sub> < V <sub>CCIO</sub>       | —                 | 120  | —     | 160  | —     | 200  | —     | 300  | —     | 500  | μA   |
| High overdrive current  | I <sub>ODH</sub>  | 0V < V <sub>IN</sub> < V <sub>CCIO</sub>       | —                 | −120 | —     | −160 | —     | −200 | —     | −300 | —     | −500 | μA   |
| Bus-hold trip point     | V <sub>TRIP</sub> | —                                              | 0.45              | 0.95 | 0.50  | 1.00 | 0.68  | 1.07 | 0.70  | 1.70 | 0.80  | 2.00 | V    |

### On-Chip Termination (OCT) Specifications

If you enable OCT calibration, calibration is automatically performed at power-up for I/Os connected to the calibration block. Table 11 lists the Stratix V OCT termination calibration accuracy specifications.

**Table 11. OCT Calibration Accuracy Specifications for Stratix V Devices <sup>(1)</sup> (Part 1 of 2)**

| Symbol             | Description                                                         | Conditions                                     | Calibration Accuracy |          |                |          | Unit |
|--------------------|---------------------------------------------------------------------|------------------------------------------------|----------------------|----------|----------------|----------|------|
|                    |                                                                     |                                                | C1                   | C2,I2    | C3,I3,<br>I3YY | C4,I4    |      |
| 25- $\Omega$ $R_S$ | Internal series termination with calibration (25- $\Omega$ setting) | $V_{CCIO} = 3.0, 2.5, 1.8, 1.5, 1.2 \text{ V}$ | $\pm 15$             | $\pm 15$ | $\pm 15$       | $\pm 15$ | %    |

**Table 12. OCT Without Calibration Resistance Tolerance Specifications for Stratix V Devices (Part 2 of 2)**

| Symbol               | Description                                                    | Conditions                        | Resistance Tolerance |        |              |        | Unit |
|----------------------|----------------------------------------------------------------|-----------------------------------|----------------------|--------|--------------|--------|------|
|                      |                                                                |                                   | C1                   | C2, I2 | C3, I3, I3YY | C4, I4 |      |
| 50-Ω R <sub>S</sub>  | Internal series termination without calibration (50-Ω setting) | V <sub>CCIO</sub> = 1.8 and 1.5 V | ±30                  | ±30    | ±40          | ±40    | %    |
| 50-Ω R <sub>S</sub>  | Internal series termination without calibration (50-Ω setting) | V <sub>CCIO</sub> = 1.2 V         | ±35                  | ±35    | ±50          | ±50    | %    |
| 100-Ω R <sub>D</sub> | Internal differential termination (100-Ω setting)              | V <sub>CCPD</sub> = 2.5 V         | ±25                  | ±25    | ±25          | ±25    | %    |

Calibration accuracy for the calibrated series and parallel OCTs are applicable at the moment of calibration. When voltage and temperature conditions change after calibration, the tolerance may change.

OCT calibration is automatically performed at power-up for OCT-enabled I/Os. Table 13 lists the OCT variation with temperature and voltage after power-up calibration. Use Table 13 to determine the OCT variation after power-up calibration and Equation 1 to determine the OCT variation without recalibration.

**Equation 1. OCT Variation Without Recalibration for Stratix V Devices <sup>(1), (2), (3), (4), (5), (6)</sup>**

$$R_{OCT} = R_{SCAL} \left( 1 + \left\langle \frac{dR}{dT} \times \Delta T \right\rangle \pm \left\langle \frac{dR}{dV} \times \Delta V \right\rangle \right)$$

**Notes to Equation 1:**

- (1) The R<sub>OCT</sub> value shows the range of OCT resistance with the variation of temperature and V<sub>CCIO</sub>.
- (2) R<sub>SCAL</sub> is the OCT resistance value at power-up.
- (3) ΔT is the variation of temperature with respect to the temperature at power-up.
- (4) ΔV is the variation of voltage with respect to the V<sub>CCIO</sub> at power-up.
- (5) dR/dT is the percentage change of R<sub>SCAL</sub> with temperature.
- (6) dR/dV is the percentage change of R<sub>SCAL</sub> with voltage.

Table 13 lists the on-chip termination variation after power-up calibration.

**Table 13. OCT Variation after Power-Up Calibration for Stratix V Devices (Part 1 of 2) <sup>(1)</sup>**

| Symbol | Description                                      | V <sub>CCIO</sub> (V) | Typical | Unit   |
|--------|--------------------------------------------------|-----------------------|---------|--------|
| dR/dV  | OCT variation with voltage without recalibration | 3.0                   | 0.0297  | % / mV |
|        |                                                  | 2.5                   | 0.0344  |        |
|        |                                                  | 1.8                   | 0.0499  |        |
|        |                                                  | 1.5                   | 0.0744  |        |
|        |                                                  | 1.2                   | 0.1241  |        |

## Internal Weak Pull-Up Resistor

Table 16 lists the weak pull-up resistor values for Stratix V devices.

**Table 16. Internal Weak Pull-Up Resistor for Stratix V Devices <sup>(1), (2)</sup>**

| Symbol          | Description                                                                                                                                         | V <sub>CCIO</sub> Conditions (V) <sup>(3)</sup> | Value <sup>(4)</sup> | Unit |
|-----------------|-----------------------------------------------------------------------------------------------------------------------------------------------------|-------------------------------------------------|----------------------|------|
| R <sub>PU</sub> | Value of the I/O pin pull-up resistor before and during configuration, as well as user mode if you enable the programmable pull-up resistor option. | 3.0 ±5%                                         | 25                   | kΩ   |
|                 |                                                                                                                                                     | 2.5 ±5%                                         | 25                   | kΩ   |
|                 |                                                                                                                                                     | 1.8 ±5%                                         | 25                   | kΩ   |
|                 |                                                                                                                                                     | 1.5 ±5%                                         | 25                   | kΩ   |
|                 |                                                                                                                                                     | 1.35 ±5%                                        | 25                   | kΩ   |
|                 |                                                                                                                                                     | 1.25 ±5%                                        | 25                   | kΩ   |
|                 |                                                                                                                                                     | 1.2 ±5%                                         | 25                   | kΩ   |

### Notes to Table 16:

- (1) All I/O pins have an option to enable the weak pull-up resistor except the configuration, test, and JTAG pins.
- (2) The internal weak pull-down feature is only available for the JTAG TCK pin. The typical value for this internal weak pull-down resistor is approximately 25 kΩ.
- (3) The pin pull-up resistance values may be lower if an external source drives the pin higher than V<sub>CCIO</sub>.
- (4) These specifications are valid with a ±10% tolerance to cover changes over PVT.

## I/O Standard Specifications

Table 17 through Table 22 list the input voltage (V<sub>IH</sub> and V<sub>IL</sub>), output voltage (V<sub>OH</sub> and V<sub>OL</sub>), and current drive characteristics (I<sub>OH</sub> and I<sub>OL</sub>) for various I/O standards supported by Stratix V devices. These tables also show the Stratix V device family I/O standard specifications. The V<sub>OL</sub> and V<sub>OH</sub> values are valid at the corresponding I<sub>OH</sub> and I<sub>OL</sub>, respectively.

For an explanation of the terms used in Table 17 through Table 22, refer to “Glossary” on page 65. For tolerance calculations across all SSTL and HSTL I/O standards, refer to Altera knowledge base solution rd07262012\_486.

**Table 17. Single-Ended I/O Standards for Stratix V Devices**

| I/O Standard | V <sub>CCIO</sub> (V) |     |       | V <sub>IL</sub> (V) |                             | V <sub>IH</sub> (V)         |                         | V <sub>OL</sub> (V)         | V <sub>OH</sub> (V)         | I <sub>OL</sub> (mA) | I <sub>OH</sub> (mA) |
|--------------|-----------------------|-----|-------|---------------------|-----------------------------|-----------------------------|-------------------------|-----------------------------|-----------------------------|----------------------|----------------------|
|              | Min                   | Typ | Max   | Min                 | Max                         | Min                         | Max                     | Max                         | Min                         |                      |                      |
| LVTTTL       | 2.85                  | 3   | 3.15  | −0.3                | 0.8                         | 1.7                         | 3.6                     | 0.4                         | 2.4                         | 2                    | −2                   |
| LVC MOS      | 2.85                  | 3   | 3.15  | −0.3                | 0.8                         | 1.7                         | 3.6                     | 0.2                         | V <sub>CCIO</sub> − 0.2     | 0.1                  | −0.1                 |
| 2.5 V        | 2.375                 | 2.5 | 2.625 | −0.3                | 0.7                         | 1.7                         | 3.6                     | 0.4                         | 2                           | 1                    | −1                   |
| 1.8 V        | 1.71                  | 1.8 | 1.89  | −0.3                | 0.35 *<br>V <sub>CCIO</sub> | 0.65 *<br>V <sub>CCIO</sub> | V <sub>CCIO</sub> + 0.3 | 0.45                        | V <sub>CCIO</sub> − 0.45    | 2                    | −2                   |
| 1.5 V        | 1.425                 | 1.5 | 1.575 | −0.3                | 0.35 *<br>V <sub>CCIO</sub> | 0.65 *<br>V <sub>CCIO</sub> | V <sub>CCIO</sub> + 0.3 | 0.25 *<br>V <sub>CCIO</sub> | 0.75 *<br>V <sub>CCIO</sub> | 2                    | −2                   |
| 1.2 V        | 1.14                  | 1.2 | 1.26  | −0.3                | 0.35 *<br>V <sub>CCIO</sub> | 0.65 *<br>V <sub>CCIO</sub> | V <sub>CCIO</sub> + 0.3 | 0.25 *<br>V <sub>CCIO</sub> | 0.75 *<br>V <sub>CCIO</sub> | 2                    | −2                   |

**Table 19. Single-Ended SSTL, HSTL, and HSUL I/O Standards Signal Specifications for Stratix V Devices (Part 2 of 2)**

| I/O Standard     | $V_{IL(DC)} (V)$ |                  | $V_{IH(DC)} (V)$ |                   | $V_{IL(AC)} (V)$ | $V_{IH(AC)} (V)$ | $V_{OL} (V)$      | $V_{OH} (V)$      | $I_{ol} (mA)$ | $I_{oh} (mA)$ |
|------------------|------------------|------------------|------------------|-------------------|------------------|------------------|-------------------|-------------------|---------------|---------------|
|                  | Min              | Max              | Min              | Max               | Max              | Min              | Max               | Min               |               |               |
| HSTL-18 Class I  | —                | $V_{REF} - 0.1$  | $V_{REF} + 0.1$  | —                 | $V_{REF} - 0.2$  | $V_{REF} + 0.2$  | 0.4               | $V_{CCIO} - 0.4$  | 8             | -8            |
| HSTL-18 Class II | —                | $V_{REF} - 0.1$  | $V_{REF} + 0.1$  | —                 | $V_{REF} - 0.2$  | $V_{REF} + 0.2$  | 0.4               | $V_{CCIO} - 0.4$  | 16            | -16           |
| HSTL-15 Class I  | —                | $V_{REF} - 0.1$  | $V_{REF} + 0.1$  | —                 | $V_{REF} - 0.2$  | $V_{REF} + 0.2$  | 0.4               | $V_{CCIO} - 0.4$  | 8             | -8            |
| HSTL-15 Class II | —                | $V_{REF} - 0.1$  | $V_{REF} + 0.1$  | —                 | $V_{REF} - 0.2$  | $V_{REF} + 0.2$  | 0.4               | $V_{CCIO} - 0.4$  | 16            | -16           |
| HSTL-12 Class I  | -0.15            | $V_{REF} - 0.08$ | $V_{REF} + 0.08$ | $V_{CCIO} + 0.15$ | $V_{REF} - 0.15$ | $V_{REF} + 0.15$ | $0.25^* V_{CCIO}$ | $0.75^* V_{CCIO}$ | 8             | -8            |
| HSTL-12 Class II | -0.15            | $V_{REF} - 0.08$ | $V_{REF} + 0.08$ | $V_{CCIO} + 0.15$ | $V_{REF} - 0.15$ | $V_{REF} + 0.15$ | $0.25^* V_{CCIO}$ | $0.75^* V_{CCIO}$ | 16            | -16           |
| HSUL-12          | —                | $V_{REF} - 0.13$ | $V_{REF} + 0.13$ | —                 | $V_{REF} - 0.22$ | $V_{REF} + 0.22$ | $0.1^* V_{CCIO}$  | $0.9^* V_{CCIO}$  | —             | —             |

**Table 20. Differential SSTL I/O Standards for Stratix V Devices**

| I/O Standard         | $V_{CCIO} (V)$ |      |       | $V_{SWING(DC)} (V)$ |                  | $V_{X(AC)} (V)$      |              |                      | $V_{SWING(AC)} (V)$       |                           |
|----------------------|----------------|------|-------|---------------------|------------------|----------------------|--------------|----------------------|---------------------------|---------------------------|
|                      | Min            | Typ  | Max   | Min                 | Max              | Min                  | Typ          | Max                  | Min                       | Max                       |
| SSTL-2 Class I, II   | 2.375          | 2.5  | 2.625 | 0.3                 | $V_{CCIO} + 0.6$ | $V_{CCIO}/2 - 0.2$   | —            | $V_{CCIO}/2 + 0.2$   | 0.62                      | $V_{CCIO} + 0.6$          |
| SSTL-18 Class I, II  | 1.71           | 1.8  | 1.89  | 0.25                | $V_{CCIO} + 0.6$ | $V_{CCIO}/2 - 0.175$ | —            | $V_{CCIO}/2 + 0.175$ | 0.5                       | $V_{CCIO} + 0.6$          |
| SSTL-15 Class I, II  | 1.425          | 1.5  | 1.575 | 0.2                 | (1)              | $V_{CCIO}/2 - 0.15$  | —            | $V_{CCIO}/2 + 0.15$  | 0.35                      | —                         |
| SSTL-135 Class I, II | 1.283          | 1.35 | 1.45  | 0.2                 | (1)              | $V_{CCIO}/2 - 0.15$  | $V_{CCIO}/2$ | $V_{CCIO}/2 + 0.15$  | $2(V_{IH(AC)} - V_{REF})$ | $2(V_{IL(AC)} - V_{REF})$ |
| SSTL-125 Class I, II | 1.19           | 1.25 | 1.31  | 0.18                | (1)              | $V_{CCIO}/2 - 0.15$  | $V_{CCIO}/2$ | $V_{CCIO}/2 + 0.15$  | $2(V_{IH(AC)} - V_{REF})$ | —                         |
| SSTL-12 Class I, II  | 1.14           | 1.2  | 1.26  | 0.18                | —                | $V_{REF} - 0.15$     | $V_{CCIO}/2$ | $V_{REF} + 0.15$     | -0.30                     | 0.30                      |

**Note to Table 20:**

(1) The maximum value for  $V_{SWING(DC)}$  is not defined. However, each single-ended signal needs to be within the respective single-ended limits ( $V_{IH(DC)}$  and  $V_{IL(DC)}$ ).

**Table 21. Differential HSTL and HSUL I/O Standards for Stratix V Devices (Part 1 of 2)**

| I/O Standard        | $V_{CCIO} (V)$ |     |       | $V_{DIF(DC)} (V)$ |     | $V_{X(AC)} (V)$ |     |      | $V_{CM(DC)} (V)$ |     |      | $V_{DIF(AC)} (V)$ |     |
|---------------------|----------------|-----|-------|-------------------|-----|-----------------|-----|------|------------------|-----|------|-------------------|-----|
|                     | Min            | Typ | Max   | Min               | Max | Min             | Typ | Max  | Min              | Typ | Max  | Min               | Max |
| HSTL-18 Class I, II | 1.71           | 1.8 | 1.89  | 0.2               | —   | 0.78            | —   | 1.12 | 0.78             | —   | 1.12 | 0.4               | —   |
| HSTL-15 Class I, II | 1.425          | 1.5 | 1.575 | 0.2               | —   | 0.68            | —   | 0.9  | 0.68             | —   | 0.9  | 0.4               | —   |

-  You typically use the interactive Excel-based Early Power Estimator before designing the FPGA to get a magnitude estimate of the device power. The Quartus II PowerPlay Power Analyzer provides better quality estimates based on the specifics of the design after you complete place-and-route. The PowerPlay Power Analyzer can apply a combination of user-entered, simulation-derived, and estimated signal activities that, when combined with detailed circuit models, yields very accurate power estimates.
-  For more information about power estimation tools, refer to the *PowerPlay Early Power Estimator User Guide* and the *PowerPlay Power Analysis* chapter in the *Quartus II Handbook*.

**Table 23. Transceiver Specifications for Stratix V GX and GS Devices <sup>(1)</sup> (Part 2 of 7)**

| Symbol/<br>Description                                             | Conditions                                             | Transceiver Speed<br>Grade 1     |                   |      | Transceiver Speed<br>Grade 2     |                   |      | Transceiver Speed<br>Grade 3     |                       |      | Unit        |
|--------------------------------------------------------------------|--------------------------------------------------------|----------------------------------|-------------------|------|----------------------------------|-------------------|------|----------------------------------|-----------------------|------|-------------|
|                                                                    |                                                        | Min                              | Typ               | Max  | Min                              | Typ               | Max  | Min                              | Typ                   | Max  |             |
| Spread-spectrum<br>downspread                                      | PCIe                                                   | —                                | 0 to<br>-0.5      | —    | —                                | 0 to<br>-0.5      | —    | —                                | 0 to<br>-0.5          | —    | %           |
| On-chip<br>termination<br>resistors <sup>(21)</sup>                | —                                                      | —                                | 100               | —    | —                                | 100               | —    | —                                | 100                   | —    | $\Omega$    |
| Absolute $V_{MAX}$ <sup>(5)</sup>                                  | Dedicated<br>reference<br>clock pin                    | —                                | —                 | 1.6  | —                                | —                 | 1.6  | —                                | —                     | 1.6  | V           |
|                                                                    | RX reference<br>clock pin                              | —                                | —                 | 1.2  | —                                | —                 | 1.2  | —                                | —                     | 1.2  |             |
| Absolute $V_{MIN}$                                                 | —                                                      | -0.4                             | —                 | —    | -0.4                             | —                 | —    | -0.4                             | —                     | —    | V           |
| Peak-to-peak<br>differential input<br>voltage                      | —                                                      | 200                              | —                 | 1600 | 200                              | —                 | 1600 | 200                              | —                     | 1600 | mV          |
| $V_{ICM}$ (AC<br>coupled) <sup>(3)</sup>                           | Dedicated<br>reference<br>clock pin                    | 1050/1000/900/850 <sup>(2)</sup> |                   |      | 1050/1000/900/850 <sup>(2)</sup> |                   |      | 1050/1000/900/850 <sup>(2)</sup> |                       |      | mV          |
|                                                                    | RX reference<br>clock pin                              | 1.0/0.9/0.85 <sup>(4)</sup>      |                   |      | 1.0/0.9/0.85 <sup>(4)</sup>      |                   |      | 1.0/0.9/0.85 <sup>(4)</sup>      |                       |      | V           |
| $V_{ICM}$ (DC coupled)                                             | HCSL I/O<br>standard for<br>PCIe<br>reference<br>clock | 250                              | —                 | 550  | 250                              | —                 | 550  | 250                              | —                     | 550  | mV          |
| Transmitter<br>REFCLK Phase<br>Noise<br>(622 MHz) <sup>(20)</sup>  | 100 Hz                                                 | —                                | —                 | -70  | —                                | —                 | -70  | —                                | —                     | -70  | dBc/Hz      |
|                                                                    | 1 kHz                                                  | —                                | —                 | -90  | —                                | —                 | -90  | —                                | —                     | -90  | dBc/Hz      |
|                                                                    | 10 kHz                                                 | —                                | —                 | -100 | —                                | —                 | -100 | —                                | —                     | -100 | dBc/Hz      |
|                                                                    | 100 kHz                                                | —                                | —                 | -110 | —                                | —                 | -110 | —                                | —                     | -110 | dBc/Hz      |
|                                                                    | $\geq 1$ MHz                                           | —                                | —                 | -120 | —                                | —                 | -120 | —                                | —                     | -120 | dBc/Hz      |
| Transmitter<br>REFCLK Phase<br>Jitter<br>(100 MHz) <sup>(17)</sup> | 10 kHz to<br>1.5 MHz<br>(PCIe)                         | —                                | —                 | 3    | —                                | —                 | 3    | —                                | —                     | 3    | ps<br>(rms) |
| $R_{REF}$ <sup>(19)</sup>                                          | —                                                      | —                                | 1800<br>$\pm 1\%$ | —    | —                                | 1800<br>$\pm 1\%$ | —    | —                                | 180<br>0<br>$\pm 1\%$ | —    | $\Omega$    |
| <b>Transceiver Clocks</b>                                          |                                                        |                                  |                   |      |                                  |                   |      |                                  |                       |      |             |
| fixedclk clock<br>frequency                                        | PCIe<br>Receiver<br>Detect                             | —                                | 100<br>or<br>125  | —    | —                                | 100<br>or<br>125  | —    | —                                | 100<br>or<br>125      | —    | MHz         |



**Table 23. Transceiver Specifications for Stratix V GX and GS Devices <sup>(1)</sup> (Part 3 of 7)**

| Symbol/<br>Description                                                                                                                               | Conditions                                                   | Transceiver Speed<br>Grade 1                         |     |       | Transceiver Speed<br>Grade 2 |     |       | Transceiver Speed<br>Grade 3 |     |                                     | Unit |
|------------------------------------------------------------------------------------------------------------------------------------------------------|--------------------------------------------------------------|------------------------------------------------------|-----|-------|------------------------------|-----|-------|------------------------------|-----|-------------------------------------|------|
|                                                                                                                                                      |                                                              | Min                                                  | Typ | Max   | Min                          | Typ | Max   | Min                          | Typ | Max                                 |      |
| Reconfiguration clock<br>( <code>mgmt_clk_clk</code> )<br>frequency                                                                                  | —                                                            | 100                                                  | —   | 125   | 100                          | —   | 125   | 100                          | —   | 125                                 | MHz  |
| <b>Receiver</b>                                                                                                                                      |                                                              |                                                      |     |       |                              |     |       |                              |     |                                     |      |
| Supported I/O Standards                                                                                                                              | —                                                            | 1.4-V PCML, 1.5-V PCML, 2.5-V PCML, LVPECL, and LVDS |     |       |                              |     |       |                              |     |                                     |      |
| Data rate<br>(Standard PCS)<br><sup>(9), (23)</sup>                                                                                                  | —                                                            | 600                                                  | —   | 12200 | 600                          | —   | 12200 | 600                          | —   | 8500/<br>10312.5<br><sup>(24)</sup> | Mbps |
| Data rate<br>(10G PCS) <sup>(9), (23)</sup>                                                                                                          | —                                                            | 600                                                  | —   | 14100 | 600                          | —   | 12500 | 600                          | —   | 8500/<br>10312.5<br><sup>(24)</sup> | Mbps |
| Absolute $V_{MAX}$ for<br>a receiver pin <sup>(5)</sup>                                                                                              | —                                                            | —                                                    | —   | 1.2   | —                            | —   | 1.2   | —                            | —   | 1.2                                 | V    |
| Absolute $V_{MIN}$ for<br>a receiver pin                                                                                                             | —                                                            | −0.4                                                 | —   | —     | −0.4                         | —   | —     | −0.4                         | —   | —                                   | V    |
| Maximum peak-<br>to-peak<br>differential input<br>voltage $V_{ID}$ (diff p-<br>p) before device<br>configuration <sup>(22)</sup>                     | —                                                            | —                                                    | —   | 1.6   | —                            | —   | 1.6   | —                            | —   | 1.6                                 | V    |
| Maximum peak-<br>to-peak<br>differential input<br>voltage $V_{ID}$ (diff p-<br>p) after device<br>configuration <sup>(18)</sup> ,<br><sup>(22)</sup> | $V_{CCR\_GXB} =$<br>1.0 V/1.05 V<br>( $V_{ICM} =$<br>0.70 V) | —                                                    | —   | 2.0   | —                            | —   | 2.0   | —                            | —   | 2.0                                 | V    |
|                                                                                                                                                      | $V_{CCR\_GXB} =$<br>0.90 V<br>( $V_{ICM} = 0.6$ V)           | —                                                    | —   | 2.4   | —                            | —   | 2.4   | —                            | —   | 2.4                                 | V    |
|                                                                                                                                                      | $V_{CCR\_GXB} =$<br>0.85 V<br>( $V_{ICM} = 0.6$ V)           | —                                                    | —   | 2.4   | —                            | —   | 2.4   | —                            | —   | 2.4                                 | V    |
| Minimum<br>differential eye<br>opening at<br>receiver serial<br>input pins <sup>(6)</sup> , <sup>(22)</sup> ,<br><sup>(27)</sup>                     | —                                                            | 85                                                   | —   | —     | 85                           | —   | —     | 85                           | —   | —                                   | mV   |

**Table 23. Transceiver Specifications for Stratix V GX and GS Devices <sup>(1)</sup> (Part 6 of 7)**

| Symbol/<br>Description                                                | Conditions                                   | Transceiver Speed<br>Grade 1 |     |                               | Transceiver Speed<br>Grade 2 |     |                               | Transceiver Speed<br>Grade 3 |     |                               | Unit |
|-----------------------------------------------------------------------|----------------------------------------------|------------------------------|-----|-------------------------------|------------------------------|-----|-------------------------------|------------------------------|-----|-------------------------------|------|
|                                                                       |                                              | Min                          | Typ | Max                           | Min                          | Typ | Max                           | Min                          | Typ | Max                           |      |
| Inter-transceiver<br>block transmitter<br>channel-to-<br>channel skew | xN PMA<br>bonded mode                        | —                            | —   | 500                           | —                            | —   | 500                           | —                            | —   | 500                           | ps   |
| <b>CMU PLL</b>                                                        |                                              |                              |     |                               |                              |     |                               |                              |     |                               |      |
| Supported Data<br>Range                                               | —                                            | 600                          | —   | 12500                         | 600                          | —   | 12500                         | 600                          | —   | 8500/<br>10312.5<br>(24)      | Mbps |
| t <sub>pll_powerdown</sub> <sup>(15)</sup>                            | —                                            | 1                            | —   | —                             | 1                            | —   | —                             | 1                            | —   | —                             | μs   |
| t <sub>pll_lock</sub> <sup>(16)</sup>                                 | —                                            | —                            | —   | 10                            | —                            | —   | 10                            | —                            | —   | 10                            | μs   |
| <b>ATX PLL</b>                                                        |                                              |                              |     |                               |                              |     |                               |                              |     |                               |      |
| Supported Data<br>Rate Range                                          | VCO<br>post-divider<br>L=2                   | 8000                         | —   | 14100                         | 8000                         | —   | 12500                         | 8000                         | —   | 8500/<br>10312.5<br>(24)      | Mbps |
|                                                                       | L=4                                          | 4000                         | —   | 7050                          | 4000                         | —   | 6600                          | 4000                         | —   | 6600                          | Mbps |
|                                                                       | L=8                                          | 2000                         | —   | 3525                          | 2000                         | —   | 3300                          | 2000                         | —   | 3300                          | Mbps |
|                                                                       | L=8,<br>Local/Central<br>Clock Divider<br>=2 | 1000                         | —   | 1762.5                        | 1000                         | —   | 1762.5                        | 1000                         | —   | 1762.5                        | Mbps |
| t <sub>pll_powerdown</sub> <sup>(15)</sup>                            | —                                            | 1                            | —   | —                             | 1                            | —   | —                             | 1                            | —   | —                             | μs   |
| t <sub>pll_lock</sub> <sup>(16)</sup>                                 | —                                            | —                            | —   | 10                            | —                            | —   | 10                            | —                            | —   | 10                            | μs   |
| <b>fPLL</b>                                                           |                                              |                              |     |                               |                              |     |                               |                              |     |                               |      |
| Supported Data<br>Range                                               | —                                            | 600                          | —   | 3250/<br>3125 <sup>(25)</sup> | 600                          | —   | 3250/<br>3125 <sup>(25)</sup> | 600                          | —   | 3250/<br>3125 <sup>(25)</sup> | Mbps |
| t <sub>pll_powerdown</sub> <sup>(15)</sup>                            | —                                            | 1                            | —   | —                             | 1                            | —   | —                             | 1                            | —   | —                             | μs   |

Table 26 shows the approximate maximum data rate using the 10G PCS.

**Table 26. Stratix V 10G PCS Approximate Maximum Data Rate <sup>(1)</sup>**

| Mode <sup>(2)</sup> | Transceiver Speed Grade | PMA Width                             | 64           | 40    | 40    | 40   | 32       | 32    |
|---------------------|-------------------------|---------------------------------------|--------------|-------|-------|------|----------|-------|
|                     |                         | PCS Width                             | 64           | 66/67 | 50    | 40   | 64/66/67 | 32    |
| FIFO or Register    | 1                       | C1, C2, C2L, I2, I2L core speed grade | 14.1         | 14.1  | 10.69 | 14.1 | 13.6     | 13.6  |
|                     | 2                       | C1, C2, C2L, I2, I2L core speed grade | 12.5         | 12.5  | 10.69 | 12.5 | 12.5     | 12.5  |
|                     |                         | C3, I3, I3L core speed grade          | 12.5         | 12.5  | 10.69 | 12.5 | 10.88    | 10.88 |
|                     | 3                       | C1, C2, C2L, I2, I2L core speed grade | 8.5 Gbps     |       |       |      |          |       |
|                     |                         | C3, I3, I3L core speed grade          |              |       |       |      |          |       |
|                     |                         | C4, I4 core speed grade               |              |       |       |      |          |       |
|                     |                         | I3YY core speed grade                 | 10.3125 Gbps |       |       |      |          |       |

**Notes to Table 26:**

- (1) The maximum data rate is in Gbps.
- (2) The Phase Compensation FIFO can be configured in FIFO mode or register mode. In the FIFO mode, the pointers are not fixed, and the latency can vary. In the register mode the pointers are fixed for low latency.

**Table 28. Transceiver Specifications for Stratix V GT Devices (Part 4 of 5) <sup>(1)</sup>**

| Symbol/<br>Description                                             | Conditions                                   | Transceiver<br>Speed Grade 2 |     |                                | Transceiver<br>Speed Grade 3 |     |                                | Unit |
|--------------------------------------------------------------------|----------------------------------------------|------------------------------|-----|--------------------------------|------------------------------|-----|--------------------------------|------|
|                                                                    |                                              | Min                          | Typ | Max                            | Min                          | Typ | Max                            |      |
| Data rate                                                          | GT channels                                  | 19,600                       | —   | 28,050                         | 19,600                       | —   | 25,780                         | Mbps |
| Differential on-chip<br>termination resistors                      | GT channels                                  | —                            | 100 | —                              | —                            | 100 | —                              | Ω    |
|                                                                    | GX channels                                  | (8)                          |     |                                |                              |     |                                |      |
| V <sub>OCM</sub> (AC coupled)                                      | GT channels                                  | —                            | 500 | —                              | —                            | 500 | —                              | mV   |
|                                                                    | GX channels                                  | (8)                          |     |                                |                              |     |                                |      |
| Rise/Fall time                                                     | GT channels                                  | —                            | 15  | —                              | —                            | 15  | —                              | ps   |
|                                                                    | GX channels                                  | (8)                          |     |                                |                              |     |                                |      |
| Intra-differential pair<br>skew                                    | GX channels                                  | (8)                          |     |                                |                              |     |                                |      |
| Intra-transceiver block<br>transmitter channel-to-<br>channel skew | GX channels                                  | (8)                          |     |                                |                              |     |                                |      |
| Inter-transceiver block<br>transmitter channel-to-<br>channel skew | GX channels                                  | (8)                          |     |                                |                              |     |                                |      |
| CMU PLL                                                            |                                              |                              |     |                                |                              |     |                                |      |
| Supported Data Range                                               | —                                            | 600                          | —   | 12500                          | 600                          | —   | 8500                           | Mbps |
| t <sub>pll_powerdown</sub> <sup>(13)</sup>                         | —                                            | 1                            | —   | —                              | 1                            | —   | —                              | μs   |
| t <sub>pll_lock</sub> <sup>(14)</sup>                              | —                                            | —                            | —   | 10                             | —                            | —   | 10                             | μs   |
| ATX PLL                                                            |                                              |                              |     |                                |                              |     |                                |      |
| Supported Data Rate<br>Range for GX Channels                       | VCO post-<br>divider L=2                     | 8000                         | —   | 12500                          | 8000                         | —   | 8500                           | Mbps |
|                                                                    | L=4                                          | 4000                         | —   | 6600                           | 4000                         | —   | 6600                           | Mbps |
|                                                                    | L=8                                          | 2000                         | —   | 3300                           | 2000                         | —   | 3300                           | Mbps |
|                                                                    | L=8,<br>Local/Central<br>Clock Divider<br>=2 | 1000                         | —   | 1762.5                         | 1000                         | —   | 1762.5                         | Mbps |
| Supported Data Rate<br>Range for GT Channels                       | VCO post-<br>divider L=2                     | 9800                         | —   | 14025                          | 9800                         | —   | 12890                          | Mbps |
| t <sub>pll_powerdown</sub> <sup>(13)</sup>                         | —                                            | 1                            | —   | —                              | 1                            | —   | —                              | μs   |
| t <sub>pll_lock</sub> <sup>(14)</sup>                              | —                                            | —                            | —   | 10                             | —                            | —   | 10                             | μs   |
| fPLL                                                               |                                              |                              |     |                                |                              |     |                                |      |
| Supported Data Range                                               | —                                            | 600                          | —   | 3250/<br>3.125 <sup>(23)</sup> | 600                          | —   | 3250/<br>3.125 <sup>(23)</sup> | Mbps |
| t <sub>pll_powerdown</sub> <sup>(13)</sup>                         | —                                            | 1                            | —   | —                              | 1                            | —   | —                              | μs   |

Figure 4 shows the differential transmitter output waveform.

**Figure 4. Differential Transmitter/Receiver Output/Input Waveform**

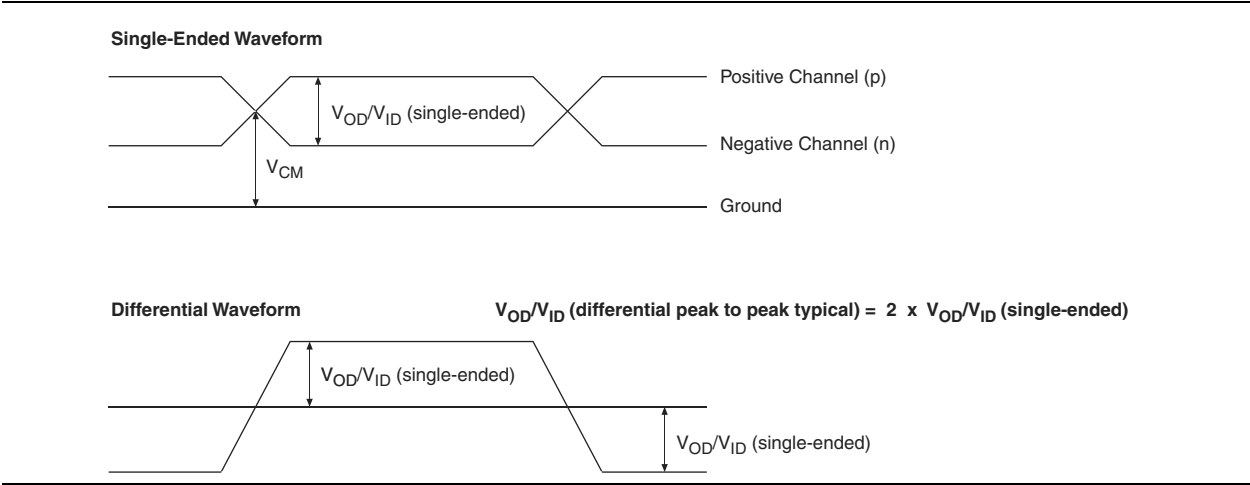


Figure 5 shows the Stratix V AC gain curves for GT channels.

**Figure 5. AC Gain Curves for GT Channels**

- XFI
- ASI
- HiGig/HiGig+
- HiGig2/HiGig2+
- Serial Data Converter (SDC)
- GPON
- SDI
- SONET
- Fibre Channel (FC)
- PCIe
- QPI
- SFF-8431

Download the Stratix V Characterization Report Tool to view the characterization report summary for these protocols.

## Core Performance Specifications

This section describes the clock tree, phase-locked loop (PLL), digital signal processing (DSP), memory blocks, configuration, and JTAG specifications.

### Clock Tree Specifications

Table 30 lists the clock tree specifications for Stratix V devices.

**Table 30. Clock Tree Performance for Stratix V Devices <sup>(1)</sup>**

| Symbol                    | Performance              |                       |        | Unit |
|---------------------------|--------------------------|-----------------------|--------|------|
|                           | C1, C2, C2L, I2, and I2L | C3, I3, I3L, and I3YY | C4, I4 |      |
| Global and Regional Clock | 717                      | 650                   | 580    | MHz  |
| Periphery Clock           | 550                      | 500                   | 500    | MHz  |

**Note to Table 30:**

(1) The Stratix V ES devices are limited to 600 MHz core clock tree performance.

**Table 31. PLL Specifications for Stratix V Devices (Part 2 of 3)**

| Symbol                                             | Parameter                                                                                                    | Min  | Typ     | Max                                          | Unit      |
|----------------------------------------------------|--------------------------------------------------------------------------------------------------------------|------|---------|----------------------------------------------|-----------|
| $t_{\text{INCCJ}}$ <sup>(3), (4)</sup>             | Input clock cycle-to-cycle jitter ( $f_{\text{REF}} \geq 100$ MHz)                                           | —    | —       | 0.15                                         | UI (p-p)  |
|                                                    | Input clock cycle-to-cycle jitter ( $f_{\text{REF}} < 100$ MHz)                                              | −750 | —       | +750                                         | ps (p-p)  |
| $t_{\text{OUTPJ\_DC}}$ <sup>(5)</sup>              | Period Jitter for dedicated clock output ( $f_{\text{OUT}} \geq 100$ MHz)                                    | —    | —       | 175 <sup>(1)</sup>                           | ps (p-p)  |
|                                                    | Period Jitter for dedicated clock output ( $f_{\text{OUT}} < 100$ MHz)                                       | —    | —       | 17.5 <sup>(1)</sup>                          | mUI (p-p) |
| $t_{\text{FOUTPJ\_DC}}$ <sup>(5)</sup>             | Period Jitter for dedicated clock output in fractional PLL ( $f_{\text{OUT}} \geq 100$ MHz)                  | —    | —       | 250 <sup>(11)</sup> ,<br>175 <sup>(12)</sup> | ps (p-p)  |
|                                                    | Period Jitter for dedicated clock output in fractional PLL ( $f_{\text{OUT}} < 100$ MHz)                     | —    | —       | 25 <sup>(11)</sup> ,<br>17.5 <sup>(12)</sup> | mUI (p-p) |
| $t_{\text{OUTCCJ\_DC}}$ <sup>(5)</sup>             | Cycle-to-Cycle Jitter for a dedicated clock output ( $f_{\text{OUT}} \geq 100$ MHz)                          | —    | —       | 175                                          | ps (p-p)  |
|                                                    | Cycle-to-Cycle Jitter for a dedicated clock output ( $f_{\text{OUT}} < 100$ MHz)                             | —    | —       | 17.5                                         | mUI (p-p) |
| $t_{\text{FOUTCCJ\_DC}}$ <sup>(5)</sup>            | Cycle-to-cycle Jitter for a dedicated clock output in fractional PLL ( $f_{\text{OUT}} \geq 100$ MHz)        | —    | —       | 250 <sup>(11)</sup> ,<br>175 <sup>(12)</sup> | ps (p-p)  |
|                                                    | Cycle-to-cycle Jitter for a dedicated clock output in fractional PLL ( $f_{\text{OUT}} < 100$ MHz)+          | —    | —       | 25 <sup>(11)</sup> ,<br>17.5 <sup>(12)</sup> | mUI (p-p) |
| $t_{\text{OUTPJ\_IO}}$ <sup>(5), (8)</sup>         | Period Jitter for a clock output on a regular I/O in integer PLL ( $f_{\text{OUT}} \geq 100$ MHz)            | —    | —       | 600                                          | ps (p-p)  |
|                                                    | Period Jitter for a clock output on a regular I/O ( $f_{\text{OUT}} < 100$ MHz)                              | —    | —       | 60                                           | mUI (p-p) |
| $t_{\text{FOUTPJ\_IO}}$ <sup>(5), (8), (11)</sup>  | Period Jitter for a clock output on a regular I/O in fractional PLL ( $f_{\text{OUT}} \geq 100$ MHz)         | —    | —       | 600 <sup>(10)</sup>                          | ps (p-p)  |
|                                                    | Period Jitter for a clock output on a regular I/O in fractional PLL ( $f_{\text{OUT}} < 100$ MHz)            | —    | —       | 60 <sup>(10)</sup>                           | mUI (p-p) |
| $t_{\text{OUTCCJ\_IO}}$ <sup>(5), (8)</sup>        | Cycle-to-cycle Jitter for a clock output on a regular I/O in integer PLL ( $f_{\text{OUT}} \geq 100$ MHz)    | —    | —       | 600                                          | ps (p-p)  |
|                                                    | Cycle-to-cycle Jitter for a clock output on a regular I/O in integer PLL ( $f_{\text{OUT}} < 100$ MHz)       | —    | —       | 60 <sup>(10)</sup>                           | mUI (p-p) |
| $t_{\text{FOUTCCJ\_IO}}$ <sup>(5), (8), (11)</sup> | Cycle-to-cycle Jitter for a clock output on a regular I/O in fractional PLL ( $f_{\text{OUT}} \geq 100$ MHz) | —    | —       | 600 <sup>(10)</sup>                          | ps (p-p)  |
|                                                    | Cycle-to-cycle Jitter for a clock output on a regular I/O in fractional PLL ( $f_{\text{OUT}} < 100$ MHz)    | —    | —       | 60                                           | mUI (p-p) |
| $t_{\text{CASC\_OUTPJ\_DC}}$ <sup>(5), (6)</sup>   | Period Jitter for a dedicated clock output in cascaded PLLs ( $f_{\text{OUT}} \geq 100$ MHz)                 | —    | —       | 175                                          | ps (p-p)  |
|                                                    | Period Jitter for a dedicated clock output in cascaded PLLs ( $f_{\text{OUT}} < 100$ MHz)                    | —    | —       | 17.5                                         | mUI (p-p) |
| $f_{\text{DRIFT}}$                                 | Frequency drift after PFDENA is disabled for a duration of 100 $\mu$ s                                       | —    | —       | $\pm 10$                                     | %         |
| $dK_{\text{BIT}}$                                  | Bit number of Delta Sigma Modulator (DSM)                                                                    | 8    | 24      | 32                                           | Bits      |
| $k_{\text{VALUE}}$                                 | Numerator of Fraction                                                                                        | 128  | 8388608 | 2147483648                                   | —         |

**Table 36. High-Speed I/O Specifications for Stratix V Devices <sup>(1), (2)</sup> (Part 2 of 4)**

| Symbol                                                                                                                           | Conditions                                                                    | C1  |     |      | C2, C2L, I2, I2L |     |      | C3, I3, I3L, I3YY |     |      | C4,I4 |     |      | Unit |
|----------------------------------------------------------------------------------------------------------------------------------|-------------------------------------------------------------------------------|-----|-----|------|------------------|-----|------|-------------------|-----|------|-------|-----|------|------|
|                                                                                                                                  |                                                                               | Min | Typ | Max  | Min              | Typ | Max  | Min               | Typ | Max  | Min   | Typ | Max  |      |
| Transmitter                                                                                                                      |                                                                               |     |     |      |                  |     |      |                   |     |      |       |     |      |      |
| True Differential I/O Standards - f <sub>HSDR</sub> (data rate)                                                                  | SERDES factor J = 3 to 10 <sup>(9), (11), (12), (13), (14), (15), (16)</sup>  | (6) | —   | 1600 | (6)              | —   | 1434 | (6)               | —   | 1250 | (6)   | —   | 1050 | Mbps |
|                                                                                                                                  | SERDES factor J ≥ 4<br><br>LVDS TX with DPA <sup>(12), (14), (15), (16)</sup> | (6) | —   | 1600 | (6)              | —   | 1600 | (6)               | —   | 1600 | (6)   | —   | 1250 | Mbps |
|                                                                                                                                  | SERDES factor J = 2, uses DDR Registers                                       | (6) | —   | (7)  | (6)              | —   | (7)  | (6)               | —   | (7)  | (6)   | —   | (7)  | Mbps |
|                                                                                                                                  | SERDES factor J = 1, uses SDR Register                                        | (6) | —   | (7)  | (6)              | —   | (7)  | (6)               | —   | (7)  | (6)   | —   | (7)  | Mbps |
| Emulated Differential I/O Standards with Three External Output Resistor Networks - f <sub>HSDR</sub> (data rate) <sup>(10)</sup> | SERDES factor J = 4 to 10 <sup>(17)</sup>                                     | (6) | —   | 1100 | (6)              | —   | 1100 | (6)               | —   | 840  | (6)   | —   | 840  | Mbps |
| t <sub>x Jitter</sub> - True Differential I/O Standards                                                                          | Total Jitter for Data Rate 600 Mbps - 1.25 Gbps                               | —   | —   | 160  | —                | —   | 160  | —                 | —   | 160  | —     | —   | 160  | ps   |
|                                                                                                                                  | Total Jitter for Data Rate < 600 Mbps                                         | —   | —   | 0.1  | —                | —   | 0.1  | —                 | —   | 0.1  | —     | —   | 0.1  | UI   |
| t <sub>x Jitter</sub> - Emulated Differential I/O Standards with Three External Output Resistor Network                          | Total Jitter for Data Rate 600 Mbps - 1.25 Gbps                               | —   | —   | 300  | —                | —   | 300  | —                 | —   | 300  | —     | —   | 325  | ps   |
|                                                                                                                                  | Total Jitter for Data Rate < 600 Mbps                                         | —   | —   | 0.2  | —                | —   | 0.2  | —                 | —   | 0.2  | —     | —   | 0.25 | UI   |



**Table 36. High-Speed I/O Specifications for Stratix V Devices <sup>(1)</sup>, <sup>(2)</sup> (Part 3 of 4)**

| Symbol                                                      | Conditions                                                                                                                          | C1             |     |                | C2, C2L, I2, I2L |     |                | C3, I3, I3L, I3YY |     |                | C4, I4         |     |                | Unit |
|-------------------------------------------------------------|-------------------------------------------------------------------------------------------------------------------------------------|----------------|-----|----------------|------------------|-----|----------------|-------------------|-----|----------------|----------------|-----|----------------|------|
|                                                             |                                                                                                                                     | Min            | Typ | Max            | Min              | Typ | Max            | Min               | Typ | Max            | Min            | Typ | Max            |      |
| $t_{DUTY}$                                                  | Transmitter output clock duty cycle for both True and Emulated Differential I/O Standards                                           | 45             | 50  | 55             | 45               | 50  | 55             | 45                | 50  | 55             | 45             | 50  | 55             | %    |
| $t_{RISE}$ & $t_{FALL}$                                     | True Differential I/O Standards                                                                                                     | —              | —   | 160            | —                | —   | 160            | —                 | —   | 200            | —              | —   | 200            | ps   |
|                                                             | Emulated Differential I/O Standards with three external output resistor networks                                                    | —              | —   | 250            | —                | —   | 250            | —                 | —   | 250            | —              | —   | 300            | ps   |
| TCCS                                                        | True Differential I/O Standards                                                                                                     | —              | —   | 150            | —                | —   | 150            | —                 | —   | 150            | —              | —   | 150            | ps   |
|                                                             | Emulated Differential I/O Standards                                                                                                 | —              | —   | 300            | —                | —   | 300            | —                 | —   | 300            | —              | —   | 300            | ps   |
| <b>Receiver</b>                                             |                                                                                                                                     |                |     |                |                  |     |                |                   |     |                |                |     |                |      |
| True Differential I/O Standards - $f_{HSDRDPA}$ (data rate) | SERDES factor J = 3 to 10 <sup>(11)</sup> , <sup>(12)</sup> , <sup>(13)</sup> , <sup>(14)</sup> , <sup>(15)</sup> , <sup>(16)</sup> | 150            | —   | 1434           | 150              | —   | 1434           | 150               | —   | 1250           | 150            | —   | 1050           | Mbps |
|                                                             | SERDES factor J $\geq 4$                                                                                                            | 150            | —   | 1600           | 150              | —   | 1600           | 150               | —   | 1600           | 150            | —   | 1250           | Mbps |
|                                                             | LVDS RX with DPA <sup>(12)</sup> , <sup>(14)</sup> , <sup>(15)</sup> , <sup>(16)</sup>                                              | 150            | —   | 1600           | 150              | —   | 1600           | 150               | —   | 1600           | 150            | —   | 1250           | Mbps |
|                                                             | SERDES factor J = 2, uses DDR Registers                                                                                             | <sup>(6)</sup> | —   | <sup>(7)</sup> | <sup>(6)</sup>   | —   | <sup>(7)</sup> | <sup>(6)</sup>    | —   | <sup>(7)</sup> | <sup>(6)</sup> | —   | <sup>(7)</sup> | Mbps |
|                                                             | SERDES factor J = 1, uses SDR Register                                                                                              | <sup>(6)</sup> | —   | <sup>(7)</sup> | <sup>(6)</sup>   | —   | <sup>(7)</sup> | <sup>(6)</sup>    | —   | <sup>(7)</sup> | <sup>(6)</sup> | —   | <sup>(7)</sup> | Mbps |

**Table 42. Memory Output Clock Jitter Specification for Stratix V Devices <sup>(1)</sup>, (Part 2 of 2) <sup>(2)</sup>, <sup>(3)</sup>**

| Clock Network | Parameter                    | Symbol          | C1    |      | C2, C2L, I2, I2L |      | C3, I3, I3L, I3YY |     | C4,I4 |     | Unit |
|---------------|------------------------------|-----------------|-------|------|------------------|------|-------------------|-----|-------|-----|------|
|               |                              |                 | Min   | Max  | Min              | Max  | Min               | Max | Min   | Max |      |
| PHY Clock     | Clock period jitter          | $t_{JIT(per)}$  | -25   | 25   | -25              | 25   | -30               | 30  | -35   | 35  | ps   |
|               | Cycle-to-cycle period jitter | $t_{JIT(cc)}$   | -50   | 50   | -50              | 50   | -60               | 60  | -70   | 70  | ps   |
|               | Duty cycle jitter            | $t_{JIT(duty)}$ | -37.5 | 37.5 | -37.5            | 37.5 | -45               | 45  | -56   | 56  | ps   |

**Notes to Table 42:**

- (1) The clock jitter specification applies to the memory output clock pins generated using differential signal-splitter and DDIO circuits clocked by a PLL output routed on a PHY, regional, or global clock network as specified. Altera recommends using PHY clock networks whenever possible.
- (2) The clock jitter specification applies to the memory output clock pins clocked by an integer PLL.
- (3) The memory output clock jitter is applicable when an input jitter of 30 ps peak-to-peak is applied with bit error rate (BER) -12, equivalent to 14 sigma.

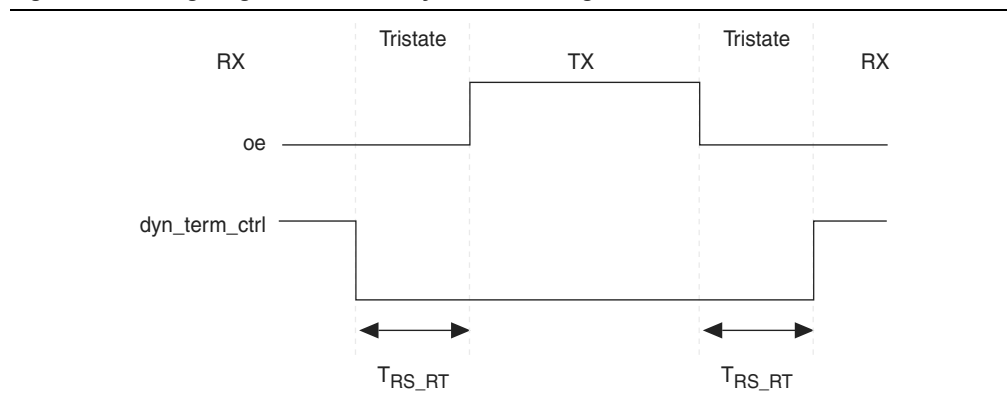
**OCT Calibration Block Specifications**

Table 43 lists the OCT calibration block specifications for Stratix V devices.

**Table 43. OCT Calibration Block Specifications for Stratix V Devices**

| Symbol         | Description                                                                                                                                                                             | Min | Typ  | Max | Unit   |
|----------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----|------|-----|--------|
| OCTUSRCLK      | Clock required by the OCT calibration blocks                                                                                                                                            | —   | —    | 20  | MHz    |
| $T_{OCTCAL}$   | Number of OCTUSRCLK clock cycles required for OCT $R_S/R_T$ calibration                                                                                                                 | —   | 1000 | —   | Cycles |
| $T_{OCTSHIFT}$ | Number of OCTUSRCLK clock cycles required for the OCT code to shift out                                                                                                                 | —   | 32   | —   | Cycles |
| $T_{RS\_RT}$   | Time required between the <code>dyn_term_ctrl</code> and <code>oe</code> signal transitions in a bidirectional I/O buffer to dynamically switch between OCT $R_S$ and $R_T$ (Figure 10) | —   | 2.5  | —   | ns     |

Figure 10 shows the timing diagram for the `oe` and `dyn_term_ctrl` signals.

**Figure 10. Timing Diagram for `oe` and `dyn_term_ctrl` Signals**

**Table 47. Uncompressed .rbf Sizes for Stratix V Devices**

| Family                     | Device | Package | Configuration .rbf Size (bits) | IOCSR .rbf Size (bits) <sup>(4), (5)</sup> |
|----------------------------|--------|---------|--------------------------------|--------------------------------------------|
| Stratix V E <sup>(1)</sup> | 5SEE9  | —       | 342,742,976                    | 700,888                                    |
|                            | 5SEEB  | —       | 342,742,976                    | 700,888                                    |

**Notes to Table 47:**

- (1) Stratix V E devices do not have PCI Express® (PCIe®) hard IP. Stratix V E devices do not support the CvP configuration scheme.
- (2) 36-transceiver devices.
- (3) 24-transceiver devices.
- (4) File size for the periphery image.
- (5) The IOCSR .rbf size is specifically for the CvP feature.

Use the data in Table 47 to estimate the file size before design compilation. Different configuration file formats, such as a hexadecimal (.hex) or tabular text file (.tff) format, have different file sizes. For the different types of configuration file and file sizes, refer to the Quartus II software. However, for a specific version of the Quartus II software, any design targeted for the same device has the same uncompressed configuration file size. If you are using compression, the file size can vary after each compilation because the compression ratio depends on your design.



For more information about setting device configuration options, refer to *Configuration, Design Security, and Remote System Upgrades in Stratix V Devices*. For creating configuration files, refer to the *Quartus II Help*.

Table 48 lists the minimum configuration time estimates for Stratix V devices.

**Table 48. Minimum Configuration Time Estimation for Stratix V Devices**

| Variant | Member Code | Active Serial <sup>(1)</sup> |            |                     | Fast Passive Parallel <sup>(2)</sup> |            |                     |
|---------|-------------|------------------------------|------------|---------------------|--------------------------------------|------------|---------------------|
|         |             | Width                        | DCLK (MHz) | Min Config Time (s) | Width                                | DCLK (MHz) | Min Config Time (s) |
| GX      | A3          | 4                            | 100        | 0.534               | 32                                   | 100        | 0.067               |
|         |             | 4                            | 100        | 0.344               | 32                                   | 100        | 0.043               |
|         | A4          | 4                            | 100        | 0.534               | 32                                   | 100        | 0.067               |
|         | A5          | 4                            | 100        | 0.675               | 32                                   | 100        | 0.084               |
|         | A7          | 4                            | 100        | 0.675               | 32                                   | 100        | 0.084               |
|         | A9          | 4                            | 100        | 0.857               | 32                                   | 100        | 0.107               |
|         | AB          | 4                            | 100        | 0.857               | 32                                   | 100        | 0.107               |
|         | B5          | 4                            | 100        | 0.676               | 32                                   | 100        | 0.085               |
|         | B6          | 4                            | 100        | 0.676               | 32                                   | 100        | 0.085               |
|         | B9          | 4                            | 100        | 0.857               | 32                                   | 100        | 0.107               |
|         | BB          | 4                            | 100        | 0.857               | 32                                   | 100        | 0.107               |
| GT      | C5          | 4                            | 100        | 0.675               | 32                                   | 100        | 0.084               |
|         | C7          | 4                            | 100        | 0.675               | 32                                   | 100        | 0.084               |

Table 60. Glossary (Part 2 of 4)

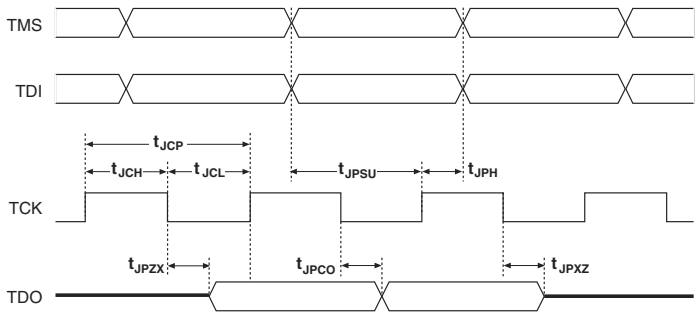
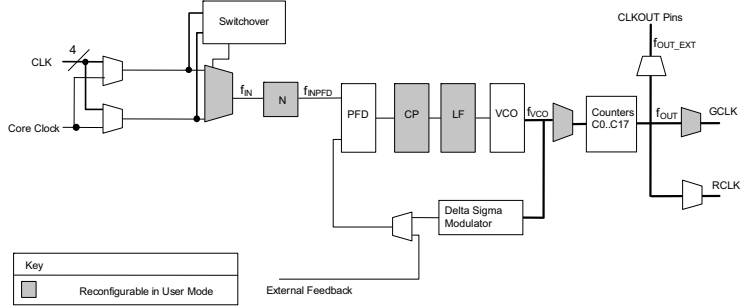
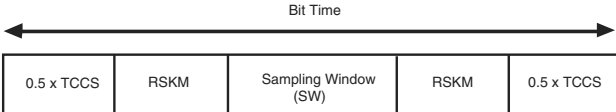
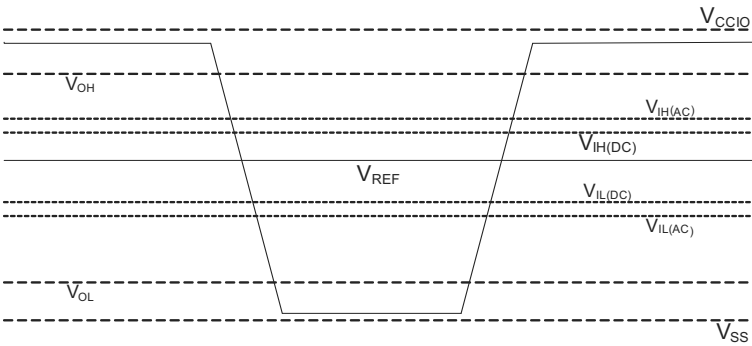
| Letter                | Subject                    | Definitions                                                                                                                                                                                                                                          |
|-----------------------|----------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| G<br>H<br>I           | —                          | —                                                                                                                                                                                                                                                    |
| J                     | JTAG Timing Specifications | <p>High-speed I/O block—Deserialization factor (width of parallel data bus).</p> <p>JTAG Timing Specifications:</p>                                                |
| K<br>L<br>M<br>N<br>O | —                          | —                                                                                                                                                                                                                                                    |
| P                     | PLL Specifications         | <p><b>Diagram of PLL Specifications <sup>(1)</sup></b></p>  <p><b>Note:</b><br/>(1) Core Clock can only be fed by dedicated clock input pins or PLL outputs.</p> |
| Q                     | —                          | —                                                                                                                                                                                                                                                    |
| R                     | R <sub>L</sub>             | Receiver differential input discrete resistor (external to the Stratix V device).                                                                                                                                                                    |

Table 60. Glossary (Part 3 of 4)

| Letter | Subject                                      | Definitions                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        |
|--------|----------------------------------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| S      | SW (sampling window)                         | <p>Timing Diagram—the period of time during which the data must be valid in order to capture it correctly. The setup and hold times determine the ideal strobe position within the sampling window, as shown:</p>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |
|        | Single-ended voltage referenced I/O standard | <p>The JEDEC standard for <b>SSTL</b> and <b>HSTL</b> I/O defines both the AC and DC input signal values. The AC values indicate the voltage levels at which the receiver must meet its timing specifications. The DC values indicate the voltage levels at which the final logic state of the receiver is unambiguously defined. After the receiver input has crossed the AC value, the receiver changes to the new logic state.</p> <p>The new logic state is then maintained as long as the input stays beyond the DC threshold. This approach is intended to provide predictable receiver timing in the presence of input waveform ringing:</p> <p><i>Single-Ended Voltage Referenced I/O Standard</i></p>  |
| T      | $t_c$                                        | High-speed receiver and transmitter input and output clock period.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 |
|        | TCCS (channel-to-channel-skew)               | The timing difference between the fastest and slowest output edges, including $t_{CO}$ variation and clock skew, across channels driven by the same PLL. The clock is included in the TCCS measurement (refer to the <i>Timing Diagram</i> figure under <b>SW</b> in this table).                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  |
|        | $t_{DUTY}$                                   | <p>High-speed I/O block—Duty cycle on the high-speed transmitter output clock.</p> <p><b>Timing Unit Interval (TUI)</b></p> <p>The timing budget allowed for skew, propagation delays, and the data sampling window. (TUI = <math>1/(\text{receiver input clock frequency multiplication factor}) = t_c/w</math>)</p>                                                                                                                                                                                                                                                                                                                                                                                                                                                                              |
|        | $t_{FALL}$                                   | Signal high-to-low transition time (80-20%)                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        |
|        | $t_{INCCJ}$                                  | Cycle-to-cycle jitter tolerance on the PLL clock input.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            |
|        | $t_{OUTPJ\_IO}$                              | Period jitter on the general purpose I/O driven by a PLL.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          |
|        | $t_{OUTPJ\_DC}$                              | Period jitter on the dedicated clock output driven by a PLL.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       |
|        | $t_{RISE}$                                   | Signal low-to-high transition time (20-80%)                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        |
| U      | —                                            | —                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  |