# Intel - 5SGXEA3K2F40C2N Datasheet

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## Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

## Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

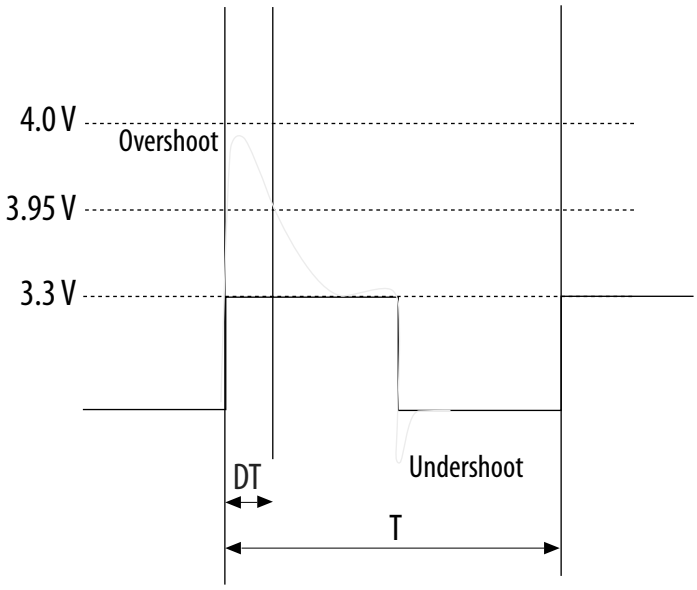
| Details | |
|---|---|
| Product Status | Obsolete |
| Number of LABs/CLBs | 128300 |
| Number of Logic Elements/Cells | 340000 |
| Total RAM Bits | 19456000 |
| Number of I/O | 696 |
| Number of Gates | - |
| Voltage - Supply | 0.87V ~ 0.93V |
| Mounting Type | Surface Mount |
| Operating Temperature | 0°C ~ 85°C (TJ) |
| Package / Case | 1517-BBGA, FCBGA |
| Supplier Device Package | 1517-FBGA (40x40) |
| Purchase URL | https://www.e-xfl.com/product-detail/intel/5sgxea3k2f40c2n |

Table 5 lists the maximum allowed input overshoot voltage and the duration of the overshoot voltage as a percentage of device lifetime. The maximum allowed overshoot duration is specified as a percentage of high time over the lifetime of the device. A DC signal is equivalent to 100% of the duty cycle. For example, a signal that overshoots to 3.95 V can be at 3.95 V for only ~21% over the lifetime of the device; for a device lifetime of 10 years, the overshoot duration amounts to ~2 years.

**Table 5. Maximum Allowed Overshoot During Transitions**

| Symbol | Description | Condition (V) | Overshoot Duration as % @ $T_J$ = 100°C | Unit |
|---|---|---|---|---|
| Vi (AC) | AC input voltage | 3.8 | 100 | % |
| | | 3.85 | 64 | % |
| | | 3.9 | 36 | % |
| | | 3.95 | 21 | % |
| | | 4 | 12 | % |
| | | 4.05 | 7 | % |
| | | 4.1 | 4 | % |
| | | 4.15 | 2 | % |
| | | 4.2 | 1 | % |

**Figure 1. Stratix V Device Overshoot Duration**



## Recommended Operating Conditions

This section lists the functional operating limits for the AC and DC parameters for Stratix V devices. Table 6 lists the steady-state voltage and current values expected from Stratix V devices. Power supply ramps must all be strictly monotonic, without plateaus.

**Table 6. Recommended Operating Conditions for Stratix V Devices (Part 1 of 2)**

| Symbol | Description | Condition | Min (4) | Typ | Max (4) | Unit |
|---|---|---|---|---|---|---|
| $V_{CC}$ | Core voltage and periphery circuitry power supply (C1, C2, I2, and I3YY speed grades) | — | 0.87 | 0.9 | 0.93 | V |
| | Core voltage and periphery circuitry power supply (C2L, C3, C4, I2L, I3, I3L, and I4 speed grades) (3) | — | 0.82 | 0.85 | 0.88 | V |
| $V_{CCPT}$ | Power supply for programmable power technology | — | 1.45 | 1.50 | 1.55 | V |
| $V_{CC\_AUX}$ | Auxiliary supply for the programmable power technology | — | 2.375 | 2.5 | 2.625 | V |
| $V_{CCPD}$ (1) | I/O pre-driver (3.0 V) power supply | — | 2.85 | 3.0 | 3.15 | V |
| | I/O pre-driver (2.5 V) power supply | — | 2.375 | 2.5 | 2.625 | V |
| $V_{CCIO}$ | I/O buffers (3.0 V) power supply | — | 2.85 | 3.0 | 3.15 | V |
| | I/O buffers (2.5 V) power supply | — | 2.375 | 2.5 | 2.625 | V |
| | I/O buffers (1.8 V) power supply | — | 1.71 | 1.8 | 1.89 | V |
| | I/O buffers (1.5 V) power supply | — | 1.425 | 1.5 | 1.575 | V |
| | I/O buffers (1.35 V) power supply | — | 1.283 | 1.35 | 1.45 | V |
| | I/O buffers (1.25 V) power supply | — | 1.19 | 1.25 | 1.31 | V |
| | I/O buffers (1.2 V) power supply | — | 1.14 | 1.2 | 1.26 | V |
| $V_{CCPGM}$ | Configuration pins (3.0 V) power supply | — | 2.85 | 3.0 | 3.15 | V |
| | Configuration pins (2.5 V) power supply | — | 2.375 | 2.5 | 2.625 | V |
| | Configuration pins (1.8 V) power supply | — | 1.71 | 1.8 | 1.89 | V |
| $V_{CCA\_FPLL}$ | PLL analog voltage regulator power supply | — | 2.375 | 2.5 | 2.625 | V |
| $V_{CCD\_FPLL}$ | PLL digital voltage regulator power supply | — | 1.45 | 1.5 | 1.55 | V |
| $V_{CCBAT}$ (2) | Battery back-up power supply (For design security volatile key register) | — | 1.2 | — | 3.0 | V |
| $V_I$ | DC input voltage | — | –0.5 | — | 3.6 | V |
| $V_O$ | Output voltage | — | 0 | — | $V_{CCIO}$ | V |
| $T_J$ | Operating junction temperature | Commercial | 0 | — | 85 | °C |
| | | Industrial | –40 | — | 100 | °C |

**Table 7. Recommended Transceiver Power Supply Operating Conditions for Stratix V GX, GS, and GT Devices (Part 2 of 2)**

| Symbol | Description | Devices | Minimum (4) | Typical | Maximum (4) | Unit |
|---|---|---|---|---|---|---|
| $V_{CCR\_GXBR}$ (2) | Receiver analog power supply (right side) | GX, GS, GT | 0.82 | 0.85 | 0.88 | V |
| | | | 0.87 | 0.90 | 0.93 | |
| | | | 0.97 | 1.0 | 1.03 | |
| | | | 1.03 | 1.05 | 1.07 | |
| $V_{CCR\_GTBR}$ | Receiver analog power supply for GT channels (right side) | GT | 1.02 | 1.05 | 1.08 | V |
| $V_{CCT\_GXBL}$ (2) | Transmitter analog power supply (left side) | GX, GS, GT | 0.82 | 0.85 | 0.88 | V |
| | | | 0.87 | 0.90 | 0.93 | |
| | | | 0.97 | 1.0 | 1.03 | |
| | | | 1.03 | 1.05 | 1.07 | |
| $V_{CCT\_GXBR}$ (2) | Transmitter analog power supply (right side) | GX, GS, GT | 0.82 | 0.85 | 0.88 | V |
| | | | 0.87 | 0.90 | 0.93 | |
| | | | 0.97 | 1.0 | 1.03 | |
| | | | 1.03 | 1.05 | 1.07 | |
| $V_{CCT\_GTBR}$ | Transmitter analog power supply for GT channels (right side) | GT | 1.02 | 1.05 | 1.08 | V |
| $V_{CCL\_GTBR}$ | Transmitter clock network power supply | GT | 1.02 | 1.05 | 1.08 | V |
| $V_{CCH\_GXBL}$ | Transmitter output buffer power supply (left side) | GX, GS, GT | 1.425 | 1.5 | 1.575 | V |
| $V_{CCH\_GXBR}$ | Transmitter output buffer power supply (right side) | GX, GS, GT | 1.425 | 1.5 | 1.575 | V |

**Notes to Table 7:**

(1) This supply must be connected to 3.0 V if the CMU PLL, receiver CDR, or both, are configured at a base data rate > 6.5 Gbps. Up to 6.5 Gbps, you can connect this supply to either 3.0 V or 2.5 V.

(2) Refer to Table 8 to select the correct power supply level for your design.

(3) When using ATX PLLs, the supply must be 3.0 V.

(4) This value describes the budget for the DC (static) power supply tolerance and does not include the dynamic tolerance requirements. Refer to the PDN tool for the additional budget for the dynamic tolerance requirements.

### I/O Pin Leakage Current

Table 9 lists the Stratix V I/O pin leakage current specifications.

**Table 9. I/O Pin Leakage Current for Stratix V Devices (1)**

| Symbol | Description | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $I_I$ | Input pin | $V_I$ = 0 V to $V_{CCIOMAX}$ | –30 | — | 30 | µA |
| $I_{OZ}$ | Tri-stated I/O pin | $V_O$ = 0 V to $V_{CCIOMAX}$ | –30 | — | 30 | µA |

**Note to Table 9:**

(1) If $V_O = V_{CCIO}$ to $V_{CCIOMax}$, 100 µA of leakage current per I/O is expected.

### Bus Hold Specifications

Table 10 lists the Stratix V device family bus hold specifications.

**Table 10. Bus Hold Parameters for Stratix V Devices**

| Parameter | Symbol | Conditions | $V_{CCIO}$ | | | | | | | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | 1.2 V | | 1.5 V | | 1.8 V | | 2.5 V | | 3.0 V | | |
| | | | Min | Max | Min | Max | Min | Max | Min | Max | Min | Max | |
| Low sustaining current | $I_{SUSL}$ | $V_{IN} > V_{IL}$ (maximum) | 22.5 | — | 25.0 | — | 30.0 | — | 50.0 | — | 70.0 | — | µA |
| High sustaining current | $I_{SUSH}$ | $V_{IN} < V_{IH}$ (minimum) | –22.5 | — | –25.0 | — | –30.0 | — | –50.0 | — | –70.0 | — | µA |
| Low overdrive current | $I_{ODL}$ | $0V < V_{IN} < V_{CCIO}$ | — | 120 | — | 160 | — | 200 | — | 300 | — | 500 | µA |
| High overdrive current | $I_{ODH}$ | $0V < V_{IN} < V_{CCIO}$ | — | –120 | — | –160 | — | –200 | — | –300 | — | –500 | µA |
| Bus-hold trip point | $V_{TRIP}$ | — | 0.45 | 0.95 | 0.50 | 1.00 | 0.68 | 1.07 | 0.70 | 1.70 | 0.80 | 2.00 | V |

### On-Chip Termination (OCT) Specifications

If you enable OCT calibration, calibration is automatically performed at power-up for I/Os connected to the calibration block. Table 11 lists the Stratix V OCT termination calibration accuracy specifications.

**Table 11. OCT Calibration Accuracy Specifications for Stratix V Devices (1) (Part 1 of 2)**

| Symbol | Description | Conditions | Calibration Accuracy | | | | Unit |
|---|---|---|---|---|---|---|---|
| | | | C1 | C2,I2 | C3,I3, I3YY | C4,I4 | |
| 25-Ω $R_S$ | Internal series termination with calibration (25-Ω setting) | $V_{CCIO}$ = 3.0, 2.5, 1.8, 1.5, 1.2 V | ±15 | ±15 | ±15 | ±15 | % |

**Table 21. Differential HSTL and HSUL I/O Standards for Stratix V Devices (Part 2 of 2)**

| I/O Standard | $V_{CCIO}$ (V) | | | $V_{DIF(DC)}$ (V) | | $V_{X(AC)}$ (V) | | | $V_{CM(DC)}$ (V) | | | $V_{DIF(AC)}$ (V) | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | Min | Typ | Max | Min | Max | Min | Typ | Max | Min | Typ | Max | Min | Max |
| HSTL-12 Class I, II | 1.14 | 1.2 | 1.26 | 0.16 | $V_{CCIO}$ + 0.3 | — | 0.5* $V_{CCIO}$ | — | 0.4* $V_{CCIO}$ | 0.5* $V_{CCIO}$ | 0.6* $V_{CCIO}$ | 0.3 | $V_{CCIO}$ + 0.48 |
| HSUL-12 | 1.14 | 1.2 | 1.3 | 0.26 | 0.26 | 0.5*$V_{CCIO}$ – 0.12 | 0.5* $V_{CCIO}$ | 0.5*$V_{CCIO}$ + 0.12 | 0.4* $V_{CCIO}$ | 0.5* $V_{CCIO}$ | 0.6* $V_{CCIO}$ | 0.44 | 0.44 |

**Table 22. Differential I/O Standard Specifications for Stratix V Devices (7)**

| I/O Standard | $V_{CCIO}$ (V) (10) | | | $V_{ID}$ (mV) (8) | | | $V_{ICM(DC)}$ (V) | | | $V_{OD}$ (V) (6) | | | $V_{OCM}$ (V) (6) | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | Min | Typ | Max | Min | Condition | Max | Min | Condition | Max | Min | Typ | Max | Min | Typ | Max |
| PCML | Transmitter, receiver, and input reference clock pins of the high-speed transceivers use the PCML I/O standard. For transmitter, receiver, and reference clock I/O pin specifications, refer to Table 23 on page 18. | | | | | | | | | | | | | | |
| 2.5 V LVDS (1) | 2.375 | 2.5 | 2.625 | 100 | $V_{CM}$ = 1.25 V | — | 0.05 | $D_{MAX} \leq$ 700 Mbps | 1.8 | 0.247 | — | 0.6 | 1.125 | 1.25 | 1.375 |
| | | | | | | — | 1.05 | $D_{MAX} >$ 700 Mbps | 1.55 | 0.247 | — | 0.6 | 1.125 | 1.25 | 1.375 |
| BLVDS (5) | 2.375 | 2.5 | 2.625 | 100 | — | — | — | — | — | — | — | — | — | — | — |
| RSDS (HIO) (2) | 2.375 | 2.5 | 2.625 | 100 | $V_{CM}$ = 1.25 V | — | 0.3 | — | 1.4 | 0.1 | 0.2 | 0.6 | 0.5 | 1.2 | 1.4 |
| Mini-LVDS (HIO) (3) | 2.375 | 2.5 | 2.625 | 200 | — | 600 | 0.4 | — | 1.325 | 0.25 | — | 0.6 | 1 | 1.2 | 1.4 |
| LVPECL (4), (9) | — | — | — | 300 | — | — | 0.6 | $D_{MAX} \leq$ 700 Mbps | 1.8 | — | — | — | — | — | — |
| | — | — | — | 300 | — | — | 1 | $D_{MAX} >$ 700 Mbps | 1.6 | — | — | — | — | — | — |

**Notes to Table 22:**

(1) For optimized LVDS receiver performance, the receiver voltage input range must be between 1.0 V to 1.6 V for data rates above 700 Mbps, and 0 V to 1.85 V for data rates below 700 Mbps.

(2) For optimized RSDS receiver performance, the receiver voltage input range must be between 0.25 V to 1.45 V.

(3) For optimized Mini-LVDS receiver performance, the receiver voltage input range must be between 0.3 V to 1.425 V.

(4) For optimized LVPECL receiver performance, the receiver voltage input range must be between 0.85 V to 1.75 V for data rate above 700 Mbps and 0.45 V to 1.95 V for data rate below 700 Mbps.

(5) There are no fixed $V_{ICM}$, $V_{OD}$, and $V_{OCM}$ specifications for BLVDS. They depend on the system topology.

(6) RL range: $90 \leq RL \leq 110\ \Omega$ .

(7) The 1.4-V and 1.5-V PCML transceiver I/O standard specifications are described in "Transceiver Performance Specifications" on page 18.

(8) The minimum VID value is applicable over the entire common mode range, VCM.

(9) LVPECL is only supported on dedicated clock input pins.

(10) Differential inputs are powered by VCCPD which requires 2.5 V.

## Power Consumption

Altera offers two ways to estimate power consumption for a design—the Excel-based Early Power Estimator and the Quartus® II PowerPlay Power Analyzer feature.

**Table 23. Transceiver Specifications for Stratix V GX and GS Devices (1) (Part 3 of 7)**

| Symbol/ Description | Conditions | Transceiver Speed Grade 1 | | | Transceiver Speed Grade 2 | | | Transceiver Speed Grade 3 | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| Reconfiguration clock (mgmt_clk_clk) frequency | — | 100 | — | 125 | 100 | — | 125 | 100 | — | 125 | MHz |
| **Receiver** | | | | | | | | | | | |
| Supported I/O Standards | — | 1.4-V PCML, 1.5-V PCML, 2.5-V PCML, LVPECL, and LVDS | | | | | | | | | |
| Data rate (Standard PCS) (9), (23) | — | 600 | — | 12200 | 600 | — | 12200 | 600 | — | 8500/ 10312.5 (24) | Mbps |
| Data rate (10G PCS) (9), (23) | — | 600 | — | 14100 | 600 | — | 12500 | 600 | — | 8500/ 10312.5 (24) | Mbps |
| Absolute $V_{MAX}$ for a receiver pin (5) | — | — | — | 1.2 | — | — | 1.2 | — | — | 1.2 | V |
| Absolute $V_{MIN}$ for a receiver pin | — | –0.4 | — | — | –0.4 | — | — | –0.4 | — | — | V |
| Maximum peak-to-peak differential input voltage $V_{ID}$ (diff p-p) before device configuration (22) | — | — | — | 1.6 | — | — | 1.6 | — | — | 1.6 | V |
| Maximum peak-to-peak differential input voltage $V_{ID}$ (diff p-p) after device configuration (18), (22) | $V_{CCR\_GXB}$ = 1.0 V/1.05 V ($V_{ICM}$ = 0.70 V) | — | — | 2.0 | — | — | 2.0 | — | — | 2.0 | V |
| | $V_{CCR\_GXB}$ = 0.90 V ($V_{ICM}$ = 0.6 V) | — | — | 2.4 | — | — | 2.4 | — | — | 2.4 | V |
| | $V_{CCR\_GXB}$ = 0.85 V ($V_{ICM}$ = 0.6 V) | — | — | 2.4 | — | — | 2.4 | — | — | 2.4 | V |
| Minimum differential eye opening at receiver serial input pins (6), (22), (27) | — | 85 | — | — | 85 | — | — | 85 | — | — | mV |

**Table 23. Transceiver Specifications for Stratix V GX and GS Devices (1) (Part 6 of 7)**

| Symbol/ Description | Conditions | Transceiver Speed Grade 1 | | | Transceiver Speed Grade 2 | | | Transceiver Speed Grade 3 | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| Inter-transceiver block transmitter channel-to-channel skew | xN PMA bonded mode | — | — | 500 | — | — | 500 | — | — | 500 | ps |
| **CMU PLL** | | | | | | | | | | | |
| Supported Data Range | — | 600 | — | 12500 | 600 | — | 12500 | 600 | — | 8500/ 10312.5 (24) | Mbps |
| $t_{pll\_powerdown}$ (15) | — | 1 | — | — | 1 | — | — | 1 | — | — | µs |
| $t_{pll\_lock}$ (16) | — | — | — | 10 | — | — | 10 | — | — | 10 | µs |
| **ATX PLL** | | | | | | | | | | | |
| Supported Data Rate Range | VCO post-divider L=2 | 8000 | — | 14100 | 8000 | — | 12500 | 8000 | — | 8500/ 10312.5 (24) | Mbps |
| | L=4 | 4000 | — | 7050 | 4000 | — | 6600 | 4000 | — | 6600 | Mbps |
| | L=8 | 2000 | — | 3525 | 2000 | — | 3300 | 2000 | — | 3300 | Mbps |
| | L=8, Local/Central Clock Divider =2 | 1000 | — | 1762.5 | 1000 | — | 1762.5 | 1000 | — | 1762.5 | Mbps |
| $t_{pll\_powerdown}$ (15) | — | 1 | — | — | 1 | — | — | 1 | — | — | µs |
| $t_{pll\_lock}$ (16) | — | — | — | 10 | — | — | 10 | — | — | 10 | µs |
| **fPLL** | | | | | | | | | | | |
| Supported Data Range | — | 600 | — | 3250/ 3125 (25) | 600 | — | 3250/ 3125 (25) | 600 | — | 3250/ 3125 (25) | Mbps |
| $t_{pll\_powerdown}$ (15) | — | 1 | — | — | 1 | — | — | 1 | — | — | µs |

Table 24 shows the maximum transmitter data rate for the clock network.

**Table 24. Clock Network Maximum Data Rate Transmitter Specifications** *(1)*

| Clock Network | ATX PLL | | | CMU PLL *(2)* | | | fPLL | | |
|---|---|---|---|---|---|---|---|---|---|
| | Non-bonded Mode (Gbps) | Bonded Mode (Gbps) | Channel Span | Non-bonded Mode (Gbps) | Bonded Mode (Gbps) | Channel Span | Non-bonded Mode (Gbps) | Bonded Mode (Gbps) | Channel Span |
| x1 *(3)* | 14.1 | — | 6 | 12.5 | — | 6 | 3.125 | — | 3 |
| x6 *(3)* | — | 14.1 | 6 | — | 12.5 | 6 | — | 3.125 | 6 |
| x6 PLL Feedback *(4)* | — | 14.1 | Side-wide | — | 12.5 | Side-wide | — | — | — |
| xN (PCIe) | — | 8.0 | 8 | — | 5.0 | 8 | — | — | — |
| xN (Native PHY IP) | 8.0 | 8.0 | Up to 13 channels above and below PLL | 7.99 | 7.99 | Up to 13 channels above and below PLL | 3.125 | 3.125 | Up to 13 channels above and below PLL |
| | — | 8.01 to 9.8304 | Up to 7 channels above and below PLL | | | | | | |

**Notes to Table 24:**

(1) Valid data rates below the maximum specified in this table depend on the reference clock frequency and the PLL counter settings. Check the MegaWizard message during the PHY IP instantiation.

(2) ATX PLL is recommended at 8 Gbps and above data rates for improved jitter performance.

(3) Channel span is within a transceiver bank.

(4) Side-wide channel bonding is allowed up to the maximum supported by the PHY IP.

Figure 4 shows the differential transmitter output waveform.

**Figure 4. Differential Transmitter/Receiver Output/Input Waveform**

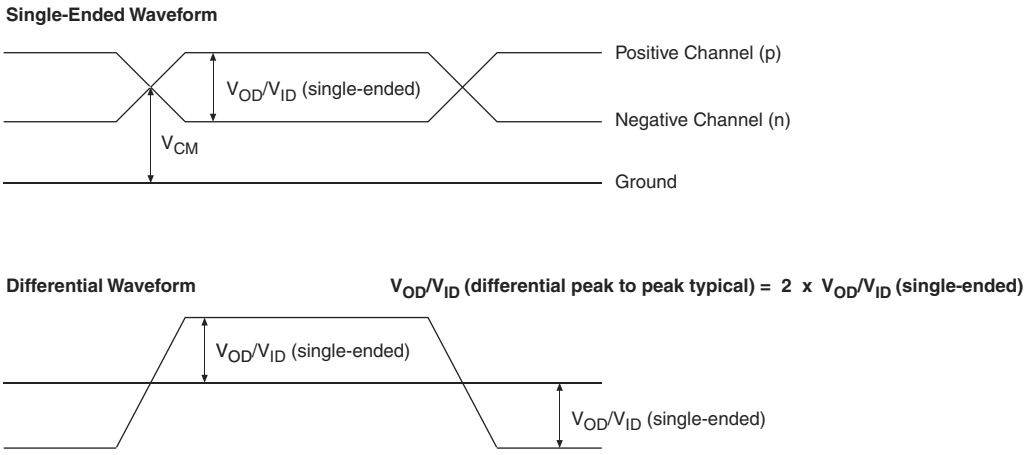



Figure 5 shows the Stratix V AC gain curves for GT channels.

**Figure 5. AC Gain Curves for GT Channels**

**Table 31. PLL Specifications for Stratix V Devices (Part 2 of 3)**

| Symbol | Parameter | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| $t_{INCCJ}$ (3), (4) | Input clock cycle-to-cycle jitter ($f_{REF} \geq 100$ MHz) | — | — | 0.15 | UI (p-p) |
| | Input clock cycle-to-cycle jitter ($f_{REF} < 100$ MHz) | –750 | — | +750 | ps (p-p) |
| $t_{OUTPJ\_DC}$ (5) | Period Jitter for dedicated clock output ($f_{OUT} \geq 100$ MHz) | — | — | 175 (1) | ps (p-p) |
| | Period Jitter for dedicated clock output ($f_{OUT} < 100$ MHz) | — | — | 17.5 (1) | mUI (p-p) |
| $t_{FOUTPJ\_DC}$ (5) | Period Jitter for dedicated clock output in fractional PLL ($f_{OUT} \geq 100$ MHz) | — | — | 250 (11), 175 (12) | ps (p-p) |
| | Period Jitter for dedicated clock output in fractional PLL ($f_{OUT} < 100$ MHz) | — | — | 25 (11), 17.5 (12) | mUI (p-p) |
| $t_{OUTCCJ\_DC}$ (5) | Cycle-to-Cycle Jitter for a dedicated clock output ($f_{OUT} \geq 100$ MHz) | — | — | 175 | ps (p-p) |
| | Cycle-to-Cycle Jitter for a dedicated clock output ($f_{OUT} < 100$ MHz) | — | — | 17.5 | mUI (p-p) |
| $t_{FOUTCCJ\_DC}$ (5) | Cycle-to-cycle Jitter for a dedicated clock output in fractional PLL ($f_{OUT} \geq 100$ MHz) | — | — | 250 (11), 175 (12) | ps (p-p) |
| | Cycle-to-cycle Jitter for a dedicated clock output in fractional PLL ($f_{OUT} < 100$ MHz)+ | — | — | 25 (11), 17.5 (12) | mUI (p-p) |
| $t_{OUTPJ\_IO}$ (5), (8) | Period Jitter for a clock output on a regular I/O in integer PLL ($f_{OUT} \geq 100$ MHz) | — | — | 600 | ps (p-p) |
| | Period Jitter for a clock output on a regular I/O ($f_{OUT} < 100$ MHz) | — | — | 60 | mUI (p-p) |
| $t_{FOUTPJ\_IO}$ (5), (8), (11) | Period Jitter for a clock output on a regular I/O in fractional PLL ($f_{OUT} \geq 100$ MHz) | — | — | 600 (10) | ps (p-p) |
| | Period Jitter for a clock output on a regular I/O in fractional PLL ($f_{OUT} < 100$ MHz) | — | — | 60 (10) | mUI (p-p) |
| $t_{OUTCCJ\_IO}$ (5), (8) | Cycle-to-cycle Jitter for a clock output on a regular I/O in integer PLL ($f_{OUT} \geq 100$ MHz) | — | — | 600 | ps (p-p) |
| | Cycle-to-cycle Jitter for a clock output on a regular I/O in integer PLL ($f_{OUT} < 100$ MHz) | — | — | 60 (10) | mUI (p-p) |
| $t_{FOUTCCJ\_IO}$ (5), (8), (11) | Cycle-to-cycle Jitter for a clock output on a regular I/O in fractional PLL ($f_{OUT} \geq 100$ MHz) | — | — | 600 (10) | ps (p-p) |
| | Cycle-to-cycle Jitter for a clock output on a regular I/O in fractional PLL ($f_{OUT} < 100$ MHz) | — | — | 60 | mUI (p-p) |
| $t_{CASC\_OUTPJ\_DC}$ (5), (6) | Period Jitter for a dedicated clock output in cascaded PLLs ($f_{OUT} \geq 100$ MHz) | — | — | 175 | ps (p-p) |
| | Period Jitter for a dedicated clock output in cascaded PLLs ($f_{OUT} < 100$ MHz) | — | — | 17.5 | mUI (p-p) |
| $f_{DRIFT}$ | Frequency drift after PFDENA is disabled for a duration of 100 µs | — | — | ±10 | % |
| $dK_{BIT}$ | Bit number of Delta Sigma Modulator (DSM) | 8 | 24 | 32 | Bits |
| $k_{VALUE}$ | Numerator of Fraction | 128 | 8388608 | 2147483648 | — |

**Table 33. Memory Block Performance Specifications for Stratix V Devices (1), (2) (Part 2 of 2)**

| Memory | Mode | Resources Used | | Performance | | | | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | ALUTs | Memory | C1 | C2, C2L | C3 | C4 | I2, I2L | I3, I3L, I3YY | I4 | |
| M20K Block | Single-port, all supported widths | 0 | 1 | 700 | 700 | 650 | 550 | 700 | 500 | 450 | MHz |
| | Simple dual-port, all supported widths | 0 | 1 | 700 | 700 | 650 | 550 | 700 | 500 | 450 | MHz |
| | Simple dual-port with the read-during-write option set to **Old Data**, all supported widths | 0 | 1 | 525 | 525 | 455 | 400 | 525 | 455 | 400 | MHz |
| | Simple dual-port with ECC enabled, 512 × 32 | 0 | 1 | 450 | 450 | 400 | 350 | 450 | 400 | 350 | MHz |
| | Simple dual-port with ECC and optional pipeline registers enabled, 512 × 32 | 0 | 1 | 600 | 600 | 500 | 450 | 600 | 500 | 450 | MHz |
| | True dual port, all supported widths | 0 | 1 | 700 | 700 | 650 | 550 | 700 | 500 | 450 | MHz |
| | ROM, all supported widths | 0 | 1 | 700 | 700 | 650 | 550 | 700 | 500 | 450 | MHz |

**Notes to Table 33:**

(1) To achieve the maximum memory block performance, use a memory block clock that comes through global clock routing from an on-chip PLL set to **50%** output duty cycle. Use the Quartus II software to report timing for this and other memory block clocking schemes.

(2) When you use the error detection cyclical redundancy check (CRC) feature, there is no degradation in $F_{MAX}$.

(3) The $F_{MAX}$ specification is only achievable with Fitter options, **MLAB Implementation In 16-Bit Deep Mode** enabled.

## Temperature Sensing Diode Specifications

Table 34 lists the internal TSD specification.

**Table 34. Internal Temperature Sensing Diode Specification**

| Temperature Range | Accuracy | Offset Calibrated Option | Sampling Rate | Conversion Time | Resolution | Minimum Resolution with no Missing Codes |
|---|---|---|---|---|---|---|
| –40°C to 100°C | ±8°C | No | 1 MHz, 500 KHz | < 100 ms | 8 bits | 8 bits |

Table 35 lists the specifications for the Stratix V external temperature sensing diode.

**Table 35. External Temperature Sensing Diode Specifications for Stratix V Devices**

| Description | Min | Typ | Max | Unit |
|---|---|---|---|---|
| $I_{bias}$, diode source current | 8 | — | 200 | μA |
| $V_{bias,}$ voltage across diode | 0.3 | — | 0.9 | V |
| Series resistance | — | — | < 1 | Ω |
| Diode ideality factor | 1.006 | 1.008 | 1.010 | — |

**Table 36. High-Speed I/O Specifications for Stratix V Devices (1), (2) (Part 2 of 4)**

| Symbol | Conditions | C1 | | | C2, C2L, I2, I2L | | | C3, I3, I3L, I3YY | | | C4,I4 | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| **Transmitter** | | | | | | | | | | | | | | |
| True Differential I/O Standards - $f_{HSDR}$ (data rate) | SERDES factor J = 3 to 10 (9), (11), (12), (13), (14), (15), (16) | (6) | — | 1600 | (6) | — | 1434 | (6) | — | 1250 | (6) | — | 1050 | Mbps |
| | SERDES factor J ≥ 4 LVDS TX with DPA (12), (14), (15), (16) | (6) | — | 1600 | (6) | — | 1600 | (6) | — | 1600 | (6) | — | 1250 | Mbps |
| | SERDES factor J = 2, uses DDR Registers | (6) | — | (7) | (6) | — | (7) | (6) | — | (7) | (6) | — | (7) | Mbps |
| | SERDES factor J = 1, uses SDR Register | (6) | — | (7) | (6) | — | (7) | (6) | — | (7) | (6) | — | (7) | Mbps |
| Emulated Differential I/O Standards with Three External Output Resistor Networks - $f_{HSDR}$ (data rate) (10) | SERDES factor J = 4 to 10 (17) | (6) | — | 1100 | (6) | — | 1100 | (6) | — | 840 | (6) | — | 840 | Mbps |
| $t_{x\ Jitter}$ - True Differential I/O Standards | Total Jitter for Data Rate 600 Mbps - 1.25 Gbps | — | — | 160 | — | — | 160 | — | — | 160 | — | — | 160 | ps |
| | Total Jitter for Data Rate < 600 Mbps | — | — | 0.1 | — | — | 0.1 | — | — | 0.1 | — | — | 0.1 | UI |
| $t_{x\ Jitter}$ - Emulated Differential I/O Standards with Three External Output Resistor Network | Total Jitter for Data Rate 600 Mbps - 1.25 Gbps | — | — | 300 | — | — | 300 | — | — | 300 | — | — | 325 | ps |
| | Total Jitter for Data Rate < 600 Mbps | — | — | 0.2 | — | — | 0.2 | — | — | 0.2 | — | — | 0.25 | UI |

**Table 47. Uncompressed .rbf Sizes for Stratix V Devices**

| Family | Device | Package | Configuration .rbf Size (bits) | IOCSR .rbf Size (bits) (4), (5) |
|---|---|---|---|---|
| Stratix V E (1) | 5SEE9 | — | 342,742,976 | 700,888 |
| | 5SEEB | — | 342,742,976 | 700,888 |

**Notes to Table 47:**

(1) Stratix V E devices do not have PCI Express® (PCIe®) hard IP. Stratix V E devices do not support the CvP configuration scheme.
(2) 36-transceiver devices.
(3) 24-transceiver devices.
(4) File size for the periphery image.
(5) The IOCSR **.rbf** size is specifically for the CvP feature.

Use the data in Table 47 to estimate the file size before design compilation. Different configuration file formats, such as a hexadecimal (**.hex**) or tabular text file (**.ttf**) format, have different file sizes. For the different types of configuration file and file sizes, refer to the Quartus II software. However, for a specific version of the Quartus II software, any design targeted for the same device has the same uncompressed configuration file size. If you are using compression, the file size can vary after each compilation because the compression ratio depends on your design.

For more information about setting device configuration options, refer to *Configuration, Design Security, and Remote System Upgrades in Stratix V Devices*. For creating configuration files, refer to the *Quartus II Help*.

Table 48 lists the minimum configuration time estimates for Stratix V devices.

**Table 48. Minimum Configuration Time Estimation for Stratix V Devices**

| Variant | Member Code | Active Serial (1) | | | Fast Passive Parallel (2) | | |
|---|---|---|---|---|---|---|---|
| | | Width | DCLK (MHz) | Min Config Time (s) | Width | DCLK (MHz) | Min Config Time (s) |
| GX | A3 | 4 | 100 | 0.534 | 32 | 100 | 0.067 |
| | | 4 | 100 | 0.344 | 32 | 100 | 0.043 |
| | A4 | 4 | 100 | 0.534 | 32 | 100 | 0.067 |
| | A5 | 4 | 100 | 0.675 | 32 | 100 | 0.084 |
| | A7 | 4 | 100 | 0.675 | 32 | 100 | 0.084 |
| | A9 | 4 | 100 | 0.857 | 32 | 100 | 0.107 |
| | AB | 4 | 100 | 0.857 | 32 | 100 | 0.107 |
| | B5 | 4 | 100 | 0.676 | 32 | 100 | 0.085 |
| | B6 | 4 | 100 | 0.676 | 32 | 100 | 0.085 |
| | B9 | 4 | 100 | 0.857 | 32 | 100 | 0.107 |
| | BB | 4 | 100 | 0.857 | 32 | 100 | 0.107 |
| GT | C5 | 4 | 100 | 0.675 | 32 | 100 | 0.084 |
| | C7 | 4 | 100 | 0.675 | 32 | 100 | 0.084 |

Table 51 lists the timing parameters for Stratix V devices for FPP configuration when the DCLK-to-DATA[] ratio is more than 1.

**Table 51. FPP Timing Parameters for Stratix V Devices When the DCLK-to-DATA[] Ratio is >1 (1)**

| Symbol | Parameter | Minimum | Maximum | Units |
|---|---|---|---|---|
| $t_{CF2CD}$ | nCONFIG low to CONF_DONE low | — | 600 | ns |
| $t_{CF2ST0}$ | nCONFIG low to nSTATUS low | — | 600 | ns |
| $t_{CFG}$ | nCONFIG low pulse width | 2 | — | µs |
| $t_{STATUS}$ | nSTATUS low pulse width | 268 | 1,506 (2) | µs |
| $t_{CF2ST1}$ | nCONFIG high to nSTATUS high | — | 1,506 (2) | µs |
| $t_{CF2CK}$ (5) | nCONFIG high to first rising edge on DCLK | 1,506 | — | µs |
| $t_{ST2CK}$ (5) | nSTATUS high to first rising edge of DCLK | 2 | — | µs |
| $t_{DSU}$ | DATA[] setup time before rising edge on DCLK | 5.5 | — | ns |
| $t_{DH}$ | DATA[] hold time after rising edge on DCLK | N–1/$f_{DCLK}$ (5) | — | s |
| $t_{CH}$ | DCLK high time | 0.45 × 1/$f_{MAX}$ | — | s |
| $t_{CL}$ | DCLK low time | 0.45 × 1/$f_{MAX}$ | — | s |
| $t_{CLK}$ | DCLK period | 1/$f_{MAX}$ | — | s |
| $f_{MAX}$ | DCLK frequency (FPP ×8/×16) | — | 125 | MHz |
| | DCLK frequency (FPP ×32) | — | 100 | MHz |
| $t_R$ | Input rise time | — | 40 | ns |
| $t_F$ | Input fall time | — | 40 | ns |
| $t_{CD2UM}$ | CONF_DONE high to user mode (3) | 175 | 437 | µs |
| $t_{CD2CU}$ | CONF_DONE high to CLKUSR enabled | 4 × maximum DCLK period | — | — |
| $t_{CD2UMC}$ | CONF_DONE high to user mode with CLKUSR option on | $t_{CD2CU}$ + (8576 × CLKUSR period) (4) | — | — |

**Notes to Table 51:**

(1) Use these timing parameters when you use the decompression and design security features.

(2) You can obtain this value if you do not delay configuration by extending the nCONFIG or nSTATUS low pulse width.

(3) The minimum and maximum numbers apply only if you use the internal oscillator as the clock source for initializing the device.

(4) To enable the CLKUSR pin as the initialization clock source and to obtain the maximum frequency specification on these pins, refer to the Initialization section of the "Configuration, Design Security, and Remote System Upgrades in Stratix V Devices" chapter.

(5) N is the DCLK-to-DATA ratio and $f_{DCLK}$ is the DCLK frequency the system is operating.

(6) If nSTATUS is monitored, follow the $t_{ST2CK}$ specification. If nSTATUS is not monitored, follow the $t_{CF2CK}$ specification.

## Active Serial Configuration Timing

Table 52 lists the DCLK frequency specification in the AS configuration scheme.

**Table 52. DCLK Frequency Specification in the AS Configuration Scheme (1), (2)**

| Minimum | Typical | Maximum | Unit |
|---|---|---|---|
| 5.3 | 7.9 | 12.5 | MHz |
| 10.6 | 15.7 | 25.0 | MHz |
| 21.3 | 31.4 | 50.0 | MHz |
| 42.6 | 62.9 | 100.0 | MHz |

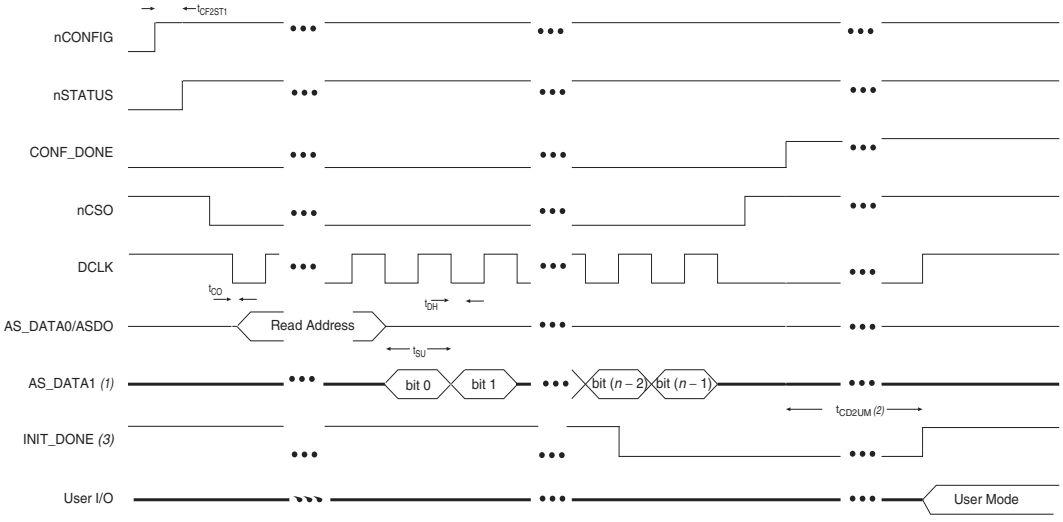
**Notes to Table 52:**

(1) This applies to the DCLK frequency specification when using the internal oscillator as the configuration clock source.

(2) The AS multi-device configuration scheme does not support DCLK frequency of 100 MHz.

Figure 14 shows the single-device configuration setup for an AS ×1 mode.

**Figure 14. AS Configuration Timing**




**Notes to Figure 14:**

(1) If you are using AS ×4 mode, this signal represents the AS_DATA[3..0] and EPCQ sends in 4-bits of data for each DCLK cycle.

(2) The initialization clock can be from internal oscillator or CLKUSR pin.

(3) After the option bit to enable the INIT_DONE pin is configured into the device, the INIT_DONE goes low.

Table 53 lists the timing parameters for AS ×1 and AS ×4 configurations in Stratix V devices.

**Table 53. AS Timing Parameters for AS ×1 and AS ×4 Configurations in Stratix V Devices (1), (2) (Part 1 of 2)**

| Symbol | Parameter | Minimum | Maximum | Units |
|---|---|---|---|---|
| $t_{CO}$ | DCLK falling edge to AS_DATA0/ASDO output | — | 2 | ns |
| $t_{SU}$ | Data setup time before falling edge on DCLK | 1.5 | — | ns |
| $t_{H}$ | Data hold time after falling edge on DCLK | 0 | — | ns |

**Table 53. AS Timing Parameters for AS ×1 and AS ×4 Configurations in Stratix V Devices (1), (2) (Part 2 of 2)**

| Symbol | Parameter | Minimum | Maximum | Units |
|---|---|---|---|---|
| $t_{CD2UM}$ | CONF_DONE high to user mode (3) | 175 | 437 | µs |
| $t_{CD2CU}$ | CONF_DONE high to CLKUSR enabled | 4 × maximum DCLK period | — | — |
| $t_{CD2UMC}$ | CONF_DONE high to user mode with CLKUSR option on | $t_{CD2CU}$ + (8576 × CLKUSR period) | — | — |

**Notes to Table 53:**

(1) The minimum and maximum numbers apply only if you choose the internal oscillator as the clock source for initializing the device.

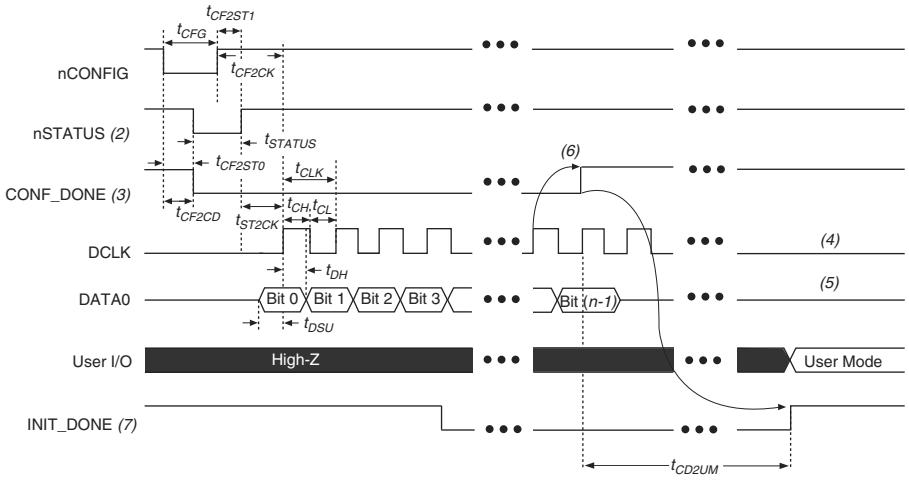
(2) $t_{CF2CD}$, $t_{CF2ST0}$, $t_{CFG}$, $t_{STATUS}$, and $t_{CF2ST1}$ timing parameters are identical to the timing parameters for PS mode listed in Table 54 on page 63.

(3) To enable the CLKUSR pin as the initialization clock source and to obtain the maximum frequency specification on this pin, refer to the Initialization section of the "Configuration, Design Security, and Remote System Upgrades in Stratix V Devices" chapter.

## Passive Serial Configuration Timing

Figure 15 shows the timing waveform for a passive serial (PS) configuration when using a MAX II device, MAX V device, or microprocessor as an external host.

**Figure 15. PS Configuration Timing Waveform (1)**




**Notes to Figure 15:**

(1) The beginning of this waveform shows the device in user mode. In user mode, nCONFIG, nSTATUS, and CONF_DONE are at logic high levels. When nCONFIG is pulled low, a reconfiguration cycle begins.

(2) After power-up, the Stratix V device holds nSTATUS low for the time of the POR delay.

(3) After power-up, before and during configuration, CONF_DONE is low.

(4) Do not leave DCLK floating after configuration. You can drive it high or low, whichever is more convenient.

(5) DATA0 is available as a user I/O pin after configuration. The state of this pin depends on the dual-purpose pin settings in the **Device and Pins Option**.

(6) To ensure a successful configuration, send the entire configuration data to the Stratix V device. CONF_DONE is released high after the Stratix V device receives all the configuration data successfully. After CONF_DONE goes high, send two additional falling edges on DCLK to begin initialization and enter user mode.

(7) After the option bit to enable the INIT_DONE pin is configured into the device, the INIT_DONE goes low.

**Table 58. IOE Programmable Delay for Stratix V Devices (Part 2 of 2)**

| Parameter (1) | Available Settings | Min Offset (2) | Fast Model | | Slow Model | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | Industrial | Commercial | C1 | C2 | C3 | C4 | I2 | I3, I3YY | I4 | Unit |
| D3 | 8 | 0 | 1.587 | 1.699 | 2.793 | 2.793 | 2.992 | 3.192 | 2.811 | 3.047 | 3.257 | ns |
| D4 | 64 | 0 | 0.464 | 0.492 | 0.838 | 0.838 | 0.924 | 1.011 | 0.843 | 0.920 | 1.006 | ns |
| D5 | 64 | 0 | 0.464 | 0.493 | 0.838 | 0.838 | 0.924 | 1.011 | 0.844 | 0.921 | 1.006 | ns |
| D6 | 32 | 0 | 0.229 | 0.244 | 0.415 | 0.415 | 0.458 | 0.503 | 0.418 | 0.456 | 0.499 | ns |

**Notes to Table 58:**

(1) You can set this value in the Quartus II software by selecting **D1**, **D2**, **D3**, **D5**, and **D6** in the **Assignment Name** column of **Assignment Editor**.

(2) Minimum offset does not include the intrinsic delay.

## Programmable Output Buffer Delay

Table 59 lists the delay chain settings that control the rising and falling edge delays of the output buffer. The default delay is 0 ps.

**Table 59. Programmable Output Buffer Delay for Stratix V Devices (1)**

| Symbol | Parameter | Typical | Unit |
|---|---|---|---|
| $D_{OUTBUF}$ | Rising and/or falling edge delay | 0 (default) | ps |
| | | 25 | ps |
| | | 50 | ps |
| | | 75 | ps |

**Note to Table 59:**

(1) You can set the programmable output buffer delay in the Quartus II software by setting the **Output Buffer Delay Control** assignment to either positive, negative, or both edges, with the specific values stated here (in ps) for the **Output Buffer Delay** assignment.

# Glossary

Table 60 lists the glossary for this chapter.

**Table 60. Glossary (Part 1 of 4)**

| Letter | Subject | Definitions |
|---|---|---|
| **A**<br>B<br>C | — | — |
| **D** | — | — |
| **E** | — | — |
| **F** | $f_{HSCLK}$ | Left and right PLL input clock frequency. |
| | $f_{HSDR}$ | High-speed I/O block—Maximum and minimum **LVDS** data transfer rate ($f_{HSDR}$ = 1/TUI), non-DPA. |
| | $f_{HSDRDPA}$ | High-speed I/O block—Maximum and minimum **LVDS** data transfer rate ($f_{HSDRDPA}$ = 1/TUI), DPA. |

**Table 60. Glossary (Part 4 of 4)**

| Letter | Subject | Definitions |
|---|---|---|
| V | $V_{CM(DC)}$ | DC common mode input voltage. |
| | $V_{ICM}$ | Input common mode voltage—The common mode of the differential signal at the receiver. |
| | $V_{ID}$ | Input differential voltage swing—The difference in voltage between the positive and complementary conductors of a differential transmission at the receiver. |
| | $V_{DIF(AC)}$ | AC differential input voltage—Minimum AC input differential voltage required for switching. |
| | $V_{DIF(DC)}$ | DC differential input voltage— Minimum DC input differential voltage required for switching. |
| | $V_{IH}$ | Voltage input high—The minimum positive voltage applied to the input which is accepted by the device as a logic high. |
| | $V_{IH(AC)}$ | High-level AC input voltage |
| | $V_{IH(DC)}$ | High-level DC input voltage |
| | $V_{IL}$ | Voltage input low—The maximum positive voltage applied to the input which is accepted by the device as a logic low. |
| | $V_{IL(AC)}$ | Low-level AC input voltage |
| | $V_{IL(DC)}$ | Low-level DC input voltage |
| | $V_{OCM}$ | Output common mode voltage—The common mode of the differential signal at the transmitter. |
| | $V_{OD}$ | Output differential voltage swing—The difference in voltage between the positive and complementary conductors of a differential transmission at the transmitter. |
| | $V_{SWING}$ | Differential input voltage |
| | $V_X$ | Input differential cross point voltage |
| | $V_{OX}$ | Output differential cross point voltage |
| W | W | High-speed I/O block—clock boost factor |
| X<br>Y<br>Z | — | — |

**Table 61. Document Revision History (Part 3 of 3)**

| Date | Version | Changes |
|---|---|---|
| May 2013 | 2.7 | ■ Updated Table 2, Table 6, Table 7, Table 20, Table 23, Table 27, Table 47, Table 60<br>■ Added Table 24, Table 48<br>■ Updated Figure 9, Figure 10, Figure 11, Figure 12 |
| February 2013 | 2.6 | ■ Updated Table 7, Table 9, Table 20, Table 23, Table 27, Table 30, Table 31, Table 35, Table 46<br>■ Updated "Maximum Allowed Overshoot and Undershoot Voltage" |
| December 2012 | 2.5 | ■ Updated Table 3, Table 6, Table 7, Table 8, Table 23, Table 24, Table 25, Table 27, Table 30, Table 32, Table 35<br>■ Added Table 33<br>■ Added "Fast Passive Parallel Configuration Timing"<br>■ Added "Active Serial Configuration Timing"<br>■ Added "Passive Serial Configuration Timing"<br>■ Added "Remote System Upgrades"<br>■ Added "User Watchdog Internal Circuitry Timing Specification"<br>■ Added "Initialization"<br>■ Added "Raw Binary File Size" |
| June 2012 | 2.4 | ■ Added Figure 1, Figure 2, and Figure 3.<br>■ Updated Table 1, Table 2, Table 3, Table 6, Table 11, Table 22, Table 23, Table 27,Table 29, Table 30, Table 31, Table 32, Table 35, Table 38, Table 39, Table 40, Table 41, Table 43, Table 56, and Table 59.<br>■ Various edits throughout to fix bugs.<br>■ Changed title of document to *Stratix V Device Datasheet*.<br>■ Removed document from the Stratix V handbook and made it a separate document. |
| February 2012 | 2.3 | ■ Updated Table 1–22, Table 1–29, Table 1–31, and Table 1–31. |
| December 2011 | 2.2 | ■ Added Table 2–31.<br>■ Updated Table 2–28 and Table 2–34. |
| November 2011 | 2.1 | ■ Added Table 2–2 and Table 2–21 and updated Table 2–5 with information about Stratix V GT devices.<br>■ Updated Table 2–11, Table 2–13, Table 2–20, and Table 2–25.<br>■ Various edits throughout to fix SPRs. |
| May 2011 | 2.0 | ■ Updated Table 2–4, Table 2–18, Table 2–19, Table 2–21, Table 2–22, Table 2–23, and Table 2–24.<br>■ Updated the "DQ Logic Block and Memory Output Clock Jitter Specifications" title.<br>■ Chapter moved to Volume 1.<br>■ Minor text edits. |
| December 2010 | 1.1 | ■ Updated Table 1–2, Table 1–4, Table 1–19, and Table 1–23.<br>■ Converted chapter to the new template.<br>■ Minor text edits. |
| July 2010 | 1.0 | Initial release. |