### Intel - 5SGXEA3K2F40I2N Datasheet





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#### Details

Product Status	Obsolete
Number of LABs/CLBs	128300
Number of Logic Elements/Cells	340000
Total RAM Bits	19456000
Number of I/O	696
Number of Gates	-
Voltage - Supply	0.87V ~ 0.93V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	1517-BBGA, FCBGA
Supplier Device Package	1517-FBGA (40x40)
Purchase URL	https://www.e-xfl.com/product-detail/intel/5sgxea3k2f40i2n

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Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

								·
Transceiver Speed				Core Spe	ed Grade			
Grade	C1	C2, C2L	C3	C4	12, 12L	13, 13L	<b>I</b> 3YY	14
3 GX channel—8.5 Gbps	_	Yes	Yes	Yes	_	Yes	Yes <sup>(4)</sup>	Yes

### Table 1. Stratix V GX and GS Commercial and Industrial Speed Grade Offering <sup>(1), (2), (3)</sup> (Part 2 of 2)

Notes to Table 1:

(1) C = Commercial temperature grade; I = Industrial temperature grade.

(2) Lower number refers to faster speed grade.

(3) C2L, I2L, and I3L speed grades are for low-power devices.

(4) I3YY speed grades can achieve up to 10.3125 Gbps.

Table 2 lists the industrial and commercial speed grades for the Stratix V GT devices. **Table 2. Stratix V GT Commercial and Industrial Speed Grade Offering** <sup>(1)</sup>, <sup>(2)</sup>

Transseiver Speed Grade		Core Speed Grade									
Transceiver Speeu draue	C1	C2	12	13							
2 GX channel—12.5 Gbps GT channel—28.05 Gbps	Yes	Yes	_	_							
3 GX channel—12.5 Gbps GT channel—25.78 Gbps	Yes	Yes	Yes	Yes							

#### Notes to Table 2:

(1) C = Commercial temperature grade; I = Industrial temperature grade.

(2) Lower number refers to faster speed grade.

### **Absolute Maximum Ratings**

Absolute maximum ratings define the maximum operating conditions for Stratix V devices. The values are based on experiments conducted with the devices and theoretical modeling of breakdown and damage mechanisms. The functional operation of the device is not implied for these conditions.



Conditions other than those listed in Table 3 may cause permanent damage to the device. Additionally, device operation at the absolute maximum ratings for extended periods of time may have adverse effects on the device.

TANIC J. ANSULULC MAXIMUM NALINYS IVI SUALIX V DEVICES (FAIL I UI Z)	Table 3.	<b>Absolute Maximum</b>	Ratings	for Stratix \	/ Devices	(Part 1 of 2)
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Symbol	Description	Minimum	Maximum	Unit
V <sub>CC</sub>	Power supply for core voltage and periphery circuitry	-0.5	1.35	V
V <sub>CCPT</sub>	Power supply for programmable power technology	-0.5	1.8	V
V <sub>CCPGM</sub>	Power supply for configuration pins	-0.5	3.9	V
V <sub>CC_AUX</sub>	Auxiliary supply for the programmable power technology	-0.5	3.4	V
V <sub>CCBAT</sub>	Battery back-up power supply for design security volatile key register	-0.5	3.9	V
V <sub>CCPD</sub>	I/O pre-driver power supply	-0.5	3.9	V
V <sub>CCIO</sub>	I/O power supply	-0.5	3.9	V

Symbol	Description	Condition	Min <sup>(4)</sup>	Тур	Max <sup>(4)</sup>	Unit
t <sub>RAMP</sub>	Power supply ramp time	Standard POR	200 µs	_	100 ms	—
	Power supply ramp time	Fast POR	200 µs		4 ms	

### Table 6. Recommended Operating Conditions for Stratix V Devices (Part 2 of 2)

#### Notes to Table 6:

(1)  $V_{CCPD}$  must be 2.5 V when  $V_{CCI0}$  is 2.5, 1.8, 1.5, 1.35, 1.25 or 1.2 V.  $V_{CCPD}$  must be 3.0 V when  $V_{CCI0}$  is 3.0 V.

(2) If you do not use the design security feature in Stratix V devices, connect V<sub>CCBAT</sub> to a 1.2- to 3.0-V power supply. Stratix V power-on-reset (POR) circuitry monitors V<sub>CCBAT</sub>. Stratix V devices will not exit POR if V<sub>CCBAT</sub> stays at logic low.

(3) C2L and I2L can also be run at 0.90 V for legacy boards that were designed for the C2 and I2 speed grades.

(4) The power supply value describes the budget for the DC (static) power supply tolerance and does not include the dynamic tolerance requirements. Refer to the PDN tool for the additional budget for the dynamic tolerance requirements.

Table 7 lists the transceiver power supply recommended operating conditions for Stratix V GX, GS, and GT devices.

# Table 7. Recommended Transceiver Power Supply Operating Conditions for Stratix V GX, GS, and GT Devices (Part 1 of 2)

Symbol	Description	Devices	Minimum <sup>(4)</sup>	Typical	Maximum <sup>(4)</sup>	Unit
V <sub>CCA GXBL</sub>	Transceiver channel PLL power supply (left		2.85	3.0	3.15	V
(1), (3)	side)	un, us, ui	2.375	2.5	2.625	v
V <sub>CCA_GXBR</sub>	Transceiver channel PLL power supply (right	CV CS	2.85	3.0	3.15	V
(1), (3)	side)	ux, us	2.375	2.5	2.625	v
V <sub>CCA_GTBR</sub>	Transceiver channel PLL power supply (right side)	GT	2.85	3.0	3.15	V
	Transceiver hard IP power supply (left side; C1, C2, I2, and I3YY speed grades)	GX, GS, GT	0.87	0.9	0.93	V
V <sub>CCHIP_L</sub>	Transceiver hard IP power supply (left side; C2L, C3, C4, I2L, I3, I3L, and I4 speed grades)	GX, GS, GT	0.82	0.85	0.88	V
	Transceiver hard IP power supply (right side; C1, C2, I2, and I3YY speed grades)	GX, GS, GT	0.87	0.9	0.93	V
V <sub>CCHIP_R</sub>	Transceiver hard IP power supply (right side; C2L, C3, C4, I2L, I3, I3L, and I4 speed grades)	GX, GS, GT	0.82	0.85	0.88	V
	Transceiver PCS power supply (left side; C1, C2, I2, and I3YY speed grades)	GX, GS, GT	0.87	0.9	0.93	V
V <sub>CCHSSI_L</sub>	Transceiver PCS power supply (left side; C2L, C3, C4, I2L, I3, I3L, and I4 speed grades)	GX, GS, GT	0.82	0.85	0.88	V
	Transceiver PCS power supply (right side; C1, C2, I2, and I3YY speed grades)	GX, GS, GT	0.87	0.9	0.93	V
V <sub>CCHSSI_R</sub>	Transceiver PCS power supply (right side; C2L, C3, C4, I2L, I3, I3L, and I4 speed grades)	GX, GS, GT	0.82	0.85	0.88	V
			0.82	0.85	0.88	
V <sub>CCR_GXBL</sub>	Receiver analog nower supply (left side)		0.87	0.90	0.93	v
(2) _	Therefore analog power supply (left Slue)	un, uo, ui	0.97	1.0	1.03	v
			1.03	1.05	1.07	

## **Switching Characteristics**

This section provides performance characteristics of the Stratix V core and periphery blocks.

These characteristics can be designated as Preliminary or Final.

- Preliminary characteristics are created using simulation results, process data, and other known parameters. The title of these tables show the designation as "Preliminary."
- Final numbers are based on actual silicon characterization and testing. The numbers reflect the actual performance of the device under worst-case silicon process, voltage, and junction temperature conditions. There are no designations on finalized tables.

### **Transceiver Performance Specifications**

This section describes transceiver performance specifications.

Table 23 lists the Stratix V GX and GS transceiver specifications.

Table 23.	Transceiver 3	Specifications	for Stratix	V GX	and GS	Devices	(1)	(Part 1	nf 7	۱
Table 20.	TIANSUCIACI	opeonitionationa	IUI UIIAIIA	I UA	anu uu	DEVICES	• •	(1 61 6 1		

Symbol/	Conditions	Tra	nsceive Grade	r Speed 1	Transceiver Speed Grade 2			Trai	er Speed e 3	Unit	
Description		Min	Тур	Max	Min	Тур	Max	Min	Тур	Max	
Reference Clock											
Supported I/O	Dedicated reference clock pin	1.2-V	2-V PCML, 1.4-V PCML, 1.5-V PCML, 2.5-V PCML, Differential LVPECL, LVDS, and HCSL								/DS, and
Standards	RX reference clock pin			1.4-V PCMI	L, 1.5-V	PCML,	2.5-V PCM	l, lvpe	CL, and	d LVDS	
Input Reference Clock Frequency (CMU PLL) <sup>(8)</sup>	_	40		710	40	_	710	40	_	710	MHz
Input Reference Clock Frequency (ATX PLL) <sup>(8)</sup>		100		710	100		710	100		710	MHz
Rise time	Measure at ±60 mV of differential signal <sup>(26)</sup>			400	_		400			400	ns
Fall time	Measure at ±60 mV of differential signal <sup>(26)</sup>		_	400	_		400			400	μσ
Duty cycle		45		55	45		55	45	—	55	%
Spread-spectrum modulating clock frequency	PCI Express® (PCIe <sup>®</sup> )	30		33	30		33	30	_	33	kHz

Symbol/	Conditions	Trai	nsceive Grade	r Speed 1	Transceiver Speed Grade 2			Trar	nsceive Grade	er Speed e 3	Unit
Description		Min	Тур	Max	Min	Тур	Max	Min	Тур	Max	
Reconfiguration clock (mgmt_clk_clk) frequency	_	100		125	100		125	100	_	125	MHz
Receiver											
Supported I/O Standards	_			1.4-V PCMI	L, 1.5-V	PCML,	2.5-V PCM	L, LVPE	CL, and	d LVDS	
Data rate (Standard PCS) <sup>(9), (23)</sup>	_	600	_	12200	600	_	12200	600	_	8500/ 10312.5 (24)	Mbps
Data rate (10G PCS) <sup>(9),</sup> <sup>(23)</sup>	_	600	_	14100	600	_	12500	600	_	8500/ 10312.5 (24)	Mbps
Absolute V <sub>MAX</sub> for a receiver pin <sup>(5)</sup>	_	_	_	1.2	_	_	1.2	_	_	1.2	V
Absolute V <sub>MIN</sub> for a receiver pin	_	-0.4	_	_	-0.4	_	_	-0.4	_	_	V
Maximum peak- to-peak differential input voltage V <sub>ID</sub> (diff p- p) before device configuration <sup>(22)</sup>	_	_	_	1.6	_	_	1.6	_		1.6	V
Maximum peak- to-peak	V <sub>CCR_GXB</sub> = 1.0 V/1.05 V (V <sub>ICM</sub> = 0.70 V)	_	_	2.0	_	_	2.0	_	_	2.0	V
voltage $V_{ID}$ (diff p- p) after device configuration <sup>(18)</sup> .	V <sub>CCR_GXB</sub> = 0.90 V (V <sub>ICM</sub> = 0.6 V)			2.4			2.4			2.4	V
(22)	$V_{CCR_GXB} = 0.85 V$ (V <sub>ICM</sub> = 0.6 V)			2.4			2.4		_	2.4	V
Minimum differential eye opening at receiver serial input pins <sup>(6), (22),</sup> (27)	_	85			85			85	_	_	mV

### Table 23. Transceiver Specifications for Stratix V GX and GS Devices <sup>(1)</sup> (Part 3 of 7)

Symbol/	Conditions	Trai	nsceive Grade	r Speed 1	Trai	nsceive Grade	r Speed 2	Trai	Unit		
Description		Min	Тур	Max	Min	Тур	Max	Min	Тур	Max	
	DC Gain Setting = 0		0	_	_	0	_	_	0	—	dB
	DC Gain Setting = 1	_	2		_	2	_	_	2	_	dB
Programmable DC gain	DC Gain Setting = 2	_	4	_	_	4	_	_	4	_	dB
	DC Gain Setting = 3	_	6	_	_	6	_	_	6	_	dB
	DC Gain Setting = 4		8			8	—		8	_	dB
Transmitter											
Supported I/O Standards	_				-	1.4-V ar	nd 1.5-V PC	ML			
Data rate (Standard PCS)	_	600	_	12200	600	_	12200	600	_	8500/ 10312.5 (24)	Mbps
Data rate (10G PCS)	_	600	_	14100	600	_	12500	600	_	8500/ 10312.5 (24)	Mbps
	85-Ω setting	_	85 ± 20%	_	_	85 ± 20%	_	_	85 ± 20%	—	Ω
Differential on-	100-Ω setting	_	100 ± 20%	_	_	100 ± 20%	_	_	100 ± 20%	_	Ω
chip termination resistors	120-Ω setting		120 ± 20%	_		120 ± 20%	_		120 ± 20%	_	Ω
	150-Ω setting	_	150 ± 20%			150 ± 20%	_		150 ± 20%	_	Ω
V <sub>OCM</sub> (AC coupled)	0.65-V setting	_	650		_	650	_	_	650	—	mV
V <sub>OCM</sub> (DC coupled)	_	_	650	_	_	650		_	650	_	mV
Rise time <sup>(7)</sup>	20% to 80%	30	—	160	30	—	160	30	—	160	ps
Fall time <sup>(7)</sup>	80% to 20%	30		160	30		160	30	—	160	ps
Intra-differential pair skew	Tx V <sub>CM</sub> = 0.5 V and slew rate of 15 ps	_	_	15			15		_	15	ps
Intra-transceiver block transmitter channel-to- channel skew	x6 PMA bonded mode	_	_	120	_	_	120	_		120	ps

### Table 23. Transceiver Specifications for Stratix V GX and GS Devices <sup>(1)</sup> (Part 5 of 7)

Mada (2)	Transceiver	PMA Width	20	20	16	16	10	10	8	8
	Speed Grade	PCS/Core Width	40	20	32	16	20	10	16	8
	1	C1, C2, C2L, I2, I2L core speed grade	12.2	11.4	9.76	9.12	6.5	5.8	5.2	4.72
FIFO	ŋ	C1, C2, C2L, I2, I2L core speed grade	12.2	11.4	9.76	9.12	6.5	5.8	5.2	4.72
	۷	C3, I3, I3L core speed grade	9.8	9.0	7.84	7.2	5.3	4.7	4.24	3.76
		C1, C2, C2L, I2, I2L core speed grade	8.5	8.5	8.5	8.5	6.5	5.8	5.2	4.72
	3	I3YY core speed grade	10.3125	10.3125	7.84	7.2	5.3	4.7	4.24	3.76
	5	C3, I3, I3L core speed grade	8.5	8.5	7.84	7.2	5.3	4.7	4.24	3.76
		C4, I4 core speed grade	8.5	8.2	7.04	6.56	4.8	4.2	3.84	3.44
	1	C1, C2, C2L, I2, I2L core speed grade	12.2	11.4	9.76	9.12	6.1	5.7	4.88	4.56
	ŋ	C1, C2, C2L, I2, I2L core speed grade	12.2	11.4	9.76	9.12	6.1	5.7	4.88	4.56
	۷	C3, I3, I3L core speed grade	9.8	9.0	7.92	7.2	4.9	4.5	3.96	3.6
Register		C1, C2, C2L, I2, I2L core speed grade	10.3125	10.3125	10.3125	10.3125	6.1	5.7	4.88	4.56
	3	I3YY core speed grade	10.3125	10.3125	7.92	7.2	4.9	4.5	3.96	3.6
	J	C3, I3, I3L core speed grade	8.5	8.5	7.92	7.2	4.9	4.5	3.96	3.6
		C4, I4 core speed grade	8.5	8.2	7.04	6.56	4.4	4.1	3.52	3.28

Table 25 shows the approximate maximum data rate using the standard PCS.

Table 25. Stratix V Standard PCS Approximate Maximum Date Rate (1), (3)

Notes to Table 25:

(1) The maximum data rate is in Gbps.

(2) The Phase Compensation FIFO can be configured in FIFO mode or register mode. In the FIFO mode, the pointers are not fixed, and the latency can vary. In the register mode the pointers are fixed for low latency.

(3) The maximum data rate is also constrained by the transceiver speed grade. Refer to Table 1 for the transceiver speed grade.

Table 27 shows the  $V_{\text{OD}}$  settings for the GX channel.

Symbol	V <sub>op</sub> Setting	V <sub>od</sub> Value (mV)	V <sub>op</sub> Setting	V <sub>op</sub> Value (mV)
	0 (1)	0	32	640
	1 (1)	20	33	660
	2 (1)	40	34	680
	3 (1)	60	35	700
	4 (1)	80	36	720
	5 <sup>(1)</sup>	100	37	740
	6	120	38	760
	7	140	39	780
	8	160	40	800
	9	180	41	820
	10	200	42	840
	11	220	43	860
	12	240	44	880
	13 260		45	900
	14	280	46	920
$V_{0D}$ differential peak to peak	15	300	47	940
typical <sup>(3)</sup>	16	320	48	960
	17	340	49	980
	18	360	50	1000
	19	380	51	1020
	20	400	52	1040
	21	420	53	1060
	22	440	54	1080
	23	460	55	1100
	24	480	56	1120
	25	500	57	1140
	26	520	58	1160
	27	540	59	1180
	28	560	60	1200
	29	580	61	1220
	30	600	62	1240
	31	620	63	1260

Table 27. Typical V\_{0D} Setting for GX Channel, TX Termination = 100  $\Omega^{\left(2\right)}$ 

#### Note to Table 27:

(1) If TX termination resistance =  $100\Omega$ , this VOD setting is illegal.

(2) The tolerance is +/-20% for all VOD settings except for settings 2 and below.

(3) Refer to Figure 2.

	Table 28.	<b>Transceiver S</b>	pecifications	for Stratix V	GT Devices	(Part 4 of 5) (1)
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Symbol/	Conditions	s	Transceive peed Grade	r 2	ר Sp	Fransceive Deed Grade	r 3	Unit
Description		Min	Тур	Max	Min	Тур	Max	
Data rate	GT channels	19,600	_	28,050	19,600		25,780	Mbps
Differential on-chip	GT channels	_	100	—		100	_	Ω
termination resistors	GX channels				(8)			
	GT channels	_	500	_		500	_	mV
V <sub>OCM</sub> (AC Coupled)	GX channels		•	•	(8)			
Dice/Fell time	GT channels	_	15	—	—	15	—	ps
Rise/Fail lime	GX channels				(8)			
Intra-differential pair skew	GX channels				(8)			
Intra-transceiver block transmitter channel-to- channel skew	r block (8)							
Inter-transceiver block transmitter channel-to- channel skew	GX channels				(8)			
CMU PLL								
Supported Data Range	—	600		12500	600		8500	Mbps
t <sub>pll_powerdown</sub> <sup>(13)</sup>	—	1	—	—	1	_	—	μs
t <sub>pll_lock</sub> <sup>(14)</sup>	—	_	—	10	_	_	10	μs
ATX PLL								
	VCO post- divider L=2	8000	_	12500	8000	_	8500	Mbps
	L=4	4000	—	6600	4000	_	6600	Mbps
Supported Data Rate	L=8	2000	—	3300	2000	_	3300	Mbps
Range for GX Channels	L=8, Local/Central Clock Divider =2	1000	_	1762.5	1000	_	1762.5	Mbps
Supported Data Rate Range for GT Channels	VCO post- divider L=2	9800	_	14025	9800	_	12890	Mbps
t <sub>pll_powerdown</sub> <sup>(13)</sup>	—	1	—	—	1	_	—	μs
t <sub>pll_lock</sub> <sup>(14)</sup>	—	_	—	10	_	_	10	μs
fPLL								
Supported Data Range		600		3250/ 3.125 <sup>(23)</sup>	600		3250/ 3.125 <sup>(23)</sup>	Mbps
t <sub>pll_powerdown</sub> <sup>(13)</sup>	—	1	—	—	1	—	—	μs

Figure 6 shows the Stratix V DC gain curves for GT channels.

Figure 6. DC Gain Curves for GT Channels

### **Transceiver Characterization**

This section summarizes the Stratix V transceiver characterization results for compliance with the following protocols:

- Interlaken
- 40G (XLAUI)/100G (CAUI)
- 10GBase-KR
- QSGMII
- XAUI
- SFI
- Gigabit Ethernet (Gbe / GIGE)
- SPAUI
- Serial Rapid IO (SRIO)
- CPRI
- OBSAI
- Hyper Transport (HT)
- SATA
- SAS
- CEI

- XFI
- ASI
- HiGig/HiGig+
- HiGig2/HiGig2+
- Serial Data Converter (SDC)
- GPON
- SDI
- SONET
- Fibre Channel (FC)
- PCIe
- QPI
- SFF-8431

Download the Stratix V Characterization Report Tool to view the characterization report summary for these protocols.

### **Core Performance Specifications**

This section describes the clock tree, phase-locked loop (PLL), digital signal processing (DSP), memory blocks, configuration, and JTAG specifications.

### **Clock Tree Specifications**

Table 30 lists the clock tree specifications for Stratix V devices.

Table 30. Clock Tree Performance for Stratix V Devices (1)

	Performance							
Symbol	C1, C2, C2L, I2, and I2L	C4, I4	Unit					
Global and Regional Clock	717	650	580	MHz				
Periphery Clock	550	500	500	MHz				

### Note to Table 30:

(1) The Stratix V ES devices are limited to 600 MHz core clock tree performance.

### **PLL Specifications**

Table 31 lists the Stratix V PLL specifications when operating in both the commercial junction temperature range (0° to  $85^{\circ}$ C) and the industrial junction temperature range (-40° to  $100^{\circ}$ C).

Table 31. PLL Specifications for Stratix V Devices (Part 1 of 3)

Symbol	Parameter	Min	Тур	Max	Unit
	Input clock frequency (C1, C2, C2L, I2, and I2L speed grades)	5		800 (1)	MHz
f <sub>IN</sub>	Input clock frequency (C3, I3, I3L, and I3YY speed grades)	5		800 (1)	MHz
	Input clock frequency (C4, I4 speed grades)	5	—	650 <sup>(1)</sup>	MHz
f <sub>INPFD</sub>	Input frequency to the PFD	5	—	325	MHz
f <sub>FINPFD</sub>	Fractional Input clock frequency to the PFD	50	—	160	MHz
	PLL VCO operating range (C1, C2, C2L, I2, I2L speed grades)	600	_	1600	MHz
f <sub>VCO</sub> (9)	PLL VCO operating range (C3, I3, I3L, I3YY speed grades)	600		1600	MHz
	PLL VCO operating range (C4, I4 speed grades)	600	—	1300	MHz
t <sub>einduty</sub>	Input clock or external feedback clock input duty cycle	40	—	60	%
	Output frequency for an internal global or regional clock (C1, C2, C2L, I2, I2L speed grades)	_	_	717 <sup>(2)</sup>	MHz
f <sub>OUT</sub>	Output frequency for an internal global or regional clock (C3, I3, I3L speed grades)			650 <sup>(2)</sup>	MHz
	Output frequency for an internal global or regional clock (C4, I4 speed grades)			580 <sup>(2)</sup>	MHz
	Output frequency for an external clock output (C1, C2, C2L, I2, I2L speed grades)			800 <sup>(2)</sup>	MHz
f <sub>OUT_EXT</sub>	Output frequency for an external clock output (C3, I3, I3L speed grades)			667 <sup>(2)</sup>	MHz
	Output frequency for an external clock output (C4, I4 speed grades)			553 <sup>(2)</sup>	MHz
t <sub>outduty</sub>	Duty cycle for a dedicated external clock output (when set to <b>50%</b> )	45	50	55	%
t <sub>FCOMP</sub>	External feedback clock compensation time	_		10	ns
f <sub>dyconfigclk</sub>	Dynamic Configuration Clock used for mgmt_clk and scanclk		_	100	MHz
t <sub>LOCK</sub>	Time required to lock from the end-of-device configuration or deassertion of areset			1	ms
t <sub>DLOCK</sub>	Time required to lock dynamically (after switchover or reconfiguring any non-post-scale counters/delays)			1	ms
	PLL closed-loop low bandwidth	—	0.3	—	MHz
f <sub>CLBW</sub>	PLL closed-loop medium bandwidth	—	1.5	—	MHz
	PLL closed-loop high bandwidth (7)	—	4	-	MHz
t <sub>PLL_PSERR</sub>	Accuracy of PLL phase shift	—	—	±50	ps
t <sub>ARESET</sub>	Minimum pulse width on the areset signal	10	—	_	ns

	Conditions		C1		C2,	C2L, I	2, I2L	C3, I3, I3L, I3YY		C4,14				
Symbol	Conditions	Min	Тур	Max	Min	Тур	Max	Min	Тур	Max	Min	Тур	Max	Unit
t <sub>duty</sub>	Transmitter output clock duty cycle for both True and Emulated Differential I/O Standards	45	50	55	45	50	55	45	50	55	45	50	55	%
	True Differential I/O Standards	_	_	160	_	_	160	_	_	200	_	_	200	ps
t <sub>rise</sub> & t <sub>fall</sub>	Emulated Differential I/O Standards with three external output resistor networks			250			250			250			300	ps
TCCS	True Differential I/O Standards	_	_	150	_	_	150	_	_	150	_	_	150	ps
	Emulated Differential I/O Standards			300			300	_		300			300	ps
Receiver														
	SERDES factor J = 3 to 10 (11), (12), (13), (14), (15), (16)	150		1434	150	_	1434	150	_	1250	150	_	1050	Mbps
True Differential I/O Standards <sup>-</sup> f <sub>HSDRDPA</sub> (data rate)	SERDES factor J ≥ 4 LVDS RX with DPA (12), (14), (15), (16)	150	_	1600	150	_	1600	150	_	1600	150	_	1250	Mbps
	SERDES factor J = 2, uses DDR Registers	(6)		(7)	(6)	_	(7)	(6)	_	(7)	(6)	_	(7)	Mbps
	SERDES factor J = 1, uses SDR Register	(6)	_	(7)	(6)	_	(7)	(6)	_	(7)	(6)		(7)	Mbps

### Table 36. High-Speed I/O Specifications for Stratix V Devices (1), (2) (Part 3 of 4)

Clock Network	Parameter	Symbol	C1		C2, C2L, I2, I2L		C3, I3, I3L, I3YY		C4,14		Unit
			Min	Max	Min	Max	Min	Max	Min	Max	
	Clock period jitter	$t_{JIT(per)}$	-25	25	-25	25	-30	30	-35	35	ps
PHY Clock	Cycle-to-cycle period jitter	$t_{\rm JIT(cc)}$	-50	50	-50	50	-60	60	-70	70	ps
	Duty cycle jitter	$t_{JIT(duty)}$	-37.5	37.5	-37.5	37.5	-45	45	-56	56	ps

### Table 42. Memory Output Clock Jitter Specification for Stratix V Devices (1), (Part 2 of 2) (2), (3)

### Notes to Table 42:

(1) The clock jitter specification applies to the memory output clock pins generated using differential signal-splitter and DDIO circuits clocked by a PLL output routed on a PHY, regional, or global clock network as specified. Altera recommends using PHY clock networks whenever possible.

(2) The clock jitter specification applies to the memory output clock pins clocked by an integer PLL.

(3) The memory output clock jitter is applicable when an input jitter of 30 ps peak-to-peak is applied with bit error rate (BER) -12, equivalent to 14 sigma.

### **OCT Calibration Block Specifications**

Table 43 lists the OCT calibration block specifications for Stratix V devices.

### Table 43. OCT Calibration Block Specifications for Stratix V Devices

Symbol	Description	Min	Тур	Max	Unit
OCTUSRCLK	Clock required by the OCT calibration blocks	—	—	20	MHz
T <sub>OCTCAL</sub>	Number of OCTUSRCLK clock cycles required for OCT $\rm R_S/R_T$ calibration		1000	_	Cycles
T <sub>OCTSHIFT</sub>	Number of OCTUSRCLK clock cycles required for the OCT code to shift out	_	32	_	Cycles
T <sub>RS_RT</sub>	Time required between the dyn_term_ctrl and oe signal transitions in a bidirectional I/O buffer to dynamically switch between OCT $R_S$ and $R_T$ (Figure 10)		2.5		ns

Figure 10 shows the timing diagram for the oe and dyn\_term\_ctrl signals.

### Figure 10. Timing Diagram for oe and dyn\_term\_ctrl Signals



### FPP Configuration Timing when DCLK-to-DATA [] = 1

Figure 12 shows the timing waveform for FPP configuration when using a MAX II or MAX V device as an external host. This waveform shows timing when the DCLK-to-DATA[] ratio is 1.





#### Notes to Figure 12:

- (1) Use this timing waveform when the DCLK-to-DATA [] ratio is 1.
- (2) The beginning of this waveform shows the device in user mode. In user mode, nCONFIG, nSTATUS, and CONF\_DONE are at logic-high levels. When nCONFIG is pulled low, a reconfiguration cycle begins.
- (3) After power-up, the Stratix V device holds nstatus low for the time of the POR delay.
- (4) After power-up, before and during configuration, CONF\_DONE is low.
- (5) Do not leave DCLK floating after configuration. DCLK is ignored after configuration is complete. It can toggle high or low if required.
- (6) For FPP ×16, use DATA [15..0]. For FPP ×8, use DATA [7..0]. DATA [31..0] are available as a user I/O pin after configuration. The state of this pin depends on the dual-purpose pin settings.
- (7) To ensure a successful configuration, send the entire configuration data to the Stratix V device. CONF\_DONE is released high when the Stratix V device receives all the configuration data successfully. After CONF\_DONE goes high, send two additional falling edges on DCLK to begin initialization and enter user mode.
- (8) After the option bit to enable the INIT\_DONE pin is configured into the device, the INIT DONE goes low.



#### Figure 13. FPP Configuration Timing Waveform When the DCLK-to-DATA[] Ratio is >1 (1), (2)

#### Notes to Figure 13:

- (1) Use this timing waveform and parameters when the DCLK-to-DATA [] ratio is >1. To find out the DCLK-to-DATA [] ratio for your system, refer to Table 49 on page 55.
- (2) The beginning of this waveform shows the device in user mode. In user mode, nCONFIG, nSTATUS, and CONF\_DONE are at logic high levels. When nCONFIG is pulled low, a reconfiguration cycle begins.
- (3) After power-up, the Stratix V device holds nSTATUS low for the time as specified by the POR delay.
- (4) After power-up, before and during configuration, CONF\_DONE is low.
- (5) Do not leave DCLK floating after configuration. You can drive it high or low, whichever is more convenient.
- (6) "r" denotes the DCLK-to-DATA [] ratio. For the DCLK-to-DATA [] ratio based on the decompression and the design security feature enable settings, refer to Table 49 on page 55.
- (7) If needed, pause DCLK by holding it low. When DCLK restarts, the external host must provide data on the DATA [31..0] pins prior to sending the first DCLK rising edge.
- (8) To ensure a successful configuration, send the entire configuration data to the Stratix V device. CONF\_DONE is released high after the Stratix V device receives all the configuration data successfully. After CONF\_DONE goes high, send two additional falling edges on DCLK to begin initialization and enter user mode.
- (9) After the option bit to enable the INIT DONE pin is configured into the device, the INIT DONE goes low.

Table 54 lists the PS configuration timing parameters for Stratix V devices.

Table 54. PS Timing Parameters for Stratix V Devices

Symbol	Parameter	Minimum	Maximum	Units
t <sub>CF2CD</sub>	nCONFIG low to CONF_DONE low	—	600	ns
t <sub>CF2ST0</sub>	nCONFIG low to nSTATUS low	—	600	ns
t <sub>CFG</sub>	nCONFIG low pulse width	2	—	μS
t <sub>status</sub>	nSTATUS low pulse width	268	1,506 <sup>(1)</sup>	μS
t <sub>CF2ST1</sub>	nCONFIG high to nSTATUS high	—	1,506 <sup>(2)</sup>	μS
t <sub>CF2CK</sub> (5)	nCONFIG high to first rising edge on DCLK	1,506	—	μS
t <sub>ST2CK</sub> (5)	nSTATUS high to first rising edge of DCLK	2	—	μS
t <sub>DSU</sub>	DATA[] setup time before rising edge on DCLK	5.5	—	ns
t <sub>DH</sub>	DATA [] hold time after rising edge on DCLK	0	—	ns
t <sub>CH</sub>	DCLK high time	$0.45\times 1/f_{MAX}$	—	S
t <sub>CL</sub>	DCLK low time	$0.45\times 1/f_{MAX}$	—	S
t <sub>CLK</sub>	DCLK period	1/f <sub>MAX</sub>	—	S
f <sub>MAX</sub>	DCLK frequency	—	125	MHz
t <sub>CD2UM</sub>	CONF_DONE high to user mode <sup>(3)</sup>	175	437	μS
t <sub>CD2CU</sub>	CONF_DONE high to CLKUSR enabled	4 × maximum DCLK period	_	_
t <sub>cd2UMC</sub>	CONF_DONE high to user mode with CLKUSR option on	$t_{CD2CU}$ + (8576 × CLKUSR period) <sup>(4)</sup>	_	_

### Notes to Table 54:

(1) This value is applicable if you do not delay configuration by extending the nCONFIG or nSTATUS low pulse width.

(2) This value is applicable if you do not delay configuration by externally holding the nSTATUS low.

(3) The minimum and maximum numbers apply only if you choose the internal oscillator as the clock source for initializing the device.

(4) To enable the CLKUSR pin as the initialization clock source and to obtain the maximum frequency specification on these pins, refer to the "Initialization" section.

(5) If nSTATUS is monitored, follow the t<sub>ST2CK</sub> specification. If nSTATUS is not monitored, follow the t<sub>CF2CK</sub> specification.

### Initialization

Table 55 lists the initialization clock source option, the applicable configuration schemes, and the maximum frequency.

Table 55.	Initialization	<b>Clock Source</b>	e Option	and the	Maximum	Frequency

Initialization Clock Source	Configuration Schemes	Maximum Frequency	Minimum Number of Clock Cycles <sup>(1)</sup>
Internal Oscillator	AS, PS, FPP	12.5 MHz	
CLKUSR	AS, PS, FPP <sup>(2)</sup>	125 MHz	8576
DCLK	PS, FPP	125 MHz	

### Notes to Table 55:

(1) The minimum number of clock cycles required for device initialization.

(2) To enable CLKUSR as the initialization clock source, turn on the Enable user-supplied start-up clock (CLKUSR) option in the Quartus II software from the General panel of the Device and Pin Options dialog box.

Parameter Available Min			Fast	Slow Model								
(1)	Settings	Offset (2)	Industrial	Commercial	C1	C2	C3	C4	12	13, 13YY	14	Unit
D3	8	0	1.587	1.699	2.793	2.793	2.992	3.192	2.811	3.047	3.257	ns
D4	64	0	0.464	0.492	0.838	0.838	0.924	1.011	0.843	0.920	1.006	ns
D5	64	0	0.464	0.493	0.838	0.838	0.924	1.011	0.844	0.921	1.006	ns
D6	32	0	0.229	0.244	0.415	0.415	0.458	0.503	0.418	0.456	0.499	ns

Table 58.	IOE Pro	grammable De	ay for	Stratix V	V Devices	(Part 2 of 2	)
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#### Notes to Table 58:

(1) You can set this value in the Quartus II software by selecting D1, D2, D3, D5, and D6 in the Assignment Name column of Assignment Editor.

(2) Minimum offset does not include the intrinsic delay.

### **Programmable Output Buffer Delay**

Table 59 lists the delay chain settings that control the rising and falling edge delays of the output buffer. The default delay is 0 ps.

Symbol	Parameter	Typical	Unit
		0 (default)	ps
Dauman	Rising and/or falling edge delay	25	ps
DOUTBUF		50	ps
		75	ps

Note to Table 59:

(1) You can set the programmable output buffer delay in the Quartus II software by setting the Output Buffer Delay Control assignment to either positive, negative, or both edges, with the specific values stated here (in ps) for the Output Buffer Delay assignment.

# Glossary

Table 60 lists the glossary for this chapter.

Table 60. Glossary (Part 1 of 4)

Letter	Subject	Definitions
Α		
В	—	—
С		
D	—	_
E	—	_
F	f <sub>HSCLK</sub>	Left and right PLL input clock frequency.
	f <sub>HSDR</sub>	High-speed I/O block—Maximum and minimum <b>LVDS</b> data transfer rate (f <sub>HSDR</sub> = 1/TUI), non-DPA.
	f <sub>hsdrdpa</sub>	High-speed I/O block—Maximum and minimum <b>LVDS</b> data transfer rate (f <sub>HSDRDPA</sub> = 1/TUI), DPA.

Table 60.	Glossary	(Part 3 of 4)
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Letter	Subject	Definitions			
S	SW (sampling window)	Timing Diagram—the period of time during which the data must be valid in order to capture it correctly. The setup and hold times determine the ideal strobe position within the sampling window, as shown:         Bit Time         0.5 x TCCS       RSKM         Sampling Window       RSKM         0.5 x TCCS       RSKM			
	Single-ended voltage referenced I/O standard	The JEDEC standard for <b>SSTL</b> and <b>HSTL</b> I/O defines both the AC and DC input signal values. The AC values indicate the voltage levels at which the receiver must meet its timing specifications. The DC values indicate the voltage levels at which the final logic state of the receiver is unambiguously defined. After the receiver input has crossed the AC value, the receiver changes to the new logic state. The new logic state is then maintained as long as the input stays beyond the DC threshold. This approach is intended to provide predictable receiver timing in the presence of input waveform ringing: <i>Single-Ended Voltage Referenced I/O Standard</i> 			
	t <sub>C</sub>	High-speed receiver and transmitter input and output clock period.			
	TCCS (channel- to-channel-skew)	The timing difference between the fastest and slowest output edges, including $t_{CO}$ variation and clock skew, across channels driven by the same PLL. The clock is included in the TCCS measurement (refer to the <i>Timing Diagram</i> figure under <b>SW</b> in this table).			
	t <sub>duty</sub>	High-speed I/O block—Duty cycle on the high-speed transmitter output clock.			
т		<b>Timing Unit Interval (TUI)</b> The timing budget allowed for skew, propagation delays, and the data sampling window.			
		(TUI = 1/(receiver input clock frequency multiplication factor) = $t_c/w$ )			
	t <sub>FALL</sub>	Signal high-to-low transition time (80-20%)			
	t <sub>INCCJ</sub>	Cycle-to-cycle jitter tolerance on the PLL clock input.			
	t <sub>outpj_i0</sub>	Period jitter on the general purpose I/O driven by a PLL.			
	t <sub>outpj_dc</sub>	Period jitter on the dedicated clock output driven by a PLL.			
	<b>t</b> <sub>RISE</sub>	Signal low-to-high transition time (20-80%)			
U		_			

Letter	Subject	Definitions		
	V <sub>CM(DC)</sub>	DC common mode input voltage.		
	V <sub>ICM</sub>	Input common mode voltage—The common mode of the differential signal at the receiver.		
	V <sub>ID</sub>	Input differential voltage swing—The difference in voltage between the positive and complementary conductors of a differential transmission at the receiver.		
	V <sub>DIF(AC)</sub>	AC differential input voltage—Minimum AC input differential voltage required for switching.		
	V <sub>DIF(DC)</sub>	DC differential input voltage— Minimum DC input differential voltage required for switching.		
	V <sub>IH</sub>	Voltage input high—The minimum positive voltage applied to the input which is accepted by the device as a logic high.		
	V <sub>IH(AC)</sub>	High-level AC input voltage		
	V <sub>IH(DC)</sub>	High-level DC input voltage		
V	V <sub>IL</sub>	Voltage input low—The maximum positive voltage applied to the input which is accepted by the device as a logic low.		
	V <sub>IL(AC)</sub>	Low-level AC input voltage		
	V <sub>IL(DC)</sub>	Low-level DC input voltage		
	V <sub>OCM</sub>	Output common mode voltage—The common mode of the differential signal at the transmitter.		
	V <sub>OD</sub>	Output differential voltage swing—The difference in voltage between the positive and complementary conductors of a differential transmission at the transmitter.		
	V <sub>SWING</sub>	Differential input voltage		
	V <sub>X</sub>	Input differential cross point voltage		
	V <sub>OX</sub>	Output differential cross point voltage		
W	W	High-speed I/O block—clock boost factor		
X				
Y	—	—		
Z				

### Table 60. Glossary (Part 4 of 4)

### Table 61. Document Revision History (Part 2 of 3)

Date	Version	Changes	
		<ul> <li>Added the I3YY speed grade and changed the data rates for the GX channel in Table 1.</li> </ul>	
		<ul> <li>Added the I3YY speed grade to the V<sub>CC</sub> description in Table 6.</li> </ul>	
		<ul> <li>Added the I3YY speed grade to V<sub>CCHIP_L</sub>, V<sub>CCHIP_R</sub>, V<sub>CCHSSI_L</sub>, and V<sub>CCHSSI_R</sub> descriptions in Table 7.</li> </ul>	
		■ Added 240-Ω to Table 11.	
		Changed CDR PPM tolerance in Table 23.	
		<ul> <li>Added additional max data rate for fPLL in Table 23.</li> </ul>	
		<ul> <li>Added the I3YY speed grade and changed the data rates for transceiver speed grade 3 in Table 25.</li> </ul>	
November 2014		<ul> <li>Added the I3YY speed grade and changed the data rates for transceiver speed grade 3 in Table 26.</li> </ul>	
		<ul> <li>Changed CDR PPM tolerance in Table 28.</li> </ul>	
		<ul> <li>Added additional max data rate for fPLL in Table 28.</li> </ul>	
		<ul> <li>Changed the mode descriptions for MLAB and M20K in Table 33.</li> </ul>	
		<ul> <li>Changed the Max value of f<sub>HSCLK_OUT</sub> for the C2, C2L, I2, I2L speed grades in Table 36.</li> </ul>	
	3.3	<ul> <li>Changed the frequency ranges for C1 and C2 in Table 39.</li> </ul>	
		<ul> <li>Changed the .rbf file sizes for 5SGSD6 and 5SGSD8 in Table 47.</li> </ul>	
		<ul> <li>Added note about nSTATUS to Table 50, Table 51, Table 54.</li> </ul>	
		<ul> <li>Changed the available settings in Table 58.</li> </ul>	
		<ul> <li>Changed the note in "Periphery Performance".</li> </ul>	
		<ul> <li>Updated the "I/O Standard Specifications" section.</li> </ul>	
		<ul> <li>Updated the "Raw Binary File Size" section.</li> </ul>	
		<ul> <li>Updated the receiver voltage input range in Table 22.</li> </ul>	
		<ul> <li>Updated the max frequency for the LVDS clock network in Table 36.</li> </ul>	
		■ Updated the DCLK note to Figure 11.	
		<ul> <li>Updated Table 23 VO<sub>CM</sub> (DC Coupled) condition.</li> </ul>	
		Updated Table 6 and Table 7.	
		<ul> <li>Added the DCLK specification to Table 55.</li> </ul>	
		Updated the notes for Table 47.	
		<ul> <li>Updated the list of parameters for Table 56.</li> </ul>	
November 2013	3.2	Updated Table 28	
November 2013	3.1	Updated Table 33	
November 2013	3.0	Updated Table 23 and Table 28	
October 2013	2.9	<ul> <li>Updated the "Transceiver Characterization" section</li> </ul>	
		<ul> <li>Updated Table 3, Table 12, Table 14, Table 19, Table 20, Table 23, Table 24, Table 28, Table 30, Table 31, Table 32, Table 33, Table 36, Table 39, Table 40, Table 41, Table 42, Table 47, Table 53, Table 58, and Table 59</li> </ul>	
Uctober 2013	2.8	<ul> <li>Added Figure 1 and Figure 3</li> </ul>	
		<ul> <li>Added the "Transceiver Characterization" section</li> </ul>	
		<ul> <li>Removed all "Preliminary" designations.</li> </ul>	