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#### Intel - 5SGXEA3K3F35I3LN Datasheet



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#### Understanding <u>Embedded - FPGAs (Field</u> <u>Programmable Gate Array)</u>

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

#### **Applications of Embedded - FPGAs**

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

#### Details

Product Status	Obsolete
Number of LABs/CLBs	128300
Number of Logic Elements/Cells	340000
Total RAM Bits	19456000
Number of I/O	432
Number of Gates	-
Voltage - Supply	0.82V ~ 0.88V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	1152-BBGA, FCBGA
Supplier Device Package	1152-FBGA (35x35)
Purchase URL	https://www.e-xfl.com/product-detail/intel/5sgxea3k3f35i3ln

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

								·		
Transceiver Speed Grade		Core Speed Grade								
	C1	C2, C2L	C3	C4	<b>12, 12L</b>	13, 13L	<b>I</b> 3YY	14		
3 GX channel—8.5 Gbps	_	Yes	Yes	Yes	_	Yes	Yes <sup>(4)</sup>	Yes		

#### Table 1. Stratix V GX and GS Commercial and Industrial Speed Grade Offering <sup>(1), (2), (3)</sup> (Part 2 of 2)

Notes to Table 1:

(1) C = Commercial temperature grade; I = Industrial temperature grade.

(2) Lower number refers to faster speed grade.

(3) C2L, I2L, and I3L speed grades are for low-power devices.

(4) I3YY speed grades can achieve up to 10.3125 Gbps.

Table 2 lists the industrial and commercial speed grades for the Stratix V GT devices. **Table 2. Stratix V GT Commercial and Industrial Speed Grade Offering** <sup>(1)</sup>, <sup>(2)</sup>

Transseiver Speed Grade	Core Speed Grade					
Transceiver Speeu draue	C1	C2	12	13		
2 GX channel—12.5 Gbps GT channel—28.05 Gbps	Yes	Yes	_	_		
3 GX channel—12.5 Gbps GT channel—25.78 Gbps	Yes	Yes	Yes	Yes		

#### Notes to Table 2:

(1) C = Commercial temperature grade; I = Industrial temperature grade.

(2) Lower number refers to faster speed grade.

## **Absolute Maximum Ratings**

Absolute maximum ratings define the maximum operating conditions for Stratix V devices. The values are based on experiments conducted with the devices and theoretical modeling of breakdown and damage mechanisms. The functional operation of the device is not implied for these conditions.



Conditions other than those listed in Table 3 may cause permanent damage to the device. Additionally, device operation at the absolute maximum ratings for extended periods of time may have adverse effects on the device.

TANIC J. ANSULULC MAXIMUM NALINYS IVI SUALIX V DEVICES (FAIL I UI Z)	Table 3.	<b>Absolute Maximum</b>	Ratings	for Stratix \	/ Devices	(Part 1 of 2)
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Symbol	Description	Minimum	Maximum	Unit
V <sub>CC</sub>	Power supply for core voltage and periphery circuitry	-0.5	1.35	V
V <sub>CCPT</sub>	Power supply for programmable power technology	-0.5	1.8	V
V <sub>CCPGM</sub>	Power supply for configuration pins	-0.5	3.9	V
V <sub>CC_AUX</sub>	Auxiliary supply for the programmable power technology	-0.5	3.4	V
V <sub>CCBAT</sub>	Battery back-up power supply for design security volatile key register	-0.5	3.9	V
V <sub>CCPD</sub>	I/O pre-driver power supply	-0.5	3.9	V
V <sub>CCIO</sub>	I/O power supply	-0.5	3.9	V

Symbol	Description	Minimum	Maximum	Unit
V <sub>CCD_FPLL</sub>	PLL digital power supply	-0.5	1.8	V
V <sub>CCA_FPLL</sub>	PLL analog power supply	-0.5	3.4	V
VI	DC input voltage	-0.5	3.8	V
TJ	Operating junction temperature	-55	125	°C
T <sub>STG</sub>	Storage temperature (No bias)	-65	150	°C
I <sub>OUT</sub>	DC output current per pin	-25	40	mA

Table 3. Absolute Maximum Ratings for Stratix V Devices (Part 2 of 2)

Table 4 lists the absolute conditions for the transceiver power supply for Stratix V GX, GS, and GT devices.

Table 4. Transceiver Power Supply Absolute Conditions for Stratix V GX, GS, and GT Devices

Symbol	Description	Devices	Minimum	Maximum	Unit
V <sub>CCA_GXBL</sub>	Transceiver channel PLL power supply (left side)	GX, GS, GT	-0.5	3.75	V
V <sub>CCA_GXBR</sub>	Transceiver channel PLL power supply (right side)	GX, GS	-0.5	3.75	V
V <sub>CCA_GTBR</sub>	Transceiver channel PLL power supply (right side)	GT	-0.5	3.75	V
V <sub>CCHIP_L</sub>	Transceiver hard IP power supply (left side)	GX, GS, GT	-0.5	1.35	V
V <sub>CCHIP_R</sub>	Transceiver hard IP power supply (right side)	GX, GS, GT	-0.5	1.35	V
V <sub>CCHSSI_L</sub>	Transceiver PCS power supply (left side)	GX, GS, GT	-0.5	1.35	V
V <sub>CCHSSI_R</sub>	Transceiver PCS power supply (right side)	GX, GS, GT	-0.5	1.35	V
V <sub>CCR_GXBL</sub>	Receiver analog power supply (left side)	GX, GS, GT	-0.5	1.35	V
V <sub>CCR_GXBR</sub>	Receiver analog power supply (right side)	GX, GS, GT	-0.5	1.35	V
V <sub>CCR_GTBR</sub>	Receiver analog power supply for GT channels (right side)	GT	-0.5	1.35	V
V <sub>CCT_GXBL</sub>	Transmitter analog power supply (left side)	GX, GS, GT	-0.5	1.35	V
V <sub>CCT_GXBR</sub>	Transmitter analog power supply (right side)	GX, GS, GT	-0.5	1.35	V
V <sub>CCT_GTBR</sub>	Transmitter analog power supply for GT channels (right side)	GT	-0.5	1.35	V
V <sub>CCL_GTBR</sub>	Transmitter clock network power supply (right side)	GT	-0.5	1.35	V
V <sub>CCH_GXBL</sub>	Transmitter output buffer power supply (left side)	GX, GS, GT	-0.5	1.8	V
V <sub>CCH_GXBR</sub>	Transmitter output buffer power supply (right side)	GX, GS, GT	-0.5	1.8	V

#### **Maximum Allowed Overshoot and Undershoot Voltage**

During transitions, input signals may overshoot to the voltage shown in Table 5 and undershoot to -2.0 V for input currents less than 100 mA and periods shorter than 20 ns.

Table 5 lists the maximum allowed input overshoot voltage and the duration of the overshoot voltage as a percentage of device lifetime. The maximum allowed overshoot duration is specified as a percentage of high time over the lifetime of the device. A DC signal is equivalent to 100% of the duty cycle. For example, a signal that overshoots to 3.95 V can be at 3.95 V for only ~21% over the lifetime of the device; for a device lifetime of 10 years, the overshoot duration amounts to ~2 years.

Symbol	Description	Condition (V)	Overshoot Duration as % @ T <sub>J</sub> = 100°C	Unit					
		3.8	100	%					
		3.85	64	%					
		3.9	36	%					
	AC input voltage	3.95	21	%					
Vi (AC)		4	12	%					
		4.05	7	%					
		4.1	4	%					
		4.15	2	%					
		4.2	1	%					

Table 5. Maximum Allowed Overshoot During Transitions

#### Figure 1. Stratix V Device Overshoot Duration



Symbol	Description	Condition	Min <sup>(4)</sup>	Тур	Max <sup>(4)</sup>	Unit
t <sub>RAMP</sub>	Power supply ramp time	Standard POR	200 µs	_	100 ms	—
	Power supply ramp time	Fast POR	200 µs		4 ms	

#### Table 6. Recommended Operating Conditions for Stratix V Devices (Part 2 of 2)

#### Notes to Table 6:

(1)  $V_{CCPD}$  must be 2.5 V when  $V_{CCI0}$  is 2.5, 1.8, 1.5, 1.35, 1.25 or 1.2 V.  $V_{CCPD}$  must be 3.0 V when  $V_{CCI0}$  is 3.0 V.

(2) If you do not use the design security feature in Stratix V devices, connect V<sub>CCBAT</sub> to a 1.2- to 3.0-V power supply. Stratix V power-on-reset (POR) circuitry monitors V<sub>CCBAT</sub>. Stratix V devices will not exit POR if V<sub>CCBAT</sub> stays at logic low.

(3) C2L and I2L can also be run at 0.90 V for legacy boards that were designed for the C2 and I2 speed grades.

(4) The power supply value describes the budget for the DC (static) power supply tolerance and does not include the dynamic tolerance requirements. Refer to the PDN tool for the additional budget for the dynamic tolerance requirements.

Table 7 lists the transceiver power supply recommended operating conditions for Stratix V GX, GS, and GT devices.

## Table 7. Recommended Transceiver Power Supply Operating Conditions for Stratix V GX, GS, and GT Devices (Part 1 of 2)

Symbol	Description	Devices	Minimum <sup>(4)</sup>	Typical	Maximum <sup>(4)</sup>	Unit
V <sub>CCA GXBL</sub>	Transceiver channel PLL power supply (left		2.85	3.0	3.15	V
(1), (3)	side)	un, us, ui	2.375	2.5	2.625	v
V <sub>CCA_GXBR</sub>	Transceiver channel PLL power supply (right	CV CS	2.85	3.0	3.15	V
(1), (3)	side)	ux, us	2.375	2.5	2.625	v
V <sub>CCA_GTBR</sub>	Transceiver channel PLL power supply (right side)	GT	2.85	3.0	3.15	V
	Transceiver hard IP power supply (left side; C1, C2, I2, and I3YY speed grades)	GX, GS, GT	0.87	0.9	0.93	V
V <sub>CCHIP_L</sub>	Transceiver hard IP power supply (left side; C2L, C3, C4, I2L, I3, I3L, and I4 speed grades)	GX, GS, GT	0.82	0.85	0.88	V
V <sub>CCHIP_R</sub>	Transceiver hard IP power supply (right side; C1, C2, I2, and I3YY speed grades)	GX, GS, GT	0.87	0.9	0.93	V
	Transceiver hard IP power supply (right side; C2L, C3, C4, I2L, I3, I3L, and I4 speed grades)	GX, GS, GT	0.82	0.85	0.88	V
	Transceiver PCS power supply (left side; C1, C2, I2, and I3YY speed grades)	GX, GS, GT	0.87	0.9	0.93	V
V <sub>CCHSSI_L</sub>	Transceiver PCS power supply (left side; C2L, C3, C4, I2L, I3, I3L, and I4 speed grades)	GX, GS, GT	0.82	0.85	0.88	V
	Transceiver PCS power supply (right side; C1, C2, I2, and I3YY speed grades)	GX, GS, GT	0.87	0.9	0.93	V
V <sub>CCHSSI_R</sub>	Transceiver PCS power supply (right side; C2L, C3, C4, I2L, I3, I3L, and I4 speed grades)	GX, GS, GT	0.82	0.85	0.88	V
			0.82	0.85	0.88	
V <sub>CCR_GXBL</sub>	Receiver analog nower supply (left side)		0.87	0.90	0.93	v
(2) _	Therefore analog power supply (left Slue)	un, uo, ui	0.97	1.0	1.03	v
			1.03	1.05	1.07	

#### I/O Pin Leakage Current

Table 9 lists the Stratix V I/O pin leakage current specifications.

Table 9.	I/O Pin	Leakage	<b>Current for</b>	Stratix V	Devices (1)
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Symbol	Description	Conditions	Min	Тур	Max	Unit
I <sub>I</sub>	Input pin	$V_I = 0 V \text{ to } V_{CCIOMAX}$	-30	_	30	μA
I <sub>OZ</sub>	Tri-stated I/O pin	$V_0 = 0 V \text{ to } V_{\text{CCIOMAX}}$	-30		30	μA

#### Note to Table 9:

(1) If  $V_0 = V_{CCI0}$  to  $V_{CCI0Max}$ , 100  $\mu$ A of leakage current per I/O is expected.

#### **Bus Hold Specifications**

Table 10 lists the Stratix V device family bus hold specifications.

Table 10. Bus Hold Parameters for Stratix V Devices

		ymbol Conditions	V <sub>CCI0</sub>										
Parameter	Symbol		1.2 V		1.5 V		1.8 V		2.5 V		3.0 V		Unit
			Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Low sustaining current	I <sub>SUSL</sub>	V <sub>IN</sub> > V <sub>IL</sub> (maximum)	22.5	_	25.0	_	30.0	_	50.0	_	70.0	_	μA
High sustaining current	I <sub>SUSH</sub>	V <sub>IN</sub> < V <sub>IH</sub> (minimum)	-22.5		-25.0	_	-30.0	_	-50.0	_	-70.0		μA
Low overdrive current	I <sub>odl</sub>	$0V < V_{IN} < V_{CCIO}$		120		160		200	_	300		500	μA
High overdrive current	I <sub>odh</sub>	$0V < V_{IN} < V_{CCIO}$		-120		-160		-200		-300		-500	μΑ
Bus-hold trip point	V <sub>TRIP</sub>	_	0.45	0.95	0.50	1.00	0.68	1.07	0.70	1.70	0.80	2.00	۷

#### **On-Chip Termination (OCT) Specifications**

If you enable OCT calibration, calibration is automatically performed at power-up for I/Os connected to the calibration block. Table 11 lists the Stratix V OCT termination calibration accuracy specifications.

Table 11. OCT Calibration Accuracy Specifications for Stratix V Devices <sup>(1)</sup> (Part 1 of 2)

			Calibration Accuracy					
Symbol	Description	Conditions	C1	C2,12	C3,I3, I3YY	C4,14	Unit	
25- $Ω$ R <sub>S</sub>	Internal series termination with calibration (25- $\Omega$ setting)	V <sub>CCI0</sub> = 3.0, 2.5, 1.8, 1.5, 1.2 V	±15	±15	±15	±15	%	

Symbol	Description	V <sub>CCIO</sub> (V)	Typical	Unit		
dR/dT		3.0	0.189			
	OCT variation with temperature without recalibration	2.5	0.208			
		1.8	0.266	%/°C		
		1.5	0.273			
		1.2	0.317			

Table 13. OCT Variation after Power-Up Calibration for Stratix V Devices (Part 2 of 2)<sup>(1)</sup>

#### Note to Table 13:

(1) Valid for a  $V_{CCIO}$  range of  $\pm 5\%$  and a temperature range of 0° to 85°C.

#### **Pin Capacitance**

Table 14 lists the Stratix V device family pin capacitance.

#### Table 14. Pin Capacitance for Stratix V Devices

Symbol	Description	Value	Unit
CIOTB	Input capacitance on the top and bottom I/O pins	6	pF
C <sub>IOLR</sub>	Input capacitance on the left and right I/O pins	6	рF
C <sub>OUTFB</sub>	Input capacitance on dual-purpose clock output and feedback pins	6	pF

#### **Hot Socketing**

Table 15 lists the hot socketing specifications for Stratix V devices.

Symbol	Description	Maximum
I <sub>IOPIN (DC)</sub>	DC current per I/O pin	300 μA
I <sub>IOPIN (AC)</sub>	AC current per I/O pin	8 mA <sup>(1)</sup>
IXCVR-TX (DC)	DC current per transceiver transmitter pin	100 mA
IXCVR-RX (DC)	DC current per transceiver receiver pin	50 mA

#### Note to Table 15:

(1) The I/O ramp rate is 10 ns or more. For ramp rates faster than 10 ns,  $|I_{10PIN}| = C dv/dt$ , in which C is the I/O pin capacitance and dv/dt is the slew rate.

Symbol/	Conditions	Transceiver Speed Grade 1			Transceiver Speed Grade 2			Transceiver Speed Grade 3			Unit
Description		Min	Тур	Max	Min	Тур	Max	Min	Тур	Max	
Spread-spectrum downspread	PCIe	_	0 to 0.5	_	_	0 to 0.5	_	_	0 to 0.5	_	%
On-chip termination resistors <sup>(21)</sup>	_	_	100		_	100		_	100		Ω
Absolute V <sub>MAX</sub> <sup>(5)</sup>	Dedicated reference clock pin	_	_	1.6	_	_	1.6	_	_	1.6	V
	RX reference clock pin	_		1.2		_	1.2			1.2	
Absolute V <sub>MIN</sub>	—	-0.4	-	_	-0.4	_		-0.4	—		V
Peak-to-peak differential input voltage	_	200	_	1600	200	_	1600	200	_	1600	mV
V <sub>ICM</sub> (AC	Dedicated reference clock pin	1050/	(1000/90	00/850 <sup>(2)</sup>	1050/1000/900/850 (2)			1050/1000/900/850 (2)			mV
coupled) (9	RX reference clock pin	1.0/0.9/0.85 <sup>(4)</sup>			1.0/0.9/0.85 <sup>(4)</sup>			1.0/0.9/0.85 <sup>(4)</sup>			V
V <sub>ICM</sub> (DC coupled)	HCSL I/O standard for PCIe reference clock	250		550	250	_	550	250	_	550	mV
	100 Hz	—	—	-70	—	—	-70	—	—	-70	dBc/Hz
Transmitter	1 kHz	—	—	-90	—	—	-90	—	—	-90	dBc/Hz
REFCLK Phase	10 kHz	—	—	-100	—	—	-100	—	—	-100	dBc/Hz
(622 MHz) <sup>(20)</sup>	100 kHz	—	—	-110	—	—	-110	—	—	-110	dBc/Hz
	≥1 MHz	—	—	-120		—	-120	—	-	-120	dBc/Hz
Transmitter REFCLK Phase Jitter (100 MHz) <sup>(17)</sup>	10 kHz to 1.5 MHz (PCIe)	_	_	3	_	_	3	_	_	3	ps (rms)
R <sub>REF</sub> (19)	_	_	1800 ±1%	_	_	1800 ±1%	_	_	180 0 ±1%	_	Ω
Transceiver Clock	s										
fixedclk <b>clock</b> frequency	PCIe Receiver Detect		100 or 125			100 or 125		_	100 or 125		MHz

## Table 23. Transceiver Specifications for Stratix V GX and GS Devices <sup>(1)</sup> (Part 2 of 7)

Table 26 shows the approximate maximum data rate using the 10G PCS.

Mode <sup>(2)</sup>	Transceiver	PMA Width	64	40	40	40	32	32	
	Speed Grade	PCS Width	64	66/67	50	40	64/66/67	32	
	1	C1, C2, C2L, I2, I2L core speed grade	14.1	14.1	10.69	14.1	13.6	13.6	
	2	C1, C2, C2L, I2, I2L core speed grade	12.5	12.5	10.69	12.5	12.5	12.5	
		C3, I3, I3L core speed grade	12.5	12.5	10.69	12.5	10.88	10.88	
FIFO or Register	3	C1, C2, C2L, I2, I2L core speed grade							
		C3, I3, I3L core speed grade	8.5 Gbps						
		C4, I4 core speed grade							
		I3YY core speed grade			10.312	25 Gbps			

Notes to Table 26:

(1) The maximum data rate is in Gbps.

(2) The Phase Compensation FIFO can be configured in FIFO mode or register mode. In the FIFO mode, the pointers are not fixed, and the latency can vary. In the register mode the pointers are fixed for low latency.

Table 29 shows the  $V_{\text{OD}}$  settings for the GT channel.

Symbol	V <sub>OD</sub> Setting	V <sub>od</sub> Value (mV)
	0	0
	1	200
V., differential neak to neak typical $(1)$	2	400
The american hear to hear thicat to	3	600
	4	800
	5	1000

#### Note:

(1) Refer to Figure 4.

Symbol	Parameter	Min	Тур	Max	Unit
+ (3) (4)	Input clock cycle-to-cycle jitter ( $f_{REF} \ge 100 \text{ MHz}$ )			0.15	UI (p-p)
LINCCJ (0), (1)	Input clock cycle-to-cycle jitter (f <sub>REF</sub> < 100 MHz)	-750		+750	ps (p-p)
t <sub>outpj_dc</sub> (5)	Period Jitter for dedicated clock output (f_{OUT} $\geq$ 100 MHz)	_	_	175 <sup>(1)</sup>	ps (p-p)
	Period Jitter for dedicated clock output (f <sub>OUT</sub> < 100 MHz)	_	_	17.5 <sup>(1)</sup>	mUI (p-p)
(5)	Period Jitter for dedicated clock output in fractional PLL ( $f_{OUT} \ge 100 \text{ MHz}$ )	_	_	250 <sup>(11)</sup> , 175 <sup>(12)</sup>	ps (p-p)
<sup>L</sup> FOUTPJ_DC	Period Jitter for dedicated clock output in fractional PLL (f <sub>OUT</sub> < 100 MHz)	_	_	25 <sup>(11)</sup> , 17.5 <sup>(12)</sup>	mUI (p-p)
+ (5)	Cycle-to-Cycle Jitter for a dedicated clock output ( $f_{\text{OUT}} \geq 100 \text{ MHz})$		_	175	ps (p-p)
COUTCCJ_DC	Cycle-to-Cycle Jitter for a dedicated clock output $(f_{OUT} < 100 \text{ MHz})$		_	17.5	mUI (p-p)
+ (5)	Cycle-to-cycle Jitter for a dedicated clock output in fractional PLL ( $f_{OUT} \ge 100 \text{ MHz}$ )		_	250 <sup>(11)</sup> , 175 <sup>(12)</sup>	ps (p-p)
<sup>T</sup> FOUTCCJ_DC <sup>(3)</sup>	Cycle-to-cycle Jitter for a dedicated clock output in fractional PLL ( $f_{OUT} < 100 \text{ MHz}$ )+		_	25 <sup>(11)</sup> , 17.5 <sup>(12)</sup>	mUI (p-p)
t <sub>outpj_io</sub> (5), (8)	Period Jitter for a clock output on a regular I/O in integer PLL ( $f_{OUT} \ge 100 \text{ MHz}$ )		_	600	ps (p-p)
	Period Jitter for a clock output on a regular I/O $(f_{OUT} < 100 \text{ MHz})$		_	60	mUI (p-p)
t <sub>EQUITE 1 10</sub> (5),	Period Jitter for a clock output on a regular I/O in fractional PLL ( $f_{OUT} \ge 100 \text{ MHz}$ )	_	_	600 <sup>(10)</sup>	ps (p-p)
(8), (11)	Period Jitter for a clock output on a regular I/O in fractional PLL (f <sub>OUT</sub> < 100 MHz)	_	_	60 <sup>(10)</sup>	mUI (p-p)
t <sub>outccj_io</sub> (5),	Cycle-to-cycle Jitter for a clock output on a regular I/O in integer PLL ( $f_{OUT} \geq 100 \mbox{ MHz})$	_	_	600	ps (p-p)
(8)	Cycle-to-cycle Jitter for a clock output on a regular I/O in integer PLL (f <sub>OUT</sub> < 100 MHz)	_	_	60 <sup>(10)</sup>	mUI (p-p)
t <sub>FOUTCCJ 10</sub> (5),	Cycle-to-cycle Jitter for a clock output on a regular I/O in fractional PLL ( $f_{OUT} \ge 100$ MHz)		_	600 <sup>(10)</sup>	ps (p-p)
(8), (11)	Cycle-to-cycle Jitter for a clock output on a regular I/O in fractional PLL (f <sub>OUT</sub> < 100 MHz)	_	_	60	mUI (p-p)
t <sub>CASC OUTPJ DC</sub>	Period Jitter for a dedicated clock output in cascaded PLLs ( $f_{OUT} \ge 100 \text{ MHz}$ )	_	_	175	ps (p-p)
(5), (6)	Period Jitter for a dedicated clock output in cascaded PLLs ( $f_{OUT}$ < 100 MHz)	_	_	17.5	mUI (p-p)
f <sub>DRIFT</sub>	Frequency drift after PFDENA is disabled for a duration of 100 $\mu s$		_	±10	%
dK <sub>BIT</sub>	Bit number of Delta Sigma Modulator (DSM)	8	24	32	Bits
k <sub>VALUE</sub>	Numerator of Fraction	128	8388608	2147483648	—

Table 31. PLL Specifications for Stratix V Devices (Part 2 of 3)

Mode										
	C1	C2, C2L	12, 12L	C3	13, 13L, 13YY	C4	14	Unit		
	Modes using Three DSPs									
One complex 18 x 25	425	425	415	340	340	275	265	MHz		
Modes using Four DSPs										
One complex 27 x 27	465	465	465	380	380	300	290	MHz		

#### Table 32. Block Performance Specifications for Stratix V DSP Devices (Part 2 of 2)

## **Memory Block Specifications**

Table 33 lists the Stratix V memory block specifications.

## Table 33. Memory Block Performance Specifications for Stratix V Devices <sup>(1), (2)</sup> (Part 1 of 2)

	Mode	<b>Resources Used</b>		Performance							
Memory		ALUTS	Memory	C1	C2, C2L	C3	C4	12, 12L	13, 13L, 13YY	14	Unit
MLAB	Single port, all supported widths	0	1	450	450	400	315	450	400	315	MHz
	Simple dual-port, x32/x64 depth	0	1	450	450	400	315	450	400	315	MHz
	Simple dual-port, x16 depth <sup>(3)</sup>	0	1	675	675	533	400	675	533	400	MHz
	ROM, all supported widths	0	1	600	600	500	450	600	500	450	MHz

Symbol	Conditiono		C1		C2,	C2L, I	2, I2L	C3,	13, 131	., I <b>3</b> YY	C4,I4			Unit
Symbol	Conditions	Min	Тур	Max	Min	Тур	Max	Min	Тур	Max	Min	Тур	Max	UIIIL
Transmitter														
True Differential I/O Standards - f <sub>HSDR</sub> (data rate)	SERDES factor J = 3 to 10 <sup>(9)</sup> , <sup>(11)</sup> , <sup>(12)</sup> , <sup>(13)</sup> , <sup>(14)</sup> , <sup>(15)</sup> , <sup>(16)</sup>	(6)	_	1600	(6)	_	1434	(6)	_	1250	(6)	_	1050	Mbps
	SERDES factor J $\geq 4$ LVDS TX with DPA (12), (14), (15), (16)	(6)		1600	(6)		1600	(6)		1600	(6)	_	1250	Mbps
	SERDES factor J = 2, uses DDR Registers	(6)	_	(7)	(6)	_	(7)	(6)	_	(7)	(6)		(7)	Mbps
	SERDES factor J = 1, uses SDR Register	(6)	_	(7)	(6)	_	(7)	(6)	_	(7)	(6)	_	(7)	Mbps
Emulated Differential I/O Standards with Three External Output Resistor Networks - f <sub>HSDR</sub> (data rate) <sup>(10)</sup>	SERDES factor J = 4 to 10 $(^{17})$	(6)		1100	(6)		1100	(6)		840	(6)		840	Mbps
t <sub>x Jitter</sub> - True Differential	Total Jitter for Data Rate 600 Mbps - 1.25 Gbps		_	160		_	160		_	160			160	ps
I/O Standards	Total Jitter for Data Rate < 600 Mbps		_	0.1			0.1			0.1		_	0.1	UI
t <sub>x Jitter</sub> - Emulated Differential I/O Standards with Three External Output Resistor Network	Total Jitter for Data Rate 600 Mbps - 1.25 Gbps	_	_	300	_		300	_	_	300	_		325	ps
	Total Jitter for Data Rate < 600 Mbps	_	_	0.2	_	_	0.2	_	_	0.2	_	_	0.25	UI

## Table 36. High-Speed I/O Specifications for Stratix V Devices (1), (2) (Part 2 of 4)

Symbol	Conditions		C1		C2,	C2, C2L, I2, I2L		C3, I3, I3L, I3YY		C4,14			Unit	
əyiinuu	Conultions	Min	Тур	Max	Min	Тур	Max	Min	Тур	Max	Min	Тур	Max	Umt
f <sub>HSDR</sub> (data rate)	SERDES factor J = 3 to 10	(6)		(8)	(6)	_	(8)	(6)		(8)	(6)		(8)	Mbps
	SERDES factor J = 2, uses DDR Registers	(6)		(7)	(6)	_	(7)	(6)	_	(7)	(6)		(7)	Mbps
	SERDES factor J = 1, uses SDR Register	(6)	_	(7)	(6)	_	(7)	(6)	_	(7)	(6)	_	(7)	Mbps
DPA Mode														
DPA run length	_			1000 0		_	1000 0	_		1000 0	_		1000 0	UI
Soft CDR mode														
Soft-CDR PPM tolerance	_	_	_	300	_	_	300	_	_	300	_	_	300	± PPM
Non DPA Mode	Non DPA Mode													
Sampling Window	_			300			300			300			300	ps

#### Table 36. High-Speed I/O Specifications for Stratix V Devices (1), (2) (Part 4 of 4)

Notes to Table 36:

(1) When J = 3 to 10, use the serializer/deserializer (SERDES) block.

(2) When J = 1 or 2, bypass the SERDES block.

(3) This only applies to DPA and soft-CDR modes.

(4) Clock Boost Factor (W) is the ratio between the input data rate to the input clock rate.

(5) This is achieved by using the **LVDS** clock network.

(6) The minimum specification depends on the clock source (for example, the PLL and clock pin) and the clock routing resource (global, regional, or local) that you use. The I/O differential buffer and input register do not have a minimum toggle rate.

(7) The maximum ideal frequency is the SERDES factor (J) x the PLL maximum output frequency (fOUT) provided you can close the design timing and the signal integrity simulation is clean.

(8) You can estimate the achievable maximum data rate for non-DPA mode by performing link timing closure analysis. You must consider the board skew margin, transmitter delay margin, and receiver sampling margin to determine the maximum data rate supported.

(9) If the receiver with DPA enabled and transmitter are using shared PLLs, the minimum data rate is 150 Mbps.

(10) You must calculate the leftover timing margin in the receiver by performing link timing closure analysis. You must consider the board skew margin, transmitter channel-to-channel skew, and receiver sampling margin to determine leftover timing margin.

(11) The F<sub>MAX</sub> specification is based on the fast clock used for serial data. The interface F<sub>MAX</sub> is also dependent on the parallel clock domain which is design-dependent and requires timing analysis.

(12) Stratix V RX LVDS will need DPA. For Stratix V TX LVDS, the receiver side component must have DPA.

(13) Stratix V LVDS serialization and de-serialization factor needs to be x4 and above.

(14) Requires package skew compensation with PCB trace length.

(15) Do not mix single-ended I/O buffer within LVDS I/O bank.

(16) Chip-to-chip communication only with a maximum load of 5 pF.

(17) When using True LVDS RX channels for emulated LVDS TX channel, only serialization factors 1 and 2 are supported.

Family	Device	Package	Configuration .rbf Size (bits)	IOCSR .rbf Size (bits) <sup>(4), (5)</sup>
Stratix V E <sup>(1)</sup>	5SEE9	—	342,742,976	700,888
	5SEEB	—	342,742,976	700,888

#### Table 47. Uncompressed .rbf Sizes for Stratix V Devices

#### Notes to Table 47:

(1) Stratix V E devices do not have PCI Express® (PCIe®) hard IP. Stratix V E devices do not support the CvP configuration scheme.

(2) 36-transceiver devices.

(3) 24-transceiver devices.

(4) File size for the periphery image.

(5) The IOCSR .rbf size is specifically for the CvP feature.

Use the data in Table 47 to estimate the file size before design compilation. Different configuration file formats, such as a hexadecimal (.hex) or tabular text file (.ttf) format, have different file sizes. For the different types of configuration file and file sizes, refer to the Quartus II software. However, for a specific version of the Quartus II software, any design targeted for the same device has the same uncompressed configuration file size. If you are using compression, the file size can vary after each compilation because the compression ratio depends on your design.

• For more information about setting device configuration options, refer to *Configuration, Design Security, and Remote System Upgrades in Stratix V Devices.* For creating configuration files, refer to the *Quartus II Help.* 

Table 48 lists the minimum configuration time estimates for Stratix V devices.

Table 48. Minimum Configuration Time Estimation for Stratix V Devi
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	Member Code		Active Serial (1)	)	Fast Passive Parallel <sup>(2)</sup>				
Variant		Width	DCLK (MHz)	Min Config Time (s)	Width	DCLK (MHz)	Min Config Time (s)		
	٨٥	4	100	0.534	32	100	0.067		
	//0	4	100	0.344	32	100	0.043		
	A4	4	100	0.534	32	100	0.067		
	A5	4	100	0.675	32	100	0.084		
	A7	4	100	0.675	32	100	0.084		
GX	A9	4	100	0.857	32	100	0.107		
	AB	4	100	0.857	32	100	0.107		
	B5	4	100	0.676	32	100	0.085		
	B6	4	100	0.676	32	100	0.085		
	B9	4	100	0.857	32	100	0.107		
	BB	4	100	0.857	32	100	0.107		
ст	C5	4	100	0.675	32	100	0.084		
ul	C7	4	100	0.675	32	100	0.084		

	Member Code		Active Serial <sup>(1)</sup>	)	Fast Passive Parallel <sup>(2)</sup>				
Variant		Width	DCLK (MHz)	Min Config Time (s)	Width	DCLK (MHz)	Min Config Time (s)		
	D3	4	100	0.344	32	100	0.043		
00	D4	4	100	0.534	32	100	0.067		
		4	100	0.344	32	100	0.043		
03	D5	4	100	0.534	32	100	0.067		
	D6	4	100	0.741	32	100	0.093		
	D8	4	100	0.741	32	100	0.093		
F	E9	4	100	0.857	32	100	0.107		
Ľ	EB	4	100	0.857	32	100	0.107		

Table 48. Minimum Configuration Time Estimation for Stratix V Devices

#### Notes to Table 48:

(1) DCLK frequency of 100 MHz using external CLKUSR.

(2) Max FPGA FPP bandwidth may exceed bandwidth available from some external storage or control logic.

## **Fast Passive Parallel Configuration Timing**

This section describes the fast passive parallel (FPP) configuration timing parameters for Stratix V devices.

## DCLK-to-DATA[] Ratio for FPP Configuration

FPP configuration requires a different DCLK-to-DATA[]ratio when you enable the design security, decompression, or both features. Table 49 lists the DCLK-to-DATA[]ratio for each combination.

Configuration Scheme	Decompression	Design Security	DCLK-to-DATA[] Ratio
	Disabled	Disabled	1
	Disabled	Enabled	1
FPP ×8	Enabled	Disabled	2
	Enabled	Enabled	2
	Disabled	Disabled	1
	Disabled	Enabled	2
FPP ×16	Enabled	Disabled	4
	Enabled	Enabled	4

 Table 49. DCLK-to-DATA[] Ratio <sup>(1)</sup> (Part 1 of 2)

Table 50 lists the timing parameters for Stratix V devices for FPP configuration when the DCLK-to-DATA[] ratio is 1.

Table 50. FPP Timing Parameters for Stratix V Devices (1)

Symbol	Parameter	Minimum	Maximum	Units
t <sub>CF2CD</sub>	nCONFIG low to CONF_DONE low	—	600	ns
t <sub>CF2ST0</sub>	nCONFIG low to nSTATUS low		600	ns
t <sub>CFG</sub>	nCONFIG low pulse width	2		μS
t <sub>status</sub>	nSTATUS low pulse width	268	1,506 <sup>(2)</sup>	μS
t <sub>CF2ST1</sub>	nCONFIG high to nSTATUS high	—	1,506 <sup>(3)</sup>	μS
t <sub>CF2CK</sub> (6)	nCONFIG high to first rising edge on DCLK	1,506		μS
t <sub>ST2CK</sub> (6)	nSTATUS high to first rising edge of DCLK	2		μS
t <sub>DSU</sub>	DATA [] setup time before rising edge on DCLK	5.5	_	ns
t <sub>DH</sub>	DATA [] hold time after rising edge on DCLK	0	_	ns
t <sub>CH</sub>	DCLK high time	$0.45\times1/f_{MAX}$		S
t <sub>CL</sub>	DCLK low time	$0.45\times1/f_{MAX}$	_	S
t <sub>CLK</sub>	DCLK period	1/f <sub>MAX</sub>		S
4	DCLK frequency (FPP ×8/×16)	—	125	MHz
IMAX	DCLK frequency (FPP ×32)	—	100	MHz
t <sub>CD2UM</sub>	CONF_DONE high to user mode <sup>(4)</sup>	175	437	μS
+	CONTR DOWN high to CT WARD analysis	4 × maximum		
LCD2CU	CONF_DONE HIGH to CLEOSE enabled	DCLK period	—	_
t <sub>cD2UMC</sub>	CONF_DONE high to user mode with CLKUSR option on	$\begin{array}{c} t_{\text{CD2CU}} + \\ (8576 \times \text{CLKUSR} \\ \text{period}) \ ^{(5)} \end{array}$		_

#### Notes to Table 50:

(1) Use these timing parameters when the decompression and design security features are disabled.

(2) This value is applicable if you do not delay configuration by extending the nCONFIG or nSTATUS low pulse width.

(3) This value is applicable if you do not delay configuration by externally holding the nSTATUS low.

- (4) The minimum and maximum numbers apply only if you chose the internal oscillator as the clock source for initializing the device.
- (5) To enable the CLKUSR pin as the initialization clock source and to obtain the maximum frequency specification on these pins, refer to the Initialization section of the "Configuration, Design Security, and Remote System Upgrades in Stratix V Devices" chapter.
- (6) If nSTATUS is monitored, follow the t<sub>ST2CK</sub> specification. If nSTATUS is not monitored, follow the t<sub>CF2CK</sub> specification.

## FPP Configuration Timing when DCLK-to-DATA [] > 1

Figure 13 shows the timing waveform for FPP configuration when using a MAX II device, MAX V device, or microprocessor as an external host. This waveform shows timing when the DCLK-to-DATA [] ratio is more than 1.

Table 51 lists the timing parameters for Stratix V devices for FPP configuration when the DCLK-to-DATA [] ratio is more than 1.

Table 51.	<b>FPP</b> Timing	Parameters f	or Stratix V	<b>Devices When</b>	the DCLK-te	o-DATA[] Ratio	is >1 (	1)
			•••••••••••••••••••••••••••••••••••••••			• • • • • • • • • • • • • • • • • • •		

Symbol	Parameter	Minimum	Maximum	Units
t <sub>CF2CD</sub>	nCONFIG low to CONF_DONE low	—	600	ns
t <sub>CF2ST0</sub>	nCONFIG low to nSTATUS low	—	600	ns
t <sub>CFG</sub>	nCONFIG low pulse width	2		μS
t <sub>STATUS</sub>	nSTATUS low pulse width	268	1,506 <sup>(2)</sup>	μS
t <sub>CF2ST1</sub>	nCONFIG high to nSTATUS high	—	1,506 <sup>(2)</sup>	μS
t <sub>CF2CK</sub> (5)	nCONFIG high to first rising edge on DCLK	1,506		μS
t <sub>ST2CK</sub> (5)	nSTATUS high to first rising edge of DCLK	2		μS
t <sub>DSU</sub>	DATA [] setup time before rising edge on DCLK	5.5		ns
t <sub>DH</sub>	DATA [] hold time after rising edge on DCLK	N-1/f <sub>DCLK</sub> (5)		S
t <sub>CH</sub>	DCLK high time	$0.45\times 1/f_{MAX}$		S
t <sub>CL</sub>	DCLK low time	$0.45\times 1/f_{MAX}$		S
t <sub>CLK</sub>	DCLK period	1/f <sub>MAX</sub>		S
f	DCLK frequency (FPP ×8/×16)	—	125	MHz
IMAX	DCLK frequency (FPP ×32)	—	100	MHz
t <sub>R</sub>	Input rise time	—	40	ns
t <sub>F</sub>	Input fall time	—	40	ns
t <sub>CD2UM</sub>	CONF_DONE high to user mode <sup>(3)</sup>	175	437	μS
t <sub>CD2CU</sub>	CONF_DONE high to CLKUSR enabled	4 × maximum DCLK period	_	_
t <sub>CD2UMC</sub>	CONF_DONE high to user mode with CLKUSR option on	t <sub>CD2CU</sub> + (8576 × CLKUSR period) <sup>(4)</sup>	_	_

#### Notes to Table 51:

- (1) Use these timing parameters when you use the decompression and design security features.
- (2) You can obtain this value if you do not delay configuration by extending the nCONFIG or nSTATUS low pulse width.
- (3) The minimum and maximum numbers apply only if you use the internal oscillator as the clock source for initializing the device.
- (4) To enable the CLKUSR pin as the initialization clock source and to obtain the maximum frequency specification on these pins, refer to the Initialization section of the "Configuration, Design Security, and Remote System Upgrades in Stratix V Devices" chapter.
- (5) N is the DCLK-to-DATA ratio and  $f_{\text{DCLK}}$  is the DCLK frequency the system is operating.
- (6) If nSTATUS is monitored, follow the t<sub>ST2CK</sub> specification. If nSTATUS is not monitored, follow the t<sub>CF2CK</sub> specification.

## **Active Serial Configuration Timing**

Table 52 lists the DCLK frequency specification in the AS configuration scheme.

Fable 52.	DCLK Frequency	Specification in th	e AS Configuration	Scheme <sup>(1),</sup>	(2)
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Minimum	Typical	Maximum	Unit
5.3	7.9	12.5	MHz
10.6	15.7	25.0	MHz
21.3	31.4	50.0	MHz
42.6	62.9	100.0	MHz

#### Notes to Table 52:

(1) This applies to the DCLK frequency specification when using the internal oscillator as the configuration clock source.

(2) The AS multi-device configuration scheme does not support DCLK frequency of 100 MHz.

Figure 14 shows the single-device configuration setup for an AS ×1 mode.





#### Notes to Figure 14:

- (1) If you are using AS  $\times 4$  mode, this signal represents the AS\_DATA[3..0] and EPCQ sends in 4-bits of data for each DCLK cycle.
- (2) The initialization clock can be from internal oscillator or CLKUSR pin.
- (3) After the option bit to enable the INIT\_DONE pin is configured into the device, the INIT\_DONE goes low.

Table 53 lists the timing parameters for AS  $\times 1$  and AS  $\times 4$  configurations in Stratix V devices.

Table JS. As fining falancees for as $\times 1$ and as $\times 4$ configurations in straits V devices $(2, 2, 2, 3, 3, 3, 3, 3, 3, 3, 3, 3, 3, 3, 3, 3,$	Table 53.	AS Timing	<b>Parameters for AS</b>	$\times$ 1 and AS $\times$ 4 Confi	gurations in Stratix V	/ Devices <sup>(1),</sup> (2)	(Part 1 of 2)
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Symbol	Parameter	Minimum	Maximum	Units
t <sub>CO</sub>	DCLK falling edge to AS_DATA0/ASDO output	—	2	ns
t <sub>SU</sub>	Data setup time before falling edge on DCLK	1.5	_	ns
t <sub>H</sub>	Data hold time after falling edge on DCLK	0	_	ns

Paramotor	Available Min		Available Min Fast Model		Slow Model							
(1)	Settings	Offset (2)	Industrial	Commercial	C1	C2	C3	C4	12	13, 13YY	14	Unit
D3	8	0	1.587	1.699	2.793	2.793	2.992	3.192	2.811	3.047	3.257	ns
D4	64	0	0.464	0.492	0.838	0.838	0.924	1.011	0.843	0.920	1.006	ns
D5	64	0	0.464	0.493	0.838	0.838	0.924	1.011	0.844	0.921	1.006	ns
D6	32	0	0.229	0.244	0.415	0.415	0.458	0.503	0.418	0.456	0.499	ns

Table 58.	IOE Pro	grammable De	ay for	Stratix V	V Devices	(Part 2 of 2	)
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#### Notes to Table 58:

(1) You can set this value in the Quartus II software by selecting D1, D2, D3, D5, and D6 in the Assignment Name column of Assignment Editor.

(2) Minimum offset does not include the intrinsic delay.

## **Programmable Output Buffer Delay**

Table 59 lists the delay chain settings that control the rising and falling edge delays of the output buffer. The default delay is 0 ps.

Symbol	Parameter	Typical	Unit
		0 (default)	ps
Dauman	Rising and/or falling edge	25	ps
DOUTBUF	delay	50 ps	ps
		75	ps

Note to Table 59:

(1) You can set the programmable output buffer delay in the Quartus II software by setting the Output Buffer Delay Control assignment to either positive, negative, or both edges, with the specific values stated here (in ps) for the Output Buffer Delay assignment.

## Glossary

Table 60 lists the glossary for this chapter.

Table 60. Glossary (Part 1 of 4)

Letter	r Subject Definitions	
Α		
В	—	—
С		
D	—	_
E	—	_
	f <sub>HSCLK</sub>	Left and right PLL input clock frequency.
F	f <sub>HSDR</sub>	High-speed I/O block—Maximum and minimum <b>LVDS</b> data transfer rate (f <sub>HSDR</sub> = 1/TUI), non-DPA.
	f <sub>hsdrdpa</sub>	High-speed I/O block—Maximum and minimum <b>LVDS</b> data transfer rate (f <sub>HSDRDPA</sub> = 1/TUI), DPA.

Letter	Subject	Definitions
	V <sub>CM(DC)</sub>	DC common mode input voltage.
	V <sub>ICM</sub>	Input common mode voltage—The common mode of the differential signal at the receiver.
	V <sub>ID</sub>	Input differential voltage swing—The difference in voltage between the positive and complementary conductors of a differential transmission at the receiver.
	V <sub>DIF(AC)</sub>	AC differential input voltage—Minimum AC input differential voltage required for switching.
	V <sub>DIF(DC)</sub>	DC differential input voltage— Minimum DC input differential voltage required for switching.
	V <sub>IH</sub>	Voltage input high—The minimum positive voltage applied to the input which is accepted by the device as a logic high.
	V <sub>IH(AC)</sub>	High-level AC input voltage
	V <sub>IH(DC)</sub>	High-level DC input voltage
V	V <sub>IL</sub>	Voltage input low—The maximum positive voltage applied to the input which is accepted by the device as a logic low.
	V <sub>IL(AC)</sub>	Low-level AC input voltage
	V <sub>IL(DC)</sub>	Low-level DC input voltage
	V <sub>OCM</sub>	Output common mode voltage—The common mode of the differential signal at the transmitter.
	V <sub>OD</sub>	Output differential voltage swing—The difference in voltage between the positive and complementary conductors of a differential transmission at the transmitter.
	V <sub>SWING</sub>	Differential input voltage
	V <sub>X</sub>	Input differential cross point voltage
	V <sub>OX</sub>	Output differential cross point voltage
W	W	High-speed I/O block—clock boost factor
X		
Y	—	—
Z		

#### Table 60. Glossary (Part 4 of 4)