### Intel - 5SGXEA4H1F35I2N Datasheet





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Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

### **Applications of Embedded - FPGAs**

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

#### Details

Product Status	Obsolete
Number of LABs/CLBs	158500
Number of Logic Elements/Cells	420000
Total RAM Bits	37888000
Number of I/O	552
Number of Gates	-
Voltage - Supply	0.87V ~ 0.93V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	1152-BBGA, FCBGA
Supplier Device Package	1152-FBGA (35x35)
Purchase URL	https://www.e-xfl.com/product-detail/intel/5sgxea4h1f35i2n

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Symbol	Description	Devices	Minimum <sup>(4)</sup>	Typical	Maximum <sup>(4)</sup>	Unit
			0.82	0.85	0.88	
V <sub>CCR_GXBR</sub>	Receiver analog power supply (right side)		0.87	0.90	0.93	v
(2)	neceiver analog power supply (right side)	ux, us, ui	0.97	1.0	1.03	v
			1.03	1.05	1.07	
V <sub>CCR_GTBR</sub>	Receiver analog power supply for GT channels (right side)	GT	1.02	1.05	1.08	V
			0.82	0.85	0.88	
V <sub>CCT GXBL</sub>	Transmitter analog newer supply (left side)		0.87	0.90	0.93	V
(2)	Transmitter analog power supply (left side)	un, uo, ui	0.97	1.0	1.03	v
			1.03	1.05	1.07	
			0.82	0.85	0.88	
V <sub>CCT GXBR</sub>	Transmitter analog newer supply (right side)		0.87	0.90	0.93	v
(2) _	Transmitter analog power supply (light side)	ux, us, ui	0.97	1.0	1.03	v
			1.03	1.05	1.07	
$V_{CCT_GTBR}$	Transmitter analog power supply for GT channels (right side)	GT	1.02	1.05	1.08	V
$V_{CCL\_GTBR}$	Transmitter clock network power supply	GT	1.02	1.05	1.08	V
V <sub>CCH_GXBL</sub>	Transmitter output buffer power supply (left side)	GX, GS, GT	1.425	1.5	1.575	V
V <sub>CCH_GXBR</sub>	Transmitter output buffer power supply (right side)	GX, GS, GT	1.425	1.5	1.575	V

Table 7.	<b>Recommended Transceiver Power Supply Operating Conditions for Stratix V GX</b> ,	<b>GS</b> , and <b>GT</b> Devices
(Part 2	of 2)	

### Notes to Table 7:

(1) This supply must be connected to 3.0 V if the CMU PLL, receiver CDR, or both, are configured at a base data rate > 6.5 Gbps. Up to 6.5 Gbps, you can connect this supply to either 3.0 V or 2.5 V.

(2) Refer to Table 8 to select the correct power supply level for your design.

(3) When using ATX PLLs, the supply must be 3.0 V.

(4) This value describes the budget for the DC (static) power supply tolerance and does not include the dynamic tolerance requirements. Refer to the PDN tool for the additional budget for the dynamic tolerance requirements.

Table 8 shows the transceiver power supply voltage requirements for various conditions.

**Table 8. Transceiver Power Supply Voltage Requirements** 

Conditions	Core Speed Grade	VCCR_GXB & VCCT_GXB <sup>(2)</sup>	VCCA_GXB	VCCH_GXB	Unit
If BOTH of the following conditions are true:	A11	1.05			
■ Data rate > 10.3 Gbps.	All	1.00			
<ul> <li>DFE is used.</li> </ul>					
If ANY of the following conditions are true <sup>(1)</sup> :			3.0		
<ul> <li>ATX PLL is used.</li> </ul>					
■ Data rate > 6.5Gbps.	All	1.0			
■ DFE (data rate ≤ 10.3 Gbps), AEQ, or EyeQ feature is used.				1.5	V
If ALL of the following	C1, C2, I2, and I3YY	0.90	2.5		
<ul> <li>ATX PLL is not used.</li> </ul>					
■ Data rate $\leq$ 6.5Gbps.	C2L, C3, C4, I2L, I3, I3L, and I4	0.85	2.5		
<ul> <li>DFE, AEQ, and EyeQ are not used.</li> </ul>					

### Notes to Table 8:

(1) Choose this power supply voltage requirement option if you plan to upgrade your design later with any of the listed conditions.

(2) If the VCCR\_GXB and VCCT\_GXB supplies are set to 1.0 V or 1.05 V, they cannot be shared with the VCC core supply. If the VCCR\_GXB and VCCT\_GXB are set to either 0.90 V or 0.85 V, they can be shared with the VCC core supply.

### **DC Characteristics**

This section lists the supply current, I/O pin leakage current, input pin capacitance, on-chip termination tolerance, and hot socketing specifications.

### **Supply Current**

Supply current is the current drawn from the respective power rails used for power budgeting. Use the Excel-based Early Power Estimator (EPE) to get supply current estimates for your design because these currents vary greatly with the resources you use.

For more information about power estimation tools, refer to the *PowerPlay Early Power Estimator User Guide* and the *PowerPlay Power Analysis* chapter in the *Quartus II Handbook*.

I/O Standard	V <sub>IL(DI</sub>	<sub>c)</sub> (V)	V <sub>IH(D</sub>	<sub>C)</sub> (V)	V <sub>IL(AC)</sub> (V)	V <sub>IH(AC)</sub> (V)	V <sub>ol</sub> (V)	V <sub>oh</sub> (V)	I (mA)	l <sub>oh</sub>
i/U Stanuaru	Min	Max	Min	Max	Max	Min	Max	Min	1 <sub>01</sub> (11174)	(mA)
HSTL-18 Class I	—	V <sub>REF</sub> – 0.1	V <sub>REF</sub> + 0.1	_	$V_{REF} - 0.2$	V <sub>REF</sub> + 0.2	0.4	V <sub>CCI0</sub> – 0.4	8	-8
HSTL-18 Class II	_	V <sub>REF</sub> – 0.1	V <sub>REF</sub> + 0.1	_	V <sub>REF</sub> - 0.2	V <sub>REF</sub> + 0.2	0.4	V <sub>CCI0</sub> – 0.4	16	-16
HSTL-15 Class I	_	V <sub>REF</sub> – 0.1	V <sub>REF</sub> + 0.1	_	V <sub>REF</sub> - 0.2	V <sub>REF</sub> + 0.2	0.4	V <sub>CCIO</sub> – 0.4	8	-8
HSTL-15 Class II	_	V <sub>REF</sub> – 0.1	V <sub>REF</sub> + 0.1	_	V <sub>REF</sub> - 0.2	V <sub>REF</sub> + 0.2	0.4	V <sub>CCI0</sub> – 0.4	16	-16
HSTL-12 Class I	-0.15	V <sub>REF</sub> - 0.08	V <sub>REF</sub> + 0.08	V <sub>CCIO</sub> + 0.15	V <sub>REF</sub> – 0.15	V <sub>REF</sub> + 0.15	0.25* V <sub>CCI0</sub>	0.75* V <sub>CCI0</sub>	8	-8
HSTL-12 Class II	-0.15	V <sub>REF</sub> - 0.08	V <sub>REF</sub> + 0.08	V <sub>CCIO</sub> + 0.15	V <sub>REF</sub> – 0.15	V <sub>REF</sub> + 0.15	0.25* V <sub>CCI0</sub>	0.75* V <sub>CCI0</sub>	16	-16
HSUL-12	—	V <sub>REF</sub> – 0.13	V <sub>REF</sub> + 0.13	_	V <sub>REF</sub> – 0.22	V <sub>REF</sub> + 0.22	0.1* V <sub>CCIO</sub>	0.9* V <sub>CCI0</sub>	_	

### Table 19. Single-Ended SSTL, HSTL, and HSUL I/O Standards Signal Specifications for Stratix V Devices (Part 2 of 2)

Table 20. Differential SSTL I/O Standards for Stratix V Devices

1/0 Standard		V <sub>ccio</sub> (V)		V <sub>SWIN</sub>	<sub>G(DC)</sub> (V)		V <sub>X(AC)</sub> (V)		V <sub>SWING(AC)</sub> (V)		
ijo Stanuaru	Min	Тур	Max	Min	Max	Min	Тур	Max	Min	Max	
SSTL-2 Class I, II	2.375	2.5	2.625	0.3	V <sub>CCI0</sub> + 0.6	V <sub>CCI0</sub> /2- 0.2	_	V <sub>CCI0</sub> /2 + 0.2	0.62	V <sub>CCI0</sub> + 0.6	
SSTL-18 Class I, II	1.71	1.8	1.89	0.25	V <sub>CCIO</sub> + 0.6	V <sub>CCI0</sub> /2- 0.175	_	V <sub>CCI0</sub> /2 + 0.175	0.5	V <sub>CCI0</sub> + 0.6	
SSTL-15 Class I, II	1.425	1.5	1.575	0.2	(1)	V <sub>CCI0</sub> /2- 0.15	_	V <sub>CCI0</sub> /2 + 0.15	0.35	_	
SSTL-135 Class I, II	1.283	1.35	1.45	0.2	(1)	V <sub>CCI0</sub> /2- 0.15	V <sub>CCI0</sub> /2	V <sub>CCI0</sub> /2 + 0.15	2(V <sub>IH(AC)</sub> - V <sub>REF</sub> )	2(V <sub>IL(AC)</sub> - V <sub>REF</sub> )	
SSTL-125 Class I, II	1.19	1.25	1.31	0.18	(1)	V <sub>CCI0</sub> /2- 0.15	V <sub>CCI0</sub> /2	V <sub>CCI0</sub> /2 + 0.15	2(V <sub>IH(AC)</sub> - V <sub>REF</sub> )	_	
SSTL-12 Class I, II	1.14	1.2	1.26	0.18	_	V <sub>REF</sub> 0.15	V <sub>CCI0</sub> /2	V <sub>REF</sub> + 0.15	-0.30	0.30	

Note to Table 20:

(1) The maximum value for  $V_{SWING(DC)}$  is not defined. However, each single-ended signal needs to be within the respective single-ended limits  $(V_{IH(DC)} \text{ and } V_{IL(DC)})$ .

								•	-				
I/O		V <sub>ccio</sub> (V)		V <sub>DIF(</sub>	<sub>DC)</sub> (V)		V <sub>X(AC)</sub> (V)			V <sub>CM(DC)</sub> (V	V <sub>DIF(AC)</sub> (V)		
Standard	Min	Тур	Max	Min	Max	Min	Тур	Max	Min	Тур	Max	Min	Max
HSTL-18 Class I, II	1.71	1.8	1.89	0.2	_	0.78	_	1.12	0.78	_	1.12	0.4	_
HSTL-15 Class I, II	1.425	1.5	1.575	0.2	_	0.68	_	0.9	0.68		0.9	0.4	_

- You typically use the interactive Excel-based Early Power Estimator before designing the FPGA to get a magnitude estimate of the device power. The Quartus II PowerPlay Power Analyzer provides better quality estimates based on the specifics of the design after you complete place-and-route. The PowerPlay Power Analyzer can apply a combination of user-entered, simulation-derived, and estimated signal activities that, when combined with detailed circuit models, yields very accurate power estimates.
- **\*** For more information about power estimation tools, refer to the *PowerPlay Early Power Estimator User Guide* and the *PowerPlay Power Analysis* chapter in the *Quartus II Handbook*.

Symbol/	Conditions	Tra	nsceive Grade	r Speed 1	Trai	nsceive Grade	r Speed 2	Trai	nsceive Grade	er Speed e 3	Unit
Description		Min	Тур	Max	Min	Тур	Max	Min	Тур	Max	
Spread-spectrum downspread	PCIe	_	0 to 0.5	_	_	0 to 0.5	_	_	0 to 0.5	_	%
On-chip termination resistors <sup>(21)</sup>	_	_	100		_	100		_	100		Ω
Absolute V <sub>MAX</sub> <sup>(5)</sup>	Dedicated reference clock pin	_	_	1.6	_	_	1.6	_	_	1.6	V
	RX reference clock pin	_		1.2		_	1.2			1.2	
Absolute V <sub>MIN</sub>	—	-0.4	-	_	-0.4	-		-0.4	—		V
Peak-to-peak differential input voltage	_	200	_	1600	200	_	1600	200	_	1600	mV
V <sub>ICM</sub> (AC	Dedicated reference clock pin	1050/	(1000/90	00/850 <sup>(2)</sup>	1050/	1000/9	00/850 <sup>(2)</sup>	1050/	1000/9	00/850 <sup>(2)</sup>	mV
coupled) (9	RX reference clock pin	1	.0/0.9/0	.85 (4)	1.	.0/0.9/0	.85 (4)	1.	.0/0.9/0	.85 <sup>(4)</sup>	V
V <sub>ICM</sub> (DC coupled)	HCSL I/O standard for PCIe reference clock	250		550	250		550	250	_	550	mV
	100 Hz	—	—	-70	—	—	-70	—	—	-70	dBc/Hz
Transmitter	1 kHz	—	—	-90	—	—	-90	—	—	-90	dBc/Hz
REFCLK Phase	10 kHz	—	—	-100	—	—	-100	—	—	-100	dBc/Hz
(622 MHz) <sup>(20)</sup>	100 kHz	—	—	-110	—	—	-110	—	—	-110	dBc/Hz
	≥1 MHz	—	—	-120		—	-120	—	—	-120	dBc/Hz
Transmitter REFCLK Phase Jitter (100 MHz) <sup>(17)</sup>	10 kHz to 1.5 MHz (PCIe)	_	_	3	_	_	3	_	_	3	ps (rms)
R <sub>REF</sub> (19)	_	_	1800 ±1%	_	_	1800 ±1%	_	_	180 0 ±1%	_	Ω
Transceiver Clock	s										
fixedclk <b>clock</b> frequency	PCIe Receiver Detect		100 or 125			100 or 125		_	100 or 125		MHz

## Table 23. Transceiver Specifications for Stratix V GX and GS Devices <sup>(1)</sup> (Part 2 of 7)

Symbol/	Conditions	Trai	nsceive Grade	r Speed 1	Trai	nsceive Grade	r Speed 2	Trai	nsceive Grade	r Speed 3	Unit
Description		Min	Тур	Max	Min	Тур	Max	Min	Тур	Max	
	DC Gain Setting = 0		0	_	_	0	_	_	0	—	dB
	DC Gain Setting = 1	_	2		_	2	_	_	2	_	dB
Programmable DC gain	DC Gain Setting = 2	_	4	_	_	4	_	_	4	_	dB
	DC Gain Setting = 3	_	6	_	_	6	_	_	6	_	dB
	DC Gain Setting = 4		8			8	_		8	_	dB
Transmitter											
Supported I/O Standards	_				-	1.4-V ar	nd 1.5-V PC	ML			
Data rate (Standard PCS)	_	600	_	12200	600	_	12200	600	_	8500/ 10312.5 (24)	Mbps
Data rate (10G PCS)	_	600	_	14100	600	_	12500	600	_	8500/ 10312.5 (24)	Mbps
	85-Ω setting	_	85 ± 20%	_	_	85 ± 20%	_	_	85 ± 20%	—	Ω
Differential on-	100-Ω setting	_	100 ± 20%	_	_	100 ± 20%	_	_	100 ± 20%	_	Ω
chip termination resistors	120-Ω setting		120 ± 20%	_		120 ± 20%	_		120 ± 20%	_	Ω
	150-Ω setting	_	150 ± 20%			150 ± 20%	_		150 ± 20%	_	Ω
V <sub>OCM</sub> (AC coupled)	0.65-V setting	_	650		_	650	_	_	650	—	mV
V <sub>OCM</sub> (DC coupled)	_	_	650	_	_	650		_	650	_	mV
Rise time <sup>(7)</sup>	20% to 80%	30	—	160	30	—	160	30	—	160	ps
Fall time <sup>(7)</sup>	80% to 20%	30		160	30		160	30	—	160	ps
Intra-differential pair skew	Tx V <sub>CM</sub> = 0.5 V and slew rate of 15 ps	_	_	15			15		_	15	ps
Intra-transceiver block transmitter channel-to- channel skew	x6 PMA bonded mode	_	_	120	_	_	120	_		120	ps

### Table 23. Transceiver Specifications for Stratix V GX and GS Devices <sup>(1)</sup> (Part 5 of 7)

## Table 23. Transceiver Specifications for Stratix V GX and GS Devices <sup>(1)</sup> (Part 6 of 7)

Symbol/	Conditions	Trai	nsceive Grade	r Speed 1	Trar	isceive Grade	r Speed 2	Tran	isceive Grade	er Speed e 3	Unit
Description		Min	Тур	Max	Min	Тур	Max	Min	Тур	Max	
Inter-transceiver block transmitter channel-to- channel skew	xN PMA bonded mode	_	_	500	_	_	500	_	_	500	ps
CMU PLL	•									•	
Supported Data Range	_	600	_	12500	600	_	12500	600	_	8500/ 10312.5 (24)	Mbps
t <sub>pll_powerdown</sub> <sup>(15)</sup>	—	1			1			1			μs
t <sub>pll_lock</sub> <sup>(16)</sup>		—		10	—	_	10	—	_	10	μs
ATX PLL											
	VCO post-divider L=2	8000	_	14100	8000	_	12500	8000	_	8500/ 10312.5 (24)	Mbps
Supported Data	L=4	4000	_	7050	4000	_	6600	4000	—	6600	Mbps
Rate Range	L=8	2000		3525	2000		3300	2000		3300	Mbps
	L=8, Local/Central Clock Divider =2	1000	_	1762.5	1000	_	1762.5	1000	_	1762.5	Mbps
t <sub>pll_powerdown</sub> (15)	—	1	_	—	1	_	—	1	_	—	μs
t <sub>pll_lock</sub> (16)	—		—	10		—	10	—		10	μs
fPLL	•										
Supported Data Range	_	600	_	3250/ 3125 <sup>(25)</sup>	600	_	3250/ 3125 <sup>(25)</sup>	600	_	3250/ 3125 <sup>(25)</sup>	Mbps
t <sub>pll_powerdown</sub> <sup>(15)</sup>	_	1	—		1	—		1			μs

Symbol/	Conditions	Transceiver Speed Grade 1			Transceiver Speed Grade 2			Transceiver Speed Grade 3			Unit
Description		Min	Тур	Max	Min	Тур	Max	Min	Тур	Max	
t <sub>pll_lock</sub> (16)	_			10			10		_	10	μs

#### Table 23. Transceiver Specifications for Stratix V GX and GS Devices <sup>(1)</sup> (Part 7 of 7)

#### Notes to Table 23:

(2) The reference clock common mode voltage is equal to the V<sub>CCR\_GXB</sub> power supply level.

(3) This supply must be connected to 1.0 V if the transceiver is configured at a data rate > 6.5 Gbps, and to 1.05 V if configured at a data rate > 10.3 Gbps when DFE is used. For data rates up to 6.5 Gbps, you can connect this supply to 0.85 V.

- (4) This supply follows VCCR\_GXB.
- (5) The device cannot tolerate prolonged operation at this absolute maximum.
- (6) The differential eye opening specification at the receiver input pins assumes that **Receiver Equalization** is disabled. If you enable **Receiver Equalization**, the receiver circuitry can tolerate a lower minimum eye opening, depending on the equalization level.
- (7) The Quartus II software automatically selects the appropriate slew rate depending on the configured data rate or functional mode.
- (8) The input reference clock frequency options depend on the data rate and the device speed grade.
- (9) The line data rate may be limited by PCS-FPGA interface speed grade.
- (10) Refer to Figure 1 for the GX channel AC gain curves. The total effective AC gain is the AC gain minus the DC gain.
- (11) t<sub>LTR</sub> is the time required for the receive CDR to lock to the input reference clock frequency after coming out of reset.
- (12) t<sub>LTD</sub> is time required for the receiver CDR to start recovering valid data after the rx\_is\_lockedtodata signal goes high.
- (13) t<sub>LTD\_manual</sub> is the time required for the receiver CDR to start recovering valid data after the rx\_is\_lockedtodata signal goes high when the CDR is functioning in the manual mode.
- (14)  $t_{LTR\_LTD\_manual}$  is the time the receiver CDR must be kept in lock to reference (LTR) mode after the rx\_is\_lockedtoref signal goes high when the CDR is functioning in the manual mode.
- (15)  $t_{pll_powerdown}$  is the PLL powerdown minimum pulse width.
- (16) t<sub>pll lock</sub> is the time required for the transmitter CMU/ATX PLL to lock to the input reference clock frequency after coming out of reset.
- (17) To calculate the REFCLK rms phase jitter requirement for PCIe at reference clock frequencies other than 100 MHz, use the following formula: REFCLK rms phase jitter at f(MHz) = REFCLK rms phase jitter at 100 MHz × 100/f.
- (18) The maximum peak to peak differential input voltage  $V_{ID}$  after device configuration is equal to 4 × (absolute  $V_{MAX}$  for receiver pin  $V_{ICM}$ ).
- (19) For ES devices,  $R_{BEF}$  is 2000  $\Omega \pm 1\%$ .
- (20) To calculate the REFCLK phase noise requirement at frequencies other than 622 MHz, use the following formula: REFCLK phase noise at f(MHz) = REFCLK phase noise at 622 MHz + 20\*log(f/622).
- (21) SFP/+ optical modules require the host interface to have RD+/- differentially terminated with 100 Ω. The internal OCT feature is available after the Stratix V FPGA configuration is completed. Altera recommends that FPGA configuration is completed before inserting the optical module. Otherwise, minimize unnecessary removal and insertion with unconfigured devices.
- (22) Refer to Figure 2.
- (23) For oversampling designs to support data rates less than the minimum specification, the CDR needs to be in LTR mode only.
- (24) I3YY devices can achieve data rates up to 10.3125 Gbps.
- (25) When you use fPLL as a TXPLL of the transceiver.
- (26) REFCLK performance requires to meet transmitter REFCLK phase noise specification.
- (27) Minimum eye opening of 85 mV is only for the unstressed input eye condition.

<sup>(1)</sup> Speed grades shown in Table 23 refer to the PMA Speed Grade in the device ordering code. The maximum data rate could be restricted by the Core/PCS speed grade. Contact your Altera Sales Representative for the maximum data rate specifications in each speed grade combination offered. For more information about device ordering codes, refer to the Stratix V Device Overview.





Figure 3 shows the Stratix V AC gain curves for GX channels.

Figure 3. AC Gain Curves for GX Channels (full bandwidth)

Stratix V GT devices contain both GX and GT channels. All transceiver specifications for the GX channels not listed in Table 28 are the same as those listed in Table 23.

Table 28 lists the Stratix V GT transceiver specifications.

Symbol/	Conditions	S	Transceive peed Grade	2	S	Fransceive Deed Grade	r 3	Unit
Description		Min	Тур	Max	Min	Тур	Max	
Differential on-chip termination resistors <sup>(7)</sup>	GT channels		100	_	_	100	_	Ω
	85- $\Omega$ setting	_	85 ± 30%	_	_	85 ± 30%	_	Ω
Differential on-chip	100-Ω setting	_	100 ± 30%	_	_	100 ± 30%	_	Ω
for GX channels <sup>(19)</sup>	120-Ω setting	_	120 ± 30%	_	—	120 ± 30%	—	Ω
	150-Ω setting		150 ± 30%	_	_	150 ± 30%	_	Ω
V <sub>ICM</sub> (AC coupled)	GT channels	_	650	_	—	650	—	mV
	VCCR_GXB = 0.85 V or 0.9 V	_	600	_	_	600	_	mV
VICM (AC and DC coupled) for GX Channels	VCCR_GXB = 1.0 V full bandwidth	_	700		_	700	_	mV
	VCCR_GXB = 1.0 V half bandwidth	_	750	_	_	750	_	mV
t <sub>LTR</sub> <sup>(9)</sup>	—	_	—	10	—	—	10	μs
t <sub>LTD</sub> <sup>(10)</sup>		4			4	_	_	μs
t <sub>LTD_manual</sub> <sup>(11)</sup>		4	_		4	_	_	μs
t <sub>LTR_LTD_manual</sub> <sup>(12)</sup>	—	15	—	_	15	—	—	μs
Run Lenath	GT channels		—	72	—	—	72	CID
	GX channels				(8)			
CDR PPM	GT channels	_	—	1000	—	—	1000	± PPM
	GX channels				(8)			
Programmable	GT channels	_		14		_	14	dB
(AC Gain) <sup>(5)</sup>	GX channels				(8)			
Programmable	GT channels	_		7.5	_		7.5	dB
DC gain <sup>(6)</sup>	GX channels				(8)			
Differential on-chip termination resistors <sup>(7)</sup>	GT channels	_	100	—	_	100	_	Ω
Transmitter								
Supported I/O Standards	_	1.4-V and 1.5-V PCML						
Data rate (Standard PCS)	GX channels	600	_	8500	600		8500	Mbps
Data rate (10G PCS)	GX channels	600		12,500	600		12,500	Mbps

## Table 28. Transceiver Specifications for Stratix V GT Devices (Part 3 of 5)<sup>(1)</sup>

Table 29 shows the  $V_{\text{OD}}$  settings for the GT channel.

Symbol	V <sub>OD</sub> Setting	V <sub>od</sub> Value (mV)
	0	0
	1	200
V., differential neak to neak typical $(1)$	2	400
The fine contrar hear to hear the field to	3	600
	4	800
	5	1000

### Note:

(1) Refer to Figure 4.

# **Periphery Performance**

This section describes periphery performance, including high-speed I/O and external memory interface.

I/O performance supports several system interfaces, such as the **LVDS** high-speed I/O interface, external memory interface, and the **PCI/PCI-X** bus interface. General-purpose I/O standards such as 3.3-, 2.5-, 1.8-, and 1.5-**LVTTL/LVCMOS** are capable of a typical 167 MHz and 1.2-**LVCMOS** at 100 MHz interfacing frequency with a 10 pF load.

The actual achievable frequency depends on design- and system-specific factors. Ensure proper timing closure in your design and perform HSPICE/IBIS simulations based on your specific design and system setup to determine the maximum achievable frequency in your system.

### **High-Speed I/O Specification**

Table 36 lists high-speed I/O timing for Stratix V devices.

Table 36. High-Speed I/O Specifications for Stratix V Devices (1), (2) (Part 1 of 4)

Sumbol	Conditions	C1		C2, C2L, I2, I2L		C3, I3, I3L, I3YY		C4,14			11			
Symbol		Min	Тур	Max	Min	Тур	Max	Min	Тур	Max	Min	Тур	Max	UNIT
f <sub>HSCLK_in</sub> (input clock frequency) True Differential I/O Standards	Clock boost factor W = 1 to 40 $^{(4)}$	5	_	800	5		800	5		625	5		525	MHz
f <sub>HSCLK_in</sub> (input clock frequency) Single Ended I/O Standards <sup>(3)</sup>	Clock boost factor W = 1 to 40 $^{(4)}$	5		800	5		800	5		625	5		525	MHz
f <sub>HSCLK_in</sub> (input clock frequency) Single Ended I/O Standards	Clock boost factor W = 1 to 40 $^{(4)}$	5	_	520	5		520	5	_	420	5	_	420	MHz
f <sub>HSCLK_OUT</sub> (output clock frequency)	_	5	_	800	5	_	800	5	_	625 (5)	5	_	525 (5)	MHz

	Conditions		C1		C2,	C2L, I	2, I2L	C3,	13, 131	., <b>I</b> 3YY	C4,14			
Symbol	Conditions	Min	Тур	Max	Min	Тур	Max	Min	Тур	Max	Min	Тур	Max	Unit
t <sub>duty</sub>	Transmitter output clock duty cycle for both True and Emulated Differential I/O Standards	45	50	55	45	50	55	45	50	55	45	50	55	%
	True Differential I/O Standards	_	_	160	_	_	160	_	_	200	_	_	200	ps
t <sub>rise</sub> & t <sub>fall</sub>	Emulated Differential I/O Standards with three external output resistor networks			250			250			250			300	ps
TCCS	True Differential I/O Standards	_	_	150	_	_	150	_	_	150	_	_	150	ps
	Emulated Differential I/O Standards			300			300	_		300			300	ps
Receiver														
	SERDES factor J = 3 to 10 (11), (12), (13), (14), (15), (16)	150		1434	150	_	1434	150	_	1250	150	_	1050	Mbps
True Differential I/O Standards - f <sub>HSDRDPA</sub> (data rate)	SERDES factor J ≥ 4 LVDS RX with DPA (12), (14), (15), (16)	150	_	1600	150	_	1600	150	_	1600	150	_	1250	Mbps
	SERDES factor J = 2, uses DDR Registers	(6)		(7)	(6)	_	(7)	(6)	_	(7)	(6)	_	(7)	Mbps
	SERDES factor J = 1, uses SDR Register	(6)	_	(7)	(6)	_	(7)	(6)	_	(7)	(6)		(7)	Mbps

# Table 36. High-Speed I/O Specifications for Stratix V Devices (1), (2) (Part 3 of 4)

Figure 7 shows the dynamic phase alignment (DPA) lock time specifications with the DPA PLL calibration option enabled.

Figure 7. DPA Lock Time Specification with DPA PLL Calibration Enabled

rx_reset			
rx_dpa_locked			<u> </u>
			-

Table 37 lists the DPA lock time specifications for Stratix V devices.

Table 37. DPA Lock Time Specifications for Stratix V GX Devices Only (1), (2), (3)

Standard	Training Pattern	Number of Data Transitions in One Repetition of the Training Pattern	Number of Repetitions per 256 Data Transitions <sup>(4)</sup>	Maximum	
SPI-4	00000000001111111111	2	128	640 data transitions	
Parallel Rapid I/O	00001111	2	128	640 data transitions	
	10010000	4	64	640 data transitions	
Miscellaneous	10101010	8	32	640 data transitions	
Wiscenareous	01010101	8	32	640 data transitions	

#### Notes to Table 37:

(1) The DPA lock time is for one channel.

(2) One data transition is defined as a 0-to-1 or 1-to-0 transition.

(3) The DPA lock time stated in this table applies to both commercial and industrial grade.

(4) This is the number of repetitions for the stated training pattern to achieve the 256 data transitions.

Figure 8 shows the **LVDS** soft-clock data recovery (CDR)/DPA sinusoidal jitter tolerance specification for a data rate  $\geq$  1.25 Gbps. Table 38 lists the **LVDS** soft-CDR/DPA sinusoidal jitter tolerance specification for a data rate  $\geq$  1.25 Gbps.





# **Duty Cycle Distortion (DCD) Specifications**

Table 44 lists the worst-case DCD for Stratix V devices.

### Table 44. Worst-Case DCD on Stratix V I/O Pins (1)

Symbol	C1 C2, C2L		, 12, 12L C3, 13, 13L, 13YY		C4,14		Unit		
-	Min	Max	Min	Max	Min	Max	Min	Max	
Output Duty Cycle	45	55	45	55	45	55	45	55	%

### Note to Table 44:

(1) The DCD numbers do not cover the core clock network.

# **Configuration Specification**

# **POR Delay Specification**

Power-on reset (POR) delay is defined as the delay between the time when all the power supplies monitored by the POR circuitry reach the minimum recommended operating voltage to the time when the nSTATUS is released high and your device is ready to begin configuration.



For more information about the POR delay, refer to the *Hot Socketing and Power-On Reset in Stratix V Devices* chapter.

Table 45 lists the fast and standard POR delay specification.

### Table 45. Fast and Standard POR Delay Specification (1)

POR Delay	Minimum	Maximum		
Fast	4 ms	12 ms		
Standard	100 ms	300 ms		

### Note to Table 45:

(1) You can select the POR delay based on the MSEL settings as described in the MSEL Pin Settings section of the "Configuration, Design Security, and Remote System Upgrades in Stratix V Devices" chapter.

# **JTAG Configuration Specifications**

Table 46 lists the JTAG timing parameters and values for Stratix V devices.

Table 46. JTAG Timing Parameters and Values for Stratix V Devices

Symbol	Description	Min	Max	Unit
t <sub>JCP</sub>	TCK clock period <sup>(2)</sup>	30		ns
t <sub>JCP</sub>	TCK clock period <sup>(2)</sup>	167	—	ns
t <sub>JCH</sub>	TCK clock high time <sup>(2)</sup>	14	—	ns
t <sub>JCL</sub>	TCK clock low time <sup>(2)</sup>	14		ns
t <sub>JPSU (TDI)</sub>	TDI JTAG port setup time	2	—	ns
t <sub>JPSU (TMS)</sub>	TMS JTAG port setup time	3	_	ns

	Member Code		Active Serial <sup>(1)</sup>	)	Fast Passive Parallel <sup>(2)</sup>				
Variant		Width	DCLK (MHz)	Min Config Time (s)	Width	DCLK (MHz)	Min Config Time (s)		
	D3	4	100	0.344	32	100	0.043		
	D4	4	100	0.534	32	100	0.067		
65	04	4	100	0.344	32	100	0.043		
03	D5	4	100	0.534	32	100	0.067		
	D6	4	100	0.741	32	100	0.093		
	D8	4	100	0.741	32	100	0.093		
E	E9	4	100	0.857	32	100	0.107		
	EB	4	100	0.857	32	100	0.107		

Table 48. Minimum Configuration Time Estimation for Stratix V Devices

### Notes to Table 48:

(1) DCLK frequency of 100 MHz using external CLKUSR.

(2) Max FPGA FPP bandwidth may exceed bandwidth available from some external storage or control logic.

# **Fast Passive Parallel Configuration Timing**

This section describes the fast passive parallel (FPP) configuration timing parameters for Stratix V devices.

# DCLK-to-DATA[] Ratio for FPP Configuration

FPP configuration requires a different DCLK-to-DATA[]ratio when you enable the design security, decompression, or both features. Table 49 lists the DCLK-to-DATA[]ratio for each combination.

Configuration Scheme	Decompression	Design Security	DCLK-to-DATA[] Ratio
	Disabled	Disabled	1
	Disabled	Enabled	1
111 ×0	Enabled	Disabled	2
	Enabled	Enabled	2
	Disabled	Disabled	1
	Disabled	Enabled	2
FPP × 10	Enabled	Disabled	4
	Enabled	Enabled	4

 Table 49. DCLK-to-DATA[] Ratio <sup>(1)</sup> (Part 1 of 2)

# **Active Serial Configuration Timing**

Table 52 lists the DCLK frequency specification in the AS configuration scheme.

Fable 52.	DCLK Frequency	Specification in th	e AS Configuration	Scheme <sup>(1),</sup>	(2)
-----------	----------------	---------------------	--------------------	------------------------	-----

Minimum	Typical	Maximum	Unit
5.3	7.9	12.5	MHz
10.6	15.7	25.0	MHz
21.3	31.4	50.0	MHz
42.6	62.9	100.0	MHz

#### Notes to Table 52:

(1) This applies to the DCLK frequency specification when using the internal oscillator as the configuration clock source.

(2) The AS multi-device configuration scheme does not support DCLK frequency of 100 MHz.

Figure 14 shows the single-device configuration setup for an AS ×1 mode.





#### Notes to Figure 14:

- (1) If you are using AS  $\times 4$  mode, this signal represents the AS\_DATA[3..0] and EPCQ sends in 4-bits of data for each DCLK cycle.
- (2) The initialization clock can be from internal oscillator or CLKUSR pin.
- (3) After the option bit to enable the INIT\_DONE pin is configured into the device, the INIT\_DONE goes low.

Table 53 lists the timing parameters for AS  $\times 1$  and AS  $\times 4$  configurations in Stratix V devices.

Table JS. As fining falancees for as $\times 1$ and as $\times 4$ configurations in straits V devices $(2, 2, 2, 3, 3, 3, 3, 3, 3, 3, 3, 3, 3, 3, 3, 3,$	Table 53.	AS Timing	<b>Parameters for AS</b>	$\times$ 1 and AS $\times$ 4 Confi	gurations in Stratix V	/ Devices <sup>(1),</sup> (2)	(Part 1 of 2)
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Symbol	Parameter	Minimum	Maximum	Units
t <sub>CO</sub>	DCLK falling edge to AS_DATA0/ASDO output	—	2	ns
t <sub>SU</sub>	Data setup time before falling edge on DCLK	1.5	_	ns
t <sub>H</sub>	Data hold time after falling edge on DCLK	0	_	ns

# **Remote System Upgrades**

Table 56 lists the timing parameter specifications for the remote system upgrade circuitry.

Table 56. Remote System Upgrade Circuitry Timing Specificatio
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Parameter	Minimum	Maximum	Unit
t <sub>RU_nCONFIG</sub> <sup>(1)</sup>	250	—	ns
t <sub>RU_nRSTIMER</sub> <sup>(2)</sup>	250	_	ns

#### Notes to Table 56:

- (1) This is equivalent to strobing the reconfiguration input of the ALTREMOTE\_UPDATE megafunction high for the minimum timing specification. For more information, refer to the Remote System Upgrade State Machine section of the "Configuration, Design Security, and Remote System Upgrades in Stratix V Devices" chapter.
- (2) This is equivalent to strobing the reset\_timer input of the ALTREMOTE\_UPDATE megafunction high for the minimum timing specification. For more information, refer to the User Watchdog Timer section of the "Configuration, Design Security, and Remote System Upgrades in Stratix V Devices" chapter.

# **User Watchdog Internal Circuitry Timing Specification**

Table 57 lists the operating range of the 12.5-MHz internal oscillator.

### Table 57. 12.5-MHz Internal Oscillator Specifications

Minimum	Typical	Maximum	Units
5.3	7.9	12.5	MHz

# I/O Timing

Altera offers two ways to determine I/O timing—the Excel-based I/O Timing and the Quartus II Timing Analyzer.

Excel-based I/O timing provides pin timing performance for each device density and speed grade. The data is typically used prior to designing the FPGA to get an estimate of the timing budget as part of the link timing analysis. The Quartus II Timing Analyzer provides a more accurate and precise I/O timing data based on the specifics of the design after you complete place-and-route.

 You can download the Excel-based I/O Timing spreadsheet from the Stratix V Devices Documentation web page.

# **Programmable IOE Delay**

Table 58 lists the Stratix V IOE programmable delay settings.

Table 58. IOE Programmable Delay for Stratix V Devices (Part 1 of 2)

Deremeter	Available	Min	Fast	Model				Slow N	lodel			
(1)	Settings	<b>Offset</b> (2)	Industrial	Commercial	C1	C2	C3	C4	12	13, 13YY	14	Unit
D1	64	0	0.464	0.493	0.838	0.838	0.924	1.011	0.844	0.921	1.006	ns
D2	32	0	0.230	0.244	0.415	0.415	0.459	0.503	0.417	0.456	0.500	ns

Table 60.	Glossary	(Part 3 of 4)
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Letter	Subject	Definitions				
	SW (sampling window)	Timing Diagram—the period of time during which the data must be valid in order to capture it correctly. The setup and hold times determine the ideal strobe position within the sampling window, as shown:         Bit Time         0.5 x TCCS       RSKM         Sampling Window       RSKM         0.5 x TCCS       RSKM				
S	Single-ended voltage referenced I/O standard	The JEDEC standard for SSTL and HSTL I/O defines both the AC and DC input signal va         The AC values indicate the voltage levels at which the receiver must meet its timing         specifications. The DC values indicate the voltage levels at which the final logic state of         receiver is unambiguously defined. After the receiver input has crossed the AC value, the         receiver changes to the new logic state.         The new logic state is then maintained as long as the input stays beyond the DC threshor         This approach is intended to provide predictable receiver timing in the presence of input waveform ringing:         Single-Ended Voltage Referenced I/O Standard				
	t <sub>C</sub>	High-speed receiver and transmitter input and output clock period.				
	TCCS (channel- to-channel-skew)	The timing difference between the fastest and slowest output edges, including $t_{CO}$ variation and clock skew, across channels driven by the same PLL. The clock is included in the TCCS measurement (refer to the <i>Timing Diagram</i> figure under <b>SW</b> in this table).				
		High-speed I/O block—Duty cycle on the high-speed transmitter output clock.				
т	t <sub>DUTY</sub>	<b>Timing Unit Interval (TUI)</b> The timing budget allowed for skew, propagation delays, and the data sampling window.				
		$(TUI = 1/(receiver input clock frequency multiplication factor) = t_c/w)$				
	t <sub>FALL</sub>	Signal high-to-low transition time (80-20%)				
	t <sub>INCCJ</sub>	Cycle-to-cycle jitter tolerance on the PLL clock input.				
	t <sub>outpj_i0</sub>	Period jitter on the general purpose I/O driven by a PLL.				
	t <sub>outpj_dc</sub>	Period jitter on the dedicated clock output driven by a PLL.				
	<b>t</b> <sub>RISE</sub>	Signal low-to-high transition time (20-80%)				
U		_				

Letter	Subject	Definitions
	V <sub>CM(DC)</sub>	DC common mode input voltage.
	V <sub>ICM</sub>	Input common mode voltage—The common mode of the differential signal at the receiver.
	V <sub>ID</sub>	Input differential voltage swing—The difference in voltage between the positive and complementary conductors of a differential transmission at the receiver.
	V <sub>DIF(AC)</sub>	AC differential input voltage—Minimum AC input differential voltage required for switching.
	V <sub>DIF(DC)</sub>	DC differential input voltage— Minimum DC input differential voltage required for switching.
	V <sub>IH</sub>	Voltage input high—The minimum positive voltage applied to the input which is accepted by the device as a logic high.
	V <sub>IH(AC)</sub>	High-level AC input voltage
	V <sub>IH(DC)</sub>	High-level DC input voltage
V	V <sub>IL</sub>	Voltage input low—The maximum positive voltage applied to the input which is accepted by the device as a logic low.
	V <sub>IL(AC)</sub>	Low-level AC input voltage
	V <sub>IL(DC)</sub>	Low-level DC input voltage
	V <sub>OCM</sub>	Output common mode voltage—The common mode of the differential signal at the transmitter.
	V <sub>OD</sub>	Output differential voltage swing—The difference in voltage between the positive and complementary conductors of a differential transmission at the transmitter.
	V <sub>SWING</sub>	Differential input voltage
	V <sub>X</sub>	Input differential cross point voltage
	V <sub>OX</sub>	Output differential cross point voltage
W	W	High-speed I/O block—clock boost factor
X		
Y	—	—
Z		

### Table 60. Glossary (Part 4 of 4)