E·XFL

Intel - 5SGXEA4K1F35C2N Datasheet



Welcome to <u>E-XFL.COM</u>

Understanding <u>Embedded - FPGAs (Field</u> <u>Programmable Gate Array)</u>

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Obsolete
Number of LABs/CLBs	158500
Number of Logic Elements/Cells	420000
Total RAM Bits	37888000
Number of I/O	432
Number of Gates	-
Voltage - Supply	0.87V ~ 0.93V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	1152-BBGA, FCBGA
Supplier Device Package	1152-FBGA (35x35)
Purchase URL	https://www.e-xfl.com/product-detail/intel/5sgxea4k1f35c2n

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

								1
Transceiver Speed				Core Spe	ed Grade			
Grade	C1	C2, C2L	C3	C4	12, 12L	13, 13L	I 3YY	14
3 GX channel—8.5 Gbps	_	Yes	Yes	Yes	_	Yes	Yes ⁽⁴⁾	Yes

Table 1. Stratix V GX and GS Commercial and Industrial Speed Grade Offering ^{(1), (2), (3)} (Part 2 of 2)

Notes to Table 1:

(1) C = Commercial temperature grade; I = Industrial temperature grade.

(2) Lower number refers to faster speed grade.

(3) C2L, I2L, and I3L speed grades are for low-power devices.

(4) I3YY speed grades can achieve up to 10.3125 Gbps.

Table 2 lists the industrial and commercial speed grades for the Stratix V GT devices. **Table 2. Stratix V GT Commercial and Industrial Speed Grade Offering** ⁽¹⁾, ⁽²⁾

Transseiver Speed Grade	Core Speed Grade							
Transceiver Speeu draue	C1	C2	12	13				
2 GX channel—12.5 Gbps GT channel—28.05 Gbps	Yes	Yes	_	_				
3 GX channel—12.5 Gbps GT channel—25.78 Gbps	Yes	Yes	Yes	Yes				

Notes to Table 2:

(1) C = Commercial temperature grade; I = Industrial temperature grade.

(2) Lower number refers to faster speed grade.

Absolute Maximum Ratings

Absolute maximum ratings define the maximum operating conditions for Stratix V devices. The values are based on experiments conducted with the devices and theoretical modeling of breakdown and damage mechanisms. The functional operation of the device is not implied for these conditions.



Conditions other than those listed in Table 3 may cause permanent damage to the device. Additionally, device operation at the absolute maximum ratings for extended periods of time may have adverse effects on the device.

TANIC J. ANSULULC MAXIMUM NALINYS IVI SUALIX V DEVICES (FAIL I UI Z)	Table 3.	Absolute Maximum	Ratings	for Stratix \	/ Devices	(Part 1 of 2)
--	----------	-------------------------	---------	---------------	-----------	---------------

Symbol	Description	Minimum	Maximum	Unit
V _{CC}	Power supply for core voltage and periphery circuitry	-0.5	1.35	V
V _{CCPT}	Power supply for programmable power technology	-0.5	1.8	V
V _{CCPGM}	Power supply for configuration pins	-0.5	3.9	V
V _{CC_AUX}	Auxiliary supply for the programmable power technology	-0.5	3.4	V
V _{CCBAT}	Battery back-up power supply for design security volatile key register	-0.5	3.9	V
V _{CCPD}	I/O pre-driver power supply	-0.5	3.9	V
V _{CCIO}	I/O power supply	-0.5	3.9	V

This section lists the functional operating limits for the AC and DC parameters for Stratix V devices. Table 6 lists the steady-state voltage and current values expected from Stratix V devices. Power supply ramps must all be strictly monotonic, without plateaus.

Table 6. Recommended Operating Conditions for Stratix V Devices (Part 1 of 2)

Symbol	Description	Condition	Min ⁽⁴⁾	Тур	Max ⁽⁴⁾	Unit
	Core voltage and periphery circuitry power supply (C1, C2, I2, and I3YY speed grades)	_	0.87	0.9	0.93	V
V _{CC}	Core voltage and periphery circuitry power supply (C2L, C3, C4, I2L, I3, I3L, and I4 speed grades) ⁽³⁾		0.82	0.85	0.88	V
V _{CCPT}	Power supply for programmable power technology	_	1.45	1.50	1.55	V
V _{CC_AUX}	Auxiliary supply for the programmable power technology		2.375	2.5	2.625	V
VI (1)	I/O pre-driver (3.0 V) power supply	_	2.85	3.0	3.15	V
VCCPD	I/O pre-driver (2.5 V) power supply		2.375	2.5	2.625	V
	I/O buffers (3.0 V) power supply	_	2.85	3.0	3.15	V
	I/O buffers (2.5 V) power supply		2.375	2.5	2.625	V
	I/O buffers (1.8 V) power supply	_	1.71	1.8	1.89	V
V _{CCIO}	I/O buffers (1.5 V) power supply	_	1.425	1.5	1.575	V
	I/O buffers (1.35 V) power supply		1.283	1.35	1.45	V
	I/O buffers (1.25 V) power supply	_	1.19	1.25	1.31	V
	I/O buffers (1.2 V) power supply	_	1.14	1.2	1.26	V
	Configuration pins (3.0 V) power supply		2.85	3.0	3.15	V
V _{CCPGM}	Configuration pins (2.5 V) power supply	_	2.375	2.5	2.625	V
	Configuration pins (1.8 V) power supply	-	1.71	1.8	1.89	V
V _{CCA_FPLL}	PLL analog voltage regulator power supply		2.375	2.5	2.625	V
V _{CCD_FPLL}	PLL digital voltage regulator power supply	-	1.45	1.5	1.55	V
V _{CCBAT} (2)	Battery back-up power supply (For design security volatile key register)	_	1.2	_	3.0	V
VI	DC input voltage	_	-0.5	—	3.6	V
V ₀	Output voltage		0	_	V _{CCIO}	V
т	Operating junction temperature	Commercial	0	—	85	°C
IJ		Industrial	-40	_	100	°C

I/O Pin Leakage Current

Table 9 lists the Stratix V I/O pin leakage current specifications.

Table 9.	I/O Pin	Leakage	Current for	Stratix V	Devices (1)
----------	---------	---------	--------------------	-----------	-------------

Symbol	Description	Conditions	Min	Тур	Max	Unit
I _I	Input pin	$V_I = 0 V \text{ to } V_{CCIOMAX}$	-30	_	30	μA
I _{OZ}	Tri-stated I/O pin	$V_0 = 0 V \text{ to } V_{\text{CCIOMAX}}$	-30		30	μA

Note to Table 9:

(1) If $V_0 = V_{CCI0}$ to $V_{CCI0Max}$, 100 μ A of leakage current per I/O is expected.

Bus Hold Specifications

Table 10 lists the Stratix V device family bus hold specifications.

Table 10. Bus Hold Parameters for Stratix V Devices

			V _{CCIO}										
Parameter	Conditions	1.2	2 V	1.5 V		1.8 V		2.5 V		3.0 V		Unit	
			Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Low sustaining current	I _{SUSL}	V _{IN} > V _{IL} (maximum)	22.5	_	25.0	_	30.0	_	50.0	_	70.0	_	μA
High sustaining current	I _{SUSH}	V _{IN} < V _{IH} (minimum)	-22.5		-25.0	_	-30.0	_	-50.0	_	-70.0		μA
Low overdrive current	I _{odl}	$0V < V_{IN} < V_{CCIO}$		120		160		200	_	300		500	μA
High overdrive current	I _{odh}	$0V < V_{IN} < V_{CCIO}$		-120		-160		-200		-300		-500	μΑ
Bus-hold trip point	V _{TRIP}	_	0.45	0.95	0.50	1.00	0.68	1.07	0.70	1.70	0.80	2.00	۷

On-Chip Termination (OCT) Specifications

If you enable OCT calibration, calibration is automatically performed at power-up for I/Os connected to the calibration block. Table 11 lists the Stratix V OCT termination calibration accuracy specifications.

Table 11. OCT Calibration Accuracy Specifications for Stratix V Devices ⁽¹⁾ (Part 1 of 2)

				Calibratio	n Accuracy		
Symbol	Description	Conditions	C1	C2,12	C3,I3, I3YY	C4,14	Unit
25- $Ω$ R _S	Internal series termination with calibration (25- Ω setting)	V _{CCI0} = 3.0, 2.5, 1.8, 1.5, 1.2 V	±15	±15	±15	±15	%

				Calibratio	n Accuracy		
Symbol	Description	Conditions	C1	C2,I2	C3,I3, I3YY	C4,14	Unit
50-Ω R _S	Internal series termination with calibration (50- Ω setting)	V _{CCI0} = 3.0, 2.5, 1.8, 1.5, 1.2 V	±15	±15	±15	±15	%
34- Ω and 40- Ω R _S	Internal series termination with calibration (34- Ω and 40- Ω setting)	V _{CCI0} = 1.5, 1.35, 1.25, 1.2 V	±15	±15	±15	±15	%
48-Ω, 60-Ω, 80-Ω, and 240-Ω R _S	Internal series termination with calibration (48- Ω , 60- Ω , 80- Ω , and 240- Ω setting)	V _{CCI0} = 1.2 V	±15	±15	±15	±15	%
50-Ω R _T	Internal parallel termination with calibration (50-Ω setting)	V _{CCI0} = 2.5, 1.8, 1.5, 1.2 V	-10 to +40	-10 to +40	-10 to +40	-10 to +40	%
20-Ω, 30-Ω, 40-Ω,60-Ω, and 120-Ω R _T	Internal parallel termination with calibration ($20 - \Omega$, $30 - \Omega$, $40 - \Omega$, $60 - \Omega$, and $120 - \Omega$ setting)	V _{CCI0} = 1.5, 1.35, 1.25 V	-10 to +40	-10 to +40	-10 to +40	-10 to +40	%
60- $Ω$ and 120- $Ω$ R _T	Internal parallel termination with calibration (60-Ω and 120-Ω setting)	V _{CCI0} = 1.2	-10 to +40	-10 to +40	-10 to +40	-10 to +40	%
$25-\Omega \\ R_{S_left_shift}$	Internal left shift series termination with calibration ($25-\Omega$ R _{S_left_shift} setting)	V _{CCI0} = 3.0, 2.5, 1.8, 1.5, 1.2 V	±15	±15	±15	±15	%

Table II. OUI Valiblation Accuracy specifications for Stratix V Devices' / (Latt 2 OF	Table 11.	OCT Calibration A	ccuracy Specificati	ons for Stratix V D	Devices ⁽¹⁾ (Part 2 of
---	-----------	--------------------------	---------------------	---------------------	--------------------------	-----------

Note to Table 11:

(1) OCT calibration accuracy is valid at the time of calibration only.

Table 12 lists the Stratix V OCT without calibration resistance to PVT changes.

Table 12.	OCT Without Calibration	Resistance 1	Tolerance	Specifications	for Stratix	V Devices	(Part 1	of 2)
-----------	-------------------------	---------------------	------------------	-----------------------	-------------	------------------	---------	-------

			Re	!			
Symbol	Description	Conditions	C1	C2,I2	C3, I3, I3YY	C4, I4	Unit
25-Ω R, 50-Ω R _S	Internal series termination without calibration (25-Ω setting)	$V_{CCIO} = 3.0$ and 2.5 V	±30	±30	±40	±40	%
25-Ω R _S	Internal series termination without calibration (25-Ω setting)	V _{CCIO} = 1.8 and 1.5 V	±30	±30	±40	±40	%
25-Ω R _S	Internal series termination without calibration (25-Ω setting)	V _{CCI0} = 1.2 V	±35	±35	±50	±50	%

I/O		V _{ccio} (V)		V _{DIF(DC)} (V)		V _{X(AC)} (V)			V _{CM(DC)} (V)			V _{DIF(AC)} (V)	
Standard	Min	Тур	Max	Min	Max	Min	Тур	Max	Min	Тур	Max	Min	Max
HSTL-12 Class I, II	1.14	1.2	1.26	0.16	V _{CCI0} + 0.3	_	0.5* V _{CCI0}	_	0.4* V _{CCIO}	0.5* V _{CCIO}	0.6* V _{CCI0}	0.3	V _{CCI0} + 0.48
HSUL-12	1.14	1.2	1.3	0.26	0.26	0.5*V _{CCI0} - 0.12	0.5* V _{CCI0}	0.5*V _{CCI0} + 0.12	0.4* V _{CCIO}	0.5* V _{CCIO}	0.6* V _{CCIO}	0.44	0.44

Table 21. Differential HSTL and HSUL I/O Standards for Stratix V Devices (Part 2 of 2)

Table 22. Differential I/O Standard Specifications for Stratix V Devices (7)

I/O	Vc	_{cio} (V)	(10)		V _{ID} (mV) ⁽⁸⁾			V _{ICM(DC)} (V)		Vo	_D (V) (6)	v	_{осм} (V)	(6)
Standard	Min	Тур	Max	Min	Condition	Max	Min	Condition	Max	Min	Тур	Max	Min	Тур	Max
PCML	Trar	nsmitte	er, receiv transmi	ver, and itter, rec	input referer ceiver, and re	nce cloo eference	ck pins e clock	of the high-s I/O pin speci	peed tra fications	nsceiver , refer to	rs use o Table	the PC e 23 on	ML I/O s page 18	standard 3.	. For
2.5 V	2 375	25	2 625	100	V _{CM} =	_	0.05	D _{MAX} ≤ 700 Mbps	1.8	0.247	_	0.6	1.125	1.25	1.375
LVDS ⁽¹⁾	2.575	2.0	2.025	100	1.25 V	_	1.05	D _{MAX} > 700 Mbps	1.55	0.247	_	0.6	1.125	1.25	1.375
BLVDS (5)	2.375	2.5	2.625	100	_	—	_	_	_	_	_	—	_	—	
RSDS (HIO) ⁽²⁾	2.375	2.5	2.625	100	V _{CM} = 1.25 V	_	0.3	_	1.4	0.1	0.2	0.6	0.5	1.2	1.4
Mini- LVDS (HIO) ⁽³⁾	2.375	2.5	2.625	200	_	600	0.4	_	1.325	0.25	_	0.6	1	1.2	1.4
LVPECL (4	_	_	_	300	_		0.6	D _{MAX} ≤ 700 Mbps	1.8		_	_	_	_	_
), (9)				300			1	D _{MAX} > 700 Mbps	1.6						

Notes to Table 22:

(1) For optimized LVDS receiver performance, the receiver voltage input range must be between 1.0 V to 1.6 V for data rates above 700 Mbps, and 0 V to 1.85 V for data rates below 700 Mbps.

(2) For optimized RSDS receiver performance, the receiver voltage input range must be between 0.25 V to 1.45 V.

(3) For optimized Mini-LVDS receiver performance, the receiver voltage input range must be between 0.3 V to 1.425 V.

- (4) For optimized LVPECL receiver performance, the receiver voltage input range must be between 0.85 V to 1.75 V for data rate above 700 Mbps and 0.45 V to 1.95 V for data rate below 700 Mbps.
- (5) There are no fixed V_{ICM} , V_{OD} , and V_{OCM} specifications for BLVDS. They depend on the system topology.
- (6) RL range: $90 \le RL \le 110 \Omega$.
- (7) The 1.4-V and 1.5-V PCML transceiver I/O standard specifications are described in "Transceiver Performance Specifications" on page 18.
- (8) The minimum VID value is applicable over the entire common mode range, VCM.
- (9) LVPECL is only supported on dedicated clock input pins.
- (10) Differential inputs are powered by VCCPD which requires 2.5 V.

Power Consumption

Altera offers two ways to estimate power consumption for a design—the Excel-based Early Power Estimator and the Quartus[®] II PowerPlay Power Analyzer feature.

- You typically use the interactive Excel-based Early Power Estimator before designing the FPGA to get a magnitude estimate of the device power. The Quartus II PowerPlay Power Analyzer provides better quality estimates based on the specifics of the design after you complete place-and-route. The PowerPlay Power Analyzer can apply a combination of user-entered, simulation-derived, and estimated signal activities that, when combined with detailed circuit models, yields very accurate power estimates.
- ***** For more information about power estimation tools, refer to the *PowerPlay Early Power Estimator User Guide* and the *PowerPlay Power Analysis* chapter in the *Quartus II Handbook*.

Symbol/	Conditions	Tra	nsceive Grade	r Speed 1	Trai	nsceive Grade	r Speed 2	Transceiver Speed Grade 3			Unit
Description		Min	Тур	Max	Min	Тур	Max	Min	Тур	Max	
Spread-spectrum downspread	PCIe	_	0 to 0.5	_	_	0 to 0.5	_	_	0 to 0.5	_	%
On-chip termination resistors ⁽²¹⁾	_	_	100		_	100		_	100		Ω
Absolute V _{MAX} ⁽⁵⁾	Dedicated reference clock pin	_	_	1.6	_	_	1.6	_	_	1.6	V
	RX reference clock pin	_		1.2		_	1.2			1.2	
Absolute V _{MIN}	—	-0.4	-	_	-0.4	_		-0.4	—		V
Peak-to-peak differential input voltage	_	200	_	1600	200	_	1600	200		1600	mV
V _{ICM} (AC	Dedicated reference clock pin	1050/	(1000/90	00/850 ⁽²⁾	1050/	1000/9	00/850 ⁽²⁾	1050/	1000/9	00/850 ⁽²⁾	mV
coupled) (9	RX reference clock pin	1.0/0.9/0.85 ⁽⁴⁾			1.	.0/0.9/0	.85 (4)	1.	.0/0.9/0	.85 ⁽⁴⁾	V
V _{ICM} (DC coupled)	HCSL I/O standard for PCIe reference clock	250		550	250		550	250	_	550	mV
	100 Hz	—	—	-70	—	—	-70	—	—	-70	dBc/Hz
Transmitter	1 kHz	—	—	-90	—	—	-90	—	—	-90	dBc/Hz
REFCLK Phase	10 kHz	—	—	-100	—	—	-100	—	—	-100	dBc/Hz
(622 MHz) ⁽²⁰⁾	100 kHz	—	—	-110	—	—	-110	—	—	-110	dBc/Hz
	≥1 MHz	—	—	-120		—	-120	—	—	-120	dBc/Hz
Transmitter REFCLK Phase Jitter (100 MHz) ⁽¹⁷⁾	10 kHz to 1.5 MHz (PCIe)	_	_	3	_	_	3	_	_	3	ps (rms)
R _{REF} (19)	_	_	1800 ±1%	_	_	1800 ±1%	_	_	180 0 ±1%	_	Ω
Transceiver Clock	s										
fixedclk clock frequency	PCIe Receiver Detect		100 or 125			100 or 125		_	100 or 125		MHz

Table 23. Transceiver Specifications for Stratix V GX and GS Devices ⁽¹⁾ (Part 2 of 7)

Table 23. Transceiver Specifications for Stratix V GX and GS Devices ⁽¹⁾ (Part 6 of 7)

Symbol/	Conditions	Trai	nsceive Grade	r Speed 1	Trar	isceive Grade	r Speed 2	Tran	isceive Grade	er Speed e 3	Unit
Description		Min	Тур	Max	Min	Тур	Max	Min	Тур	Max	
Inter-transceiver block transmitter channel-to- channel skew	xN PMA bonded mode	_	_	500	_	_	500	_	_	500	ps
CMU PLL	•										
Supported Data Range	_	600	_	12500	600	_	12500	600	_	8500/ 10312.5 (24)	Mbps
t _{pll_powerdown} ⁽¹⁵⁾	—	1			1			1			μs
t _{pll_lock} ⁽¹⁶⁾		—		10	—	_	10	—	_	10	μs
ATX PLL											
	VCO post-divider L=2	8000	_	14100	8000	_	12500	8000	_	8500/ 10312.5 (24)	Mbps
Supported Data	L=4	4000	_	7050	4000	_	6600	4000	—	6600	Mbps
Rate Range	L=8	2000		3525	2000		3300	2000		3300	Mbps
	L=8, Local/Central Clock Divider =2	1000	_	1762.5	1000	_	1762.5	1000	_	1762.5	Mbps
t _{pll_powerdown} (15)	—	1	_	—	1	_	—	1	_	—	μs
t _{pll_lock} (16)	—		—	10		—	10	—		10	μs
fPLL	•									•	
Supported Data Range	_	600	_	3250/ 3125 ⁽²⁵⁾	600	_	3250/ 3125 ⁽²⁵⁾	600	_	3250/ 3125 ⁽²⁵⁾	Mbps
t _{pll_powerdown} ⁽¹⁵⁾	_	1	—		1	—		1			μs

Symbol/ Description	Conditions	Transceiver Speed Grade 1			Transceiver Speed Grade 2			Transceiver Speed Grade 3			Unit
		Min	Тур	Max	Min	Тур	Max	Min	Тур	Max	
t _{pll_lock} (16)	_			10			10		_	10	μs

Table 23. Transceiver Specifications for Stratix V GX and GS Devices ⁽¹⁾ (Part 7 of 7)

Notes to Table 23:

(2) The reference clock common mode voltage is equal to the V_{CCR_GXB} power supply level.

(3) This supply must be connected to 1.0 V if the transceiver is configured at a data rate > 6.5 Gbps, and to 1.05 V if configured at a data rate > 10.3 Gbps when DFE is used. For data rates up to 6.5 Gbps, you can connect this supply to 0.85 V.

- (4) This supply follows VCCR_GXB.
- (5) The device cannot tolerate prolonged operation at this absolute maximum.
- (6) The differential eye opening specification at the receiver input pins assumes that **Receiver Equalization** is disabled. If you enable **Receiver Equalization**, the receiver circuitry can tolerate a lower minimum eye opening, depending on the equalization level.
- (7) The Quartus II software automatically selects the appropriate slew rate depending on the configured data rate or functional mode.
- (8) The input reference clock frequency options depend on the data rate and the device speed grade.
- (9) The line data rate may be limited by PCS-FPGA interface speed grade.
- (10) Refer to Figure 1 for the GX channel AC gain curves. The total effective AC gain is the AC gain minus the DC gain.
- (11) t_{LTR} is the time required for the receive CDR to lock to the input reference clock frequency after coming out of reset.
- (12) t_{LTD} is time required for the receiver CDR to start recovering valid data after the rx_is_lockedtodata signal goes high.
- (13) t_{LTD_manual} is the time required for the receiver CDR to start recovering valid data after the rx_is_lockedtodata signal goes high when the CDR is functioning in the manual mode.
- (14) $t_{LTR_LTD_manual}$ is the time the receiver CDR must be kept in lock to reference (LTR) mode after the rx_is_lockedtoref signal goes high when the CDR is functioning in the manual mode.
- (15) $t_{pll_powerdown}$ is the PLL powerdown minimum pulse width.
- (16) t_{pll lock} is the time required for the transmitter CMU/ATX PLL to lock to the input reference clock frequency after coming out of reset.
- (17) To calculate the REFCLK rms phase jitter requirement for PCIe at reference clock frequencies other than 100 MHz, use the following formula: REFCLK rms phase jitter at f(MHz) = REFCLK rms phase jitter at 100 MHz × 100/f.
- (18) The maximum peak to peak differential input voltage V_{ID} after device configuration is equal to 4 × (absolute V_{MAX} for receiver pin V_{ICM}).
- (19) For ES devices, R_{BEF} is 2000 $\Omega \pm 1\%$.
- (20) To calculate the REFCLK phase noise requirement at frequencies other than 622 MHz, use the following formula: REFCLK phase noise at f(MHz) = REFCLK phase noise at 622 MHz + 20*log(f/622).
- (21) SFP/+ optical modules require the host interface to have RD+/- differentially terminated with 100 Ω. The internal OCT feature is available after the Stratix V FPGA configuration is completed. Altera recommends that FPGA configuration is completed before inserting the optical module. Otherwise, minimize unnecessary removal and insertion with unconfigured devices.
- (22) Refer to Figure 2.
- (23) For oversampling designs to support data rates less than the minimum specification, the CDR needs to be in LTR mode only.
- (24) I3YY devices can achieve data rates up to 10.3125 Gbps.
- (25) When you use fPLL as a TXPLL of the transceiver.
- (26) REFCLK performance requires to meet transmitter REFCLK phase noise specification.
- (27) Minimum eye opening of 85 mV is only for the unstressed input eye condition.

⁽¹⁾ Speed grades shown in Table 23 refer to the PMA Speed Grade in the device ordering code. The maximum data rate could be restricted by the Core/PCS speed grade. Contact your Altera Sales Representative for the maximum data rate specifications in each speed grade combination offered. For more information about device ordering codes, refer to the Stratix V Device Overview.

Mada (2)	Transceiver	PMA Width	20	20	16	16	10	10	8	8
	Speed Grade	PCS/Core Width	40	20	32	16	20	10	16	8
	1	C1, C2, C2L, I2, I2L core speed grade	12.2	11.4	9.76	9.12	6.5	5.8	5.2	4.72
	ŋ	C1, C2, C2L, I2, I2L core speed grade	12.2	11.4	9.76	9.12	6.5	5.8	5.2	4.72
	۷	C3, I3, I3L core speed grade	9.8	9.0	7.84	7.2	5.3	4.7	4.24	3.76
FIFO		C1, C2, C2L, I2, I2L core speed grade	8.5	8.5	8.5	8.5	6.5	5.8	5.2	4.72
	3	I3YY core speed grade	10.3125	10.3125	7.84	7.2	5.3	4.7	4.24	3.76
	0	C3, I3, I3L core speed grade	8.5	8.5	7.84	7.2	5.3	4.7	4.24	3.76
		C4, I4 core speed grade	8.5	8.2	7.04	6.56	4.8	4.2	3.84	3.44
	1	C1, C2, C2L, I2, I2L core speed grade	12.2	11.4	9.76	9.12	6.1	5.7	4.88	4.56
	ŋ	C1, C2, C2L, I2, I2L core speed grade	12.2	11.4	9.76	9.12	6.1	5.7	4.88	4.56
	۷	C3, I3, I3L core speed grade	9.8	9.0	7.92	7.2	4.9	4.5	3.96	3.6
Register		C1, C2, C2L, I2, I2L core speed grade	10.3125	10.3125	10.3125	10.3125	6.1	5.7	4.88	4.56
	3	I3YY core speed grade	10.3125	10.3125	7.92	7.2	4.9	4.5	3.96	3.6
	J	C3, I3, I3L core speed grade	8.5	8.5	7.92	7.2	4.9	4.5	3.96	3.6
		C4, I4 core speed grade	8.5	8.2	7.04	6.56	4.4	4.1	3.52	3.28

Table 25 shows the approximate maximum data rate using the standard PCS.

Table 25. Stratix V Standard PCS Approximate Maximum Date Rate (1), (3)

Notes to Table 25:

(1) The maximum data rate is in Gbps.

(2) The Phase Compensation FIFO can be configured in FIFO mode or register mode. In the FIFO mode, the pointers are not fixed, and the latency can vary. In the register mode the pointers are fixed for low latency.

(3) The maximum data rate is also constrained by the transceiver speed grade. Refer to Table 1 for the transceiver speed grade.

Table 27 shows the V_{OD} settings for the GX channel.

Symbol	V _{op} Setting	V _{od} Value (mV)	V _{op} Setting	V _{op} Value (mV)
	0 (1)	0	32	640
	1 (1)	20	33	660
	2 (1)	40	34	680
	3 (1)	60	35	700
	4 (1)	80	36	720
	5 ⁽¹⁾	100	37	740
	6	120	38	760
	7	140	39	780
	8	160	40	800
	9	180	41	820
	10	200	42	840
	11	220	43	860
	12	240	44	880
	13	260	45	900
	14	280	46	920
V_{0D} differential peak to peak	15	300	47	940
typical ⁽³⁾	16	320	48	960
	17	340	49	980
	18	360	50	1000
	19	380	51	1020
	20	400	52	1040
	21	420	53	1060
	22	440	54	1080
	23	460	55	1100
	24	480	56	1120
	25	500	57	1140
	26	520	58	1160
	27	540	59	1180
	28	560	60	1200
	29	580	61	1220
	30	600	62	1240
	31	620	63	1260

Table 27. Typical V_{0D} Setting for GX Channel, TX Termination = 100 $\Omega^{\left(2\right)}$

Note to Table 27:

(1) If TX termination resistance = 100Ω , this VOD setting is illegal.

(2) The tolerance is +/-20% for all VOD settings except for settings 2 and below.

(3) Refer to Figure 2.

Table 28. Tra	ansceiver Sp	ecifications	for Stratix \	V GT Devices	(Part 5 of 5) (1)
---------------	--------------	--------------	---------------	--------------	-------------------

Symbol/ Description	Conditions	S	Transceivei peed Grade	2	ן Sr	Unit		
		Min	Тур	Max	Min	Тур	Max	
t _{pll_lock} ⁽¹⁴⁾	—	—	—	10	—	—	10	μs

Notes to Table 28:

- (1) Speed grades shown refer to the PMA Speed Grade in the device ordering code. The maximum data rate could be restricted by the Core/PCS speed grade. Contact your Altera Sales Representative for the maximum data rate specifications in each speed grade combination offered. For more information about device ordering codes, refer to the Stratix V Device Overview.
- (2) The reference clock common mode voltage is equal to the VCCR_GXB power supply level.
- (3) The device cannot tolerate prolonged operation at this absolute maximum.
- (4) The differential eye opening specification at the receiver input pins assumes that receiver equalization is disabled. If you enable receiver equalization, the receiver circuitry can tolerate a lower minimum eye opening, depending on the equalization level.
- (5) Refer to Figure 5 for the GT channel AC gain curves. The total effective AC gain is the AC gain minus the DC gain.
- (6) Refer to Figure 6 for the GT channel DC gain curves.
- (7) CFP2 optical modules require the host interface to have the receiver data pins differentially terminated with 100 Ω. The internal OCT feature is available after the Stratix V FPGA configuration is completed. Altera recommends that FPGA configuration is completed before inserting the optical module. Otherwise, minimize unnecessary removal and insertion with unconfigured devices.
- (8) Specifications for this parameter are the same as for Stratix V GX and GS devices. See Table 23 for specifications.
- (9) t_{1 TR} is the time required for the receive CDR to lock to the input reference clock frequency after coming out of reset.
- (10) t_{LTD} is time required for the receiver CDR to start recovering valid data after the rx is lockedtodata signal goes high.
- (11) t_{LTD_manual} is the time required for the receiver CDR to start recovering valid data after the rx_is_lockedtodata signal goes high when the CDR is functioning in the manual mode.
- (12) t_{LTR_LTD_manual} is the time the receiver CDR must be kept in lock to reference (LTR) mode after the rx_is_lockedtoref signal goes high when the CDR is functioning in the manual mode.
- (13) tpll_powerdown is the PLL powerdown minimum pulse width.
- (14) tpll lock is the time required for the transmitter CMU/ATX PLL to lock to the input reference clock frequency after coming out of reset.
- (15) To calculate the REFCLK rms phase jitter requirement for PCle at reference clock frequencies other than 100 MHz, use the following formula: REFCLK rms phase jitter at f(MHz) = REFCLK rms phase jitter at 100 MHz × 100/f.
- (16) The maximum peak to peak differential input voltage V_{ID} after device configuration is equal to 4 × (absolute V_{MAX} for receiver pin V_{ICM}).
- (17) For ES devices, RREF is 2000 $\Omega \pm 1\%$.
- (18) To calculate the REFCLK phase noise requirement at frequencies other than 622 MHz, use the following formula: REFCLK phase noise at f(MHz) = REFCLK phase noise at 622 MHz + 20*log(f/622).
- (19) SFP/+ optical modules require the host interface to have RD+/- differentially terminated with 100 Ω. The internal OCT feature is available after the Stratix V FPGA configuration is completed. Altera recommends that FPGA configuration is completed before inserting the optical module. Otherwise, minimize unnecessary removal and insertion with unconfigured devices.
- (20) Refer to Figure 4.
- (21) For oversampling design to support data rates less than the minimum specification, the CDR needs to be in LTR mode only.
- (22) This supply follows VCCR_GXB for both GX and GT channels.
- (23) When you use fPLL as a TXPLL of the transceiver.

- XFI
- ASI
- HiGig/HiGig+
- HiGig2/HiGig2+
- Serial Data Converter (SDC)
- GPON
- SDI
- SONET
- Fibre Channel (FC)
- PCIe
- QPI
- SFF-8431

Download the Stratix V Characterization Report Tool to view the characterization report summary for these protocols.

Core Performance Specifications

This section describes the clock tree, phase-locked loop (PLL), digital signal processing (DSP), memory blocks, configuration, and JTAG specifications.

Clock Tree Specifications

Table 30 lists the clock tree specifications for Stratix V devices.

Table 30. Clock Tree Performance for Stratix V Devices (1)

		Performance		
Symbol	C1, C2, C2L, I2, and I2L	C3, I3, I3L, and I3YY	C4, I4	Unit
Global and Regional Clock	717	650	580	MHz
Periphery Clock	550	500	500	MHz

Note to Table 30:

(1) The Stratix V ES devices are limited to 600 MHz core clock tree performance.

PLL Specifications

Table 31 lists the Stratix V PLL specifications when operating in both the commercial junction temperature range (0° to 85° C) and the industrial junction temperature range (-40° to 100° C).

Table 31. PLL Specifications for Stratix V Devices (Part 1 of 3)

Symbol	Parameter	Min	Тур	Max	Unit
	Input clock frequency (C1, C2, C2L, I2, and I2L speed grades)	5		800 (1)	MHz
f _{IN}	Input clock frequency (C3, I3, I3L, and I3YY speed grades)	5		800 (1)	MHz
	Input clock frequency (C4, I4 speed grades)	5	—	650 ⁽¹⁾	MHz
f _{INPFD}	Input frequency to the PFD	5	—	325	MHz
f _{FINPFD}	Fractional Input clock frequency to the PFD	50	—	160	MHz
	PLL VCO operating range (C1, C2, C2L, I2, I2L speed grades)	600	_	1600	MHz
f _{VCO} (9)	PLL VCO operating range (C3, I3, I3L, I3YY speed grades)	600		1600	MHz
	PLL VCO operating range (C4, I4 speed grades)	600	—	1300	MHz
t _{einduty}	Input clock or external feedback clock input duty cycle	40	—	60	%
	Output frequency for an internal global or regional clock (C1, C2, C2L, I2, I2L speed grades)	_	_	717 ⁽²⁾	MHz
f _{OUT}	Output frequency for an internal global or regional clock (C3, I3, I3L speed grades)			650 ⁽²⁾	MHz
	Output frequency for an internal global or regional clock (C4, I4 speed grades)			580 ⁽²⁾	Max Unit 800 (1) MHz 800 (1) MHz 650 (1) MHz 325 MHz 160 MHz 160 MHz 160 MHz 160 MHz 1600 MHz 1600 MHz 1600 MHz 1600 MHz 1600 MHz 1600 MHz 600 % 717 (2) MHz 650 (2) MHz 667 (2) MHz 667 (2) MHz 553 (2) MHz 553 (2) MHz 10 ns 100 MHz 11 ms 11 ms 11 ms 11 ms 12 MHz 1300 MHz 14 ms 15 MHz <tr tr=""> 10 ms</tr>
	Output frequency for an external clock output (C1, C2, C2L, I2, I2L speed grades)			800 ⁽²⁾	MHz
f _{OUT_EXT}	Output frequency for an external clock output (C3, I3, I3L speed grades)			667 ⁽²⁾	MHz
	Output frequency for an external clock output (C4, I4 speed grades)			553 ⁽²⁾	MHz
t _{outduty}	Duty cycle for a dedicated external clock output (when set to 50%)	45	50	55	%
t _{FCOMP}	External feedback clock compensation time	_		10	ns
f _{dyconfigclk}	Dynamic Configuration Clock used for mgmt_clk and scanclk		_	100	MHz
t _{LOCK}	Time required to lock from the end-of-device configuration or deassertion of areset			1	ms
t _{DLOCK}	Time required to lock dynamically (after switchover or reconfiguring any non-post-scale counters/delays)			1	ms
	PLL closed-loop low bandwidth	—	0.3	—	MHz
f _{CLBW}	PLL closed-loop medium bandwidth	—	1.5	—	MHz
	PLL closed-loop high bandwidth (7)	—	4	-	MHz
t _{PLL_PSERR}	Accuracy of PLL phase shift	—	—	±50	ps
t _{ARESET}	Minimum pulse width on the areset signal	10	—	_	ns

Mode	C1	C2, C2L	12, 12L	C3	13, 13L, 13YY	C4	14	Unit		
Modes using Three DSPs										
One complex 18 x 25	425	425	415	340	340	275	265	MHz		
Modes using Four DSPs										
One complex 27 x 27	465	465	465	380	380	300	290	MHz		

Table 32. Block Performance Specifications for Stratix V DSP Devices (Part 2 of 2)

Memory Block Specifications

Table 33 lists the Stratix V memory block specifications.

Table 33. Memory Block Performance Specifications for Stratix V Devices ^{(1), (2)} (Part 1 of 2)

Memory		Resour	ces Used			Pe	erforman	ce			
	Mode	ALUTS	Memory	C1	C2, C2L	C3	C4	12, 12L	13, 13L, 13YY	14	Unit
MLAB	Single port, all supported widths	0	1	450	450	400	315	450	400	315	MHz
	Simple dual-port, x32/x64 depth	0	1	450	450	400	315	450	400	315	MHz
	Simple dual-port, x16 depth ⁽³⁾	0	1	675	675	533	400	675	533	400	MHz
	ROM, all supported widths	0	1	600	600	500	450	600	500	450	MHz

Periphery Performance

This section describes periphery performance, including high-speed I/O and external memory interface.

I/O performance supports several system interfaces, such as the **LVDS** high-speed I/O interface, external memory interface, and the **PCI/PCI-X** bus interface. General-purpose I/O standards such as 3.3-, 2.5-, 1.8-, and 1.5-**LVTTL/LVCMOS** are capable of a typical 167 MHz and 1.2-**LVCMOS** at 100 MHz interfacing frequency with a 10 pF load.

The actual achievable frequency depends on design- and system-specific factors. Ensure proper timing closure in your design and perform HSPICE/IBIS simulations based on your specific design and system setup to determine the maximum achievable frequency in your system.

High-Speed I/O Specification

Table 36 lists high-speed I/O timing for Stratix V devices.

Table 36. High-Speed I/O Specifications for Stratix V Devices (1), (2) (Part 1 of 4)

Sumbol	Conditions	C1		C2, C2L, I2, I2L		C3, I3, I3L, I3YY			C4,14			11		
Symbol	Conditions	Min	Тур	Max	Min	Тур	Max	Min	Тур	Max	Min	Тур	Max	UNIT
f _{HSCLK_in} (input clock frequency) True Differential I/O Standards	Clock boost factor W = 1 to 40 $^{(4)}$	5	_	800	5		800	5		625	5		525	MHz
f _{HSCLK_in} (input clock frequency) Single Ended I/O Standards ⁽³⁾	Clock boost factor W = 1 to 40 $^{(4)}$	5		800	5		800	5		625	5		525	MHz
f _{HSCLK_in} (input clock frequency) Single Ended I/O Standards	Clock boost factor W = 1 to 40 $^{(4)}$	5	_	520	5		520	5	_	420	5	_	420	MHz
f _{HSCLK_OUT} (output clock frequency)	_	5	_	800	5	_	800	5	_	625 (5)	5	_	525 (5)	MHz

Figure 7 shows the dynamic phase alignment (DPA) lock time specifications with the DPA PLL calibration option enabled.

Figure 7. DPA Lock Time Specification with DPA PLL Calibration Enabled

rx_reset			
rx_dpa_locked			<u> </u>
···			-

Table 37 lists the DPA lock time specifications for Stratix V devices.

Table 37. DPA Lock Time Specifications for Stratix V GX Devices Only (1), (2), (3)

Standard	Training Pattern	Number of Data Transitions in One Repetition of the Training Pattern	Number of Repetitions per 256 Data Transitions ⁽⁴⁾	Maximum
SPI-4	000000000111111111 2		128	640 data transitions
Parallel Rapid I/O	00001111	2	128	640 data transitions
	10010000	4	64	640 data transitions
Missellanaous	10101010	8	32	640 data transitions
Wiscenareous	01010101	8	32	640 data transitions

Notes to Table 37:

(1) The DPA lock time is for one channel.

(2) One data transition is defined as a 0-to-1 or 1-to-0 transition.

(3) The DPA lock time stated in this table applies to both commercial and industrial grade.

(4) This is the number of repetitions for the stated training pattern to achieve the 256 data transitions.

Figure 8 shows the **LVDS** soft-clock data recovery (CDR)/DPA sinusoidal jitter tolerance specification for a data rate \geq 1.25 Gbps. Table 38 lists the **LVDS** soft-CDR/DPA sinusoidal jitter tolerance specification for a data rate \geq 1.25 Gbps.





Family	Device	Package	Configuration .rbf Size (bits)	IOCSR .rbf Size (bits) ^{(4), (5)}		
Stratix V E ⁽¹⁾	5SEE9	—	342,742,976	700,888		
	5SEEB	—	342,742,976	700,888		

Table 47. Uncompressed .rbf Sizes for Stratix V Devices

Notes to Table 47:

(1) Stratix V E devices do not have PCI Express® (PCIe®) hard IP. Stratix V E devices do not support the CvP configuration scheme.

(2) 36-transceiver devices.

(3) 24-transceiver devices.

(4) File size for the periphery image.

(5) The IOCSR .rbf size is specifically for the CvP feature.

Use the data in Table 47 to estimate the file size before design compilation. Different configuration file formats, such as a hexadecimal (.hex) or tabular text file (.ttf) format, have different file sizes. For the different types of configuration file and file sizes, refer to the Quartus II software. However, for a specific version of the Quartus II software, any design targeted for the same device has the same uncompressed configuration file size. If you are using compression, the file size can vary after each compilation because the compression ratio depends on your design.

• For more information about setting device configuration options, refer to *Configuration, Design Security, and Remote System Upgrades in Stratix V Devices.* For creating configuration files, refer to the *Quartus II Help.*

Table 48 lists the minimum configuration time estimates for Stratix V devices.

Table 48. Minimum Configuration Time Estimation for Stratix V Devi
--

Variant GX	Mombor		Active Serial (1))	Fast Passive Parallel ⁽²⁾				
	Code	Width	DCLK (MHz)	Min Config Time (s)	Width	DCLK (MHz)	Min Config Time (s)		
	٨٥	4	100	0.534	32	100	0.067		
	AJ	4	100	0.344	32	100	0.043		
	A4	4	100	0.534	32	100	0.067		
	A5	4	100	0.675	32	100	0.084		
	A7	4	100	0.675	32	100	0.084		
GX	A9	4	100	0.857	32	100	0.107		
	AB	4	100	0.857	32	100	0.107		
	B5	4	100	0.676	32	100	0.085		
	B6	4	100	0.676	32	100	0.085		
	B9	4	100	0.857	32	100	0.107		
	BB	4	100	0.857	32	100	0.107		
ст	C5	4	100	0.675	32	100	0.084		
ul	C7	4	100	0.675	32	32 100 0. 32 100 0. 32 100 0. 32 100 0. 32 100 0. 32 100 0. 32 100 0. 32 100 0. 32 100 0. 32 100 0. 32 100 0. 32 100 0. 32 100 0.	0.084		

Paramotor	Available Settings	Available	Available	Available	Available	Available	Available Min		Fast	Model	Slow Model							
(1)		s Offset	Industrial	Commercial	C1	C2	C3	C4	12	13, 13YY	14	Unit						
D3	8	0	1.587	1.699	2.793	2.793	2.992	3.192	2.811	3.047	3.257	ns						
D4	64	0	0.464	0.492	0.838	0.838	0.924	1.011	0.843	0.920	1.006	ns						
D5	64	0	0.464	0.493	0.838	0.838	0.924	1.011	0.844	0.921	1.006	ns						
D6	32	0	0.229	0.244	0.415	0.415	0.458	0.503	0.418	0.456	0.499	ns						

Table 58.	IOE Pro	grammable De	lay for	Stratix V	V Devices	(Part 2 of 2)
-----------	---------	--------------	---------	-----------	-----------	--------------	---

Notes to Table 58:

(1) You can set this value in the Quartus II software by selecting D1, D2, D3, D5, and D6 in the Assignment Name column of Assignment Editor.

(2) Minimum offset does not include the intrinsic delay.

Programmable Output Buffer Delay

Table 59 lists the delay chain settings that control the rising and falling edge delays of the output buffer. The default delay is 0 ps.

Symbol	Parameter	Typical	Unit
	Rising and/or falling edge delay	0 (default)	ps
Dauman		25	ps
DOUTBUF		50	ps
		75	ps

Note to Table 59:

(1) You can set the programmable output buffer delay in the Quartus II software by setting the Output Buffer Delay Control assignment to either positive, negative, or both edges, with the specific values stated here (in ps) for the Output Buffer Delay assignment.

Glossary

Table 60 lists the glossary for this chapter.

Table 60. Glossary (Part 1 of 4)

Letter	Subject	Definitions	
Α			
В	—	—	
С			
D	—	_	
E	—	—	
F	f _{HSCLK}	Left and right PLL input clock frequency.	
	f _{HSDR}	High-speed I/O block—Maximum and minimum LVDS data transfer rate (f _{HSDR} = 1/TUI), non-DPA.	
	f _{hsdrdpa}	High-speed I/O block—Maximum and minimum LVDS data transfer rate (f _{HSDRDPA} = 1/TUI), DPA.	

Document Revision History

Table 61 lists the revision history for this chapter.

 Table 61. Document Revision History (Part 1 of 3)

Date	Version	Changes	
June 2018	3.9	 Added the "Stratix V Device Overshoot Duration" figure. 	
April 2017	3.8	Added a footnote to the "High-Speed I/O Specifications for Stratix V Devices" table.	
		 Changed the minimum value for t_{CD2UMC} in the "PS Timing Parameters for Stratix V Devices" table. 	
		 Changed the condition for 100-Ω R_D in the "OCT Without Calibration Resistance Tolerance Specifications for Stratix V Devices" table. 	
		 Changed the minimum value for t_{CD2UMC} in the "AS Timing Parameters for AS '1 and AS '4 Configurations in Stratix V Devices" table 	
		 Changed the minimum value for t_{CD2UMC} in the "FPP Timing Parameters for Stratix V Devices When the DCLK-to-DATA[] Ratio is >1" table. 	
		 Changed the minimum value for t_{CD2UMC} in the "FPP Timing Parameters for Stratix V Devices When the DCLK-to-DATA[] Ratio is >1" table. 	
		 Changed the minimum number of clock cycles value in the "Initialization Clock Source Option and the Maximum Frequency" table. 	
June 2016	3.7	 Added the V_{ID} minimum specification for LVPECL in the "Differential I/O Standard Specifications for Stratix V Devices" table 	
		 Added the I_{OUT} specification to the "Absolute Maximum Ratings for Stratix V Devices" table. 	
December 2015	3.6	Added a footnote to the "High-Speed I/O Specifications for Stratix V Devices" table.	
December 2015	3.5	 Changed the transmitter, receiver, and ATX PLL data rate specifications in the "Transceiver Specifications for Stratix V GX and GS Devices" table. 	
		 Changed the configuration .rbf sizes in the "Uncompressed .rbf Sizes for Stratix V Devices" table. 	
	3.4	• Changed the data rate specification for transceiver speed grade 3 in the following tables:	
July 2015		 "Transceiver Specifications for Stratix V GX and GS Devices" 	
		 "Stratix V Standard PCS Approximate Maximum Date Rate" 	
		 "Stratix V 10G PCS Approximate Maximum Data Rate" 	
		 Changed the conditions for reference clock rise and fall time, and added a note to the "Transceiver Specifications for Stratix V GX and GS Devices" table. 	
		 Added a note to the "Minimum differential eye opening at receiver serial input pins" specification in the "Transceiver Specifications for Stratix V GX and GS Devices" table. 	
		 Changed the t_{c0} maximum value in the "AS Timing Parameters for AS '1 and AS '4 Configurations in Stratix V Devices" table. 	
		 Removed the CDR ppm tolerance specification from the "Transceiver Specifications for Stratix V GX and GS Devices" table. 	