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Intel - 5SGXEA4K2F35I2LN Datasheet



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Understanding <u>Embedded - FPGAs (Field</u> <u>Programmable Gate Array)</u>

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Obsolete
Number of LABs/CLBs	158500
Number of Logic Elements/Cells	420000
Total RAM Bits	37888000
Number of I/O	432
Number of Gates	-
Voltage - Supply	0.82V ~ 0.88V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	1152-BBGA, FCBGA
Supplier Device Package	1152-FBGA (35x35)
Purchase URL	https://www.e-xfl.com/product-detail/intel/5sgxea4k2f35i2ln

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			Resistance Tolerance						
Symbol	Description	Conditions	C1	C2,I2	C3, I3, I3YY	C4, I4	Unit		
50-Ω R _S	Internal series termination without calibration (50- Ω setting)	$V_{CCIO} = 1.8$ and 1.5 V	±30	±30	±40	±40	%		
50-Ω R _S	Internal series termination without calibration (50- Ω setting)	V _{CCI0} = 1.2 V	±35	±35	±50	±50	%		
100-Ω R _D	Internal differential termination (100- Ω setting)	V _{CCPD} = 2.5 V	±25	±25	±25	±25	%		

Table 12. OCT Without Calibration Resistance Tolerance Specifications for Stratix V Devices (Part 2 of 2)

Calibration accuracy for the calibrated series and parallel OCTs are applicable at the moment of calibration. When voltage and temperature conditions change after calibration, the tolerance may change.

OCT calibration is automatically performed at power-up for OCT-enabled I/Os. Table 13 lists the OCT variation with temperature and voltage after power-up calibration. Use Table 13 to determine the OCT variation after power-up calibration and Equation 1 to determine the OCT variation without recalibration.

Equation 1. OCT Variation Without Recalibration for Stratix V Devices (1), (2), (3), (4), (5), (6)

$$R_{OCT} \,=\, R_{SCAL} \Big(1 + \langle \frac{dR}{dT} \times \Delta T \rangle \pm \langle \frac{dR}{dV} \times \Delta V \rangle \Big) \label{eq:ROCT}$$

Notes to Equation 1:

- (1) The R_{OCT} value shows the range of OCT resistance with the variation of temperature and V_{CCIO} .
- (2) R_{SCAL} is the OCT resistance value at power-up.
- (3) ΔT is the variation of temperature with respect to the temperature at power-up.
- (4) ΔV is the variation of voltage with respect to the V_{CCIO} at power-up.
- (5) dR/dT is the percentage change of R_{SCAL} with temperature.
- (6) dR/dV is the percentage change of $\mathsf{R}_{\mathsf{SCAL}}$ with voltage.

Table 13 lists the on-chip termination variation after power-up calibration.

Table 13. OCT Variation after Power-Up Calibration for Stratix V Devices (Part 1 of 2)
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Symbol	Description	V _{CCIO} (V)	Typical	Unit
dR/dV		3.0	0.0297	
	OCT variation with voltage without	2.5	0.0344	
		1.8	0.0499	%/mV
		1.5	0.0744	
		1.2	0.1241	

Internal Weak Pull-Up Resistor

Table 16 lists the weak pull-up resistor values for Stratix V devices.

Symbol	Description	V _{CCIO} Conditions (V) ⁽³⁾	Value ⁽⁴⁾	Unit
		3.0 ±5%	25	kΩ
		2.5 ±5%	25	kΩ
	Value of the I/O pin pull-up resistor before	1.8 ±5%	25	kΩ
R _{PU}	and during configuration, as well as user mode if you enable the programmable	1.5 ±5%	25	kΩ
	pull-up resistor option.	1.35 ±5%	25	kΩ
		1.25 ±5%	25	kΩ
		1.2 ±5%	25	kΩ

Table 16. Internal Weak Pull-Up Resistor for Stratix V Devices (1), (2)

Notes to Table 16:

(1) All I/O pins have an option to enable the weak pull-up resistor except the configuration, test, and JTAG pins.

(2) The internal weak pull-down feature is only available for the JTAG TCK pin. The typical value for this internal weak pull-down resistor is approximately 25 k Ω .

- (3) The pin pull-up resistance values may be lower if an external source drives the pin higher than V_{CCIO}.
- (4) These specifications are valid with a $\pm 10\%$ tolerance to cover changes over PVT.

I/O Standard Specifications

Table 17 through Table 22 list the input voltage (V_{IH} and V_{IL}), output voltage (V_{OH} and V_{OL}), and current drive characteristics (I_{OH} and I_{OL}) for various I/O standards supported by Stratix V devices. These tables also show the Stratix V device family I/O standard specifications. The V_{OL} and V_{OH} values are valid at the corresponding I_{OH} and I_{OL}, respectively.

For an explanation of the terms used in Table 17 through Table 22, refer to "Glossary" on page 65. For tolerance calculations across all SSTL and HSTL I/O standards, refer to Altera knowledge base solution rd07262012_486.

I/O		V _{CCIO} (V)			V _{IL} (V)		(V)	V _{OL} (V)	V _{OH} (V)	I _{OL}	I _{oh}
Standard	Min	Тур	Max	Min	Max	Min	Max	Max	Min	(mA)	(mA)
LVTTL	2.85	3	3.15	-0.3	0.8	1.7	3.6	0.4	2.4	2	-2
LVCMOS	2.85	3	3.15	-0.3	0.8	1.7	3.6	0.2	$V_{CCIO} - 0.2$	0.1	-0.1
2.5 V	2.375	2.5	2.625	-0.3	0.7	1.7	3.6	0.4	2	1	-1
1.8 V	1.71	1.8	1.89	-0.3	0.35 * V _{CCIO}	0.65 * V _{CCIO}	V _{CCI0} + 0.3	0.45	V _{CCI0} – 0.45	2	-2
1.5 V	1.425	1.5	1.575	-0.3	0.35 * V _{CCI0}	0.65 * V _{CCI0}	V _{CCI0} + 0.3	0.25 * V _{CCIO}	0.75 * V _{CCIO}	2	-2
1.2 V	1.14	1.2	1.26	-0.3	0.35 * V _{CCI0}	0.65 * V _{CCI0}	V _{CCI0} + 0.3	0.25 * V _{CCIO}	0.75 * V _{CCIO}	2	-2

Table 17. Single-Ended I/O Standards for Stratix V Devices

I/O Standard	V _{IL(DC)} (V)		V _{IH(D}	_{C)} (V)	V _{IL(AC)} (V)	V _{IH(AC)} (V)	V _{ol} (V)	V _{oh} (V)	I (mA)	l _{oh}
i/U Stanuaru	Min Max		Min Max		Max	Min	Max	Max Min		(mA)
HSTL-18 Class I	—	V _{REF} – 0.1	V _{REF} + 0.1	_	$V_{REF} - 0.2$	V _{REF} + 0.2	0.4	V _{CCI0} – 0.4	8	-8
HSTL-18 Class II	_	V _{REF} – 0.1	V _{REF} + 0.1	_	V _{REF} - 0.2	V _{REF} + 0.2	0.4	V _{CCI0} – 0.4	16	-16
HSTL-15 Class I	_	V _{REF} – 0.1	V _{REF} + 0.1	_	V _{REF} - 0.2	V _{REF} + 0.2	0.4	V _{CCI0} – 0.4	8	-8
HSTL-15 Class II	_	V _{REF} – 0.1	V _{REF} + 0.1	_	V _{REF} - 0.2	V _{REF} + 0.2	0.4	V _{CCI0} – 0.4	16	-16
HSTL-12 Class I	-0.15	V _{REF} - 0.08	V _{REF} + 0.08	V _{CCIO} + 0.15	V _{REF} – 0.15	V _{REF} + 0.15	0.25* V _{CCI0}	0.75* V _{CCI0}	8	-8
HSTL-12 Class II	-0.15	V _{REF} - 0.08	V _{REF} + 0.08	V _{CCIO} + 0.15	V _{REF} – 0.15	V _{REF} + 0.15	0.25* V _{CCI0}	0.75* V _{CCI0}	16	-16
HSUL-12	—	V _{REF} - 0.13	V _{REF} + 0.13	_	V _{REF} – 0.22	V _{REF} + 0.22	0.1* V _{CCIO}	0.9* V _{CCI0}	_	

Table 19. Single-Ended SSTL, HSTL, and HSUL I/O Standards Signal Specifications for Stratix V Devices (Part 2 of 2)

Table 20. Differential SSTL I/O Standards for Stratix V Devices

1/0 Standard	V _{CCIO} (V)			V _{SWIN}	_{G(DC)} (V)		V _{X(AC)} (V)		V _{SWING(AC)} (V)		
ijo Stanuaru	Min	Тур	Max	Min	Max	Min	Тур	Max	Min	Max	
SSTL-2 Class I, II	2.375	2.5	2.625	0.3	V _{CCI0} + 0.6	V _{CCI0} /2- 0.2	_	V _{CCI0} /2 + 0.2	0.62	V _{CCI0} + 0.6	
SSTL-18 Class I, II	1.71	1.8	1.89	0.25	V _{CCIO} + 0.6	V _{CCI0} /2- 0.175	_	V _{CCI0} /2 + 0.175	0.5	V _{CCI0} + 0.6	
SSTL-15 Class I, II	1.425	1.5	1.575	0.2	(1)	V _{CCI0} /2- 0.15	_	V _{CCI0} /2 + 0.15	0.35	_	
SSTL-135 Class I, II	1.283	1.35	1.45	0.2	(1)	V _{CCI0} /2- 0.15	V _{CCI0} /2	V _{CCI0} /2 + 0.15	2(V _{IH(AC)} - V _{REF})	2(V _{IL(AC)} - V _{REF})	
SSTL-125 Class I, II	1.19	1.25	1.31	0.18	(1)	V _{CCI0} /2- 0.15	V _{CCI0} /2	V _{CCI0} /2 + 0.15	2(V _{IH(AC)} - V _{REF})	_	
SSTL-12 Class I, II	1.14	1.2	1.26	0.18	_	V _{REF} 0.15	V _{CCI0} /2	V _{REF} + 0.15	-0.30	0.30	

Note to Table 20:

(1) The maximum value for $V_{SWING(DC)}$ is not defined. However, each single-ended signal needs to be within the respective single-ended limits $(V_{IH(DC)} \text{ and } V_{IL(DC)})$.

								•	-				
I/O	V _{CCIO} (V)			V _{DIF(DC)} (V)		V _{X(AC)} (V)				V _{CM(DC)} (V	V _{DIF(AC)} (V)		
Standard	Min	Тур	Max	Min	Max	Min	Тур	Max	Min	Тур	Max	Min	Max
HSTL-18 Class I, II	1.71	1.8	1.89	0.2	_	0.78	_	1.12	0.78	_	1.12	0.4	_
HSTL-15 Class I, II	1.425	1.5	1.575	0.2	_	0.68	_	0.9	0.68		0.9	0.4	_

- You typically use the interactive Excel-based Early Power Estimator before designing the FPGA to get a magnitude estimate of the device power. The Quartus II PowerPlay Power Analyzer provides better quality estimates based on the specifics of the design after you complete place-and-route. The PowerPlay Power Analyzer can apply a combination of user-entered, simulation-derived, and estimated signal activities that, when combined with detailed circuit models, yields very accurate power estimates.
- ***** For more information about power estimation tools, refer to the *PowerPlay Early Power Estimator User Guide* and the *PowerPlay Power Analysis* chapter in the *Quartus II Handbook*.

Symbol/	Conditions	Tra	nsceive Grade	r Speed 1	Tra	Transceiver Speed Grade 2			Transceiver Speed Grade 3			
Description		Min	Тур	Max	Min	Тур	Max	Min	Тур	Max		
	85– Ω setting	_	85 ± 30%		_	85 ± 30%		—	85 ± 30%		Ω	
Differential on-	100–Ω setting	_	100 ± 30%		_	100 ± 30%		_	100 ± 30%	_	Ω	
chip termination resistors ⁽²¹⁾	120–Ω setting	_	120 ± 30%		_	120 ± 30%		_	120 ± 30%	_	Ω	
	150-Ω setting	_	150 ± 30%		_	150 ± 30%	_	_	150 ± 30%	_	Ω	
V _{ICM} (AC and DC	V _{CCR_GXB} = 0.85 V or 0.9 V full bandwidth	_	600	_	_	600	_		600	_	mV	
	V _{CCR_GXB} = 0.85 V or 0.9 V half bandwidth		600	_		600	_		600	_	mV	
(oupled)	V _{CCR_GXB} = 1.0 V/1.05 V full bandwidth	_	700	_	_	700	_	_	700	_	mV	
	V _{CCR_GXB} = 1.0 V half bandwidth		750	_	_	750	_	_	750	_	mV	
t _{LTR} ⁽¹¹⁾	—	_	_	10	_	—	10	_	—	10	μs	
t _{LTD} ⁽¹²⁾	—	4	_		4	—		4	-	—	μs	
t _{LTD_manual} ⁽¹³⁾	—	4			4	—		4	—	—	μs	
t _{LTR_LTD_manual} ⁽¹⁴⁾	—	15	_		15	—		15	—	—	μs	
Run Length		_		200	_	—	200	_	—	200	UI	
Programmable equalization (AC Gain) ⁽¹⁰⁾	Full bandwidth (6.25 GHz) Half bandwidth (3.125 GHz)		_	16	_	_	16	_		16	dB	

 Table 23. Transceiver Specifications for Stratix V GX and GS Devices ⁽¹⁾ (Part 4 of 7)

Table 23. Transceiver Specifications for Stratix V GX and GS Devices ⁽¹⁾ (Part 6 of 7)

Symbol/	Conditions	Trai	nsceive Grade	r Speed 1	Trar	isceive Grade	r Speed 2	Tran	isceive Grade	er Speed e 3	Unit
Description		Min	Тур	Max	Min	Тур	Max	Min	Тур	Max	
Inter-transceiver block transmitter channel-to- channel skew	xN PMA bonded mode	_	_	500	_	_	500	_	_	500	ps
CMU PLL	•										
Supported Data Range	_	600	_	12500	600	_	12500	600	_	8500/ 10312.5 (24)	Mbps
t _{pll_powerdown} ⁽¹⁵⁾	—	1			1			1			μs
t _{pll_lock} ⁽¹⁶⁾		—		10	—	_	10	—	_	10	μs
ATX PLL											
	VCO post-divider L=2	8000	_	14100	8000	_	12500	8000	_	8500/ 10312.5 (24)	Mbps
Supported Data	L=4	4000	_	7050	4000	_	6600	4000	—	6600	Mbps
Rate Range	L=8	2000		3525	2000		3300	2000		3300	Mbps
	L=8, Local/Central Clock Divider =2	1000	_	1762.5	1000	_	1762.5	1000	_	1762.5	Mbps
t _{pll_powerdown} (15)	—	1	_	—	1	_	—	1	_	—	μs
t _{pll_lock} (16)	—		—	10		—	10	—		10	μs
fPLL	•										
Supported Data Range	_	600	_	3250/ 3125 ⁽²⁵⁾	600	_	3250/ 3125 ⁽²⁵⁾	600	_	3250/ 3125 ⁽²⁵⁾	Mbps
t _{pll_powerdown} ⁽¹⁵⁾	_	1	—		1	—		1			μs

Table 24 shows the maximum transmitter data rate for the clock network.

Table 24. Clock Network Maximum Data Rate Transmitter Specifications (1)

		ATX PLL			CMU PLL ⁽²⁾)	fPLL			
Clock Network	Non- bonded Mode (Gbps)	Bonded Mode (Gbps)	Channel Span	Non- bonded Mode (Gbps)	Bonded Mode (Gbps)	Channel Span	Non- bonded Mode (Gbps)	Bonded Mode (Gbps)	Channel Span	
x1 ⁽³⁾	14.1	_	6	12.5	_	6	3.125	—	3	
x6 ⁽³⁾	_	14.1	6	—	12.5	6	—	3.125	6	
x6 PLL Feedback ⁽⁴⁾	_	14.1	Side- wide	_	12.5	Side- wide	_	_	_	
xN (PCIe)	_	8.0	8	—	5.0	8	—	—	—	
VNI (Native DHV ID)	8.0	8.0	Up to 13 channels above and below PLL	7 00	7 00	Up to 13 channels above	3 125	3 125	Up to 13 channels above	
xN (Native PHY IP) -	_	8.01 to 9.8304	Up to 7 channels above and below PLL	7.99	7.99	and below PLL	3.125	0.120	and below PLL	

Notes to Table 24:

(1) Valid data rates below the maximum specified in this table depend on the reference clock frequency and the PLL counter settings. Check the MegaWizard message during the PHY IP instantiation.

(2) ATX PLL is recommended at 8 Gbps and above data rates for improved jitter performance.

(3) Channel span is within a transceiver bank.

(4) Side-wide channel bonding is allowed up to the maximum supported by the PHY IP.





Figure 3 shows the Stratix V AC gain curves for GX channels.

Figure 3. AC Gain Curves for GX Channels (full bandwidth)

Stratix V GT devices contain both GX and GT channels. All transceiver specifications for the GX channels not listed in Table 28 are the same as those listed in Table 23.

Table 28 lists the Stratix V GT transceiver specifications.

Mode	C1	C2, C2L	12, 12L	C3	13, 13L, 13YY	C4	14	Unit
		Modes us	ing Three	DSPs				
One complex 18 x 25	425	425	415	340	340	275	265	MHz
Modes using Four DSPs								
One complex 27 x 27	465	465	465	380	380	300	290	MHz

Table 32. Block Performance Specifications for Stratix V DSP Devices (Part 2 of 2)

Memory Block Specifications

Table 33 lists the Stratix V memory block specifications.

Table 33. Memory Block Performance Specifications for Stratix V Devices ^{(1), (2)} (Part 1 of 2)

		Resour	ces Used	d Performance							
Memory	Mode	ALUTS	Memory	C1	C2, C2L	C3	C4	12, 12L	13, 13L, 13YY	14	Unit
	Single port, all supported widths	0	1	450	450	400	315	450	400	315	MHz
MLAR	Simple dual-port, x32/x64 depth	0	1	450	450	400	315	450	400	315	MHz
WILAD	Simple dual-port, x16 depth ⁽³⁾	0	1	675	675	533	400	675	533	400	MHz
	ROM, all supported widths	0	1	600	600	500	450	600	500	450	MHz

		Resour	ces Used			Pe	erforman	ce			
Memory	Mode	ALUTS	Memory	C1	C2, C2L	C3	C4	12, 12L	13, 13L, 13YY	14	Unit
	Single-port, all supported widths	0	1	700	700	650	550	700	500	450	MHz
	Simple dual-port, all supported widths	0	1	700	700	650	550	700	500	450	MHz
	Simple dual-port with the read-during-write option set to Old Data , all supported widths	0	1	525	525	455	400	525	455	400	MHz
M20K Block	Simple dual-port with ECC enabled, 512 × 32	0	1	450	450	400	350	450	400	350	MHz
	Simple dual-port with ECC and optional pipeline registers enabled, 512 × 32	0	1	600	600	500	450	600	500	450	MHz
	True dual port, all supported widths	0	1	700	700	650	550	700	500	450	MHz
	ROM, all supported widths	0	1	700	700	650	550	700	500	450	MHz

Table 33. Memory Block Performance Specifications for Stratix V Devices ^{(1), (2)} (Part 2 of 2)

Notes to Table 33:

(1) To achieve the maximum memory block performance, use a memory block clock that comes through global clock routing from an on-chip PLL set to **50**% output duty cycle. Use the Quartus II software to report timing for this and other memory block clocking schemes.

(2) When you use the error detection cyclical redundancy check (CRC) feature, there is no degradation in F_{MAX}.

(3) The F_{MAX} specification is only achievable with Fitter options, MLAB Implementation In 16-Bit Deep Mode enabled.

Temperature Sensing Diode Specifications

Table 34 lists the internal TSD specification.

Table 34. Internal Temperature Sensing Diode Specification

Temperature Range	Accuracy	Offset Calibrated Option	Sampling Rate	Conversion Time	Resolution	Minimum Resolution with no Missing Codes
-40°C to 100°C	±8°C	No	1 MHz, 500 KHz	< 100 ms	8 bits	8 bits

Table 35 lists the specifications for the Stratix V external temperature sensing diode.

Table 35.	External	Temperature	Sensing D	iode Speci	fications f	for Stratix V	Devices
-----------	----------	-------------	-----------	------------	-------------	---------------	---------

Description	Min	Тур	Max	Unit
I _{bias} , diode source current	8	—	200	μA
V _{bias,} voltage across diode	0.3	—	0.9	V
Series resistance	—	_	< 1	Ω
Diode ideality factor	1.006	1.008	1.010	_

Periphery Performance

This section describes periphery performance, including high-speed I/O and external memory interface.

I/O performance supports several system interfaces, such as the **LVDS** high-speed I/O interface, external memory interface, and the **PCI/PCI-X** bus interface. General-purpose I/O standards such as 3.3-, 2.5-, 1.8-, and 1.5-**LVTTL/LVCMOS** are capable of a typical 167 MHz and 1.2-**LVCMOS** at 100 MHz interfacing frequency with a 10 pF load.

The actual achievable frequency depends on design- and system-specific factors. Ensure proper timing closure in your design and perform HSPICE/IBIS simulations based on your specific design and system setup to determine the maximum achievable frequency in your system.

High-Speed I/O Specification

Table 36 lists high-speed I/O timing for Stratix V devices.

Table 36. High-Speed I/O Specifications for Stratix V Devices (1), (2) (Part 1 of 4)

Sumbol	Conditions		C1		C2,	C2L, I	2, I2L	C3,	13, 13 1	., I3YY	C4,14		Unit MHz	
Symbol	Conditions	Min	Тур	Max	Min	Тур	Max	Min	Тур	Max	Min	Тур	Max	Unit MHz MHz MHz
f _{HSCLK_in} (input clock frequency) True Differential I/O Standards	Clock boost factor W = 1 to 40 $^{(4)}$	5	_	800	5		800	5		625	5		525	MHz
f _{HSCLK_in} (input clock frequency) Single Ended I/O Standards ⁽³⁾	Clock boost factor W = 1 to 40 $^{(4)}$	5		800	5		800	5		625	5		525	MHz
f _{HSCLK_in} (input clock frequency) Single Ended I/O Standards	Clock boost factor W = 1 to 40 $^{(4)}$	5	_	520	5		520	5	_	420	5	_	420	MHz
f _{HSCLK_OUT} (output clock frequency)	_	5	_	800	5	_	800	5	_	625 (5)	5	_	525 (5)	MHz

Symbol	Conditiono		C1		C2,	C2, C2L, I2, I2L		C3, I3, I3L, I3YY			C4,I4			Ilnit
əyiinuu	Conultions	Min	Тур	Max	Min	Тур	Max	Min	Тур	Max	Min	Тур	Max	Umt
	SERDES factor J = 3 to 10	(6)		(8)	(6)	_	(8)	(6)		(8)	(6)		(8)	Mbps
f _{HSDR} (data rate)	SERDES factor J = 2, uses DDR Registers	(6)		(7)	(6)	_	(7)	(6)	_	(7)	(6)		(7)	Mbps
	SERDES factor J = 1, uses SDR Register	(6)	_	(7)	(6)	_	(7)	(6)	_	(7)	(6)	_	(7)	Mbps
DPA Mode														
DPA run length	_			1000 0		_	1000 0	_		1000 0	_		1000 0	UI
Soft CDR mode														
Soft-CDR PPM tolerance	_	_	_	300	_	_	300	_	_	300	_	_	300	± PPM
Non DPA Mode	Non DPA Mode													
Sampling Window	_			300			300			300			300	ps

Table 36. High-Speed I/O Specifications for Stratix V Devices (1), (2) (Part 4 of 4)

Notes to Table 36:

(1) When J = 3 to 10, use the serializer/deserializer (SERDES) block.

(2) When J = 1 or 2, bypass the SERDES block.

(3) This only applies to DPA and soft-CDR modes.

(4) Clock Boost Factor (W) is the ratio between the input data rate to the input clock rate.

(5) This is achieved by using the **LVDS** clock network.

(6) The minimum specification depends on the clock source (for example, the PLL and clock pin) and the clock routing resource (global, regional, or local) that you use. The I/O differential buffer and input register do not have a minimum toggle rate.

(7) The maximum ideal frequency is the SERDES factor (J) x the PLL maximum output frequency (fOUT) provided you can close the design timing and the signal integrity simulation is clean.

(8) You can estimate the achievable maximum data rate for non-DPA mode by performing link timing closure analysis. You must consider the board skew margin, transmitter delay margin, and receiver sampling margin to determine the maximum data rate supported.

(9) If the receiver with DPA enabled and transmitter are using shared PLLs, the minimum data rate is 150 Mbps.

(10) You must calculate the leftover timing margin in the receiver by performing link timing closure analysis. You must consider the board skew margin, transmitter channel-to-channel skew, and receiver sampling margin to determine leftover timing margin.

(11) The F_{MAX} specification is based on the fast clock used for serial data. The interface F_{MAX} is also dependent on the parallel clock domain which is design-dependent and requires timing analysis.

(12) Stratix V RX LVDS will need DPA. For Stratix V TX LVDS, the receiver side component must have DPA.

(13) Stratix V LVDS serialization and de-serialization factor needs to be x4 and above.

(14) Requires package skew compensation with PCB trace length.

(15) Do not mix single-ended I/O buffer within LVDS I/O bank.

(16) Chip-to-chip communication only with a maximum load of 5 pF.

(17) When using True LVDS RX channels for emulated LVDS TX channel, only serialization factors 1 and 2 are supported.

Figure 7 shows the dynamic phase alignment (DPA) lock time specifications with the DPA PLL calibration option enabled.

Figure 7. DPA Lock Time Specification with DPA PLL Calibration Enabled

rx_reset			
rx_dpa_locked			<u> </u>
			-

Table 37 lists the DPA lock time specifications for Stratix V devices.

Table 37. DPA Lock Time Specifications for Stratix V GX Devices Only (1), (2), (3)

Standard	Training Pattern	Number of Data Transitions in One Repetition of the Training Pattern	Number of Repetitions per 256 Data Transitions ⁽⁴⁾	Maximum
SPI-4	00000000001111111111	2	128	640 data transitions
Parallel Rapid I/O	00001111	2	128	640 data transitions
	10010000	4	64	640 data transitions
Miscellaneous	10101010	8	32	640 data transitions
Wiscenareous	01010101	8	32	640 data transitions

Notes to Table 37:

(1) The DPA lock time is for one channel.

(2) One data transition is defined as a 0-to-1 or 1-to-0 transition.

(3) The DPA lock time stated in this table applies to both commercial and industrial grade.

(4) This is the number of repetitions for the stated training pattern to achieve the 256 data transitions.

Figure 8 shows the **LVDS** soft-clock data recovery (CDR)/DPA sinusoidal jitter tolerance specification for a data rate \geq 1.25 Gbps. Table 38 lists the **LVDS** soft-CDR/DPA sinusoidal jitter tolerance specification for a data rate \geq 1.25 Gbps.





Jitter Free	Sinusoidal Jitter (UI)	
F1	10,000	25.000
F2	17,565	25.000
F3	1,493,000	0.350
F4	50,000,000	0.350

iadie 38. lvus sott-luk/upa sinusoidai jitter mask vaiues tor a uata kate > 1.2	25 G	.2	1.	1	>	>		Ì	e	F	Ł	đ	a	2	1	R	P							Ľ	I.		I.	Ì	1	3	a	3	a	2	2	2	ŀ	t	t	t	ſ	ľ	3	2	2	2	2	2	1)	D		I		Ľ	1	2	2	ź	â	i		۴	ŕ	r	r		I	I	Ì	1	Π	٥	٢	i	F	f	f	1	1		5	S	S	S	2	2	e	E	I	U	h	I	١	a	ŀ	I	V	۱			ľ	٢	k	k	s	S	S	1	a	2	2		И	V	N			•	۴	r	r	1	1	1	2	2	2	2	e	e	e	E	t	t	i	ŀ	t	ľ	i	i	f	f	ŀ	ŀ	li
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Figure 9 shows the **LVDS** soft-CDR/DPA sinusoidal jitter tolerance specification for a data rate < 1.25 Gbps.





DLL Range, DQS Logic Block, and Memory Output Clock Jitter Specifications

Table 39 lists the DLL range specification for Stratix V devices. The DLL is always in 8-tap mode in Stratix V devices.

Table 39. DLL Range Specifications for Stratix V Devices (1)

C1	C2, C2L, I2, I2L	C3, I3, I3L, I3YY	C4,I4	Unit
300-933	300-933	300-890	300-890	MHz

Note to Table 39:

(1) Stratix V devices support memory interface frequencies lower than 300 MHz, although the reference clock that feeds the DLL must be at least 300 MHz. To support interfaces below 300 MHz, multiply the reference clock feeding the DLL to ensure the frequency is within the supported range of the DLL.

Table 40 lists the DQS phase offset delay per stage for Stratix V devices.

Table 40. DQS Phase Offset Delay Per Setting for Stratix V Devices ^{(1), (2)} (Part 1 of 2)

Speed Grade	Min	Max	Unit
C1	8	14	ps
C2, C2L, I2, I2L	8	14	ps
C3,I3, I3L, I3YY	8	15	ps

Speed Grade	Min	Max	Unit
C4,I4	8	16	ps

Table 40. DQS Phase Offset Delay Per Setting for Stratix V Devices ^{(1), (2)} (Part 2 of 2)

Notes to Table 40:

(1) The typical value equals the average of the minimum and maximum values.

(2) The delay settings are linear with a cumulative delay variation of 40 ps for all speed grades. For example, when using a -2 speed grade and applying a 10-phase offset setting to a 90° phase shift at 400 MHz, the expected average cumulative delay is [625 ps + (10 × 10 ps) ± 20 ps] = 725 ps ± 20 ps.

Table 41 lists the DQS phase shift error for Stratix V devices.

Table 41. DQS Phase Shift Error Specification for DLL-Delayed Clock (t_{DQS_PSERR}) for Stratix V Devices ⁽¹⁾

Number of DQS Delay Buffers	C1	C2, C2L, I2, I2L	C3, I3, I3L, I3YY	C4,14	Unit
1	28	28	30	32	ps
2	56	56	60	64	ps
3	84	84	90	96	ps
4	112	112	120	128	ps

Notes to Table 41:

(1) This error specification is the absolute maximum and minimum error. For example, skew on three DQS delay buffers in a -2 speed grade is ± 78 ps or ± 39 ps.

Table 42 lists the memory output clock jitter specifications for Stratix V devices.

Table 42. Memory Output Clock Jitter Specification for Stratix V Devices (1	^{),} (Part 1 of 2) ^{(2), (3)}
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Clock	Parameter	Symbol	C	1	C2, C2L	, 12, 12L	C3, I3 I3	8, 13L, YY	C4	,14	Unit
NELWURK		-	Min	Max	Min	Max	Min	Max	Min	Max	
	Clock period jitter	$t_{JIT(per)}$	-50	50	-50	50	-55	55	-55	55	ps
Regional	Cycle-to-cycle period jitter	$t_{\text{JIT(cc)}}$	-100	100	-100	100	-110	110	-110	110	ps
	Duty cycle jitter	$t_{JIT(duty)}$	-50	50	-50	50	-82.5	82.5	-82.5	82.5	ps
	Clock period jitter	$t_{JIT(per)}$	-75	75	-75	75	-82.5	82.5	-82.5	82.5	ps
Global	Cycle-to-cycle period jitter	$t_{\text{JIT(cc)}}$	-150	150	-150	150	-165	165	-165	165	ps
	Duty cycle jitter	$t_{JIT(duty)}$	-75	75	-75	75	-90	90	-90	90	ps

Symbol	Description	Min	Max	Unit
t _{JPH}	JTAG port hold time	5	—	ns
t _{JPCO}	JTAG port clock to output	—	11 ⁽¹⁾	ns
t _{JPZX}	JTAG port high impedance to valid output	—	14 ⁽¹⁾	ns
t _{JPXZ}	JTAG port valid output to high impedance	—	14 ⁽¹⁾	ns

Table 46. JTAG Timing Parameters and Values for Stratix V Devices

Notes to Table 46:

(1) A 1 ns adder is required for each V_{CCI0} voltage step down from 3.0 V. For example, $t_{JPC0} = 12$ ns if V_{CCI0} of the TDO I/O bank = 2.5 V, or 13 ns if it equals 1.8 V.

(2) The minimum TCK clock period is 167 ns if VCCBAT is within the range 1.2V-1.5V when you perform the volatile key programming.

Raw Binary File Size

For the POR delay specification, refer to the "POR Delay Specification" section of the "Configuration, Design Security, and Remote System Upgrades in Stratix V Devices".

Table 47 lists the uncompressed raw binary file (.rbf) sizes for Stratix V devices.

Family	Device	Package	Configuration .rbf Size (bits)	IOCSR .rbf Size (bits) ^{(4), (5)}
	500742	H35, F40, F35 ⁽²⁾	213,798,880	562,392
	JOUNAS	H29, F35 ⁽³⁾	137,598,880	564,504
	5SGXA4	—	213,798,880	563,672
	5SGXA5	—	269,979,008	562,392
	5SGXA7	—	269,979,008	562,392
Stratix V GX	5SGXA9	—	342,742,976	700,888
	5SGXAB	—	342,742,976	700,888
	5SGXB5	—	270,528,640	584,344
	5SGXB6	—	270,528,640	584,344
	5SGXB9	—	342,742,976	700,888
	5SGXBB	—	342,742,976	700,888
Stratix V CT	5SGTC5	—	269,979,008	562,392
	5SGTC7	—	269,979,008	562,392
	5SGSD3	—	137,598,880	564,504
	590904	F1517	213,798,880	563,672
Stratix V GS	J303D4	_	137,598,880	564,504
	5SGSD5		213,798,880	563,672
	5SGSD6		293,441,888	565,528
	5SGSD8	—	293,441,888	565,528

Table 47. Uncompressed .rbf Sizes for Stratix V Devices

Active Serial Configuration Timing

Table 52 lists the DCLK frequency specification in the AS configuration scheme.

Fable 52.	DCLK Frequency	Specification in th	e AS Configuration	Scheme ^{(1),}	(2)
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Minimum	Typical	Maximum	Unit
5.3	7.9	12.5	MHz
10.6	15.7	25.0	MHz
21.3	31.4	50.0	MHz
42.6	62.9	100.0	MHz

Notes to Table 52:

(1) This applies to the DCLK frequency specification when using the internal oscillator as the configuration clock source.

(2) The AS multi-device configuration scheme does not support DCLK frequency of 100 MHz.

Figure 14 shows the single-device configuration setup for an AS ×1 mode.





Notes to Figure 14:

- (1) If you are using AS $\times 4$ mode, this signal represents the AS_DATA[3..0] and EPCQ sends in 4-bits of data for each DCLK cycle.
- (2) The initialization clock can be from internal oscillator or CLKUSR pin.
- (3) After the option bit to enable the INIT_DONE pin is configured into the device, the INIT_DONE goes low.

Table 53 lists the timing parameters for AS $\times 1$ and AS $\times 4$ configurations in Stratix V devices.

Table JS. As fining falancees for as $\times 1$ and as $\times 4$ configurations in straits V devices $(2, 2, 2, 3, 3, 3, 3, 3, 3, 3, 3, 3, 3, 3, 3, 3,$	Table 53.	AS Timing	Parameters for AS	\times 1 and AS \times 4 Confi	gurations in Stratix V	/ Devices ^{(1), (2)}	(Part 1 of 2)
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Symbol	Parameter	Minimum	Maximum	Units
t _{CO}	DCLK falling edge to AS_DATA0/ASDO output	—	2	ns
t _{SU}	Data setup time before falling edge on DCLK	1.5	_	ns
t _H	Data hold time after falling edge on DCLK	0	_	ns

Remote System Upgrades

Table 56 lists the timing parameter specifications for the remote system upgrade circuitry.

Table 56. Remote System Upgrade Circuitry Timing Specificatio

Parameter	Minimum	Maximum	Unit	
t _{RU_nCONFIG} ⁽¹⁾	250	—	ns	
t _{RU_nRSTIMER} ⁽²⁾	250	_	ns	

Notes to Table 56:

- (1) This is equivalent to strobing the reconfiguration input of the ALTREMOTE_UPDATE megafunction high for the minimum timing specification. For more information, refer to the Remote System Upgrade State Machine section of the "Configuration, Design Security, and Remote System Upgrades in Stratix V Devices" chapter.
- (2) This is equivalent to strobing the reset_timer input of the ALTREMOTE_UPDATE megafunction high for the minimum timing specification. For more information, refer to the User Watchdog Timer section of the "Configuration, Design Security, and Remote System Upgrades in Stratix V Devices" chapter.

User Watchdog Internal Circuitry Timing Specification

Table 57 lists the operating range of the 12.5-MHz internal oscillator.

Table 57. 12.5-MHz Internal Oscillator Specifications

Minimum	Typical	Maximum	Units	
5.3	7.9	12.5	MHz	

I/O Timing

Altera offers two ways to determine I/O timing—the Excel-based I/O Timing and the Quartus II Timing Analyzer.

Excel-based I/O timing provides pin timing performance for each device density and speed grade. The data is typically used prior to designing the FPGA to get an estimate of the timing budget as part of the link timing analysis. The Quartus II Timing Analyzer provides a more accurate and precise I/O timing data based on the specifics of the design after you complete place-and-route.

 You can download the Excel-based I/O Timing spreadsheet from the Stratix V Devices Documentation web page.

Programmable IOE Delay

Table 58 lists the Stratix V IOE programmable delay settings.

Table 58. IOE Programmable Delay for Stratix V Devices (Part 1 of 2)

Deremeter	Available	Min Offset (2)	Fast Model		Slow Model							
(1)	Settings Offs		Industrial	Commercial	C1	C2	C3	C4	12	13, 13YY	14	Unit
D1	64	0	0.464	0.493	0.838	0.838	0.924	1.011	0.844	0.921	1.006	ns
D2	32	0	0.230	0.244	0.415	0.415	0.459	0.503	0.417	0.456	0.500	ns

Table 61. Document Revision History (Part 2 of 3)

Date	Version	Changes		
		 Added the I3YY speed grade and changed the data rates for the GX channel in Table 1. 		
		 Added the I3YY speed grade to the V_{CC} description in Table 6. 		
		 Added the I3YY speed grade to V_{CCHIP_L}, V_{CCHIP_R}, V_{CCHSSI_L}, and V_{CCHSSI_R} descriptions in Table 7. 		
		■ Added 240-Ω to Table 11.		
		Changed CDR PPM tolerance in Table 23.		
		 Added additional max data rate for fPLL in Table 23. 		
		 Added the I3YY speed grade and changed the data rates for transceiver speed grade 3 in Table 25. 		
		 Added the I3YY speed grade and changed the data rates for transceiver speed grade 3 in Table 26. 		
		 Changed CDR PPM tolerance in Table 28. 		
		 Added additional max data rate for fPLL in Table 28. 		
		 Changed the mode descriptions for MLAB and M20K in Table 33. 		
November 2014		 Changed the Max value of f_{HSCLK_OUT} for the C2, C2L, I2, I2L speed grades in Table 36. 		
	3.3	 Changed the frequency ranges for C1 and C2 in Table 39. 		
		 Changed the .rbf file sizes for 5SGSD6 and 5SGSD8 in Table 47. 		
		 Added note about nSTATUS to Table 50, Table 51, Table 54. 		
		 Changed the available settings in Table 58. 		
		 Changed the note in "Periphery Performance". 		
		 Updated the "I/O Standard Specifications" section. 		
		 Updated the "Raw Binary File Size" section. 		
		 Updated the receiver voltage input range in Table 22. 		
		 Updated the max frequency for the LVDS clock network in Table 36. 		
		■ Updated the DCLK note to Figure 11.		
		 Updated Table 23 VO_{CM} (DC Coupled) condition. 		
		Updated Table 6 and Table 7.		
		 Added the DCLK specification to Table 55. 		
		Updated the notes for Table 47.		
		 Updated the list of parameters for Table 56. 		
November 2013	3.2	Updated Table 28		
November 2013	3.1	Updated Table 33		
November 2013	3.0	Updated Table 23 and Table 28		
October 2013	2.9	 Updated the "Transceiver Characterization" section 		
		 Updated Table 3, Table 12, Table 14, Table 19, Table 20, Table 23, Table 24, Table 28, Table 30, Table 31, Table 32, Table 33, Table 36, Table 39, Table 40, Table 41, Table 42, Table 47, Table 53, Table 58, and Table 59 		
Uctober 2013	2.8	 Added Figure 1 and Figure 3 		
		 Added the "Transceiver Characterization" section 		
		 Removed all "Preliminary" designations. 		

 Table 61. Document Revision History (Part 3 of 3)

Date	Version	Changes	
		■ Updated Table 2, Table 6, Table 7, Table 20, Table 23, Table 27, Table 47, Table 60	
May 2013	2.7	Added Table 24, Table 48	
		 Updated Figure 9, Figure 10, Figure 11, Figure 12 	
February 2013	26	 Updated Table 7, Table 9, Table 20, Table 23, Table 27, Table 30, Table 31, Table 35, Table 46 	
		Updated "Maximum Allowed Overshoot and Undershoot Voltage"	
		 Updated Table 3, Table 6, Table 7, Table 8, Table 23, Table 24, Table 25, Table 27, Table 30, Table 32, Table 35 	
		Added Table 33	
		 Added "Fast Passive Parallel Configuration Timing" 	
		 Added "Active Serial Configuration Timing" 	
December 2012	2.5	 Added "Passive Serial Configuration Timing" 	
		 Added "Remote System Upgrades" 	
		 Added "User Watchdog Internal Circuitry Timing Specification" 	
		Added "Initialization"	
		Added "Raw Binary File Size"	
	2.4	 Added Figure 1, Figure 2, and Figure 3. 	
June 2012		 Updated Table 1, Table 2, Table 3, Table 6, Table 11, Table 22, Table 23, Table 27, Table 29, Table 30, Table 31, Table 32, Table 35, Table 38, Table 39, Table 40, Table 41, Table 43, Table 56, and Table 59. 	
		 Various edits throughout to fix bugs. 	
		Changed title of document to <i>Stratix V Device Datasheet</i> .	
		 Removed document from the Stratix V handbook and made it a separate document. 	
February 2012	2.3	■ Updated Table 1–22, Table 1–29, Table 1–31, and Table 1–31.	
December 2011	22	■ Added Table 2–31.	
December 2011	2.2	■ Updated Table 2–28 and Table 2–34.	
	2.1	 Added Table 2–2 and Table 2–21 and updated Table 2–5 with information about Stratix V GT devices. 	
November 2011		 Updated Table 2–11, Table 2–13, Table 2–20, and Table 2–25. 	
		 Various edits throughout to fix SPRs. 	
		■ Updated Table 2–4, Table 2–18, Table 2–19, Table 2–21, Table 2–22, Table 2–23, and Table 2–24.	
May 2011	2.0	 Updated the "DQ Logic Block and Memory Output Clock Jitter Specifications" title. 	
		Chapter moved to Volume 1.	
		 Minor text edits. 	
		■ Updated Table 1–2, Table 1–4, Table 1–19, and Table 1–23.	
December 2010	1.1	 Converted chapter to the new template. 	
		 Minor text edits. 	
July 2010	1.0	Initial release.	