

Welcome to [E-XFL.COM](https://www.e-xfl.com)

### Understanding [Embedded - FPGAs \(Field Programmable Gate Array\)](#)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

### Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

#### Details

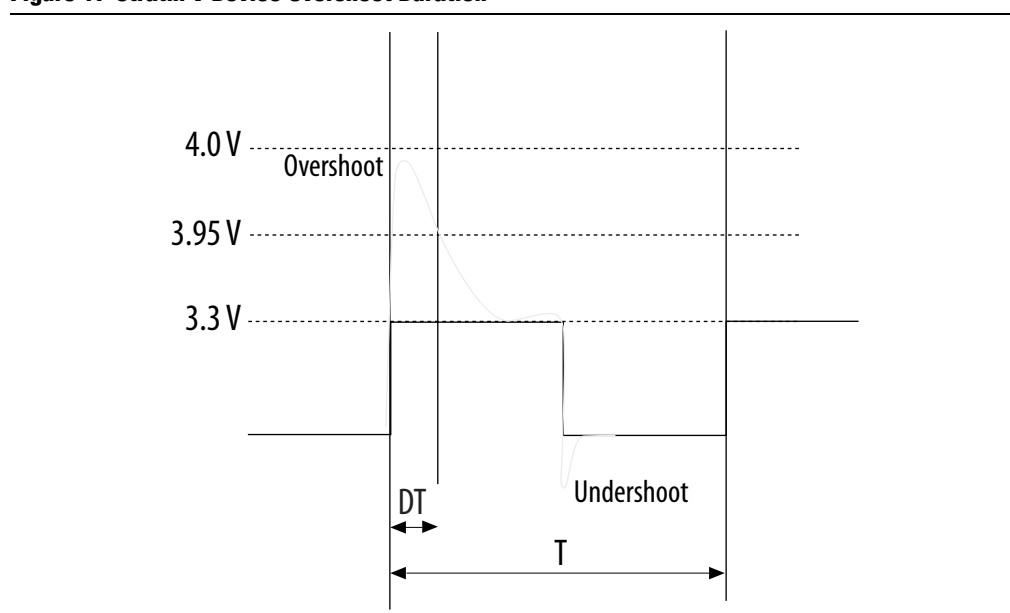
|                                |   |
|--------------------------------|---|
| Product Status                 | Obsolete  |
| Number of LABs/CLBs            | 185000  |
| Number of Logic Elements/Cells | 490000  |
| Total RAM Bits                 | 46080000  |
| Number of I/O                  | 552   |
| Number of Gates                | -   |
| Voltage - Supply               | 0.87V ~ 0.93V   |
| Mounting Type                  | Surface Mount   |
| Operating Temperature          | -40°C ~ 100°C (TJ)  |
| Package / Case                 | 1152-BBGA, FCBGA  |
| Supplier Device Package        | 1152-FBGA (35x35)   |
| Purchase URL                   | <a href="https://www.e-xfl.com/product-detail/intel/5sgxea5h1f35i2n">https://www.e-xfl.com/product-detail/intel/5sgxea5h1f35i2n</a> |

Table 5 lists the maximum allowed input overshoot voltage and the duration of the overshoot voltage as a percentage of device lifetime. The maximum allowed overshoot duration is specified as a percentage of high time over the lifetime of the device. A DC signal is equivalent to 100% of the duty cycle. For example, a signal that overshoots to 3.95 V can be at 3.95 V for only ~21% over the lifetime of the device; for a device lifetime of 10 years, the overshoot duration amounts to ~2 years.

**Table 5. Maximum Allowed Overshoot During Transitions**

| Symbol     | Description      | Condition (V) | Overshoot Duration as %<br>@ $T_J = 100^{\circ}\text{C}$ | Unit |
|------------|------------------|---------------|--|------|
| $V_i$ (AC) | AC input voltage | 3.8           | 100  | %    |
|            |                  | 3.85          | 64   | %    |
|            |                  | 3.9           | 36   | %    |
|            |                  | 3.95          | 21   | %    |
|            |                  | 4             | 12   | %    |
|            |                  | 4.05          | 7  | %    |
|            |                  | 4.1           | 4  | %    |
|            |                  | 4.15          | 2  | %    |
|            |                  | 4.2           | 1  | %    |

**Figure 1. Stratix V Device Overshoot Duration**



## Recommended Operating Conditions

This section lists the functional operating limits for the AC and DC parameters for Stratix V devices. Table 6 lists the steady-state voltage and current values expected from Stratix V devices. Power supply ramps must all be strictly monotonic, without plateaus.

**Table 6. Recommended Operating Conditions for Stratix V Devices (Part 1 of 2)**

| Symbol                            | Description   | Condition  | Min <sup>(4)</sup> | Typ  | Max <sup>(4)</sup> | Unit |
|-----------------------------------|---|------------|--------------------|------|--------------------|------|
| V <sub>CC</sub>                   | Core voltage and periphery circuitry power supply (C1, C2, I2, and I3YY speed grades)                             | —          | 0.87               | 0.9  | 0.93               | V    |
|                                   | Core voltage and periphery circuitry power supply (C2L, C3, C4, I2L, I3, I3L, and I4 speed grades) <sup>(3)</sup> | —          | 0.82               | 0.85 | 0.88               | V    |
| V <sub>CCPT</sub>                 | Power supply for programmable power technology  | —          | 1.45               | 1.50 | 1.55               | V    |
| V <sub>CC_AUX</sub>               | Auxiliary supply for the programmable power technology  | —          | 2.375              | 2.5  | 2.625              | V    |
| V <sub>CCPD</sub> <sup>(1)</sup>  | I/O pre-driver (3.0 V) power supply   | —          | 2.85               | 3.0  | 3.15               | V    |
|                                   | I/O pre-driver (2.5 V) power supply   | —          | 2.375              | 2.5  | 2.625              | V    |
| V <sub>CCIO</sub>                 | I/O buffers (3.0 V) power supply  | —          | 2.85               | 3.0  | 3.15               | V    |
|                                   | I/O buffers (2.5 V) power supply  | —          | 2.375              | 2.5  | 2.625              | V    |
|                                   | I/O buffers (1.8 V) power supply  | —          | 1.71               | 1.8  | 1.89               | V    |
|                                   | I/O buffers (1.5 V) power supply  | —          | 1.425              | 1.5  | 1.575              | V    |
|                                   | I/O buffers (1.35 V) power supply   | —          | 1.283              | 1.35 | 1.45               | V    |
|                                   | I/O buffers (1.25 V) power supply   | —          | 1.19               | 1.25 | 1.31               | V    |
|                                   | I/O buffers (1.2 V) power supply  | —          | 1.14               | 1.2  | 1.26               | V    |
| V <sub>CCPGM</sub>                | Configuration pins (3.0 V) power supply   | —          | 2.85               | 3.0  | 3.15               | V    |
|                                   | Configuration pins (2.5 V) power supply   | —          | 2.375              | 2.5  | 2.625              | V    |
|                                   | Configuration pins (1.8 V) power supply   | —          | 1.71               | 1.8  | 1.89               | V    |
| V <sub>CCA_FPLL</sub>             | PLL analog voltage regulator power supply   | —          | 2.375              | 2.5  | 2.625              | V    |
| V <sub>CCD_FPLL</sub>             | PLL digital voltage regulator power supply  | —          | 1.45               | 1.5  | 1.55               | V    |
| V <sub>CCBAT</sub> <sup>(2)</sup> | Battery back-up power supply (For design security volatile key register)  | —          | 1.2                | —    | 3.0                | V    |
| V <sub>I</sub>                    | DC input voltage  | —          | −0.5               | —    | 3.6                | V    |
| V <sub>O</sub>                    | Output voltage  | —          | 0                  | —    | V <sub>CCIO</sub>  | V    |
| T <sub>J</sub>                    | Operating junction temperature  | Commercial | 0                  | —    | 85                 | °C   |
|                                   |   | Industrial | −40                | —    | 100                | °C   |

**Table 6. Recommended Operating Conditions for Stratix V Devices (Part 2 of 2)**

| Symbol            | Description            | Condition    | Min <sup>(4)</sup> | Typ | Max <sup>(4)</sup> | Unit |
|-------------------|------------------------|--------------|--------------------|-----|--------------------|------|
| t <sub>RAMP</sub> | Power supply ramp time | Standard POR | 200 $\mu$ s        | —   | 100 ms             | —    |
|                   |                        | Fast POR     | 200 $\mu$ s        | —   | 4 ms               | —    |

**Notes to Table 6:**

- (1) V<sub>CCPD</sub> must be 2.5 V when V<sub>CCIO</sub> is 2.5, 1.8, 1.5, 1.35, 1.25 or 1.2 V. V<sub>CCPD</sub> must be 3.0 V when V<sub>CCIO</sub> is 3.0 V.
- (2) If you do not use the design security feature in Stratix V devices, connect V<sub>CCBAT</sub> to a 1.2- to 3.0-V power supply. Stratix V power-on-reset (POR) circuitry monitors V<sub>CCBAT</sub>. Stratix V devices will not exit POR if V<sub>CCBAT</sub> stays at logic low.
- (3) C2L and I2L can also be run at 0.90 V for legacy boards that were designed for the C2 and I2 speed grades.
- (4) The power supply value describes the budget for the DC (static) power supply tolerance and does not include the dynamic tolerance requirements. Refer to the PDN tool for the additional budget for the dynamic tolerance requirements.

Table 7 lists the transceiver power supply recommended operating conditions for Stratix V GX, GS, and GT devices.

**Table 7. Recommended Transceiver Power Supply Operating Conditions for Stratix V GX, GS, and GT Devices (Part 1 of 2)**

| Symbol                            | Description   | Devices    | Minimum <sup>(4)</sup> | Typical | Maximum <sup>(4)</sup> | Unit |
|-----------------------------------|---|------------|------------------------|---------|------------------------|------|
| V <sub>CCA_GXBL</sub><br>(1), (3) | Transceiver channel PLL power supply (left side)  | GX, GS, GT | 2.85                   | 3.0     | 3.15                   | V    |
|                                   |   |            | 2.375                  | 2.5     | 2.625                  |      |
| V <sub>CCA_GXBR</sub><br>(1), (3) | Transceiver channel PLL power supply (right side)   | GX, GS     | 2.85                   | 3.0     | 3.15                   | V    |
|                                   |   |            | 2.375                  | 2.5     | 2.625                  |      |
| V <sub>CCA_GTBR</sub>             | Transceiver channel PLL power supply (right side)   | GT         | 2.85                   | 3.0     | 3.15                   | V    |
| V <sub>CCHIP_L</sub>              | Transceiver hard IP power supply (left side; C1, C2, I2, and I3YY speed grades)               | GX, GS, GT | 0.87                   | 0.9     | 0.93                   | V    |
|                                   | Transceiver hard IP power supply (left side; C2L, C3, C4, I2L, I3, I3L, and I4 speed grades)  | GX, GS, GT | 0.82                   | 0.85    | 0.88                   | V    |
| V <sub>CCHIP_R</sub>              | Transceiver hard IP power supply (right side; C1, C2, I2, and I3YY speed grades)              | GX, GS, GT | 0.87                   | 0.9     | 0.93                   | V    |
|                                   | Transceiver hard IP power supply (right side; C2L, C3, C4, I2L, I3, I3L, and I4 speed grades) | GX, GS, GT | 0.82                   | 0.85    | 0.88                   | V    |
| V <sub>CCHSSI_L</sub>             | Transceiver PCS power supply (left side; C1, C2, I2, and I3YY speed grades)                   | GX, GS, GT | 0.87                   | 0.9     | 0.93                   | V    |
|                                   | Transceiver PCS power supply (left side; C2L, C3, C4, I2L, I3, I3L, and I4 speed grades)      | GX, GS, GT | 0.82                   | 0.85    | 0.88                   | V    |
| V <sub>CCHSSI_R</sub>             | Transceiver PCS power supply (right side; C1, C2, I2, and I3YY speed grades)                  | GX, GS, GT | 0.87                   | 0.9     | 0.93                   | V    |
|                                   | Transceiver PCS power supply (right side; C2L, C3, C4, I2L, I3, I3L, and I4 speed grades)     | GX, GS, GT | 0.82                   | 0.85    | 0.88                   | V    |
| V <sub>CCR_GXBL</sub><br>(2)      | Receiver analog power supply (left side)  | GX, GS, GT | 0.82                   | 0.85    | 0.88                   | V    |
|                                   |   |            | 0.87                   | 0.90    | 0.93                   |      |
|                                   |   |            | 0.97                   | 1.0     | 1.03                   |      |
|                                   |   |            | 1.03                   | 1.05    | 1.07                   |      |

**Table 7. Recommended Transceiver Power Supply Operating Conditions for Stratix V GX, GS, and GT Devices (Part 2 of 2)**

| Symbol                 | Description  | Devices    | Minimum <sup>(4)</sup> | Typical | Maximum <sup>(4)</sup> | Unit |
|------------------------|--|------------|------------------------|---------|------------------------|------|
| $V_{CCR\_GXBR}$<br>(2) | Receiver analog power supply (right side)                    | GX, GS, GT | 0.82                   | 0.85    | 0.88                   | V    |
|                        |  |            | 0.87                   | 0.90    | 0.93                   |      |
|                        |  |            | 0.97                   | 1.0     | 1.03                   |      |
|                        |  |            | 1.03                   | 1.05    | 1.07                   |      |
| $V_{CCR\_GTBR}$        | Receiver analog power supply for GT channels (right side)    | GT         | 1.02                   | 1.05    | 1.08                   | V    |
| $V_{CCT\_GXBL}$<br>(2) | Transmitter analog power supply (left side)                  | GX, GS, GT | 0.82                   | 0.85    | 0.88                   | V    |
|                        |  |            | 0.87                   | 0.90    | 0.93                   |      |
|                        |  |            | 0.97                   | 1.0     | 1.03                   |      |
|                        |  |            | 1.03                   | 1.05    | 1.07                   |      |
| $V_{CCT\_GXBR}$<br>(2) | Transmitter analog power supply (right side)                 | GX, GS, GT | 0.82                   | 0.85    | 0.88                   | V    |
|                        |  |            | 0.87                   | 0.90    | 0.93                   |      |
|                        |  |            | 0.97                   | 1.0     | 1.03                   |      |
|                        |  |            | 1.03                   | 1.05    | 1.07                   |      |
| $V_{CCT\_GTBR}$        | Transmitter analog power supply for GT channels (right side) | GT         | 1.02                   | 1.05    | 1.08                   | V    |
| $V_{CCL\_GTBR}$        | Transmitter clock network power supply                       | GT         | 1.02                   | 1.05    | 1.08                   | V    |
| $V_{CCH\_GXBL}$        | Transmitter output buffer power supply (left side)           | GX, GS, GT | 1.425                  | 1.5     | 1.575                  | V    |
| $V_{CCH\_GXBR}$        | Transmitter output buffer power supply (right side)          | GX, GS, GT | 1.425                  | 1.5     | 1.575                  | V    |

**Notes to Table 7:**

- (1) This supply must be connected to 3.0 V if the CMU PLL, receiver CDR, or both, are configured at a base data rate > 6.5 Gbps. Up to 6.5 Gbps, you can connect this supply to either 3.0 V or 2.5 V.
- (2) Refer to Table 8 to select the correct power supply level for your design.
- (3) When using ATX PLLs, the supply must be 3.0 V.
- (4) This value describes the budget for the DC (static) power supply tolerance and does not include the dynamic tolerance requirements. Refer to the PDN tool for the additional budget for the dynamic tolerance requirements.

**Table 18. Single-Ended SSTL, HSTL, and HSUL I/O Reference Voltage Specifications for Stratix V Devices**

| I/O Standard            | $V_{CCIO}$ (V) |      |       | $V_{REF}$ (V)     |                  |                   | $V_{TT}$ (V)      |                  |                   |
|-------------------------|----------------|------|-------|-------------------|------------------|-------------------|-------------------|------------------|-------------------|
|                         | Min            | Typ  | Max   | Min               | Typ              | Max               | Min               | Typ              | Max               |
| SSTL-2<br>Class I, II   | 2.375          | 2.5  | 2.625 | $0.49 * V_{CCIO}$ | $0.5 * V_{CCIO}$ | $0.51 * V_{CCIO}$ | $V_{REF} - 0.04$  | $V_{REF}$        | $V_{REF} + 0.04$  |
| SSTL-18<br>Class I, II  | 1.71           | 1.8  | 1.89  | 0.833             | 0.9              | 0.969             | $V_{REF} - 0.04$  | $V_{REF}$        | $V_{REF} + 0.04$  |
| SSTL-15<br>Class I, II  | 1.425          | 1.5  | 1.575 | $0.49 * V_{CCIO}$ | $0.5 * V_{CCIO}$ | $0.51 * V_{CCIO}$ | $0.49 * V_{CCIO}$ | $0.5 * V_{CCIO}$ | $0.51 * V_{CCIO}$ |
| SSTL-135<br>Class I, II | 1.283          | 1.35 | 1.418 | $0.49 * V_{CCIO}$ | $0.5 * V_{CCIO}$ | $0.51 * V_{CCIO}$ | $0.49 * V_{CCIO}$ | $0.5 * V_{CCIO}$ | $0.51 * V_{CCIO}$ |
| SSTL-125<br>Class I, II | 1.19           | 1.25 | 1.26  | $0.49 * V_{CCIO}$ | $0.5 * V_{CCIO}$ | $0.51 * V_{CCIO}$ | $0.49 * V_{CCIO}$ | $0.5 * V_{CCIO}$ | $0.51 * V_{CCIO}$ |
| SSTL-12<br>Class I, II  | 1.14           | 1.20 | 1.26  | $0.49 * V_{CCIO}$ | $0.5 * V_{CCIO}$ | $0.51 * V_{CCIO}$ | $0.49 * V_{CCIO}$ | $0.5 * V_{CCIO}$ | $0.51 * V_{CCIO}$ |
| HSTL-18<br>Class I, II  | 1.71           | 1.8  | 1.89  | 0.85              | 0.9              | 0.95              | —                 | $V_{CCIO}/2$     | —                 |
| HSTL-15<br>Class I, II  | 1.425          | 1.5  | 1.575 | 0.68              | 0.75             | 0.9               | —                 | $V_{CCIO}/2$     | —                 |
| HSTL-12<br>Class I, II  | 1.14           | 1.2  | 1.26  | $0.47 * V_{CCIO}$ | $0.5 * V_{CCIO}$ | $0.53 * V_{CCIO}$ | —                 | $V_{CCIO}/2$     | —                 |
| HSUL-12                 | 1.14           | 1.2  | 1.3   | $0.49 * V_{CCIO}$ | $0.5 * V_{CCIO}$ | $0.51 * V_{CCIO}$ | —                 | —                | —                 |

**Table 19. Single-Ended SSTL, HSTL, and HSUL I/O Standards Signal Specifications for Stratix V Devices (Part 1 of 2)**

| I/O Standard            | $V_{IL(DC)}$ (V) |                   | $V_{IH(DC)}$ (V)  |                  | $V_{IL(AC)}$ (V)  | $V_{IH(AC)}$ (V)  | $V_{OL}$ (V)     | $V_{OH}$ (V)      | $I_{OI}$ (mA) | $I_{OH}$ (mA) |
|-------------------------|------------------|-------------------|-------------------|------------------|-------------------|-------------------|------------------|-------------------|---------------|---------------|
|                         | Min              | Max               | Min               | Max              | Max               | Min               | Max              | Min               |               |               |
| SSTL-2<br>Class I       | -0.3             | $V_{REF} - 0.15$  | $V_{REF} + 0.15$  | $V_{CCIO} + 0.3$ | $V_{REF} - 0.31$  | $V_{REF} + 0.31$  | $V_{TT} - 0.608$ | $V_{TT} + 0.608$  | 8.1           | -8.1          |
| SSTL-2<br>Class II      | -0.3             | $V_{REF} - 0.15$  | $V_{REF} + 0.15$  | $V_{CCIO} + 0.3$ | $V_{REF} - 0.31$  | $V_{REF} + 0.31$  | $V_{TT} - 0.81$  | $V_{TT} + 0.81$   | 16.2          | -16.2         |
| SSTL-18<br>Class I      | -0.3             | $V_{REF} - 0.125$ | $V_{REF} + 0.125$ | $V_{CCIO} + 0.3$ | $V_{REF} - 0.25$  | $V_{REF} + 0.25$  | $V_{TT} - 0.603$ | $V_{TT} + 0.603$  | 6.7           | -6.7          |
| SSTL-18<br>Class II     | -0.3             | $V_{REF} - 0.125$ | $V_{REF} + 0.125$ | $V_{CCIO} + 0.3$ | $V_{REF} - 0.25$  | $V_{REF} + 0.25$  | 0.28             | $V_{CCIO} - 0.28$ | 13.4          | -13.4         |
| SSTL-15<br>Class I      | —                | $V_{REF} - 0.1$   | $V_{REF} + 0.1$   | —                | $V_{REF} - 0.175$ | $V_{REF} + 0.175$ | $0.2 * V_{CCIO}$ | $0.8 * V_{CCIO}$  | 8             | -8            |
| SSTL-15<br>Class II     | —                | $V_{REF} - 0.1$   | $V_{REF} + 0.1$   | —                | $V_{REF} - 0.175$ | $V_{REF} + 0.175$ | $0.2 * V_{CCIO}$ | $0.8 * V_{CCIO}$  | 16            | -16           |
| SSTL-135<br>Class I, II | —                | $V_{REF} - 0.09$  | $V_{REF} + 0.09$  | —                | $V_{REF} - 0.16$  | $V_{REF} + 0.16$  | $0.2 * V_{CCIO}$ | $0.8 * V_{CCIO}$  | —             | —             |
| SSTL-125<br>Class I, II | —                | $V_{REF} - 0.85$  | $V_{REF} + 0.85$  | —                | $V_{REF} - 0.15$  | $V_{REF} + 0.15$  | $0.2 * V_{CCIO}$ | $0.8 * V_{CCIO}$  | —             | —             |
| SSTL-12<br>Class I, II  | —                | $V_{REF} - 0.1$   | $V_{REF} + 0.1$   | —                | $V_{REF} - 0.15$  | $V_{REF} + 0.15$  | $0.2 * V_{CCIO}$ | $0.8 * V_{CCIO}$  | —             | —             |

**Table 19. Single-Ended SSTL, HSTL, and HSUL I/O Standards Signal Specifications for Stratix V Devices (Part 2 of 2)**

| I/O Standard     | $V_{IL(DC)}$ (V) |                  | $V_{IH(DC)}$ (V) |                   | $V_{IL(AC)}$ (V) | $V_{IH(AC)}$ (V) | $V_{OL}$ (V)      | $V_{OH}$ (V)      | $I_{ol}$ (mA) | $I_{oh}$ (mA) |
|------------------|------------------|------------------|------------------|-------------------|------------------|------------------|-------------------|-------------------|---------------|---------------|
|                  | Min              | Max              | Min              | Max               | Max              | Min              | Max               | Min               |               |               |
| HSTL-18 Class I  | —                | $V_{REF} - 0.1$  | $V_{REF} + 0.1$  | —                 | $V_{REF} - 0.2$  | $V_{REF} + 0.2$  | 0.4               | $V_{CCIO} - 0.4$  | 8             | -8            |
| HSTL-18 Class II | —                | $V_{REF} - 0.1$  | $V_{REF} + 0.1$  | —                 | $V_{REF} - 0.2$  | $V_{REF} + 0.2$  | 0.4               | $V_{CCIO} - 0.4$  | 16            | -16           |
| HSTL-15 Class I  | —                | $V_{REF} - 0.1$  | $V_{REF} + 0.1$  | —                 | $V_{REF} - 0.2$  | $V_{REF} + 0.2$  | 0.4               | $V_{CCIO} - 0.4$  | 8             | -8            |
| HSTL-15 Class II | —                | $V_{REF} - 0.1$  | $V_{REF} + 0.1$  | —                 | $V_{REF} - 0.2$  | $V_{REF} + 0.2$  | 0.4               | $V_{CCIO} - 0.4$  | 16            | -16           |
| HSTL-12 Class I  | -0.15            | $V_{REF} - 0.08$ | $V_{REF} + 0.08$ | $V_{CCIO} + 0.15$ | $V_{REF} - 0.15$ | $V_{REF} + 0.15$ | $0.25^* V_{CCIO}$ | $0.75^* V_{CCIO}$ | 8             | -8            |
| HSTL-12 Class II | -0.15            | $V_{REF} - 0.08$ | $V_{REF} + 0.08$ | $V_{CCIO} + 0.15$ | $V_{REF} - 0.15$ | $V_{REF} + 0.15$ | $0.25^* V_{CCIO}$ | $0.75^* V_{CCIO}$ | 16            | -16           |
| HSUL-12          | —                | $V_{REF} - 0.13$ | $V_{REF} + 0.13$ | —                 | $V_{REF} - 0.22$ | $V_{REF} + 0.22$ | $0.1^* V_{CCIO}$  | $0.9^* V_{CCIO}$  | —             | —             |

**Table 20. Differential SSTL I/O Standards for Stratix V Devices**

| I/O Standard         | $V_{CCIO}$ (V) |      |       | $V_{SWING(DC)}$ (V) |                  | $V_{X(AC)}$ (V)      |              |                      | $V_{SWING(AC)}$ (V)       |                           |
|----------------------|----------------|------|-------|---------------------|------------------|----------------------|--------------|----------------------|---------------------------|---------------------------|
|                      | Min            | Typ  | Max   | Min                 | Max              | Min                  | Typ          | Max                  | Min                       | Max                       |
| SSTL-2 Class I, II   | 2.375          | 2.5  | 2.625 | 0.3                 | $V_{CCIO} + 0.6$ | $V_{CCIO}/2 - 0.2$   | —            | $V_{CCIO}/2 + 0.2$   | 0.62                      | $V_{CCIO} + 0.6$          |
| SSTL-18 Class I, II  | 1.71           | 1.8  | 1.89  | 0.25                | $V_{CCIO} + 0.6$ | $V_{CCIO}/2 - 0.175$ | —            | $V_{CCIO}/2 + 0.175$ | 0.5                       | $V_{CCIO} + 0.6$          |
| SSTL-15 Class I, II  | 1.425          | 1.5  | 1.575 | 0.2                 | (1)              | $V_{CCIO}/2 - 0.15$  | —            | $V_{CCIO}/2 + 0.15$  | 0.35                      | —                         |
| SSTL-135 Class I, II | 1.283          | 1.35 | 1.45  | 0.2                 | (1)              | $V_{CCIO}/2 - 0.15$  | $V_{CCIO}/2$ | $V_{CCIO}/2 + 0.15$  | $2(V_{IH(AC)} - V_{REF})$ | $2(V_{IL(AC)} - V_{REF})$ |
| SSTL-125 Class I, II | 1.19           | 1.25 | 1.31  | 0.18                | (1)              | $V_{CCIO}/2 - 0.15$  | $V_{CCIO}/2$ | $V_{CCIO}/2 + 0.15$  | $2(V_{IH(AC)} - V_{REF})$ | —                         |
| SSTL-12 Class I, II  | 1.14           | 1.2  | 1.26  | 0.18                | —                | $V_{REF} - 0.15$     | $V_{CCIO}/2$ | $V_{REF} + 0.15$     | -0.30                     | 0.30                      |

**Note to Table 20:**

(1) The maximum value for  $V_{SWING(DC)}$  is not defined. However, each single-ended signal needs to be within the respective single-ended limits ( $V_{IH(DC)}$  and  $V_{IL(DC)}$ ).

**Table 21. Differential HSTL and HSUL I/O Standards for Stratix V Devices (Part 1 of 2)**

| I/O Standard        | $V_{CCIO}$ (V) |     |       | $V_{DIF(DC)}$ (V) |     | $V_{X(AC)}$ (V) |     |      | $V_{CM(DC)}$ (V) |     |      | $V_{DIF(AC)}$ (V) |     |
|---------------------|----------------|-----|-------|-------------------|-----|-----------------|-----|------|------------------|-----|------|-------------------|-----|
|                     | Min            | Typ | Max   | Min               | Max | Min             | Typ | Max  | Min              | Typ | Max  | Min               | Max |
| HSTL-18 Class I, II | 1.71           | 1.8 | 1.89  | 0.2               | —   | 0.78            | —   | 1.12 | 0.78             | —   | 1.12 | 0.4               | —   |
| HSTL-15 Class I, II | 1.425          | 1.5 | 1.575 | 0.2               | —   | 0.68            | —   | 0.9  | 0.68             | —   | 0.9  | 0.4               | —   |

-  You typically use the interactive Excel-based Early Power Estimator before designing the FPGA to get a magnitude estimate of the device power. The Quartus II PowerPlay Power Analyzer provides better quality estimates based on the specifics of the design after you complete place-and-route. The PowerPlay Power Analyzer can apply a combination of user-entered, simulation-derived, and estimated signal activities that, when combined with detailed circuit models, yields very accurate power estimates.
-  For more information about power estimation tools, refer to the *PowerPlay Early Power Estimator User Guide* and the *PowerPlay Power Analysis* chapter in the *Quartus II Handbook*.



**Table 23. Transceiver Specifications for Stratix V GX and GS Devices <sup>(1)</sup> (Part 2 of 7)**

| Symbol/<br>Description   | Conditions   | Transceiver Speed<br>Grade 1     |                   |      | Transceiver Speed<br>Grade 2     |                   |      | Transceiver Speed<br>Grade 3     |                       |      | Unit        |
|--|--|----------------------------------|-------------------|------|----------------------------------|-------------------|------|----------------------------------|-----------------------|------|-------------|
|  |  | Min                              | Typ               | Max  | Min                              | Typ               | Max  | Min                              | Typ                   | Max  |             |
| Spread-spectrum<br>downspread                                      | PCIe   | —                                | 0 to<br>-0.5      | —    | —                                | 0 to<br>-0.5      | —    | —                                | 0 to<br>-0.5          | —    | %           |
| On-chip<br>termination<br>resistors <sup>(21)</sup>                | —  | —                                | 100               | —    | —                                | 100               | —    | —                                | 100                   | —    | $\Omega$    |
| Absolute $V_{MAX}$ <sup>(5)</sup>                                  | Dedicated<br>reference<br>clock pin                    | —                                | —                 | 1.6  | —                                | —                 | 1.6  | —                                | —                     | 1.6  | V           |
|  | RX reference<br>clock pin                              | —                                | —                 | 1.2  | —                                | —                 | 1.2  | —                                | —                     | 1.2  |             |
| Absolute $V_{MIN}$   | —  | -0.4                             | —                 | —    | -0.4                             | —                 | —    | -0.4                             | —                     | —    | V           |
| Peak-to-peak<br>differential input<br>voltage                      | —  | 200                              | —                 | 1600 | 200                              | —                 | 1600 | 200                              | —                     | 1600 | mV          |
| $V_{ICM}$ (AC<br>coupled) <sup>(3)</sup>                           | Dedicated<br>reference<br>clock pin                    | 1050/1000/900/850 <sup>(2)</sup> |                   |      | 1050/1000/900/850 <sup>(2)</sup> |                   |      | 1050/1000/900/850 <sup>(2)</sup> |                       |      | mV          |
|  | RX reference<br>clock pin                              | 1.0/0.9/0.85 <sup>(4)</sup>      |                   |      | 1.0/0.9/0.85 <sup>(4)</sup>      |                   |      | 1.0/0.9/0.85 <sup>(4)</sup>      |                       |      | V           |
| $V_{ICM}$ (DC coupled)   | HCSL I/O<br>standard for<br>PCIe<br>reference<br>clock | 250                              | —                 | 550  | 250                              | —                 | 550  | 250                              | —                     | 550  | mV          |
| Transmitter<br>REFCLK Phase<br>Noise<br>(622 MHz) <sup>(20)</sup>  | 100 Hz   | —                                | —                 | -70  | —                                | —                 | -70  | —                                | —                     | -70  | dBc/Hz      |
|  | 1 kHz  | —                                | —                 | -90  | —                                | —                 | -90  | —                                | —                     | -90  | dBc/Hz      |
|  | 10 kHz   | —                                | —                 | -100 | —                                | —                 | -100 | —                                | —                     | -100 | dBc/Hz      |
|  | 100 kHz  | —                                | —                 | -110 | —                                | —                 | -110 | —                                | —                     | -110 | dBc/Hz      |
|  | $\geq 1$ MHz   | —                                | —                 | -120 | —                                | —                 | -120 | —                                | —                     | -120 | dBc/Hz      |
| Transmitter<br>REFCLK Phase<br>Jitter<br>(100 MHz) <sup>(17)</sup> | 10 kHz to<br>1.5 MHz<br>(PCIe)                         | —                                | —                 | 3    | —                                | —                 | 3    | —                                | —                     | 3    | ps<br>(rms) |
| $R_{REF}$ <sup>(19)</sup>  | —  | —                                | 1800<br>$\pm 1\%$ | —    | —                                | 1800<br>$\pm 1\%$ | —    | —                                | 180<br>0<br>$\pm 1\%$ | —    | $\Omega$    |
| <b>Transceiver Clocks</b>  |  |                                  |                   |      |                                  |                   |      |                                  |                       |      |             |
| fixedclk clock<br>frequency  | PCIe<br>Receiver<br>Detect                             | —                                | 100<br>or<br>125  | —    | —                                | 100<br>or<br>125  | —    | —                                | 100<br>or<br>125      | —    | MHz         |

**Table 23. Transceiver Specifications for Stratix V GX and GS Devices <sup>(1)</sup> (Part 7 of 7)**

| Symbol/<br>Description | Conditions | Transceiver Speed<br>Grade 1 |     |     | Transceiver Speed<br>Grade 2 |     |     | Transceiver Speed<br>Grade 3 |     |     | Unit |
|------------------------|------------|------------------------------|-----|-----|------------------------------|-----|-----|------------------------------|-----|-----|------|
|                        |            | Min                          | Typ | Max | Min                          | Typ | Max | Min                          | Typ | Max |      |
| $t_{pll\_lock}^{(16)}$ | —          | —                            | —   | 10  | —                            | —   | 10  | —                            | —   | 10  | μs   |

**Notes to Table 23:**

- (1) Speed grades shown in Table 23 refer to the PMA Speed Grade in the device ordering code. The maximum data rate could be restricted by the Core/PCS speed grade. Contact your Altera Sales Representative for the maximum data rate specifications in each speed grade combination offered. For more information about device ordering codes, refer to the *Stratix V Device Overview*.
- (2) The reference clock common mode voltage is equal to the  $V_{CCR\_GXB}$  power supply level.
- (3) This supply must be connected to 1.0 V if the transceiver is configured at a data rate > 6.5 Gbps, and to 1.05 V if configured at a data rate > 10.3 Gbps when DFE is used. For data rates up to 6.5 Gbps, you can connect this supply to 0.85 V.
- (4) This supply follows  $V_{CCR\_GXB}$ .
- (5) The device cannot tolerate prolonged operation at this absolute maximum.
- (6) The differential eye opening specification at the receiver input pins assumes that **Receiver Equalization** is disabled. If you enable **Receiver Equalization**, the receiver circuitry can tolerate a lower minimum eye opening, depending on the equalization level.
- (7) The Quartus II software automatically selects the appropriate slew rate depending on the configured data rate or functional mode.
- (8) The input reference clock frequency options depend on the data rate and the device speed grade.
- (9) The line data rate may be limited by PCS-FPGA interface speed grade.
- (10) Refer to Figure 1 for the GX channel AC gain curves. The total effective AC gain is the AC gain minus the DC gain.
- (11)  $t_{LTR}$  is the time required for the receive CDR to lock to the input reference clock frequency after coming out of reset.
- (12)  $t_{LTD}$  is time required for the receiver CDR to start recovering valid data after the rx\_is\_lockedtodata signal goes high.
- (13)  $t_{LTD\_manual}$  is the time required for the receiver CDR to start recovering valid data after the rx\_is\_lockedtodata signal goes high when the CDR is functioning in the manual mode.
- (14)  $t_{LTR\_LTD\_manual}$  is the time the receiver CDR must be kept in lock to reference (LTR) mode after the rx\_is\_lockedtoref signal goes high when the CDR is functioning in the manual mode.
- (15)  $t_{pll\_powerdown}$  is the PLL powerdown minimum pulse width.
- (16)  $t_{pll\_lock}$  is the time required for the transmitter CMU/ATX PLL to lock to the input reference clock frequency after coming out of reset.
- (17) To calculate the REFCLK rms phase jitter requirement for PCIe at reference clock frequencies other than 100 MHz, use the following formula: REFCLK rms phase jitter at f(MHz) = REFCLK rms phase jitter at 100 MHz  $\times$  100/f.
- (18) The maximum peak to peak differential input voltage  $V_{ID}$  after device configuration is equal to  $4 \times (\text{absolute } V_{MAX} \text{ for receiver pin} - V_{ICM})$ .
- (19) For ES devices,  $R_{REF}$  is  $2000 \Omega \pm 1\%$ .
- (20) To calculate the REFCLK phase noise requirement at frequencies other than 622 MHz, use the following formula: REFCLK phase noise at f(MHz) = REFCLK phase noise at 622 MHz +  $20 \times \log(f/622)$ .
- (21) SFP/+ optical modules require the host interface to have RD+/- differentially terminated with  $100 \Omega$ . The internal OCT feature is available after the Stratix V FPGA configuration is completed. Altera recommends that FPGA configuration is completed before inserting the optical module. Otherwise, minimize unnecessary removal and insertion with unconfigured devices.
- (22) Refer to Figure 2.
- (23) For oversampling designs to support data rates less than the minimum specification, the CDR needs to be in LTR mode only.
- (24) I3YY devices can achieve data rates up to 10.3125 Gbps.
- (25) When you use fPLL as a TXPLL of the transceiver.
- (26) REFCLK performance requires to meet transmitter REFCLK phase noise specification.
- (27) Minimum eye opening of 85 mV is only for the unstressed input eye condition.

Table 25 shows the approximate maximum data rate using the standard PCS.

**Table 25. Stratix V Standard PCS Approximate Maximum Date Rate <sup>(1)</sup>, <sup>(3)</sup>**

| Mode <sup>(2)</sup> | Transceiver Speed Grade | PMA Width                             | 20      | 20      | 16      | 16      | 10  | 10  | 8    | 8    |
|---------------------|-------------------------|---------------------------------------|---------|---------|---------|---------|-----|-----|------|------|
|                     |                         | PCS/Core Width                        | 40      | 20      | 32      | 16      | 20  | 10  | 16   | 8    |
| FIFO                | 1                       | C1, C2, C2L, I2, I2L core speed grade | 12.2    | 11.4    | 9.76    | 9.12    | 6.5 | 5.8 | 5.2  | 4.72 |
|                     | 2                       | C1, C2, C2L, I2, I2L core speed grade | 12.2    | 11.4    | 9.76    | 9.12    | 6.5 | 5.8 | 5.2  | 4.72 |
|                     |                         | C3, I3, I3L core speed grade          | 9.8     | 9.0     | 7.84    | 7.2     | 5.3 | 4.7 | 4.24 | 3.76 |
|                     | 3                       | C1, C2, C2L, I2, I2L core speed grade | 8.5     | 8.5     | 8.5     | 8.5     | 6.5 | 5.8 | 5.2  | 4.72 |
|                     |                         | I3YY core speed grade                 | 10.3125 | 10.3125 | 7.84    | 7.2     | 5.3 | 4.7 | 4.24 | 3.76 |
|                     |                         | C3, I3, I3L core speed grade          | 8.5     | 8.5     | 7.84    | 7.2     | 5.3 | 4.7 | 4.24 | 3.76 |
|                     |                         | C4, I4 core speed grade               | 8.5     | 8.2     | 7.04    | 6.56    | 4.8 | 4.2 | 3.84 | 3.44 |
| Register            | 1                       | C1, C2, C2L, I2, I2L core speed grade | 12.2    | 11.4    | 9.76    | 9.12    | 6.1 | 5.7 | 4.88 | 4.56 |
|                     | 2                       | C1, C2, C2L, I2, I2L core speed grade | 12.2    | 11.4    | 9.76    | 9.12    | 6.1 | 5.7 | 4.88 | 4.56 |
|                     |                         | C3, I3, I3L core speed grade          | 9.8     | 9.0     | 7.92    | 7.2     | 4.9 | 4.5 | 3.96 | 3.6  |
|                     | 3                       | C1, C2, C2L, I2, I2L core speed grade | 10.3125 | 10.3125 | 10.3125 | 10.3125 | 6.1 | 5.7 | 4.88 | 4.56 |
|                     |                         | I3YY core speed grade                 | 10.3125 | 10.3125 | 7.92    | 7.2     | 4.9 | 4.5 | 3.96 | 3.6  |
|                     |                         | C3, I3, I3L core speed grade          | 8.5     | 8.5     | 7.92    | 7.2     | 4.9 | 4.5 | 3.96 | 3.6  |
|                     |                         | C4, I4 core speed grade               | 8.5     | 8.2     | 7.04    | 6.56    | 4.4 | 4.1 | 3.52 | 3.28 |

**Notes to Table 25:**

- (1) The maximum data rate is in Gbps.
- (2) The Phase Compensation FIFO can be configured in FIFO mode or register mode. In the FIFO mode, the pointers are not fixed, and the latency can vary. In the register mode the pointers are fixed for low latency.
- (3) The maximum data rate is also constrained by the transceiver speed grade. Refer to Table 1 for the transceiver speed grade.

Figure 2 shows the differential transmitter output waveform.

**Figure 2. Differential Transmitter Output Waveform**

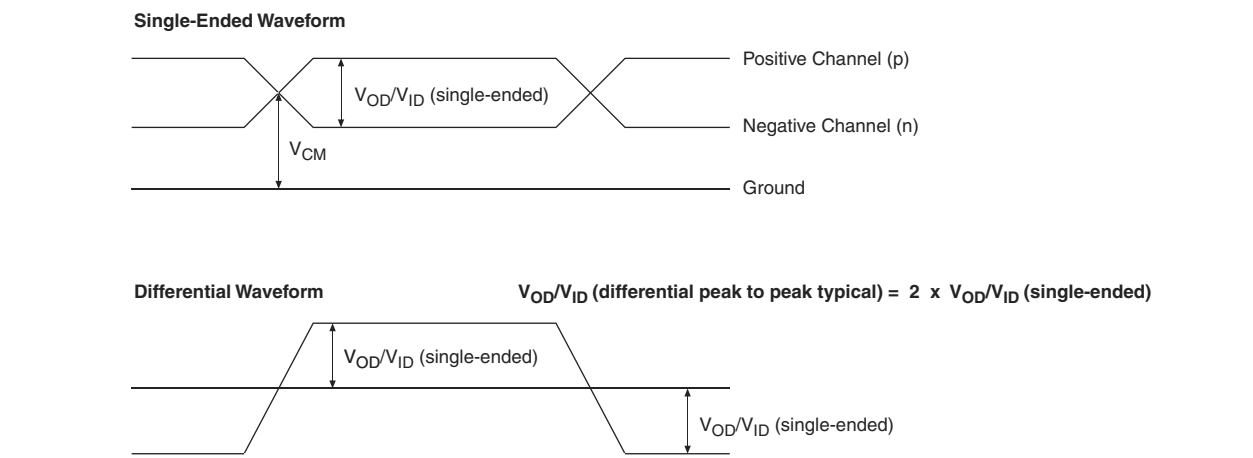


Figure 3 shows the Stratix V AC gain curves for GX channels.

**Figure 3. AC Gain Curves for GX Channels (full bandwidth)**



Stratix V GT devices contain both GX and GT channels. All transceiver specifications for the GX channels not listed in Table 28 are the same as those listed in Table 23.

Table 28 lists the Stratix V GT transceiver specifications.

Table 29 shows the  $V_{OD}$  settings for the GT channel.

**Table 29. Typical  $V_{OD}$  Setting for GT Channel, TX Termination = 100  $\Omega$**

| Symbol  | $V_{OD}$ Setting | $V_{OD}$ Value (mV) |
|---|------------------|---------------------|
| $V_{OD}$ differential peak to peak typical <sup>(1)</sup> | 0                | 0                   |
|   | 1                | 200                 |
|   | 2                | 400                 |
|   | 3                | 600                 |
|   | 4                | 800                 |
|   | 5                | 1000                |

**Note:**

(1) Refer to Figure 4.

- XFI
- ASI
- HiGig/HiGig+
- HiGig2/HiGig2+
- Serial Data Converter (SDC)
- GPON
- SDI
- SONET
- Fibre Channel (FC)
- PCIe
- QPI
- SFF-8431

Download the Stratix V Characterization Report Tool to view the characterization report summary for these protocols.

## Core Performance Specifications

This section describes the clock tree, phase-locked loop (PLL), digital signal processing (DSP), memory blocks, configuration, and JTAG specifications.

### Clock Tree Specifications

Table 30 lists the clock tree specifications for Stratix V devices.

**Table 30. Clock Tree Performance for Stratix V Devices <sup>(1)</sup>**

| Symbol                    | Performance              |                       |        | Unit |
|---------------------------|--------------------------|-----------------------|--------|------|
|                           | C1, C2, C2L, I2, and I2L | C3, I3, I3L, and I3YY | C4, I4 |      |
| Global and Regional Clock | 717                      | 650                   | 580    | MHz  |
| Periphery Clock           | 550                      | 500                   | 500    | MHz  |

**Note to Table 30:**

(1) The Stratix V ES devices are limited to 600 MHz core clock tree performance.

**Table 32. Block Performance Specifications for Stratix V DSP Devices (Part 2 of 2)**

| Mode                   | Peformance |         |         |     |               |     |     | Unit |
|------------------------|------------|---------|---------|-----|---------------|-----|-----|------|
|                        | C1         | C2, C2L | I2, I2L | C3  | I3, I3L, I3YY | C4  | I4  |      |
| Modes using Three DSPs |            |         |         |     |               |     |     |      |
| One complex 18 x 25    | 425        | 425     | 415     | 340 | 340           | 275 | 265 | MHz  |
| Modes using Four DSPs  |            |         |         |     |               |     |     |      |
| One complex 27 x 27    | 465        | 465     | 465     | 380 | 380           | 300 | 290 | MHz  |

### Memory Block Specifications

Table 33 lists the Stratix V memory block specifications.

**Table 33. Memory Block Performance Specifications for Stratix V Devices <sup>(1)</sup>, <sup>(2)</sup> (Part 1 of 2)**

| Memory | Mode                                       | Resources Used |        | Performance |         |     |     |         |               |     | Unit |
|--------|--|----------------|--------|-------------|---------|-----|-----|---------|---------------|-----|------|
|        |  | ALUTs          | Memory | C1          | C2, C2L | C3  | C4  | I2, I2L | I3, I3L, I3YY | I4  |      |
| MLAB   | Single port, all supported widths          | 0              | 1      | 450         | 450     | 400 | 315 | 450     | 400           | 315 | MHz  |
|        | Simple dual-port, x32/x64 depth            | 0              | 1      | 450         | 450     | 400 | 315 | 450     | 400           | 315 | MHz  |
|        | Simple dual-port, x16 depth <sup>(3)</sup> | 0              | 1      | 675         | 675     | 533 | 400 | 675     | 533           | 400 | MHz  |
|        | ROM, all supported widths                  | 0              | 1      | 600         | 600     | 500 | 450 | 600     | 500           | 450 | MHz  |

**Table 36. High-Speed I/O Specifications for Stratix V Devices <sup>(1), (2)</sup> (Part 2 of 4)**

| Symbol   | Conditions  | C1  |     |      | C2, C2L, I2, I2L |     |      | C3, I3, I3L, I3YY |     |      | C4,I4 |     |      | Unit |
|--|---|-----|-----|------|------------------|-----|------|-------------------|-----|------|-------|-----|------|------|
|  |   | Min | Typ | Max  | Min              | Typ | Max  | Min               | Typ | Max  | Min   | Typ | Max  |      |
| Transmitter  |   |     |     |      |                  |     |      |                   |     |      |       |     |      |      |
| True Differential I/O Standards - f <sub>HSDR</sub> (data rate)  | SERDES factor J = 3 to 10 <sup>(9), (11), (12), (13), (14), (15), (16)</sup>  | (6) | —   | 1600 | (6)              | —   | 1434 | (6)               | —   | 1250 | (6)   | —   | 1050 | Mbps |
|  | SERDES factor J ≥ 4<br><br>LVDS TX with DPA <sup>(12), (14), (15), (16)</sup> | (6) | —   | 1600 | (6)              | —   | 1600 | (6)               | —   | 1600 | (6)   | —   | 1250 | Mbps |
|  | SERDES factor J = 2,<br>uses DDR Registers                                    | (6) | —   | (7)  | (6)              | —   | (7)  | (6)               | —   | (7)  | (6)   | —   | (7)  | Mbps |
|  | SERDES factor J = 1,<br>uses SDR Register                                     | (6) | —   | (7)  | (6)              | —   | (7)  | (6)               | —   | (7)  | (6)   | —   | (7)  | Mbps |
| Emulated Differential I/O Standards with Three External Output Resistor Networks - f <sub>HSDR</sub> (data rate) <sup>(10)</sup> | SERDES factor J = 4 to 10 <sup>(17)</sup>                                     | (6) | —   | 1100 | (6)              | —   | 1100 | (6)               | —   | 840  | (6)   | —   | 840  | Mbps |
| t <sub>x Jitter</sub> - True Differential I/O Standards  | Total Jitter for Data Rate 600 Mbps - 1.25 Gbps                               | —   | —   | 160  | —                | —   | 160  | —                 | —   | 160  | —     | —   | 160  | ps   |
|  | Total Jitter for Data Rate < 600 Mbps   | —   | —   | 0.1  | —                | —   | 0.1  | —                 | —   | 0.1  | —     | —   | 0.1  | UI   |
| t <sub>x Jitter</sub> - Emulated Differential I/O Standards with Three External Output Resistor Network                          | Total Jitter for Data Rate 600 Mbps - 1.25 Gbps                               | —   | —   | 300  | —                | —   | 300  | —                 | —   | 300  | —     | —   | 325  | ps   |
|  | Total Jitter for Data Rate < 600 Mbps   | —   | —   | 0.2  | —                | —   | 0.2  | —                 | —   | 0.2  | —     | —   | 0.25 | UI   |



**Table 46. JTAG Timing Parameters and Values for Stratix V Devices**

| Symbol     | Description                              | Min | Max               | Unit |
|------------|--|-----|-------------------|------|
| $t_{JPH}$  | JTAG port hold time                      | 5   | —                 | ns   |
| $t_{JPCO}$ | JTAG port clock to output                | —   | 11 <sup>(1)</sup> | ns   |
| $t_{JPZX}$ | JTAG port high impedance to valid output | —   | 14 <sup>(1)</sup> | ns   |
| $t_{JPXZ}$ | JTAG port valid output to high impedance | —   | 14 <sup>(1)</sup> | ns   |

**Notes to Table 46:**

- (1) A 1 ns adder is required for each  $V_{CCIO}$  voltage step down from 3.0 V. For example,  $t_{JPCO}$  = 12 ns if  $V_{CCIO}$  of the TDO I/O bank = 2.5 V, or 13 ns if it equals 1.8 V.
- (2) The minimum TCK clock period is 167 ns if VCCBAT is within the range 1.2V-1.5V when you perform the volatile key programming.

## Raw Binary File Size

For the POR delay specification, refer to the “POR Delay Specification” section of the “Configuration, Design Security, and Remote System Upgrades in Stratix V Devices”.

Table 47 lists the uncompressed raw binary file (.rbf) sizes for Stratix V devices.

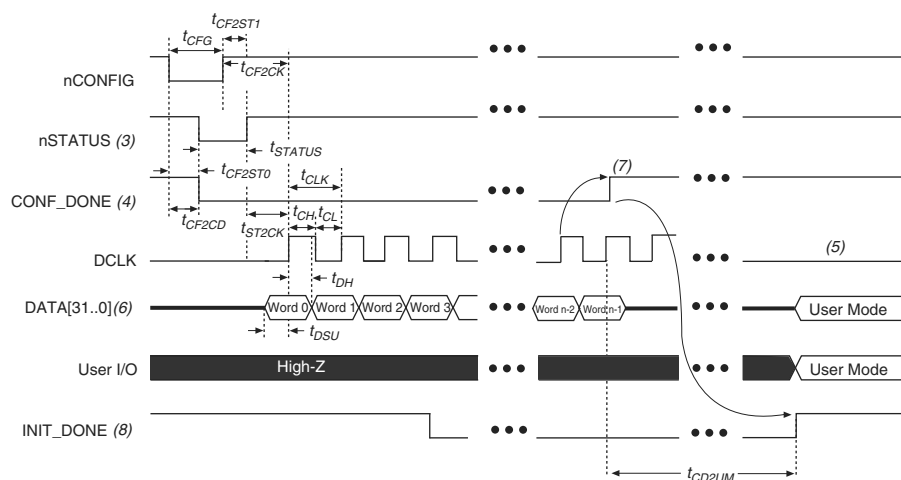
**Table 47. Uncompressed .rbf Sizes for Stratix V Devices**

| Family       | Device | Package                      | Configuration .rbf Size (bits) | IOCSR .rbf Size (bits) <sup>(4), (5)</sup> |
|--------------|--------|------------------------------|--------------------------------|--|
| Stratix V GX | 5SGXA3 | H35, F40, F35 <sup>(2)</sup> | 213,798,880                    | 562,392                                    |
|              |        | H29, F35 <sup>(3)</sup>      | 137,598,880                    | 564,504                                    |
|              | 5SGXA4 | —                            | 213,798,880                    | 563,672                                    |
|              | 5SGXA5 | —                            | 269,979,008                    | 562,392                                    |
|              | 5SGXA7 | —                            | 269,979,008                    | 562,392                                    |
|              | 5SGXA9 | —                            | 342,742,976                    | 700,888                                    |
|              | 5SGXAB | —                            | 342,742,976                    | 700,888                                    |
|              | 5SGXB5 | —                            | 270,528,640                    | 584,344                                    |
|              | 5SGXB6 | —                            | 270,528,640                    | 584,344                                    |
|              | 5SGXB9 | —                            | 342,742,976                    | 700,888                                    |
|              | 5SGXBB | —                            | 342,742,976                    | 700,888                                    |
| Stratix V GT | 5SGTC5 | —                            | 269,979,008                    | 562,392                                    |
|              | 5SGTC7 | —                            | 269,979,008                    | 562,392                                    |
| Stratix V GS | 5SGSD3 | —                            | 137,598,880                    | 564,504                                    |
|              | 5SGSD4 | F1517                        | 213,798,880                    | 563,672                                    |
|              |        | —                            | 137,598,880                    | 564,504                                    |
|              | 5SGSD5 | —                            | 213,798,880                    | 563,672                                    |
|              | 5SGSD6 | —                            | 293,441,888                    | 565,528                                    |
|              | 5SGSD8 | —                            | 293,441,888                    | 565,528                                    |

## FPP Configuration Timing when DCLK-to-DATA [] = 1

Figure 12 shows the timing waveform for FPP configuration when using a MAX II or MAX V device as an external host. This waveform shows timing when the DCLK-to-DATA [] ratio is 1.

**Figure 12. FPP Configuration Timing Waveform When the DCLK-to-DATA[] Ratio is 1 <sup>(1), (2)</sup>**



### Notes to Figure 12:

- (1) Use this timing waveform when the DCLK-to-DATA [] ratio is 1.
- (2) The beginning of this waveform shows the device in user mode. In user mode, nCONFIG, nSTATUS, and CONF\_DONE are at logic-high levels. When nCONFIG is pulled low, a reconfiguration cycle begins.
- (3) After power-up, the Stratix V device holds nSTATUS low for the time of the POR delay.
- (4) After power-up, before and during configuration, CONF\_DONE is low.
- (5) Do not leave DCLK floating after configuration. DCLK is ignored after configuration is complete. It can toggle high or low if required.
- (6) For FPP  $\times 16$ , use DATA [15..0]. For FPP  $\times 8$ , use DATA [7..0]. DATA [31..0] are available as a user I/O pin after configuration. The state of this pin depends on the dual-purpose pin settings.
- (7) To ensure a successful configuration, send the entire configuration data to the Stratix V device. CONF\_DONE is released high when the Stratix V device receives all the configuration data successfully. After CONF\_DONE goes high, send two additional falling edges on DCLK to begin initialization and enter user mode.
- (8) After the option bit to enable the INIT\_DONE pin is configured into the device, the INIT\_DONE goes low.

Table 51 lists the timing parameters for Stratix V devices for FPP configuration when the DCLK-to-DATA [ ] ratio is more than 1.

**Table 51. FPP Timing Parameters for Stratix V Devices When the DCLK-to-DATA[ ] Ratio is >1 <sup>(1)</sup>**

| Symbol                     | Parameter   | Minimum   | Maximum              | Units   |
|----------------------------|---|---|----------------------|---------|
| $t_{CF2CD}$                | nCONFIG low to CONF_DONE low                      | —   | 600                  | ns      |
| $t_{CF2ST0}$               | nCONFIG low to nSTATUS low                        | —   | 600                  | ns      |
| $t_{CFG}$                  | nCONFIG low pulse width                           | 2   | —                    | $\mu$ s |
| $t_{STATUS}$               | nSTATUS low pulse width                           | 268   | 1,506 <sup>(2)</sup> | $\mu$ s |
| $t_{CF2ST1}$               | nCONFIG high to nSTATUS high                      | —   | 1,506 <sup>(2)</sup> | $\mu$ s |
| $t_{CF2CK}$ <sup>(5)</sup> | nCONFIG high to first rising edge on DCLK         | 1,506   | —                    | $\mu$ s |
| $t_{ST2CK}$ <sup>(5)</sup> | nSTATUS high to first rising edge of DCLK         | 2   | —                    | $\mu$ s |
| $t_{DSU}$                  | DATA [ ] setup time before rising edge on DCLK    | 5.5   | —                    | ns      |
| $t_{DH}$                   | DATA [ ] hold time after rising edge on DCLK      | $N-1/f_{DCLK}$ <sup>(5)</sup>                                   | —                    | s       |
| $t_{CH}$                   | DCLK high time                                    | $0.45 \times 1/f_{MAX}$   | —                    | s       |
| $t_{CL}$                   | DCLK low time                                     | $0.45 \times 1/f_{MAX}$   | —                    | s       |
| $t_{CLK}$                  | DCLK period                                       | $1/f_{MAX}$   | —                    | s       |
| $f_{MAX}$                  | DCLK frequency (FPP $\times 8/\times 16$ )        | —   | 125                  | MHz     |
|                            | DCLK frequency (FPP $\times 32$ )                 | —   | 100                  | MHz     |
| $t_R$                      | Input rise time                                   | —   | 40                   | ns      |
| $t_F$                      | Input fall time                                   | —   | 40                   | ns      |
| $t_{CD2UM}$                | CONF_DONE high to user mode <sup>(3)</sup>        | 175   | 437                  | $\mu$ s |
| $t_{CD2CU}$                | CONF_DONE high to CLKUSR enabled                  | $4 \times$ maximum DCLK period                                  | —                    | —       |
| $t_{CD2UMC}$               | CONF_DONE high to user mode with CLKUSR option on | $t_{CD2CU} + (8576 \times \text{CLKUSR period})$ <sup>(4)</sup> | —                    | —       |

**Notes to Table 51:**

- (1) Use these timing parameters when you use the decompression and design security features.
- (2) You can obtain this value if you do not delay configuration by extending the nCONFIG or nSTATUS low pulse width.
- (3) The minimum and maximum numbers apply only if you use the internal oscillator as the clock source for initializing the device.
- (4) To enable the CLKUSR pin as the initialization clock source and to obtain the maximum frequency specification on these pins, refer to the Initialization section of the “Configuration, Design Security, and Remote System Upgrades in Stratix V Devices” chapter.
- (5) N is the DCLK-to-DATA ratio and  $f_{DCLK}$  is the DCLK frequency the system is operating.
- (6) If nSTATUS is monitored, follow the  $t_{ST2CK}$  specification. If nSTATUS is not monitored, follow the  $t_{CF2CK}$  specification.

**Table 58. IOE Programmable Delay for Stratix V Devices (Part 2 of 2)**

| Parameter<br>(1) | Available<br>Settings | Min<br>Offset<br>(2) | Fast Model |            | Slow Model |       |       |       |       |             |       |      |
|------------------|-----------------------|----------------------|------------|------------|------------|-------|-------|-------|-------|-------------|-------|------|
|                  |                       |                      | Industrial | Commercial | C1         | C2    | C3    | C4    | I2    | I3,<br>I3YY | I4    | Unit |
| D3               | 8                     | 0                    | 1.587      | 1.699      | 2.793      | 2.793 | 2.992 | 3.192 | 2.811 | 3.047       | 3.257 | ns   |
| D4               | 64                    | 0                    | 0.464      | 0.492      | 0.838      | 0.838 | 0.924 | 1.011 | 0.843 | 0.920       | 1.006 | ns   |
| D5               | 64                    | 0                    | 0.464      | 0.493      | 0.838      | 0.838 | 0.924 | 1.011 | 0.844 | 0.921       | 1.006 | ns   |
| D6               | 32                    | 0                    | 0.229      | 0.244      | 0.415      | 0.415 | 0.458 | 0.503 | 0.418 | 0.456       | 0.499 | ns   |

**Notes to Table 58:**

- (1) You can set this value in the Quartus II software by selecting **D1**, **D2**, **D3**, **D5**, and **D6** in the **Assignment Name** column of **Assignment Editor**.
- (2) Minimum offset does not include the intrinsic delay.

## Programmable Output Buffer Delay

Table 59 lists the delay chain settings that control the rising and falling edge delays of the output buffer. The default delay is 0 ps.

**Table 59. Programmable Output Buffer Delay for Stratix V Devices (1)**

| Symbol              | Parameter                        | Typical     | Unit |
|---------------------|----------------------------------|-------------|------|
| D <sub>OUTBUF</sub> | Rising and/or falling edge delay | 0 (default) | ps   |
|                     |                                  | 25          | ps   |
|                     |                                  | 50          | ps   |
|                     |                                  | 75          | ps   |

**Note to Table 59:**

- (1) You can set the programmable output buffer delay in the Quartus II software by setting the **Output Buffer Delay Control** assignment to either positive, negative, or both edges, with the specific values stated here (in ps) for the **Output Buffer Delay** assignment.

## Glossary

Table 60 lists the glossary for this chapter.

**Table 60. Glossary (Part 1 of 4)**

| Letter | Subject              | Definitions   |
|--------|----------------------|---|
| A      | —                    | —   |
| B      |                      |   |
| C      |                      |   |
| D      | —                    | —   |
| E      | —                    | —   |
| F      | f <sub>HCLK</sub>    | Left and right PLL input clock frequency.   |
|        | f <sub>HSDR</sub>    | High-speed I/O block—Maximum and minimum <b>LVDS</b> data transfer rate (f <sub>HSDR</sub> = 1/TUI), non-DPA. |
|        | f <sub>HSDRDPA</sub> | High-speed I/O block—Maximum and minimum <b>LVDS</b> data transfer rate (f <sub>HSDRDPA</sub> = 1/TUI), DPA.  |

**Table 60. Glossary (Part 2 of 4)**

| Letter                | Subject                    | Definitions  |
|-----------------------|----------------------------|--|
| G<br>H<br>I           | —                          | —  |
| J                     | JTAG Timing Specifications | <p>High-speed I/O block—Deserialization factor (width of parallel data bus).</p> <p>JTAG Timing Specifications:</p>  |
| K<br>L<br>M<br>N<br>O | —                          | —  |
| P                     | PLL Specifications         | <p><b>Diagram of PLL Specifications</b> <sup>(1)</sup></p> <p><b>Note:</b></p> <p>(1) Core Clock can only be fed by dedicated clock input pins or PLL outputs.</p> |
| Q                     | —                          | —  |
| R                     | R <sub>L</sub>             | Receiver differential input discrete resistor (external to the Stratix V device).  |