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### Understanding [Embedded - FPGAs \(Field Programmable Gate Array\)](#)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

### Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

#### Details

Product Status	Obsolete
Number of LABs/CLBs	185000
Number of Logic Elements/Cells	490000
Total RAM Bits	46080000
Number of I/O	432
Number of Gates	-
Voltage - Supply	0.82V ~ 0.88V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	1152-BBGA, FCBGA
Supplier Device Package	1152-FBGA (35x35)
Purchase URL	<a href="https://www.e-xfl.com/product-detail/intel/5sgxea5k2f35i3ln">https://www.e-xfl.com/product-detail/intel/5sgxea5k2f35i3ln</a>

Table 5 lists the maximum allowed input overshoot voltage and the duration of the overshoot voltage as a percentage of device lifetime. The maximum allowed overshoot duration is specified as a percentage of high time over the lifetime of the device. A DC signal is equivalent to 100% of the duty cycle. For example, a signal that overshoots to 3.95 V can be at 3.95 V for only ~21% over the lifetime of the device; for a device lifetime of 10 years, the overshoot duration amounts to ~2 years.

**Table 5. Maximum Allowed Overshoot During Transitions**

Symbol	Description	Condition (V)	Overshoot Duration as % @ $T_J = 100^\circ\text{C}$	Unit
$V_i$ (AC)	AC input voltage	3.8	100	%
		3.85	64	%
		3.9	36	%
		3.95	21	%
		4	12	%
		4.05	7	%
		4.1	4	%
		4.15	2	%
		4.2	1	%

**Figure 1. Stratix V Device Overshoot Duration**



**Table 7. Recommended Transceiver Power Supply Operating Conditions for Stratix V GX, GS, and GT Devices (Part 2 of 2)**

Symbol	Description	Devices	Minimum <sup>(4)</sup>	Typical	Maximum <sup>(4)</sup>	Unit
$V_{CCR\_GXBR}$ (2)	Receiver analog power supply (right side)	GX, GS, GT	0.82	0.85	0.88	V
			0.87	0.90	0.93	
			0.97	1.0	1.03	
			1.03	1.05	1.07	
$V_{CCR\_GTBR}$	Receiver analog power supply for GT channels (right side)	GT	1.02	1.05	1.08	V
$V_{CCT\_GXBL}$ (2)	Transmitter analog power supply (left side)	GX, GS, GT	0.82	0.85	0.88	V
			0.87	0.90	0.93	
			0.97	1.0	1.03	
			1.03	1.05	1.07	
$V_{CCT\_GXBR}$ (2)	Transmitter analog power supply (right side)	GX, GS, GT	0.82	0.85	0.88	V
			0.87	0.90	0.93	
			0.97	1.0	1.03	
			1.03	1.05	1.07	
$V_{CCT\_GTBR}$	Transmitter analog power supply for GT channels (right side)	GT	1.02	1.05	1.08	V
$V_{CCL\_GTBR}$	Transmitter clock network power supply	GT	1.02	1.05	1.08	V
$V_{CCH\_GXBL}$	Transmitter output buffer power supply (left side)	GX, GS, GT	1.425	1.5	1.575	V
$V_{CCH\_GXBR}$	Transmitter output buffer power supply (right side)	GX, GS, GT	1.425	1.5	1.575	V

**Notes to Table 7:**

- (1) This supply must be connected to 3.0 V if the CMU PLL, receiver CDR, or both, are configured at a base data rate > 6.5 Gbps. Up to 6.5 Gbps, you can connect this supply to either 3.0 V or 2.5 V.
- (2) Refer to Table 8 to select the correct power supply level for your design.
- (3) When using ATX PLLs, the supply must be 3.0 V.
- (4) This value describes the budget for the DC (static) power supply tolerance and does not include the dynamic tolerance requirements. Refer to the PDN tool for the additional budget for the dynamic tolerance requirements.

**Table 11. OCT Calibration Accuracy Specifications for Stratix V Devices <sup>(1)</sup> (Part 2 of 2)**

Symbol	Description	Conditions	Calibration Accuracy				Unit
			C1	C2,I2	C3,I3,I3YY	C4,I4	
50-Ω R <sub>S</sub>	Internal series termination with calibration (50-Ω setting)	V <sub>CCIO</sub> = 3.0, 2.5, 1.8, 1.5, 1.2 V	±15	±15	±15	±15	%
34-Ω and 40-Ω R <sub>S</sub>	Internal series termination with calibration (34-Ω and 40-Ω setting)	V <sub>CCIO</sub> = 1.5, 1.35, 1.25, 1.2 V	±15	±15	±15	±15	%
48-Ω, 60-Ω, 80-Ω, and 240-Ω R <sub>S</sub>	Internal series termination with calibration (48-Ω, 60-Ω, 80-Ω, and 240-Ω setting)	V <sub>CCIO</sub> = 1.2 V	±15	±15	±15	±15	%
50-Ω R <sub>T</sub>	Internal parallel termination with calibration (50-Ω setting)	V <sub>CCIO</sub> = 2.5, 1.8, 1.5, 1.2 V	-10 to +40	-10 to +40	-10 to +40	-10 to +40	%
20-Ω, 30-Ω, 40-Ω, 60-Ω, and 120-Ω R <sub>T</sub>	Internal parallel termination with calibration (20-Ω, 30-Ω, 40-Ω, 60-Ω, and 120-Ω setting)	V <sub>CCIO</sub> = 1.5, 1.35, 1.25 V	-10 to +40	-10 to +40	-10 to +40	-10 to +40	%
60-Ω and 120-Ω R <sub>T</sub>	Internal parallel termination with calibration (60-Ω and 120-Ω setting)	V <sub>CCIO</sub> = 1.2	-10 to +40	-10 to +40	-10 to +40	-10 to +40	%
25-Ω R <sub>S_left_shift</sub>	Internal left shift series termination with calibration (25-Ω R <sub>S_left_shift</sub> setting)	V <sub>CCIO</sub> = 3.0, 2.5, 1.8, 1.5, 1.2 V	±15	±15	±15	±15	%

**Note to Table 11:**

(1) OCT calibration accuracy is valid at the time of calibration only.

Table 12 lists the Stratix V OCT without calibration resistance tolerance to PVT changes.

**Table 12. OCT Without Calibration Resistance Tolerance Specifications for Stratix V Devices (Part 1 of 2)**

Symbol	Description	Conditions	Resistance Tolerance				Unit
			C1	C2,I2	C3, I3, I3YY	C4, I4	
25-Ω R, 50-Ω R <sub>S</sub>	Internal series termination without calibration (25-Ω setting)	V <sub>CCIO</sub> = 3.0 and 2.5 V	±30	±30	±40	±40	%
25-Ω R <sub>S</sub>	Internal series termination without calibration (25-Ω setting)	V <sub>CCIO</sub> = 1.8 and 1.5 V	±30	±30	±40	±40	%
25-Ω R <sub>S</sub>	Internal series termination without calibration (25-Ω setting)	V <sub>CCIO</sub> = 1.2 V	±35	±35	±50	±50	%

**Table 23. Transceiver Specifications for Stratix V GX and GS Devices <sup>(1)</sup> (Part 2 of 7)**

Symbol/ Description	Conditions	Transceiver Speed Grade 1			Transceiver Speed Grade 2			Transceiver Speed Grade 3			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Spread-spectrum downspread	PCIe	—	0 to -0.5	—	—	0 to -0.5	—	—	0 to -0.5	—	%
On-chip termination resistors <sup>(21)</sup>	—	—	100	—	—	100	—	—	100	—	$\Omega$
Absolute $V_{MAX}$ <sup>(5)</sup>	Dedicated reference clock pin	—	—	1.6	—	—	1.6	—	—	1.6	V
	RX reference clock pin	—	—	1.2	—	—	1.2	—	—	1.2	
Absolute $V_{MIN}$	—	-0.4	—	—	-0.4	—	—	-0.4	—	—	V
Peak-to-peak differential input voltage	—	200	—	1600	200	—	1600	200	—	1600	mV
$V_{ICM}$ (AC coupled) <sup>(3)</sup>	Dedicated reference clock pin	1050/1000/900/850 <sup>(2)</sup>			1050/1000/900/850 <sup>(2)</sup>			1050/1000/900/850 <sup>(2)</sup>			mV
	RX reference clock pin	1.0/0.9/0.85 <sup>(4)</sup>			1.0/0.9/0.85 <sup>(4)</sup>			1.0/0.9/0.85 <sup>(4)</sup>			V
$V_{ICM}$ (DC coupled)	HCSL I/O standard for PCIe reference clock	250	—	550	250	—	550	250	—	550	mV
Transmitter REFCLK Phase Noise (622 MHz) <sup>(20)</sup>	100 Hz	—	—	-70	—	—	-70	—	—	-70	dBc/Hz
	1 kHz	—	—	-90	—	—	-90	—	—	-90	dBc/Hz
	10 kHz	—	—	-100	—	—	-100	—	—	-100	dBc/Hz
	100 kHz	—	—	-110	—	—	-110	—	—	-110	dBc/Hz
	$\geq 1$ MHz	—	—	-120	—	—	-120	—	—	-120	dBc/Hz
Transmitter REFCLK Phase Jitter (100 MHz) <sup>(17)</sup>	10 kHz to 1.5 MHz (PCIe)	—	—	3	—	—	3	—	—	3	ps (rms)
$R_{REF}$ <sup>(19)</sup>	—	—	1800 $\pm 1\%$	—	—	1800 $\pm 1\%$	—	—	1800 $\pm 1\%$	—	$\Omega$
<b>Transceiver Clocks</b>											
fixedclk clock frequency	PCIe Receiver Detect	—	100 or 125	—	—	100 or 125	—	—	100 or 125	—	MHz

**Table 23. Transceiver Specifications for Stratix V GX and GS Devices <sup>(1)</sup> (Part 3 of 7)**

Symbol/ Description	Conditions	Transceiver Speed Grade 1			Transceiver Speed Grade 2			Transceiver Speed Grade 3			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Reconfiguration clock ( <code>mgmt_clk_clk</code> ) frequency	—	100	—	125	100	—	125	100	—	125	MHz
<b>Receiver</b>											
Supported I/O Standards	—	1.4-V PCML, 1.5-V PCML, 2.5-V PCML, LVPECL, and LVDS									
Data rate (Standard PCS) (9), (23)	—	600	—	12200	600	—	12200	600	—	8500/ 10312.5 (24)	Mbps
Data rate (10G PCS) (9), (23)	—	600	—	14100	600	—	12500	600	—	8500/ 10312.5 (24)	Mbps
Absolute $V_{MAX}$ for a receiver pin <sup>(5)</sup>	—	—	—	1.2	—	—	1.2	—	—	1.2	V
Absolute $V_{MIN}$ for a receiver pin	—	−0.4	—	—	−0.4	—	—	−0.4	—	—	V
Maximum peak- to-peak differential input voltage $V_{ID}$ (diff p- p) before device configuration <sup>(22)</sup>	—	—	—	1.6	—	—	1.6	—	—	1.6	V
Maximum peak- to-peak differential input voltage $V_{ID}$ (diff p- p) after device configuration <sup>(18)</sup> , (22)	$V_{CCR\_GXB} =$ 1.0 V/1.05 V ( $V_{ICM} =$ 0.70 V)	—	—	2.0	—	—	2.0	—	—	2.0	V
	$V_{CCR\_GXB} =$ 0.90 V ( $V_{ICM} = 0.6$ V)	—	—	2.4	—	—	2.4	—	—	2.4	V
	$V_{CCR\_GXB} =$ 0.85 V ( $V_{ICM} = 0.6$ V)	—	—	2.4	—	—	2.4	—	—	2.4	V
Minimum differential eye opening at receiver serial input pins <sup>(6)</sup> , (22), (27)	—	85	—	—	85	—	—	85	—	—	mV

**Table 23. Transceiver Specifications for Stratix V GX and GS Devices <sup>(1)</sup> (Part 4 of 7)**

Symbol/ Description	Conditions	Transceiver Speed Grade 1			Transceiver Speed Grade 2			Transceiver Speed Grade 3			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Differential on-chip termination resistors <sup>(21)</sup>	85- $\Omega$ setting	—	85 $\pm$ 30%	—	—	85 $\pm$ 30%	—	—	85 $\pm$ 30%	—	$\Omega$
	100- $\Omega$ setting	—	100 $\pm$ 30%	—	—	100 $\pm$ 30%	—	—	100 $\pm$ 30%	—	$\Omega$
	120- $\Omega$ setting	—	120 $\pm$ 30%	—	—	120 $\pm$ 30%	—	—	120 $\pm$ 30%	—	$\Omega$
	150- $\Omega$ setting	—	150 $\pm$ 30%	—	—	150 $\pm$ 30%	—	—	150 $\pm$ 30%	—	$\Omega$
$V_{ICM}$ (AC and DC coupled)	$V_{CCR\_GXB} = 0.85\text{ V}$ or 0.9 V full bandwidth	—	600	—	—	600	—	—	600	—	mV
	$V_{CCR\_GXB} = 0.85\text{ V}$ or 0.9 V half bandwidth	—	600	—	—	600	—	—	600	—	mV
	$V_{CCR\_GXB} = 1.0\text{ V}/1.05\text{ V}$ full bandwidth	—	700	—	—	700	—	—	700	—	mV
	$V_{CCR\_GXB} = 1.0\text{ V}$ half bandwidth	—	750	—	—	750	—	—	750	—	mV
$t_{LTR}$ <sup>(11)</sup>	—	—	—	10	—	—	10	—	—	10	$\mu\text{s}$
$t_{LTD}$ <sup>(12)</sup>	—	4	—	—	4	—	—	4	—	—	$\mu\text{s}$
$t_{LTD\_manual}$ <sup>(13)</sup>	—	4	—	—	4	—	—	4	—	—	$\mu\text{s}$
$t_{LTR\_LTD\_manual}$ <sup>(14)</sup>	—	15	—	—	15	—	—	15	—	—	$\mu\text{s}$
Run Length	—	—	—	200	—	—	200	—	—	200	UI
Programmable equalization (AC Gain) <sup>(10)</sup>	Full bandwidth (6.25 GHz) Half bandwidth (3.125 GHz)	—	—	16	—	—	16	—	—	16	dB

Table 25 shows the approximate maximum data rate using the standard PCS.

**Table 25. Stratix V Standard PCS Approximate Maximum Date Rate <sup>(1)</sup>, <sup>(3)</sup>**

Mode <sup>(2)</sup>	Transceiver Speed Grade	PMA Width	20	20	16	16	10	10	8	8
		PCS/Core Width	40	20	32	16	20	10	16	8
FIFO	1	C1, C2, C2L, I2, I2L core speed grade	12.2	11.4	9.76	9.12	6.5	5.8	5.2	4.72
	2	C1, C2, C2L, I2, I2L core speed grade	12.2	11.4	9.76	9.12	6.5	5.8	5.2	4.72
		C3, I3, I3L core speed grade	9.8	9.0	7.84	7.2	5.3	4.7	4.24	3.76
	3	C1, C2, C2L, I2, I2L core speed grade	8.5	8.5	8.5	8.5	6.5	5.8	5.2	4.72
		I3YY core speed grade	10.3125	10.3125	7.84	7.2	5.3	4.7	4.24	3.76
		C3, I3, I3L core speed grade	8.5	8.5	7.84	7.2	5.3	4.7	4.24	3.76
		C4, I4 core speed grade	8.5	8.2	7.04	6.56	4.8	4.2	3.84	3.44
Register	1	C1, C2, C2L, I2, I2L core speed grade	12.2	11.4	9.76	9.12	6.1	5.7	4.88	4.56
	2	C1, C2, C2L, I2, I2L core speed grade	12.2	11.4	9.76	9.12	6.1	5.7	4.88	4.56
		C3, I3, I3L core speed grade	9.8	9.0	7.92	7.2	4.9	4.5	3.96	3.6
	3	C1, C2, C2L, I2, I2L core speed grade	10.3125	10.3125	10.3125	10.3125	6.1	5.7	4.88	4.56
		I3YY core speed grade	10.3125	10.3125	7.92	7.2	4.9	4.5	3.96	3.6
		C3, I3, I3L core speed grade	8.5	8.5	7.92	7.2	4.9	4.5	3.96	3.6
		C4, I4 core speed grade	8.5	8.2	7.04	6.56	4.4	4.1	3.52	3.28

**Notes to Table 25:**

- (1) The maximum data rate is in Gbps.
- (2) The Phase Compensation FIFO can be configured in FIFO mode or register mode. In the FIFO mode, the pointers are not fixed, and the latency can vary. In the register mode the pointers are fixed for low latency.
- (3) The maximum data rate is also constrained by the transceiver speed grade. Refer to Table 1 for the transceiver speed grade.



Figure 2 shows the differential transmitter output waveform.

**Figure 2. Differential Transmitter Output Waveform**

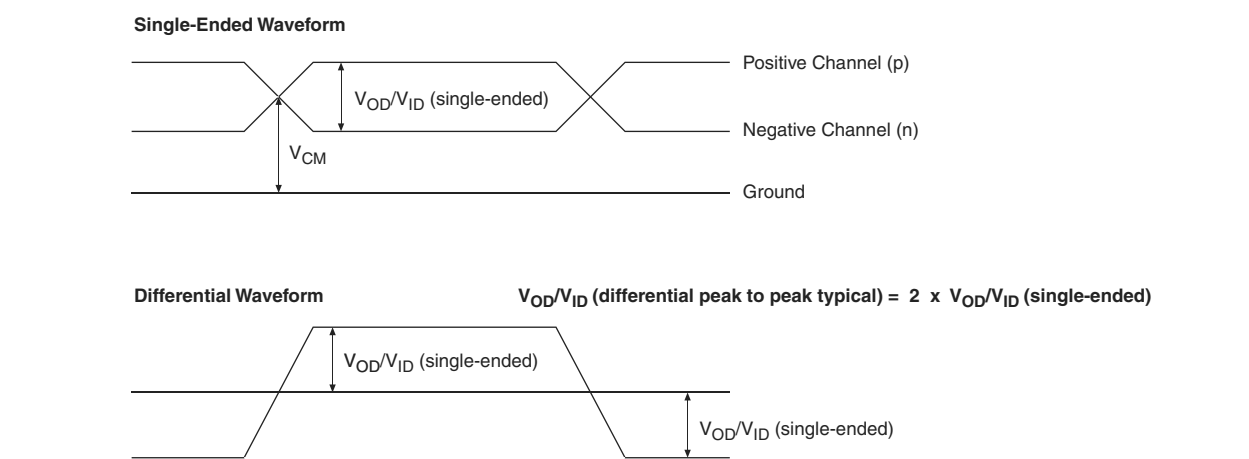


Figure 3 shows the Stratix V AC gain curves for GX channels.

**Figure 3. AC Gain Curves for GX Channels (full bandwidth)**



Stratix V GT devices contain both GX and GT channels. All transceiver specifications for the GX channels not listed in Table 28 are the same as those listed in Table 23.

Table 28 lists the Stratix V GT transceiver specifications.

**Table 28. Transceiver Specifications for Stratix V GT Devices (Part 4 of 5) <sup>(1)</sup>**

Symbol/ Description	Conditions	Transceiver Speed Grade 2			Transceiver Speed Grade 3			Unit
		Min	Typ	Max	Min	Typ	Max	
Data rate	GT channels	19,600	—	28,050	19,600	—	25,780	Mbps
Differential on-chip termination resistors	GT channels	—	100	—	—	100	—	Ω
	GX channels	(8)						
V <sub>OCM</sub> (AC coupled)	GT channels	—	500	—	—	500	—	mV
	GX channels	(8)						
Rise/Fall time	GT channels	—	15	—	—	15	—	ps
	GX channels	(8)						
Intra-differential pair skew	GX channels	(8)						
Intra-transceiver block transmitter channel-to- channel skew	GX channels	(8)						
Inter-transceiver block transmitter channel-to- channel skew	GX channels	(8)						
CMU PLL								
Supported Data Range	—	600	—	12500	600	—	8500	Mbps
t <sub>pll_powerdown</sub> <sup>(13)</sup>	—	1	—	—	1	—	—	μs
t <sub>pll_lock</sub> <sup>(14)</sup>	—	—	—	10	—	—	10	μs
ATX PLL								
Supported Data Rate Range for GX Channels	VCO post- divider L=2	8000	—	12500	8000	—	8500	Mbps
	L=4	4000	—	6600	4000	—	6600	Mbps
	L=8	2000	—	3300	2000	—	3300	Mbps
	L=8, Local/Central Clock Divider =2	1000	—	1762.5	1000	—	1762.5	Mbps
Supported Data Rate Range for GT Channels	VCO post- divider L=2	9800	—	14025	9800	—	12890	Mbps
t <sub>pll_powerdown</sub> <sup>(13)</sup>	—	1	—	—	1	—	—	μs
t <sub>pll_lock</sub> <sup>(14)</sup>	—	—	—	10	—	—	10	μs
fPLL								
Supported Data Range	—	600	—	3250/ 3.125 <sup>(23)</sup>	600	—	3250/ 3.125 <sup>(23)</sup>	Mbps
t <sub>pll_powerdown</sub> <sup>(13)</sup>	—	1	—	—	1	—	—	μs

**Table 36. High-Speed I/O Specifications for Stratix V Devices <sup>(1), (2)</sup> (Part 4 of 4)**

Symbol	Conditions	C1			C2, C2L, I2, I2L			C3, I3, I3L, I3YY			C4, I4			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
f <sub>HSDR</sub> (data rate)	SERDES factor J = 3 to 10	(6)	—	(8)	(6)	—	(8)	(6)	—	(8)	(6)	—	(8)	Mbps
	SERDES factor J = 2, uses DDR Registers	(6)	—	(7)	(6)	—	(7)	(6)	—	(7)	(6)	—	(7)	Mbps
	SERDES factor J = 1, uses SDR Register	(6)	—	(7)	(6)	—	(7)	(6)	—	(7)	(6)	—	(7)	Mbps
<b>DPA Mode</b>														
DPA run length	—	—	—	1000 0	—	—	1000 0	—	—	1000 0	—	—	1000 0	UI
<b>Soft CDR mode</b>														
Soft-CDR PPM tolerance	—	—	—	300	—	—	300	—	—	300	—	—	300	± PPM
<b>Non DPA Mode</b>														
Sampling Window	—	—	—	300	—	—	300	—	—	300	—	—	300	ps

**Notes to Table 36:**

- (1) When J = 3 to 10, use the serializer/deserializer (SERDES) block.
- (2) When J = 1 or 2, bypass the SERDES block.
- (3) This only applies to DPA and soft-CDR modes.
- (4) Clock Boost Factor (W) is the ratio between the input data rate to the input clock rate.
- (5) This is achieved by using the **LVDS** clock network.
- (6) The minimum specification depends on the clock source (for example, the PLL and clock pin) and the clock routing resource (global, regional, or local) that you use. The I/O differential buffer and input register do not have a minimum toggle rate.
- (7) The maximum ideal frequency is the SERDES factor (J) x the PLL maximum output frequency (f<sub>OUT</sub>) provided you can close the design timing and the signal integrity simulation is clean.
- (8) You can estimate the achievable maximum data rate for non-DPA mode by performing link timing closure analysis. You must consider the board skew margin, transmitter delay margin, and receiver sampling margin to determine the maximum data rate supported.
- (9) If the receiver with DPA enabled and transmitter are using shared PLLs, the minimum data rate is 150 Mbps.
- (10) You must calculate the leftover timing margin in the receiver by performing link timing closure analysis. You must consider the board skew margin, transmitter channel-to-channel skew, and receiver sampling margin to determine leftover timing margin.
- (11) The F<sub>MAX</sub> specification is based on the fast clock used for serial data. The interface F<sub>MAX</sub> is also dependent on the parallel clock domain which is design-dependent and requires timing analysis.
- (12) Stratix V RX LVDS will need DPA. For Stratix V TX LVDS, the receiver side component must have DPA.
- (13) Stratix V LVDS serialization and de-serialization factor needs to be x4 and above.
- (14) Requires package skew compensation with PCB trace length.
- (15) Do not mix single-ended I/O buffer within LVDS I/O bank.
- (16) Chip-to-chip communication only with a maximum load of 5 pF.
- (17) When using True LVDS RX channels for emulated LVDS TX channel, only serialization factors 1 and 2 are supported.

**Table 42. Memory Output Clock Jitter Specification for Stratix V Devices <sup>(1)</sup>, (Part 2 of 2) <sup>(2)</sup>, <sup>(3)</sup>**

Clock Network	Parameter	Symbol	C1		C2, C2L, I2, I2L		C3, I3, I3L, I3YY		C4,I4		Unit
			Min	Max	Min	Max	Min	Max	Min	Max	
PHY Clock	Clock period jitter	$t_{JIT(per)}$	-25	25	-25	25	-30	30	-35	35	ps
	Cycle-to-cycle period jitter	$t_{JIT(cc)}$	-50	50	-50	50	-60	60	-70	70	ps
	Duty cycle jitter	$t_{JIT(duty)}$	-37.5	37.5	-37.5	37.5	-45	45	-56	56	ps

**Notes to Table 42:**

- (1) The clock jitter specification applies to the memory output clock pins generated using differential signal-splitter and DDIO circuits clocked by a PLL output routed on a PHY, regional, or global clock network as specified. Altera recommends using PHY clock networks whenever possible.
- (2) The clock jitter specification applies to the memory output clock pins clocked by an integer PLL.
- (3) The memory output clock jitter is applicable when an input jitter of 30 ps peak-to-peak is applied with bit error rate (BER) -12, equivalent to 14 sigma.

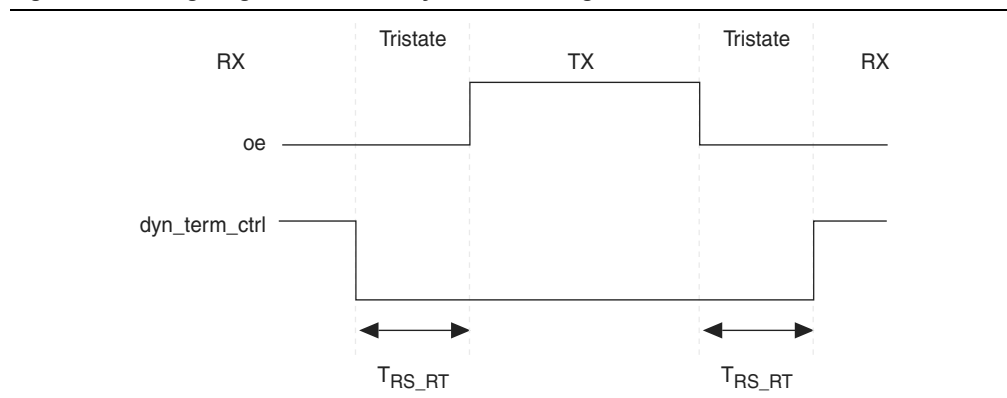
**OCT Calibration Block Specifications**

Table 43 lists the OCT calibration block specifications for Stratix V devices.

**Table 43. OCT Calibration Block Specifications for Stratix V Devices**

Symbol	Description	Min	Typ	Max	Unit
OCTUSRCLK	Clock required by the OCT calibration blocks	—	—	20	MHz
$T_{OCTCAL}$	Number of OCTUSRCLK clock cycles required for OCT $R_S/R_T$ calibration	—	1000	—	Cycles
$T_{OCTSHIFT}$	Number of OCTUSRCLK clock cycles required for the OCT code to shift out	—	32	—	Cycles
$T_{RS\_RT}$	Time required between the <code>dyn_term_ctrl</code> and <code>oe</code> signal transitions in a bidirectional I/O buffer to dynamically switch between OCT $R_S$ and $R_T$ (Figure 10)	—	2.5	—	ns

Figure 10 shows the timing diagram for the `oe` and `dyn_term_ctrl` signals.

**Figure 10. Timing Diagram for `oe` and `dyn_term_ctrl` Signals**

## Duty Cycle Distortion (DCD) Specifications

Table 44 lists the worst-case DCD for Stratix V devices.

**Table 44. Worst-Case DCD on Stratix V I/O Pins <sup>(1)</sup>**

Symbol	C1		C2, C2L, I2, I2L		C3, I3, I3L, I3YY		C4, I4		Unit
	Min	Max	Min	Max	Min	Max	Min	Max	
Output Duty Cycle	45	55	45	55	45	55	45	55	%

**Note to Table 44:**

(1) The DCD numbers do not cover the core clock network.

## Configuration Specification

### POR Delay Specification

Power-on reset (POR) delay is defined as the delay between the time when all the power supplies monitored by the POR circuitry reach the minimum recommended operating voltage to the time when the nSTATUS is released high and your device is ready to begin configuration.



For more information about the POR delay, refer to the *Hot Socketing and Power-On Reset in Stratix V Devices* chapter.

Table 45 lists the fast and standard POR delay specification.

**Table 45. Fast and Standard POR Delay Specification <sup>(1)</sup>**

POR Delay	Minimum	Maximum
Fast	4 ms	12 ms
Standard	100 ms	300 ms

**Note to Table 45:**

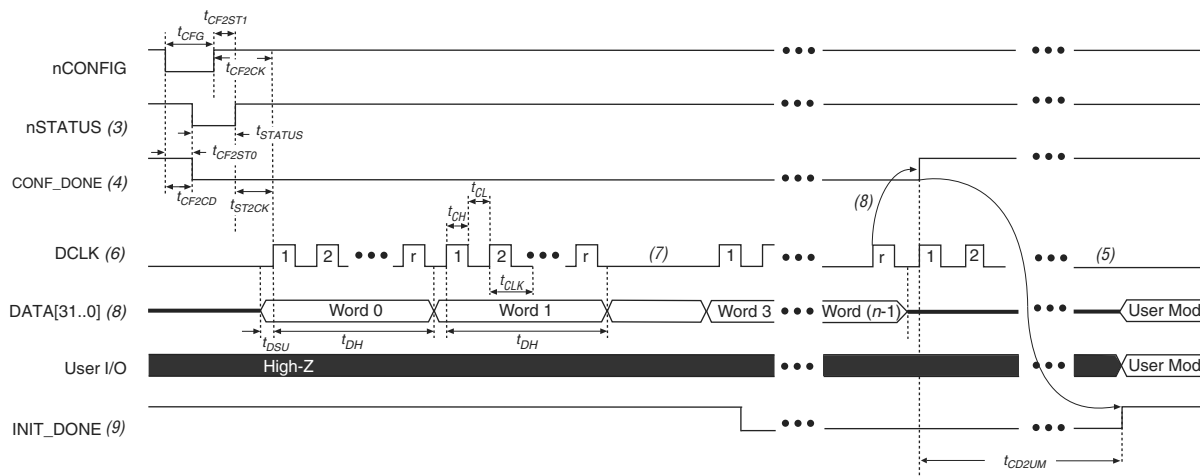
(1) You can select the POR delay based on the MSEL settings as described in the MSEL Pin Settings section of the “Configuration, Design Security, and Remote System Upgrades in Stratix V Devices” chapter.

### JTAG Configuration Specifications

Table 46 lists the JTAG timing parameters and values for Stratix V devices.

**Table 46. JTAG Timing Parameters and Values for Stratix V Devices**

Symbol	Description	Min	Max	Unit
t <sub>JCP</sub>	TCK clock period <sup>(2)</sup>	30	—	ns
t <sub>JCP</sub>	TCK clock period <sup>(2)</sup>	167	—	ns
t <sub>JCH</sub>	TCK clock high time <sup>(2)</sup>	14	—	ns
t <sub>JCL</sub>	TCK clock low time <sup>(2)</sup>	14	—	ns
t <sub>JPSU (TDI)</sub>	TDI JTAG port setup time	2	—	ns
t <sub>JPSU (TMS)</sub>	TMS JTAG port setup time	3	—	ns

**Figure 13. FPP Configuration Timing Waveform When the DCLK-to-DATA[] Ratio is >1 (1), (2)****Notes to Figure 13:**

- (1) Use this timing waveform and parameters when the DCLK-to-DATA [] ratio is >1. To find out the DCLK-to-DATA [] ratio for your system, refer to Table 49 on page 55.
- (2) The beginning of this waveform shows the device in user mode. In user mode, nCONFIG, nSTATUS, and CONF\_DONE are at logic high levels. When nCONFIG is pulled low, a reconfiguration cycle begins.
- (3) After power-up, the Stratix V device holds nSTATUS low for the time as specified by the POR delay.
- (4) After power-up, before and during configuration, CONF\_DONE is low.
- (5) Do not leave DCLK floating after configuration. You can drive it high or low, whichever is more convenient.
- (6) "r" denotes the DCLK-to-DATA [] ratio. For the DCLK-to-DATA [] ratio based on the decompression and the design security feature enable settings, refer to Table 49 on page 55.
- (7) If needed, pause DCLK by holding it low. When DCLK restarts, the external host must provide data on the DATA [31 . . 0] pins prior to sending the first DCLK rising edge.
- (8) To ensure a successful configuration, send the entire configuration data to the Stratix V device. CONF\_DONE is released high after the Stratix V device receives all the configuration data successfully. After CONF\_DONE goes high, send two additional falling edges on DCLK to begin initialization and enter user mode.
- (9) After the option bit to enable the INIT\_DONE pin is configured into the device, the INIT\_DONE goes low.

## Active Serial Configuration Timing

Table 52 lists the DCLK frequency specification in the AS configuration scheme.

**Table 52. DCLK Frequency Specification in the AS Configuration Scheme <sup>(1), (2)</sup>**

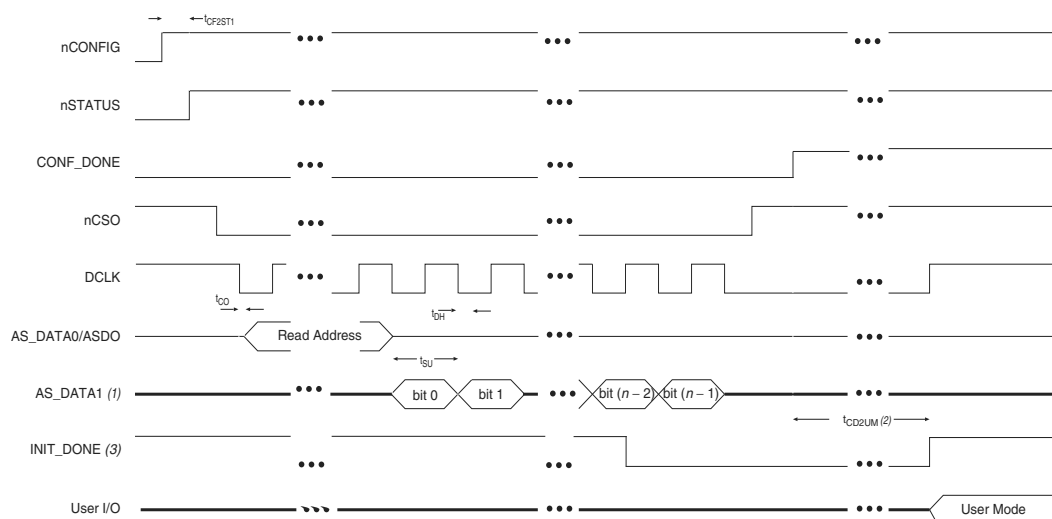
Minimum	Typical	Maximum	Unit
5.3	7.9	12.5	MHz
10.6	15.7	25.0	MHz
21.3	31.4	50.0	MHz
42.6	62.9	100.0	MHz

**Notes to Table 52:**

- (1) This applies to the DCLK frequency specification when using the internal oscillator as the configuration clock source.
- (2) The AS multi-device configuration scheme does not support DCLK frequency of 100 MHz.

Figure 14 shows the single-device configuration setup for an AS ×1 mode.

**Figure 14. AS Configuration Timing**



**Notes to Figure 14:**

- (1) If you are using AS ×4 mode, this signal represents the AS\_DATA [3 : 0] and EPCQ sends in 4-bits of data for each DCLK cycle.
- (2) The initialization clock can be from internal oscillator or CLKUSR pin.
- (3) After the option bit to enable the INIT\_DONE pin is configured into the device, the INIT\_DONE goes low.

Table 53 lists the timing parameters for AS ×1 and AS ×4 configurations in Stratix V devices.

**Table 53. AS Timing Parameters for AS ×1 and AS ×4 Configurations in Stratix V Devices <sup>(1), (2)</sup> (Part 1 of 2)**

Symbol	Parameter	Minimum	Maximum	Units
$t_{CO}$	DCLK falling edge to AS_DATA0/ASDO output	—	2	ns
$t_{SU}$	Data setup time before falling edge on DCLK	1.5	—	ns
$t_{H}$	Data hold time after falling edge on DCLK	0	—	ns

## Remote System Upgrades

Table 56 lists the timing parameter specifications for the remote system upgrade circuitry.

**Table 56. Remote System Upgrade Circuitry Timing Specifications**

Parameter	Minimum	Maximum	Unit
$t_{RU\_nCONFIG}^{(1)}$	250	—	ns
$t_{RU\_nRSTIMER}^{(2)}$	250	—	ns

**Notes to Table 56:**

- (1) This is equivalent to strobing the reconfiguration input of the ALTREMOTE\_UPDATE megafunction high for the minimum timing specification. For more information, refer to the Remote System Upgrade State Machine section of the “Configuration, Design Security, and Remote System Upgrades in Stratix V Devices” chapter.
- (2) This is equivalent to strobing the reset\_timer input of the ALTREMOTE\_UPDATE megafunction high for the minimum timing specification. For more information, refer to the User Watchdog Timer section of the “Configuration, Design Security, and Remote System Upgrades in Stratix V Devices” chapter.

## User Watchdog Internal Circuitry Timing Specification

Table 57 lists the operating range of the 12.5-MHz internal oscillator.

**Table 57. 12.5-MHz Internal Oscillator Specifications**

Minimum	Typical	Maximum	Units
5.3	7.9	12.5	MHz

## I/O Timing

Altera offers two ways to determine I/O timing—the Excel-based I/O Timing and the Quartus II Timing Analyzer.

Excel-based I/O timing provides pin timing performance for each device density and speed grade. The data is typically used prior to designing the FPGA to get an estimate of the timing budget as part of the link timing analysis. The Quartus II Timing Analyzer provides a more accurate and precise I/O timing data based on the specifics of the design after you complete place-and-route.



You can download the Excel-based I/O Timing spreadsheet from the Stratix V Devices Documentation web page.

## Programmable IOE Delay

Table 58 lists the Stratix V IOE programmable delay settings.

**Table 58. IOE Programmable Delay for Stratix V Devices (Part 1 of 2)**

Parameter (1)	Available Settings	Min Offset (2)	Fast Model		Slow Model							
			Industrial	Commercial	C1	C2	C3	C4	I2	I3, I3YY	I4	Unit
D1	64	0	0.464	0.493	0.838	0.838	0.924	1.011	0.844	0.921	1.006	ns
D2	32	0	0.230	0.244	0.415	0.415	0.459	0.503	0.417	0.456	0.500	ns



**Table 58. IOE Programmable Delay for Stratix V Devices (Part 2 of 2)**

Parameter (1)	Available Settings	Min Offset (2)	Fast Model		Slow Model							
			Industrial	Commercial	C1	C2	C3	C4	I2	I3, I3YY	I4	Unit
D3	8	0	1.587	1.699	2.793	2.793	2.992	3.192	2.811	3.047	3.257	ns
D4	64	0	0.464	0.492	0.838	0.838	0.924	1.011	0.843	0.920	1.006	ns
D5	64	0	0.464	0.493	0.838	0.838	0.924	1.011	0.844	0.921	1.006	ns
D6	32	0	0.229	0.244	0.415	0.415	0.458	0.503	0.418	0.456	0.499	ns

**Notes to Table 58:**

- (1) You can set this value in the Quartus II software by selecting **D1**, **D2**, **D3**, **D5**, and **D6** in the **Assignment Name** column of **Assignment Editor**.
- (2) Minimum offset does not include the intrinsic delay.

## Programmable Output Buffer Delay

Table 59 lists the delay chain settings that control the rising and falling edge delays of the output buffer. The default delay is 0 ps.

**Table 59. Programmable Output Buffer Delay for Stratix V Devices (1)**

Symbol	Parameter	Typical	Unit
D <sub>OUTBUF</sub>	Rising and/or falling edge delay	0 (default)	ps
		25	ps
		50	ps
		75	ps

**Note to Table 59:**

- (1) You can set the programmable output buffer delay in the Quartus II software by setting the **Output Buffer Delay Control** assignment to either positive, negative, or both edges, with the specific values stated here (in ps) for the **Output Buffer Delay** assignment.

## Glossary

Table 60 lists the glossary for this chapter.

**Table 60. Glossary (Part 1 of 4)**

Letter	Subject	Definitions
A	—	—
B		
C		
D	—	—
E	—	—
F	f <sub>HCLK</sub>	Left and right PLL input clock frequency.
	f <sub>HSDR</sub>	High-speed I/O block—Maximum and minimum <b>LVDS</b> data transfer rate (f <sub>HSDR</sub> = 1/TUI), non-DPA.
	f <sub>HSDRDPA</sub>	High-speed I/O block—Maximum and minimum <b>LVDS</b> data transfer rate (f <sub>HSDRDPA</sub> = 1/TUI), DPA.



## Document Revision History

Table 61 lists the revision history for this chapter.

**Table 61. Document Revision History (Part 1 of 3)**

Date	Version	Changes
June 2018	3.9	<ul style="list-style-type: none"> <li>■ Added the “Stratix V Device Overshoot Duration” figure.</li> </ul>
April 2017	3.8	<ul style="list-style-type: none"> <li>■ Added a footnote to the “High-Speed I/O Specifications for Stratix V Devices” table.</li> <li>■ Changed the minimum value for <math>t_{CD2UMC}</math> in the “PS Timing Parameters for Stratix V Devices” table.</li> <li>■ Changed the condition for <math>100\text{-}\Omega</math> <math>R_D</math> in the “OCT Without Calibration Resistance Tolerance Specifications for Stratix V Devices” table.</li> <li>■ Changed the minimum value for <math>t_{CD2UMC}</math> in the “AS Timing Parameters for AS ‘1 and AS ‘4 Configurations in Stratix V Devices” table</li> <li>■ Changed the minimum value for <math>t_{CD2UMC}</math> in the “FPP Timing Parameters for Stratix V Devices When the DCLK-to-DATA[] Ratio is &gt;1” table.</li> <li>■ Changed the minimum value for <math>t_{CD2UMC}</math> in the “FPP Timing Parameters for Stratix V Devices When the DCLK-to-DATA[] Ratio is &gt;1” table.</li> <li>■ Changed the minimum number of clock cycles value in the “Initialization Clock Source Option and the Maximum Frequency” table.</li> </ul>
June 2016	3.7	<ul style="list-style-type: none"> <li>■ Added the <math>V_{ID}</math> minimum specification for LVPECL in the “Differential I/O Standard Specifications for Stratix V Devices” table</li> <li>■ Added the <math>I_{OUT}</math> specification to the “Absolute Maximum Ratings for Stratix V Devices” table.</li> </ul>
December 2015	3.6	<ul style="list-style-type: none"> <li>■ Added a footnote to the “High-Speed I/O Specifications for Stratix V Devices” table.</li> </ul>
December 2015	3.5	<ul style="list-style-type: none"> <li>■ Changed the transmitter, receiver, and ATX PLL data rate specifications in the “Transceiver Specifications for Stratix V GX and GS Devices” table.</li> <li>■ Changed the configuration .rbf sizes in the “Uncompressed .rbf Sizes for Stratix V Devices” table.</li> </ul>
July 2015	3.4	<ul style="list-style-type: none"> <li>■ Changed the data rate specification for transceiver speed grade 3 in the following tables:               <ul style="list-style-type: none"> <li>■ “Transceiver Specifications for Stratix V GX and GS Devices”</li> <li>■ “Stratix V Standard PCS Approximate Maximum Date Rate”</li> <li>■ “Stratix V 10G PCS Approximate Maximum Data Rate”</li> </ul> </li> <li>■ Changed the conditions for reference clock rise and fall time, and added a note to the “Transceiver Specifications for Stratix V GX and GS Devices” table.</li> <li>■ Added a note to the “Minimum differential eye opening at receiver serial input pins” specification in the “Transceiver Specifications for Stratix V GX and GS Devices” table.</li> <li>■ Changed the <math>t_{CO}</math> maximum value in the “AS Timing Parameters for AS ‘1 and AS ‘4 Configurations in Stratix V Devices” table.</li> <li>■ Removed the CDR ppm tolerance specification from the “Transceiver Specifications for Stratix V GX and GS Devices” table.</li> </ul>

**Table 61. Document Revision History (Part 2 of 3)**

Date	Version	Changes
November 2014	3.3	<ul style="list-style-type: none"> <li>■ Added the I3YY speed grade and changed the data rates for the GX channel in Table 1.</li> <li>■ Added the I3YY speed grade to the <math>V_{CC}</math> description in Table 6.</li> <li>■ Added the I3YY speed grade to <math>V_{CCHIP\_L}</math>, <math>V_{CCHIP\_R}</math>, <math>V_{CCHSSI\_L}</math>, and <math>V_{CCHSSI\_R}</math> descriptions in Table 7.</li> <li>■ Added 240-Ω to Table 11.</li> <li>■ Changed CDR PPM tolerance in Table 23.</li> <li>■ Added additional max data rate for fPLL in Table 23.</li> <li>■ Added the I3YY speed grade and changed the data rates for transceiver speed grade 3 in Table 25.</li> <li>■ Added the I3YY speed grade and changed the data rates for transceiver speed grade 3 in Table 26.</li> <li>■ Changed CDR PPM tolerance in Table 28.</li> <li>■ Added additional max data rate for fPLL in Table 28.</li> <li>■ Changed the mode descriptions for MLAB and M20K in Table 33.</li> <li>■ Changed the Max value of <math>f_{HCLK\_OUT}</math> for the C2, C2L, I2, I2L speed grades in Table 36.</li> <li>■ Changed the frequency ranges for C1 and C2 in Table 39.</li> <li>■ Changed the .rbf file sizes for 5SGSD6 and 5SGSD8 in Table 47.</li> <li>■ Added note about nSTATUS to Table 50, Table 51, Table 54.</li> <li>■ Changed the available settings in Table 58.</li> <li>■ Changed the note in “Periphery Performance”.</li> <li>■ Updated the “I/O Standard Specifications” section.</li> <li>■ Updated the “Raw Binary File Size” section.</li> <li>■ Updated the receiver voltage input range in Table 22.</li> <li>■ Updated the max frequency for the LVDS clock network in Table 36.</li> <li>■ Updated the DCLK note to Figure 11.</li> <li>■ Updated Table 23 <math>VO_{CM}</math> (DC Coupled) condition.</li> <li>■ Updated Table 6 and Table 7.</li> <li>■ Added the DCLK specification to Table 55.</li> <li>■ Updated the notes for Table 47.</li> <li>■ Updated the list of parameters for Table 56.</li> </ul>
November 2013	3.2	■ Updated Table 28
November 2013	3.1	■ Updated Table 33
November 2013	3.0	■ Updated Table 23 and Table 28
October 2013	2.9	■ Updated the “Transceiver Characterization” section
October 2013	2.8	<ul style="list-style-type: none"> <li>■ Updated Table 3, Table 12, Table 14, Table 19, Table 20, Table 23, Table 24, Table 28, Table 30, Table 31, Table 32, Table 33, Table 36, Table 39, Table 40, Table 41, Table 42, Table 47, Table 53, Table 58, and Table 59</li> <li>■ Added Figure 1 and Figure 3</li> <li>■ Added the “Transceiver Characterization” section</li> <li>■ Removed all “Preliminary” designations.</li> </ul>

**Table 61. Document Revision History (Part 3 of 3)**

Date	Version	Changes
May 2013	2.7	<ul style="list-style-type: none"> <li>■ Updated Table 2, Table 6, Table 7, Table 20, Table 23, Table 27, Table 47, Table 60</li> <li>■ Added Table 24, Table 48</li> <li>■ Updated Figure 9, Figure 10, Figure 11, Figure 12</li> </ul>
February 2013	2.6	<ul style="list-style-type: none"> <li>■ Updated Table 7, Table 9, Table 20, Table 23, Table 27, Table 30, Table 31, Table 35, Table 46</li> <li>■ Updated “Maximum Allowed Overshoot and Undershoot Voltage”</li> </ul>
December 2012	2.5	<ul style="list-style-type: none"> <li>■ Updated Table 3, Table 6, Table 7, Table 8, Table 23, Table 24, Table 25, Table 27, Table 30, Table 32, Table 35</li> <li>■ Added Table 33</li> <li>■ Added “Fast Passive Parallel Configuration Timing”</li> <li>■ Added “Active Serial Configuration Timing”</li> <li>■ Added “Passive Serial Configuration Timing”</li> <li>■ Added “Remote System Upgrades”</li> <li>■ Added “User Watchdog Internal Circuitry Timing Specification”</li> <li>■ Added “Initialization”</li> <li>■ Added “Raw Binary File Size”</li> </ul>
June 2012	2.4	<ul style="list-style-type: none"> <li>■ Added Figure 1, Figure 2, and Figure 3.</li> <li>■ Updated Table 1, Table 2, Table 3, Table 6, Table 11, Table 22, Table 23, Table 27, Table 29, Table 30, Table 31, Table 32, Table 35, Table 38, Table 39, Table 40, Table 41, Table 43, Table 56, and Table 59.</li> <li>■ Various edits throughout to fix bugs.</li> <li>■ Changed title of document to <i>Stratix V Device Datasheet</i>.</li> <li>■ Removed document from the Stratix V handbook and made it a separate document.</li> </ul>
February 2012	2.3	<ul style="list-style-type: none"> <li>■ Updated Table 1–22, Table 1–29, Table 1–31, and Table 1–31.</li> </ul>
December 2011	2.2	<ul style="list-style-type: none"> <li>■ Added Table 2–31.</li> <li>■ Updated Table 2–28 and Table 2–34.</li> </ul>
November 2011	2.1	<ul style="list-style-type: none"> <li>■ Added Table 2–2 and Table 2–21 and updated Table 2–5 with information about Stratix V GT devices.</li> <li>■ Updated Table 2–11, Table 2–13, Table 2–20, and Table 2–25.</li> <li>■ Various edits throughout to fix SPRs.</li> </ul>
May 2011	2.0	<ul style="list-style-type: none"> <li>■ Updated Table 2–4, Table 2–18, Table 2–19, Table 2–21, Table 2–22, Table 2–23, and Table 2–24.</li> <li>■ Updated the “DQ Logic Block and Memory Output Clock Jitter Specifications” title.</li> <li>■ Chapter moved to Volume 1.</li> <li>■ Minor text edits.</li> </ul>
December 2010	1.1	<ul style="list-style-type: none"> <li>■ Updated Table 1–2, Table 1–4, Table 1–19, and Table 1–23.</li> <li>■ Converted chapter to the new template.</li> <li>■ Minor text edits.</li> </ul>
July 2010	1.0	Initial release.