Welcome to E-XFL.COM

Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	185000
Number of Logic Elements/Cells	490000
Total RAM Bits	46080000
Number of I/O	696
Number of Gates	-
Voltage - Supply	0.87V ~ 0.93V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	1517-BBGA, FCBGA
Supplier Device Package	1517-FBGA (40x40)
Purchase URL	https://www.e-xfl.com/product-detail/intel/5sgxea5k2f40c1n

Table 6. Recommended Operating Conditions for Stratix V Devices (Part 2 of 2)

Symbol	Description	Condition	Min (4)	Typ	Max (4)	Unit
t_{RAMP}	Power supply ramp time	Standard POR	200 µs	—	100 ms	—
		Fast POR	200 µs	—	4 ms	—

Notes to Table 6:

(1) V_{CCPD} must be 2.5 V when V_{CCIO} is 2.5, 1.8, 1.5, 1.35, 1.25 or 1.2 V. V_{CCPD} must be 3.0 V when V_{CCIO} is 3.0 V.

(2) If you do not use the design security feature in Stratix V devices, connect V_{CCBAT} to a 1.2- to 3.0-V power supply. Stratix V power-on-reset (POR) circuitry monitors V_{CCBAT}. Stratix V devices will not exit POR if V_{CCBAT} stays at logic low.

(3) C2L and I2L can also be run at 0.90 V for legacy boards that were designed for the C2 and I2 speed grades.

(4) The power supply value describes the budget for the DC (static) power supply tolerance and does not include the dynamic tolerance requirements. Refer to the PDN tool for the additional budget for the dynamic tolerance requirements.

Table 7 lists the transceiver power supply recommended operating conditions for Stratix V GX, GS, and GT devices.

Table 7. Recommended Transceiver Power Supply Operating Conditions for Stratix V GX, GS, and GT Devices (Part 1 of 2)

Symbol	Description	Devices	Minimum (4)	Typical	Maximum (4)	Unit
V_{CCA_GXBL} (1), (3)	Transceiver channel PLL power supply (left side)	GX, GS, GT	2.85	3.0	3.15	V
			2.375	2.5	2.625	
V_{CCA_GXBR} (1), (3)	Transceiver channel PLL power supply (right side)	GX, GS	2.85	3.0	3.15	V
			2.375	2.5	2.625	
V_{CCA_GTBR}	Transceiver channel PLL power supply (right side)	GT	2.85	3.0	3.15	V
V_{CCHIP_L}	Transceiver hard IP power supply (left side; C1, C2, I2, and I3YY speed grades)	GX, GS, GT	0.87	0.9	0.93	V
	Transceiver hard IP power supply (left side; C2L, C3, C4, I2L, I3, I3L, and I4 speed grades)	GX, GS, GT	0.82	0.85	0.88	V
V_{CCHIP_R}	Transceiver hard IP power supply (right side; C1, C2, I2, and I3YY speed grades)	GX, GS, GT	0.87	0.9	0.93	V
	Transceiver hard IP power supply (right side; C2L, C3, C4, I2L, I3, I3L, and I4 speed grades)	GX, GS, GT	0.82	0.85	0.88	V
V_{CCHSSI_L}	Transceiver PCS power supply (left side; C1, C2, I2, and I3YY speed grades)	GX, GS, GT	0.87	0.9	0.93	V
	Transceiver PCS power supply (left side; C2L, C3, C4, I2L, I3, I3L, and I4 speed grades)	GX, GS, GT	0.82	0.85	0.88	V
V_{CCHSSI_R}	Transceiver PCS power supply (right side; C1, C2, I2, and I3YY speed grades)	GX, GS, GT	0.87	0.9	0.93	V
	Transceiver PCS power supply (right side; C2L, C3, C4, I2L, I3, I3L, and I4 speed grades)	GX, GS, GT	0.82	0.85	0.88	V
V_{CCR_GXBL} (2)	Receiver analog power supply (left side)	GX, GS, GT	0.82	0.85	0.88	V
			0.87	0.90	0.93	
			0.97	1.0	1.03	
			1.03	1.05	1.07	

Internal Weak Pull-Up Resistor

Table 16 lists the weak pull-up resistor values for Stratix V devices.

Table 16. Internal Weak Pull-Up Resistor for Stratix V Devices (1), (2)

Symbol	Description	V_{CCIO} Conditions (V) (3)	Value (4)	Unit
R_{PU}	Value of the I/O pin pull-up resistor before and during configuration, as well as user mode if you enable the programmable pull-up resistor option.	3.0 ±5%	25	kΩ
		2.5 ±5%	25	kΩ
		1.8 ±5%	25	kΩ
		1.5 ±5%	25	kΩ
		1.35 ±5%	25	kΩ
		1.25 ±5%	25	kΩ
		1.2 ±5%	25	kΩ

Notes to Table 16:

(1) All I/O pins have an option to enable the weak pull-up resistor except the configuration, test, and JTAG pins.

(2) The internal weak pull-down feature is only available for the JTAG TCK pin. The typical value for this internal weak pull-down resistor is approximately 25 kΩ.

(3) The pin pull-up resistance values may be lower if an external source drives the pin higher than V_{CCIO}.

(4) These specifications are valid with a ±10% tolerance to cover changes over PVT.

I/O Standard Specifications

Table 17 through Table 22 list the input voltage (V_{IH} and V_{IL}), output voltage (V_{OH} and V_{OL}), and current drive characteristics (I_{OH} and I_{OL}) for various I/O standards supported by Stratix V devices. These tables also show the Stratix V device family I/O standard specifications. The V_{OL} and V_{OH} values are valid at the corresponding I_{OH} and I_{OL}, respectively.

For an explanation of the terms used in Table 17 through Table 22, refer to "Glossary" on page 65. For tolerance calculations across all SSTL and HSTL I/O standards, refer to Altera knowledge base solution rd07262012_486.

Table 17. Single-Ended I/O Standards for Stratix V Devices

I/O Standard	V_{CCIO} (V)			V_{IL} (V)		V_{IH} (V)		V_{OL} (V)	V_{OH} (V)	I_{OL} (mA)	I_{OH} (mA)
	Min	Typ	Max	Min	Max	Min	Max	Max	Min		
LVTTL	2.85	3	3.15	–0.3	0.8	1.7	3.6	0.4	2.4	2	–2
LVCMOS	2.85	3	3.15	–0.3	0.8	1.7	3.6	0.2	V_{CCIO} – 0.2	0.1	–0.1
2.5 V	2.375	2.5	2.625	–0.3	0.7	1.7	3.6	0.4	2	1	–1
1.8 V	1.71	1.8	1.89	–0.3	0.35 * V_{CCIO}	0.65 * V_{CCIO}	V_{CCIO} + 0.3	0.45	V_{CCIO} – 0.45	2	–2
1.5 V	1.425	1.5	1.575	–0.3	0.35 * V_{CCIO}	0.65 * V_{CCIO}	V_{CCIO} + 0.3	0.25 * V_{CCIO}	0.75 * V_{CCIO}	2	–2
1.2 V	1.14	1.2	1.26	–0.3	0.35 * V_{CCIO}	0.65 * V_{CCIO}	V_{CCIO} + 0.3	0.25 * V_{CCIO}	0.75 * V_{CCIO}	2	–2

You typically use the interactive Excel-based Early Power Estimator before designing the FPGA to get a magnitude estimate of the device power. The Quartus II PowerPlay Power Analyzer provides better quality estimates based on the specifics of the design after you complete place-and-route. The PowerPlay Power Analyzer can apply a combination of user-entered, simulation-derived, and estimated signal activities that, when combined with detailed circuit models, yields very accurate power estimates.

For more information about power estimation tools, refer to the *PowerPlay Early Power Estimator User Guide* and the *PowerPlay Power Analysis* chapter in the *Quartus II Handbook*.

Table 23. Transceiver Specifications for Stratix V GX and GS Devices (1) (Part 3 of 7)

Symbol/ Description	Conditions	Transceiver Speed Grade 1			Transceiver Speed Grade 2			Transceiver Speed Grade 3			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Reconfiguration clock (mgmt_clk_clk) frequency	—	100	—	125	100	—	125	100	—	125	MHz
Receiver											
Supported I/O Standards	—	1.4-V PCML, 1.5-V PCML, 2.5-V PCML, LVPECL, and LVDS									
Data rate (Standard PCS) (9), (23)	—	600	—	12200	600	—	12200	600	—	8500/ 10312.5 (24)	Mbps
Data rate (10G PCS) (9), (23)	—	600	—	14100	600	—	12500	600	—	8500/ 10312.5 (24)	Mbps
Absolute V_{MAX} for a receiver pin (5)	—	—	—	1.2	—	—	1.2	—	—	1.2	V
Absolute V_{MIN} for a receiver pin	—	–0.4	—	—	–0.4	—	—	–0.4	—	—	V
Maximum peak-to-peak differential input voltage V_{ID} (diff p-p) before device configuration (22)	—	—	—	1.6	—	—	1.6	—	—	1.6	V
Maximum peak-to-peak differential input voltage V_{ID} (diff p-p) after device configuration (18), (22)	V_{CCR_GXB} = 1.0 V/1.05 V (V_{ICM} = 0.70 V)	—	—	2.0	—	—	2.0	—	—	2.0	V
	V_{CCR_GXB} = 0.90 V (V_{ICM} = 0.6 V)	—	—	2.4	—	—	2.4	—	—	2.4	V
	V_{CCR_GXB} = 0.85 V (V_{ICM} = 0.6 V)	—	—	2.4	—	—	2.4	—	—	2.4	V
Minimum differential eye opening at receiver serial input pins (6), (22), (27)	—	85	—	—	85	—	—	85	—	—	mV

Table 23. Transceiver Specifications for Stratix V GX and GS Devices (1) (Part 6 of 7)

Symbol/ Description	Conditions	Transceiver Speed Grade 1			Transceiver Speed Grade 2			Transceiver Speed Grade 3			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Inter-transceiver block transmitter channel-to-channel skew	xN PMA bonded mode	—	—	500	—	—	500	—	—	500	ps
CMU PLL											
Supported Data Range	—	600	—	12500	600	—	12500	600	—	8500/ 10312.5 (24)	Mbps
$t_{pll\_powerdown}$ (15)	—	1	—	—	1	—	—	1	—	—	µs
t_{pll_lock} (16)	—	—	—	10	—	—	10	—	—	10	µs
ATX PLL											
Supported Data Rate Range	VCO post-divider L=2	8000	—	14100	8000	—	12500	8000	—	8500/ 10312.5 (24)	Mbps
	L=4	4000	—	7050	4000	—	6600	4000	—	6600	Mbps
	L=8	2000	—	3525	2000	—	3300	2000	—	3300	Mbps
	L=8, Local/Central Clock Divider =2	1000	—	1762.5	1000	—	1762.5	1000	—	1762.5	Mbps
$t_{pll\_powerdown}$ (15)	—	1	—	—	1	—	—	1	—	—	µs
t_{pll_lock} (16)	—	—	—	10	—	—	10	—	—	10	µs
fPLL											
Supported Data Range	—	600	—	3250/ 3125 (25)	600	—	3250/ 3125 (25)	600	—	3250/ 3125 (25)	Mbps
$t_{pll\_powerdown}$ (15)	—	1	—	—	1	—	—	1	—	—	µs

Table 26 shows the approximate maximum data rate using the 10G PCS.

Table 26. Stratix V 10G PCS Approximate Maximum Data Rate *(1)*

Mode *(2)*	Transceiver Speed Grade	PMA Width	64	40	40	40	32	32
		PCS Width	**64**	**66/67**	**50**	**40**	**64/66/67**	**32**
FIFO or Register	1	C1, C2, C2L, I2, I2L core speed grade	14.1	14.1	10.69	14.1	13.6	13.6
	2	C1, C2, C2L, I2, I2L core speed grade	12.5	12.5	10.69	12.5	12.5	12.5
		C3, I3, I3L core speed grade	12.5	12.5	10.69	12.5	10.88	10.88
	3	C1, C2, C2L, I2, I2L core speed grade	8.5 Gbps					
		C3, I3, I3L core speed grade						
		C4, I4 core speed grade						
		I3YY core speed grade	10.3125 Gbps					

Notes to Table 26:

(1) The maximum data rate is in Gbps.

(2) The Phase Compensation FIFO can be configured in FIFO mode or register mode. In the FIFO mode, the pointers are not fixed, and the latency can vary. In the register mode the pointers are fixed for low latency.

Table 28. Transceiver Specifications for Stratix V GT Devices (Part 1 of 5) (1)

Symbol/ Description	Conditions	Transceiver Speed Grade 2			Transceiver Speed Grade 3			Unit
		Min	Typ	Max	Min	Typ	Max	
Reference Clock								
Supported I/O Standards	Dedicated reference clock pin	1.2-V PCML, 1.4-V PCML, 1.5-V PCML, 2.5-V PCML, Differential LVPECL, LVDS, and HCSL						
	RX reference clock pin	1.4-V PCML, 1.5-V PCML, 2.5-V PCML, LVPECL, and LVDS						
Input Reference Clock Frequency (CMU PLL) (6)	—	40	—	710	40	—	710	MHz
Input Reference Clock Frequency (ATX PLL) (6)	—	100	—	710	100	—	710	MHz
Rise time	20% to 80%	—	—	400	—	—	400	ps
Fall time	80% to 20%	—	—	400	—	—	400	
Duty cycle	—	45	—	55	45	—	55	%
Spread-spectrum modulating clock frequency	PCI Express (PCIe)	30	—	33	30	—	33	kHz
Spread-spectrum downspread	PCIe	—	0 to –0.5	—	—	0 to –0.5	—	%
On-chip termination resistors (19)	—	—	100	—	—	100	—	Ω
Absolute V_{MAX} (3)	Dedicated reference clock pin	—	—	1.6	—	—	1.6	V
	RX reference clock pin	—	—	1.2	—	—	1.2	
Absolute V_{MIN}	—	-0.4	—	—	-0.4	—	—	V
Peak-to-peak differential input voltage	—	200	—	1600	200	—	1600	mV
V_{ICM} (AC coupled)	Dedicated reference clock pin	1050/1000 (2)			1050/1000 (2)			mV
	RX reference clock pin	1.0/0.9/0.85 (22)			1.0/0.9/0.85 (22)			V
V_{ICM} (DC coupled)	HCSL I/O standard for PCIe reference clock	250	—	550	250	—	550	mV

Table 28. Transceiver Specifications for Stratix V GT Devices (Part 4 of 5) (1)

Symbol/ Description	Conditions	Transceiver Speed Grade 2			Transceiver Speed Grade 3			Unit
		Min	Typ	Max	Min	Typ	Max	
Data rate	GT channels	19,600	—	28,050	19,600	—	25,780	Mbps
Differential on-chip termination resistors	GT channels	—	100	—	—	100	—	Ω
	GX channels	(8)						
V_{OCM} (AC coupled)	GT channels	—	500	—	—	500	—	mV
	GX channels	(8)						
Rise/Fall time	GT channels	—	15	—	—	15	—	ps
	GX channels	(8)						
Intra-differential pair skew	GX channels	(8)						
Intra-transceiver block transmitter channel-to-channel skew	GX channels	(8)						
Inter-transceiver block transmitter channel-to-channel skew	GX channels	(8)						
CMU PLL								
Supported Data Range	—	600	—	12500	600	—	8500	Mbps
$t_{pll\_powerdown}$ (13)	—	1	—	—	1	—	—	µs
t_{pll_lock} (14)	—	—	—	10	—	—	10	µs
ATX PLL								
Supported Data Rate Range for GX Channels	VCO post-divider L=2	8000	—	12500	8000	—	8500	Mbps
	L=4	4000	—	6600	4000	—	6600	Mbps
	L=8	2000	—	3300	2000	—	3300	Mbps
	L=8, Local/Central Clock Divider =2	1000	—	1762.5	1000	—	1762.5	Mbps
Supported Data Rate Range for GT Channels	VCO post-divider L=2	9800	—	14025	9800	—	12890	Mbps
$t_{pll\_powerdown}$ (13)	—	1	—	—	1	—	—	µs
t_{pll_lock} (14)	—	—	—	10	—	—	10	µs
fPLL								
Supported Data Range	—	600	—	3250/ 3.125 (23)	600	—	3250/ 3.125 (23)	Mbps
$t_{pll\_powerdown}$ (13)	—	1	—	—	1	—	—	µs

Table 28. Transceiver Specifications for Stratix V GT Devices (Part 5 of 5) (1)

Symbol/ Description	Conditions	Transceiver Speed Grade 2			Transceiver Speed Grade 3			Unit
		Min	Typ	Max	Min	Typ	Max	
t_{pll_lock} (14)	—	—	—	10	—	—	10	µs

Notes to Table 28:

(1) Speed grades shown refer to the PMA Speed Grade in the device ordering code. The maximum data rate could be restricted by the Core/PCS speed grade. Contact your Altera Sales Representative for the maximum data rate specifications in each speed grade combination offered. For more information about device ordering codes, refer to the *Stratix V Device Overview*.

(2) The reference clock common mode voltage is equal to the VCCR_GXB power supply level.

(3) The device cannot tolerate prolonged operation at this absolute maximum.

(4) The differential eye opening specification at the receiver input pins assumes that receiver equalization is disabled. If you enable receiver equalization, the receiver circuitry can tolerate a lower minimum eye opening, depending on the equalization level.

(5) Refer to Figure 5 for the GT channel AC gain curves. The total effective AC gain is the AC gain minus the DC gain.

(6) Refer to Figure 6 for the GT channel DC gain curves.

(7) CFP2 optical modules require the host interface to have the receiver data pins differentially terminated with 100 Ω. The internal OCT feature is available after the Stratix V FPGA configuration is completed. Altera recommends that FPGA configuration is completed before inserting the optical module. Otherwise, minimize unnecessary removal and insertion with unconfigured devices.

(8) Specifications for this parameter are the same as for Stratix V GX and GS devices. See Table 23 for specifications.

(9) t_{LTR} is the time required for the receive CDR to lock to the input reference clock frequency after coming out of reset.

(10) t_{LTD} is time required for the receiver CDR to start recovering valid data after the `rx_is_lockedtodata` signal goes high.

(11) t_{LTD_manual} is the time required for the receiver CDR to start recovering valid data after the `rx_is_lockedtodata` signal goes high when the CDR is functioning in the manual mode.

(12) $t_{LTR\_LTD\_manual}$ is the time the receiver CDR must be kept in lock to reference (LTR) mode after the `rx_is_lockedtoref` signal goes high when the CDR is functioning in the manual mode.

(13) `tpll_powerdown` is the PLL powerdown minimum pulse width.

(14) `tpll_lock` is the time required for the transmitter CMU/ATX PLL to lock to the input reference clock frequency after coming out of reset.

(15) To calculate the REFCLK rms phase jitter requirement for PCIe at reference clock frequencies other than 100 MHz, use the following formula: REFCLK rms phase jitter at f(MHz) = REFCLK rms phase jitter at 100 MHz × 100/f.

(16) The maximum peak to peak differential input voltage V_{ID} after device configuration is equal to 4 × (absolute V_{MAX} for receiver pin - V_{ICM}).

(17) For ES devices, RREF is 2000 Ω ±1%.

(18) To calculate the REFCLK phase noise requirement at frequencies other than 622 MHz, use the following formula: REFCLK phase noise at f(MHz) = REFCLK phase noise at 622 MHz + 20*log(f/622).

(19) SFP/+ optical modules require the host interface to have RD+/- differentially terminated with 100 Ω. The internal OCT feature is available after the Stratix V FPGA configuration is completed. Altera recommends that FPGA configuration is completed before inserting the optical module. Otherwise, minimize unnecessary removal and insertion with unconfigured devices.

(20) Refer to Figure 4.

(21) For oversampling design to support data rates less than the minimum specification, the CDR needs to be in LTR mode only.

(22) This supply follows VCCR_GXB for both GX and GT channels.

(23) When you use fPLL as a TXPLL of the transceiver.

Table 29 shows the V_{OD} settings for the GT channel.

Table 29. Typical V_{OD} Setting for GT Channel, TX Termination = 100 Ω

Symbol	V_{OD} Setting	V_{OD} Value (mV)
V_{OD} differential peak to peak typical (1)	0	0
	1	200
	2	400
	3	600
	4	800
	5	1000

Note:

(1) Refer to Figure 4.

Figure 6 shows the Stratix V DC gain curves for GT channels.

Figure 6. DC Gain Curves for GT Channels

Transceiver Characterization

This section summarizes the Stratix V transceiver characterization results for compliance with the following protocols:

- Interlaken
- 40G (XLAUI)/100G (CAUI)
- 10GBase-KR
- QSGMII
- XAUI
- SFI
- Gigabit Ethernet (Gbe / GIGE)
- SPAUI
- Serial Rapid IO (SRIO)
- CPRI
- OBSAI
- Hyper Transport (HT)
- SATA
- SAS
- CEI

Table 31. PLL Specifications for Stratix V Devices (Part 2 of 3)

Symbol	Parameter	Min	Typ	Max	Unit
t_{INCCJ} (3), (4)	Input clock cycle-to-cycle jitter ($f_{REF} \geq 100$ MHz)	—	—	0.15	UI (p-p)
	Input clock cycle-to-cycle jitter ($f_{REF} < 100$ MHz)	–750	—	+750	ps (p-p)
t_{OUTPJ_DC} (5)	Period Jitter for dedicated clock output ($f_{OUT} \geq 100$ MHz)	—	—	175 (1)	ps (p-p)
	Period Jitter for dedicated clock output ($f_{OUT} < 100$ MHz)	—	—	17.5 (1)	mUI (p-p)
t_{FOUTPJ_DC} (5)	Period Jitter for dedicated clock output in fractional PLL ($f_{OUT} \geq 100$ MHz)	—	—	250 (11), 175 (12)	ps (p-p)
	Period Jitter for dedicated clock output in fractional PLL ($f_{OUT} < 100$ MHz)	—	—	25 (11), 17.5 (12)	mUI (p-p)
t_{OUTCCJ_DC} (5)	Cycle-to-Cycle Jitter for a dedicated clock output ($f_{OUT} \geq 100$ MHz)	—	—	175	ps (p-p)
	Cycle-to-Cycle Jitter for a dedicated clock output ($f_{OUT} < 100$ MHz)	—	—	17.5	mUI (p-p)
$t_{FOUTCCJ\_DC}$ (5)	Cycle-to-cycle Jitter for a dedicated clock output in fractional PLL ($f_{OUT} \geq 100$ MHz)	—	—	250 (11), 175 (12)	ps (p-p)
	Cycle-to-cycle Jitter for a dedicated clock output in fractional PLL ($f_{OUT} < 100$ MHz)+	—	—	25 (11), 17.5 (12)	mUI (p-p)
t_{OUTPJ_IO} (5), (8)	Period Jitter for a clock output on a regular I/O in integer PLL ($f_{OUT} \geq 100$ MHz)	—	—	600	ps (p-p)
	Period Jitter for a clock output on a regular I/O ($f_{OUT} < 100$ MHz)	—	—	60	mUI (p-p)
t_{FOUTPJ_IO} (5), (8), (11)	Period Jitter for a clock output on a regular I/O in fractional PLL ($f_{OUT} \geq 100$ MHz)	—	—	600 (10)	ps (p-p)
	Period Jitter for a clock output on a regular I/O in fractional PLL ($f_{OUT} < 100$ MHz)	—	—	60 (10)	mUI (p-p)
t_{OUTCCJ_IO} (5), (8)	Cycle-to-cycle Jitter for a clock output on a regular I/O in integer PLL ($f_{OUT} \geq 100$ MHz)	—	—	600	ps (p-p)
	Cycle-to-cycle Jitter for a clock output on a regular I/O in integer PLL ($f_{OUT} < 100$ MHz)	—	—	60 (10)	mUI (p-p)
$t_{FOUTCCJ\_IO}$ (5), (8), (11)	Cycle-to-cycle Jitter for a clock output on a regular I/O in fractional PLL ($f_{OUT} \geq 100$ MHz)	—	—	600 (10)	ps (p-p)
	Cycle-to-cycle Jitter for a clock output on a regular I/O in fractional PLL ($f_{OUT} < 100$ MHz)	—	—	60	mUI (p-p)
$t_{CASC\_OUTPJ\_DC}$ (5), (6)	Period Jitter for a dedicated clock output in cascaded PLLs ($f_{OUT} \geq 100$ MHz)	—	—	175	ps (p-p)
	Period Jitter for a dedicated clock output in cascaded PLLs ($f_{OUT} < 100$ MHz)	—	—	17.5	mUI (p-p)
f_{DRIFT}	Frequency drift after PFDENA is disabled for a duration of 100 µs	—	—	±10	%
dK_{BIT}	Bit number of Delta Sigma Modulator (DSM)	8	24	32	Bits
k_{VALUE}	Numerator of Fraction	128	8388608	2147483648	—

Table 36. High-Speed I/O Specifications for Stratix V Devices (1), (2) (Part 2 of 4)

Symbol	Conditions	C1			C2, C2L, I2, I2L			C3, I3, I3L, I3YY			C4,I4			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Transmitter														
True Differential I/O Standards - f_{HSDR} (data rate)	SERDES factor J = 3 to 10 (9), (11), (12), (13), (14), (15), (16)	(6)	—	1600	(6)	—	1434	(6)	—	1250	(6)	—	1050	Mbps
	SERDES factor J ≥ 4 LVDS TX with DPA (12), (14), (15), (16)	(6)	—	1600	(6)	—	1600	(6)	—	1600	(6)	—	1250	Mbps
	SERDES factor J = 2, uses DDR Registers	(6)	—	(7)	(6)	—	(7)	(6)	—	(7)	(6)	—	(7)	Mbps
	SERDES factor J = 1, uses SDR Register	(6)	—	(7)	(6)	—	(7)	(6)	—	(7)	(6)	—	(7)	Mbps
Emulated Differential I/O Standards with Three External Output Resistor Networks - f_{HSDR} (data rate) (10)	SERDES factor J = 4 to 10 (17)	(6)	—	1100	(6)	—	1100	(6)	—	840	(6)	—	840	Mbps
$t_{x\ Jitter}$ - True Differential I/O Standards	Total Jitter for Data Rate 600 Mbps - 1.25 Gbps	—	—	160	—	—	160	—	—	160	—	—	160	ps
	Total Jitter for Data Rate < 600 Mbps	—	—	0.1	—	—	0.1	—	—	0.1	—	—	0.1	UI
$t_{x\ Jitter}$ - Emulated Differential I/O Standards with Three External Output Resistor Network	Total Jitter for Data Rate 600 Mbps - 1.25 Gbps	—	—	300	—	—	300	—	—	300	—	—	325	ps
	Total Jitter for Data Rate < 600 Mbps	—	—	0.2	—	—	0.2	—	—	0.2	—	—	0.25	UI

Table 42. Memory Output Clock Jitter Specification for Stratix V Devices (1), (Part 2 of 2) (2), (3)

Clock Network	Parameter	Symbol	C1		C2, C2L, I2, I2L		C3, I3, I3L, I3YY		C4,I4		Unit
			Min	Max	Min	Max	Min	Max	Min	Max	
PHY Clock	Clock period jitter	$t_{JIT(per)}$	–25	25	–25	25	–30	30	–35	35	ps
	Cycle-to-cycle period jitter	$t_{JIT(cc)}$	–50	50	–50	50	–60	60	–70	70	ps
	Duty cycle jitter	$t_{JIT(duty)}$	–37.5	37.5	–37.5	37.5	–45	45	–56	56	ps

Notes to Table 42:

(1) The clock jitter specification applies to the memory output clock pins generated using differential signal-splitter and DDIO circuits clocked by a PLL output routed on a PHY, regional, or global clock network as specified. Altera recommends using PHY clock networks whenever possible.

(2) The clock jitter specification applies to the memory output clock pins clocked by an integer PLL.

(3) The memory output clock jitter is applicable when an input jitter of 30 ps peak-to-peak is applied with bit error rate (BER) -12, equivalent to 14 sigma.

OCT Calibration Block Specifications

Table 43 lists the OCT calibration block specifications for Stratix V devices.

Table 43. OCT Calibration Block Specifications for Stratix V Devices

Symbol	Description	Min	Typ	Max	Unit
OCTUSRCLK	Clock required by the OCT calibration blocks	—	—	20	MHz
T_{OCTCAL}	Number of OCTUSRCLK clock cycles required for OCT R_S/R_T calibration	—	1000	—	Cycles
$T_{OCTSHIFT}$	Number of OCTUSRCLK clock cycles required for the OCT code to shift out	—	32	—	Cycles
T_{RS_RT}	Time required between the `dyn_term_ctrl` and `oe` signal transitions in a bidirectional I/O buffer to dynamically switch between OCT R_S and R_T (Figure 10)	—	2.5	—	ns

Figure 10 shows the timing diagram for the `oe` and `dyn_term_ctrl` signals.

Figure 10. Timing Diagram for oe and dyn_term_ctrl Signals

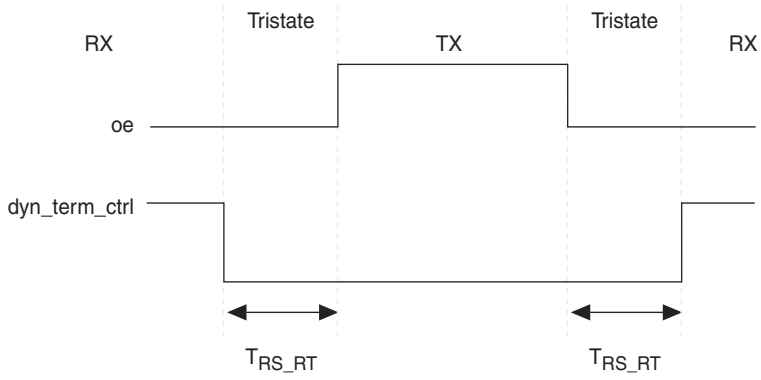


Table 46. JTAG Timing Parameters and Values for Stratix V Devices

Symbol	Description	Min	Max	Unit
t_{JPH}	JTAG port hold time	5	—	ns
t_{JPCO}	JTAG port clock to output	—	11 (1)	ns
t_{JPZX}	JTAG port high impedance to valid output	—	14 (1)	ns
t_{JPXZ}	JTAG port valid output to high impedance	—	14 (1)	ns

Notes to Table 46:

(1) A 1 ns adder is required for each V_{CCIO} voltage step down from 3.0 V. For example, t_{JPCO} = 12 ns if V_{CCIO} of the TDO I/O bank = 2.5 V, or 13 ns if it equals 1.8 V.

(2) The minimum TCK clock period is 167 ns if VCCBAT is within the range 1.2V-1.5V when you perform the volatile key programming.

Raw Binary File Size

For the POR delay specification, refer to the "POR Delay Specification" section of the "Configuration, Design Security, and Remote System Upgrades in Stratix V Devices".

Table 47 lists the uncompressed raw binary file (**.rbf**) sizes for Stratix V devices.

Table 47. Uncompressed .rbf Sizes for Stratix V Devices

Family	Device	Package	Configuration .rbf Size (bits)	IOCSR .rbf Size (bits) (4), (5)
Stratix V GX	5SGXA3	H35, F40, F35 (2)	213,798,880	562,392
		H29, F35 (3)	137,598,880	564,504
	5SGXA4	—	213,798,880	563,672
	5SGXA5	—	269,979,008	562,392
	5SGXA7	—	269,979,008	562,392
	5SGXA9	—	342,742,976	700,888
	5SGXAB	—	342,742,976	700,888
	5SGXB5	—	270,528,640	584,344
	5SGXB6	—	270,528,640	584,344
	5SGXB9	—	342,742,976	700,888
	5SGXBB	—	342,742,976	700,888
Stratix V GT	5SGTC5	—	269,979,008	562,392
	5SGTC7	—	269,979,008	562,392
Stratix V GS	5SGSD3	—	137,598,880	564,504
	5SGSD4	F1517	213,798,880	563,672
		—	137,598,880	564,504
	5SGSD5	—	213,798,880	563,672
	5SGSD6	—	293,441,888	565,528
	5SGSD8	—	293,441,888	565,528

Table 54 lists the PS configuration timing parameters for Stratix V devices.

Table 54. PS Timing Parameters for Stratix V Devices

Symbol	Parameter	Minimum	Maximum	Units
t_{CF2CD}	nCONFIG low to CONF_DONE low	—	600	ns
t_{CF2ST0}	nCONFIG low to nSTATUS low	—	600	ns
t_{CFG}	nCONFIG low pulse width	2	—	µs
t_{STATUS}	nSTATUS low pulse width	268	1,506 (1)	µs
t_{CF2ST1}	nCONFIG high to nSTATUS high	—	1,506 (2)	µs
t_{CF2CK} (5)	nCONFIG high to first rising edge on DCLK	1,506	—	µs
t_{ST2CK} (5)	nSTATUS high to first rising edge of DCLK	2	—	µs
t_{DSU}	DATA[] setup time before rising edge on DCLK	5.5	—	ns
t_{DH}	DATA[] hold time after rising edge on DCLK	0	—	ns
t_{CH}	DCLK high time	$0.45 \times 1/f_{MAX}$	—	s
t_{CL}	DCLK low time	$0.45 \times 1/f_{MAX}$	—	s
t_{CLK}	DCLK period	$1/f_{MAX}$	—	s
f_{MAX}	DCLK frequency	—	125	MHz
t_{CD2UM}	CONF_DONE high to user mode (3)	175	437	µs
t_{CD2CU}	CONF_DONE high to CLKUSR enabled	4 × maximum DCLK period	—	—
t_{CD2UMC}	CONF_DONE high to user mode with CLKUSR option on	t_{CD2CU} + (8576 × CLKUSR period) (4)	—	—

Notes to Table 54:

(1) This value is applicable if you do not delay configuration by extending the nCONFIG or nSTATUS low pulse width.

(2) This value is applicable if you do not delay configuration by externally holding the nSTATUS low.

(3) The minimum and maximum numbers apply only if you choose the internal oscillator as the clock source for initializing the device.

(4) To enable the CLKUSR pin as the initialization clock source and to obtain the maximum frequency specification on these pins, refer to the "Initialization" section.

(5) If nSTATUS is monitored, follow the t_{ST2CK} specification. If nSTATUS is not monitored, follow the t_{CF2CK} specification.

Initialization

Table 55 lists the initialization clock source option, the applicable configuration schemes, and the maximum frequency.

Table 55. Initialization Clock Source Option and the Maximum Frequency

Initialization Clock Source	Configuration Schemes	Maximum Frequency	Minimum Number of Clock Cycles (1)
Internal Oscillator	AS, PS, FPP	12.5 MHz	8576
CLKUSR	AS, PS, FPP (2)	125 MHz	
DCLK	PS, FPP	125 MHz	

Notes to Table 55:

(1) The minimum number of clock cycles required for device initialization.

(2) To enable CLKUSR as the initialization clock source, turn on the **Enable user-supplied start-up clock (CLKUSR)** option in the Quartus II software from the **General** panel of the **Device and Pin Options** dialog box.

Remote System Upgrades

Table 56 lists the timing parameter specifications for the remote system upgrade circuitry.

Table 56. Remote System Upgrade Circuitry Timing Specifications

Parameter	Minimum	Maximum	Unit
$t_{RU\_nCONFIG}$ (1)	250	—	ns
$t_{RU\_nRSTIMER}$ (2)	250	—	ns

Notes to Table 56:

(1) This is equivalent to strobing the reconfiguration input of the ALTREMOTE_UPDATE megafunction high for the minimum timing specification. For more information, refer to the Remote System Upgrade State Machine section of the "Configuration, Design Security, and Remote System Upgrades in Stratix V Devices" chapter.

(2) This is equivalent to strobing the reset_timer input of the ALTREMOTE_UPDATE megafunction high for the minimum timing specification. For more information, refer to the User Watchdog Timer section of the "Configuration, Design Security, and Remote System Upgrades in Stratix V Devices" chapter.

User Watchdog Internal Circuitry Timing Specification

Table 57 lists the operating range of the 12.5-MHz internal oscillator.

Table 57. 12.5-MHz Internal Oscillator Specifications

Minimum	Typical	Maximum	Units
5.3	7.9	12.5	MHz

I/O Timing

Altera offers two ways to determine I/O timing—the Excel-based I/O Timing and the Quartus II Timing Analyzer.

Excel-based I/O timing provides pin timing performance for each device density and speed grade. The data is typically used prior to designing the FPGA to get an estimate of the timing budget as part of the link timing analysis. The Quartus II Timing Analyzer provides a more accurate and precise I/O timing data based on the specifics of the design after you complete place-and-route.

You can download the Excel-based I/O Timing spreadsheet from the Stratix V Devices Documentation web page.

Programmable IOE Delay

Table 58 lists the Stratix V IOE programmable delay settings.

Table 58. IOE Programmable Delay for Stratix V Devices (Part 1 of 2)

Parameter (1)	Available Settings	Min Offset (2)	Fast Model		Slow Model							
			Industrial	Commercial	C1	C2	C3	C4	I2	I3, I3YY	I4	Unit
D1	64	0	0.464	0.493	0.838	0.838	0.924	1.011	0.844	0.921	1.006	ns
D2	32	0	0.230	0.244	0.415	0.415	0.459	0.503	0.417	0.456	0.500	ns

Table 58. IOE Programmable Delay for Stratix V Devices (Part 2 of 2)

Parameter (1)	Available Settings	Min Offset (2)	Fast Model		Slow Model							
			Industrial	Commercial	C1	C2	C3	C4	I2	I3, I3YY	I4	Unit
D3	8	0	1.587	1.699	2.793	2.793	2.992	3.192	2.811	3.047	3.257	ns
D4	64	0	0.464	0.492	0.838	0.838	0.924	1.011	0.843	0.920	1.006	ns
D5	64	0	0.464	0.493	0.838	0.838	0.924	1.011	0.844	0.921	1.006	ns
D6	32	0	0.229	0.244	0.415	0.415	0.458	0.503	0.418	0.456	0.499	ns

Notes to Table 58:

(1) You can set this value in the Quartus II software by selecting **D1**, **D2**, **D3**, **D5**, and **D6** in the **Assignment Name** column of **Assignment Editor**.

(2) Minimum offset does not include the intrinsic delay.

Programmable Output Buffer Delay

Table 59 lists the delay chain settings that control the rising and falling edge delays of the output buffer. The default delay is 0 ps.

Table 59. Programmable Output Buffer Delay for Stratix V Devices (1)

Symbol	Parameter	Typical	Unit
D_{OUTBUF}	Rising and/or falling edge delay	0 (default)	ps
		25	ps
		50	ps
		75	ps

Note to Table 59:

(1) You can set the programmable output buffer delay in the Quartus II software by setting the **Output Buffer Delay Control** assignment to either positive, negative, or both edges, with the specific values stated here (in ps) for the **Output Buffer Delay** assignment.

Glossary

Table 60 lists the glossary for this chapter.

Table 60. Glossary (Part 1 of 4)

Letter	Subject	Definitions
A B C	—	—
D	—	—
E	—	—
F	f_{HSCLK}	Left and right PLL input clock frequency.
	f_{HSDR}	High-speed I/O block—Maximum and minimum **LVDS** data transfer rate (f_{HSDR} = 1/TUI), non-DPA.
	$f_{HSDRDPA}$	High-speed I/O block—Maximum and minimum **LVDS** data transfer rate ($f_{HSDRDPA}$ = 1/TUI), DPA.

Table 60. Glossary (Part 2 of 4)

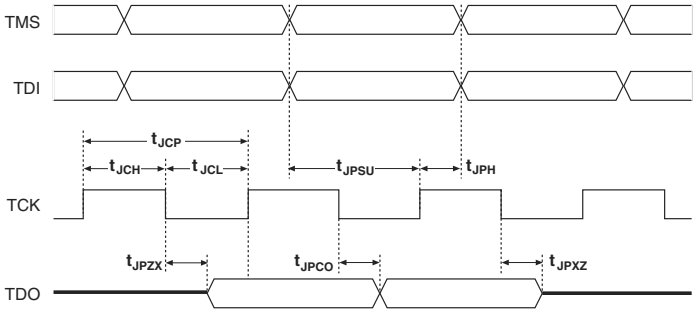
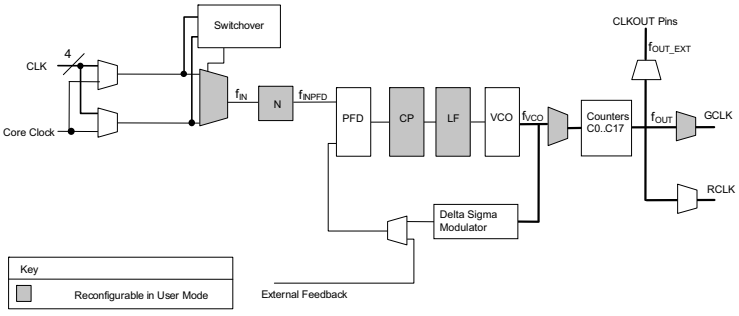
Letter	Subject	Definitions
G H I	—	—
J	J	High-speed I/O block—Deserialization factor (width of parallel data bus).
J	JTAG Timing Specifications	JTAG Timing Specifications: 
K L M N O	—	—
P	**PLL Specifications**	**Diagram of PLL Specifications** *(1)*  **Note:** (1) `Core Clock` can only be fed by dedicated clock input pins or PLL outputs.
Q	—	—
R	R_L	Receiver differential input discrete resistor (external to the Stratix V device).

Table 61. Document Revision History (Part 2 of 3)

Date	Version	Changes
November 2014	3.3	■ Added the I3YY speed grade and changed the data rates for the GX channel in Table 1. ■ Added the I3YY speed grade to the V_{CC} description in Table 6. ■ Added the I3YY speed grade to V_{CCHIP_L}, V_{CCHIP_R}, V_{CCHSSI_L}, and V_{CCHSSI_R} descriptions in Table 7. ■ Added 240-Ω to Table 11. ■ Changed CDR PPM tolerance in Table 23. ■ Added additional max data rate for fPLL in Table 23. ■ Added the I3YY speed grade and changed the data rates for transceiver speed grade 3 in Table 25. ■ Added the I3YY speed grade and changed the data rates for transceiver speed grade 3 in Table 26. ■ Changed CDR PPM tolerance in Table 28. ■ Added additional max data rate for fPLL in Table 28. ■ Changed the mode descriptions for MLAB and M20K in Table 33. ■ Changed the Max value of f_{HSCLK_OUT} for the C2, C2L, I2, I2L speed grades in Table 36. ■ Changed the frequency ranges for C1 and C2 in Table 39. ■ Changed the **.rbf** file sizes for 5SGSD6 and 5SGSD8 in Table 47. ■ Added note about `nSTATUS` to Table 50, Table 51, Table 54. ■ Changed the available settings in Table 58. ■ Changed the note in “Periphery Performance”. ■ Updated the “I/O Standard Specifications” section. ■ Updated the “Raw Binary File Size” section. ■ Updated the receiver voltage input range in Table 22. ■ Updated the max frequency for the LVDS clock network in Table 36. ■ Updated the `DCLK` note to Figure 11. ■ Updated Table 23 VO_{CM} (DC Coupled) condition. ■ Updated Table 6 and Table 7. ■ Added the `DCLK` specification to Table 55. ■ Updated the notes for Table 47. ■ Updated the list of parameters for Table 56.
November 2013	3.2	■ Updated Table 28
November 2013	3.1	■ Updated Table 33
November 2013	3.0	■ Updated Table 23 and Table 28
October 2013	2.9	■ Updated the “Transceiver Characterization” section
October 2013	2.8	■ Updated Table 3, Table 12, Table 14, Table 19, Table 20, Table 23, Table 24, Table 28, Table 30, Table 31, Table 32, Table 33, Table 36, Table 39, Table 40, Table 41, Table 42, Table 47, Table 53, Table 58, and Table 59 ■ Added Figure 1 and Figure 3 ■ Added the “Transceiver Characterization” section ■ Removed all “Preliminary” designations.