#### Intel - 5SGXEA5K2F40I2L Datasheet





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#### **Applications of Embedded - FPGAs**

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

#### Details

Product Status	Obsolete
Number of LABs/CLBs	185000
Number of Logic Elements/Cells	490000
Total RAM Bits	46080000
Number of I/O	696
Number of Gates	-
Voltage - Supply	0.82V ~ 0.88V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	1517-BBGA, FCBGA
Supplier Device Package	1517-FBGA (40x40)
Purchase URL	https://www.e-xfl.com/product-detail/intel/5sgxea5k2f40i2l

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Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

Symbol	Description	Minimum	Maximum	Unit
V <sub>CCD_FPLL</sub>	PLL digital power supply	-0.5	1.8	V
V <sub>CCA_FPLL</sub>	PLL analog power supply	-0.5	3.4	V
VI	DC input voltage	-0.5	3.8	V
TJ	Operating junction temperature	-55	125	°C
T <sub>STG</sub>	Storage temperature (No bias)	-65	150	°C
I <sub>OUT</sub>	DC output current per pin	-25	40	mA

Table 3. Absolute Maximum Ratings for Stratix V Devices (Part 2 of 2)

Table 4 lists the absolute conditions for the transceiver power supply for Stratix V GX, GS, and GT devices.

Table 4. Transceiver Power Supply Absolute Conditions for Stratix V GX, GS, and GT Devices

Symbol	Description	Devices	Minimum	Maximum	Unit
V <sub>CCA_GXBL</sub>	Transceiver channel PLL power supply (left side)	GX, GS, GT	-0.5	3.75	V
V <sub>CCA_GXBR</sub>	Transceiver channel PLL power supply (right side)	GX, GS	-0.5	3.75	V
V <sub>CCA_GTBR</sub>	Transceiver channel PLL power supply (right side)	GT	-0.5	3.75	V
V <sub>CCHIP_L</sub>	Transceiver hard IP power supply (left side)	GX, GS, GT	-0.5	1.35	V
V <sub>CCHIP_R</sub>	Transceiver hard IP power supply (right side)	GX, GS, GT	-0.5	1.35	V
V <sub>CCHSSI_L</sub>	Transceiver PCS power supply (left side)	GX, GS, GT	-0.5	1.35	V
V <sub>CCHSSI_R</sub>	Transceiver PCS power supply (right side)	GX, GS, GT	-0.5	1.35	V
V <sub>CCR_GXBL</sub>	Receiver analog power supply (left side)	GX, GS, GT	-0.5	1.35	V
V <sub>CCR_GXBR</sub>	Receiver analog power supply (right side)	GX, GS, GT	-0.5	1.35	V
V <sub>CCR_GTBR</sub>	Receiver analog power supply for GT channels (right side)	GT	-0.5	1.35	V
V <sub>CCT_GXBL</sub>	Transmitter analog power supply (left side)	GX, GS, GT	-0.5	1.35	V
V <sub>CCT_GXBR</sub>	Transmitter analog power supply (right side)	GX, GS, GT	-0.5	1.35	V
V <sub>CCT_GTBR</sub>	Transmitter analog power supply for GT channels (right side)	GT	-0.5	1.35	V
V <sub>CCL_GTBR</sub>	Transmitter clock network power supply (right side)	GT	-0.5	1.35	V
V <sub>CCH_GXBL</sub>	Transmitter output buffer power supply (left side)	GX, GS, GT	-0.5	1.8	V
V <sub>CCH_GXBR</sub>	Transmitter output buffer power supply (right side)	GX, GS, GT	-0.5	1.8	V

#### **Maximum Allowed Overshoot and Undershoot Voltage**

During transitions, input signals may overshoot to the voltage shown in Table 5 and undershoot to -2.0 V for input currents less than 100 mA and periods shorter than 20 ns.

Symbol	Description	Condition	Min <sup>(4)</sup>	Тур	Max <sup>(4)</sup>	Unit
t <sub>RAMP</sub>	Power supply ramp time	Standard POR	200 µs	_	100 ms	—
		Fast POR	200 µs		4 ms	

#### Table 6. Recommended Operating Conditions for Stratix V Devices (Part 2 of 2)

#### Notes to Table 6:

(1)  $V_{CCPD}$  must be 2.5 V when  $V_{CCI0}$  is 2.5, 1.8, 1.5, 1.35, 1.25 or 1.2 V.  $V_{CCPD}$  must be 3.0 V when  $V_{CCI0}$  is 3.0 V.

(2) If you do not use the design security feature in Stratix V devices, connect V<sub>CCBAT</sub> to a 1.2- to 3.0-V power supply. Stratix V power-on-reset (POR) circuitry monitors V<sub>CCBAT</sub>. Stratix V devices will not exit POR if V<sub>CCBAT</sub> stays at logic low.

(3) C2L and I2L can also be run at 0.90 V for legacy boards that were designed for the C2 and I2 speed grades.

(4) The power supply value describes the budget for the DC (static) power supply tolerance and does not include the dynamic tolerance requirements. Refer to the PDN tool for the additional budget for the dynamic tolerance requirements.

Table 7 lists the transceiver power supply recommended operating conditions for Stratix V GX, GS, and GT devices.

# Table 7. Recommended Transceiver Power Supply Operating Conditions for Stratix V GX, GS, and GT Devices (Part 1 of 2)

Symbol	Description	Devices	Minimum <sup>(4)</sup>	Typical	Maximum <sup>(4)</sup>	Unit
V <sub>CCA GXBL</sub>	Transceiver channel PLL power supply (left		2.85	3.0	3.15	V
(1), (3)	side)	un, us, ui	2.375	2.5	2.625	v
V <sub>CCA_GXBR</sub>	Transceiver channel PLL power supply (right	CV CS	2.85	3.0	3.15	V
(1), (3)	side)	ux, us	2.375	2.5	2.625	v
V <sub>CCA_GTBR</sub>	Transceiver channel PLL power supply (right side)	GT	2.85	3.0	3.15	V
	Transceiver hard IP power supply (left side; C1, C2, I2, and I3YY speed grades)	GX, GS, GT	0.87	0.9	0.93	V
V <sub>CCHIP_L</sub>	Transceiver hard IP power supply (left side; C2L, C3, C4, I2L, I3, I3L, and I4 speed grades)	GX, GS, GT	0.82	0.85	0.88	V
	Transceiver hard IP power supply (right side; C1, C2, I2, and I3YY speed grades)	GX, GS, GT	0.87	0.9	0.93	V
V <sub>CCHIP_R</sub>	Transceiver hard IP power supply (right side; C2L, C3, C4, I2L, I3, I3L, and I4 speed grades)	GX, GS, GT	0.82	0.85	0.88	V
	Transceiver PCS power supply (left side; C1, C2, I2, and I3YY speed grades)	GX, GS, GT	0.87	0.9	0.93	V
V <sub>CCHSSI_L</sub>	Transceiver PCS power supply (left side; C2L, C3, C4, I2L, I3, I3L, and I4 speed grades)	GX, GS, GT	0.82	0.85	0.88	V
	Transceiver PCS power supply (right side; C1, C2, I2, and I3YY speed grades)	GX, GS, GT	0.87	0.9	0.93	V
V <sub>CCHSSI_R</sub>	Transceiver PCS power supply (right side; C2L, C3, C4, I2L, I3, I3L, and I4 speed grades)	GX, GS, GT	0.82	0.85	0.88	V
			0.82	0.85	0.88	
V <sub>CCR_GXBL</sub>	Receiver analog nower supply (left side)		0.87	0.90	0.93	v
(2) _	Therefore analog power supply (left Slue)	un, uo, ui	0.97	1.0	1.03	v
			1.03	1.05	1.07	

#### I/O Pin Leakage Current

Table 9 lists the Stratix V I/O pin leakage current specifications.

Table 9.	I/O Pin	Leakage	<b>Current for</b>	Stratix V	Devices (1)
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Symbol	Description	Conditions	Min	Тур	Max	Unit
I <sub>I</sub>	Input pin	$V_I = 0 V \text{ to } V_{CCIOMAX}$	-30	_	30	μA
I <sub>OZ</sub>	Tri-stated I/O pin	$V_0 = 0 V \text{ to } V_{\text{CCIOMAX}}$	-30		30	μA

#### Note to Table 9:

(1) If  $V_0 = V_{CCI0}$  to  $V_{CCI0Max}$ , 100  $\mu$ A of leakage current per I/O is expected.

#### **Bus Hold Specifications**

Table 10 lists the Stratix V device family bus hold specifications.

Table 10. Bus Hold Parameters for Stratix V Devices

			V <sub>CCI0</sub>										
Parameter	Symbol	Conditions	1.2	2 V	1.	5 V	1.8	B V	2.5	5 V	3.0	V	Unit
			Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Low sustaining current	I <sub>SUSL</sub>	V <sub>IN</sub> > V <sub>IL</sub> (maximum)	22.5	_	25.0	_	30.0	_	50.0	_	70.0	_	μA
High sustaining current	I <sub>SUSH</sub>	V <sub>IN</sub> < V <sub>IH</sub> (minimum)	-22.5		-25.0	_	-30.0	_	-50.0	_	-70.0		μA
Low overdrive current	I <sub>odl</sub>	$0V < V_{IN} < V_{CCIO}$		120		160		200	_	300		500	μA
High overdrive current	I <sub>odh</sub>	$0V < V_{IN} < V_{CCIO}$		-120		-160		-200		-300		-500	μΑ
Bus-hold trip point	V <sub>TRIP</sub>	_	0.45	0.95	0.50	1.00	0.68	1.07	0.70	1.70	0.80	2.00	۷

#### **On-Chip Termination (OCT) Specifications**

If you enable OCT calibration, calibration is automatically performed at power-up for I/Os connected to the calibration block. Table 11 lists the Stratix V OCT termination calibration accuracy specifications.

Table 11. OCT Calibration Accuracy Specifications for Stratix V Devices <sup>(1)</sup> (Part 1 of 2)

			Calibration Accuracy					
Symbol	Description	Conditions	C1	C2,12	C3,I3, I3YY	C4,14	Unit	
25- $Ω$ R <sub>S</sub>	Internal series termination with calibration (25- $\Omega$ setting)	V <sub>CCI0</sub> = 3.0, 2.5, 1.8, 1.5, 1.2 V	±15	±15	±15	±15	%	

Symbol	Description	V <sub>CCIO</sub> (V)	Typical	Unit	
dR/dT		3.0	0.189		
	OCT variation with temperature without recalibration	2.5	0.208		
		1.8	0.266	%/°C	
		1.5	0.273	1	
		1.2	0.317		

Table 13. OCT Variation after Power-Up Calibration for Stratix V Devices (Part 2 of 2)<sup>(1)</sup>

#### Note to Table 13:

(1) Valid for a  $V_{CCIO}$  range of  $\pm 5\%$  and a temperature range of 0° to 85°C.

#### **Pin Capacitance**

Table 14 lists the Stratix V device family pin capacitance.

#### Table 14. Pin Capacitance for Stratix V Devices

Symbol	Description	Value	Unit
CIOTB	Input capacitance on the top and bottom I/O pins	6	pF
C <sub>IOLR</sub>	Input capacitance on the left and right I/O pins	6	рF
C <sub>OUTFB</sub>	Input capacitance on dual-purpose clock output and feedback pins	6	pF

#### **Hot Socketing**

Table 15 lists the hot socketing specifications for Stratix V devices.

Symbol	Description	Maximum
I <sub>IOPIN (DC)</sub>	DC current per I/O pin	300 μA
I <sub>IOPIN (AC)</sub>	AC current per I/O pin	8 mA <sup>(1)</sup>
IXCVR-TX (DC)	DC current per transceiver transmitter pin	100 mA
IXCVR-RX (DC)	DC current per transceiver receiver pin	50 mA

#### Note to Table 15:

(1) The I/O ramp rate is 10 ns or more. For ramp rates faster than 10 ns,  $|I_{10PIN}| = C dv/dt$ , in which C is the I/O pin capacitance and dv/dt is the slew rate.

## **Switching Characteristics**

This section provides performance characteristics of the Stratix V core and periphery blocks.

These characteristics can be designated as Preliminary or Final.

- Preliminary characteristics are created using simulation results, process data, and other known parameters. The title of these tables show the designation as "Preliminary."
- Final numbers are based on actual silicon characterization and testing. The numbers reflect the actual performance of the device under worst-case silicon process, voltage, and junction temperature conditions. There are no designations on finalized tables.

### **Transceiver Performance Specifications**

This section describes transceiver performance specifications.

Table 23 lists the Stratix V GX and GS transceiver specifications.

Table 23.	Transceiver 3	Specifications	for Stratix	V GX	and GS	Devices	(1)	(Part 1	nf 7	۱
Table 20.	TIANSUCIACI	opeonitionationa	IUI UIIAIIA	I UA	anu uu	DEVICES	• •	(1 61 6 1		

Symbol/	Conditions	Tra	nsceive Grade	r Speed 1	Trai	nsceive Grade	r Speed 2	Transceiver Speed Grade 3			Unit
Description		Min	Тур	Max	Min	Тур	Max	Min	Тур	Max	
Reference Clock											
Supported I/O	Dedicated reference clock pin	1.2-V	PCML,	1.4-V PCM	IL, 1.5-∖	/ PCML	, 2.5-V PCN HCSL	1L, Diffe	rential	LVPECL, L\	/DS, and
Standards	RX reference clock pin		1.4-V PCML, 1.5-V PCML, 2.5-V PCML, LVPECL, and LVDS								
Input Reference Clock Frequency (CMU PLL) <sup>(8)</sup>	_	40		710	40	_	710	40	_	710	MHz
Input Reference Clock Frequency (ATX PLL) <sup>(8)</sup>		100		710	100		710	100		710	MHz
Rise time	Measure at ±60 mV of differential signal <sup>(26)</sup>			400	_		400			400	ns
Fall time	Measure at ±60 mV of differential signal <sup>(26)</sup>		_	400	_		400			400	μσ
Duty cycle		45		55	45		55	45	—	55	%
Spread-spectrum modulating clock frequency	PCI Express® (PCIe <sup>®</sup> )	30		33	30		33	30	_	33	kHz

Symbol/	Conditions	Trai	nsceive Grade	r Speed 1	Trai	nsceive Grade	r Speed 2	Trar	Unit		
Description		Min	Тур	Max	Min	Тур	Max	Min	Тур	Max	
Reconfiguration clock (mgmt_clk_clk) frequency	_	100		125	100		125	100	_	125	MHz
Receiver											
Supported I/O Standards	_			1.4-V PCMI	L, 1.5-V	PCML,	2.5-V PCM	L, LVPE	CL, and	d LVDS	
Data rate (Standard PCS) (9), (23)	_	600	_	12200	600	_	12200	600	_	8500/ 10312.5 (24)	Mbps
Data rate (10G PCS) <sup>(9),</sup> <sup>(23)</sup>	_	600	_	14100	600	_	12500	600	_	8500/ 10312.5 (24)	Mbps
Absolute V <sub>MAX</sub> for a receiver pin <sup>(5)</sup>	_	_	_	1.2	_	_	1.2	_	_	1.2	V
Absolute V <sub>MIN</sub> for a receiver pin	_	-0.4	_	_	-0.4	_	_	-0.4	_	_	V
Maximum peak- to-peak differential input voltage V <sub>ID</sub> (diff p- p) before device configuration <sup>(22)</sup>	_	_	_	1.6	_	_	1.6	_		1.6	V
Maximum peak- to-peak	V <sub>CCR_GXB</sub> = 1.0 V/1.05 V (V <sub>ICM</sub> = 0.70 V)	_	_	2.0	_	_	2.0	_	_	2.0	V
voltage $V_{ID}$ (diff p- p) after device configuration <sup>(18)</sup> .	$V_{CCR_GXB} = 0.90 V$ (V <sub>ICM</sub> = 0.6 V)			2.4			2.4			2.4	V
configuration <sup>(18)</sup> , (22)	$V_{CCR_GXB} = 0.85 V$ (V <sub>ICM</sub> = 0.6 V)			2.4			2.4		_	2.4	V
Minimum differential eye opening at receiver serial input pins <sup>(6), (22),</sup> (27)	_	85			85			85	_	_	mV

### Table 23. Transceiver Specifications for Stratix V GX and GS Devices <sup>(1)</sup> (Part 3 of 7)

Symbol/	Conditions	Trai	nsceive Grade	r Speed 1	Trai	nsceive Grade	r Speed 2	Trai	nsceive Grade	r Speed 3	Unit
Description		Min	Тур	Max	Min	Тур	Max	Min	Тур	Max	
	DC Gain Setting = 0		0	_	_	0	_	_	0	—	dB
	DC Gain Setting = 1	_	2		_	2	_	_	2	_	dB
Programmable DC gain	DC Gain Setting = 2	_	4	_	_	4	_	_	4	_	dB
	DC Gain Setting = 3	_	6	_	_	6	_	_	6	_	dB
	DC Gain Setting = 4		8			8	—		8	_	dB
Transmitter											
Supported I/O Standards	_	1.4-V and 1.5-V PCML									
Data rate (Standard PCS)	_	600	_	12200	600	_	12200	600	_	8500/ 10312.5 (24)	Mbps
Data rate (10G PCS)	_	600	_	14100	600	_	12500	600	_	8500/ 10312.5 (24)	Mbps
	85-Ω setting	_	85 ± 20%	_	_	85 ± 20%	_	_	85 ± 20%	—	Ω
Differential on-	100-Ω setting	_	100 ± 20%	_	_	100 ± 20%	_	_	100 ± 20%	_	Ω
chip termination resistors	120-Ω setting		120 ± 20%	_		120 ± 20%	_		120 ± 20%	_	Ω
	150-Ω setting	_	150 ± 20%			150 ± 20%	_		150 ± 20%	_	Ω
V <sub>OCM</sub> (AC coupled)	0.65-V setting	_	650		_	650	_	_	650	—	mV
V <sub>OCM</sub> (DC coupled)	_	_	650	_	_	650		_	650	_	mV
Rise time <sup>(7)</sup>	20% to 80%	30	—	160	30	—	160	30	—	160	ps
Fall time <sup>(7)</sup>	80% to 20%	30		160	30		160	30	—	160	ps
Intra-differential pair skew	Tx V <sub>CM</sub> = 0.5 V and slew rate of 15 ps	_	_	15			15		_	15	ps
Intra-transceiver block transmitter channel-to- channel skew	x6 PMA bonded mode	_	_	120	_	_	120	_		120	ps

#### Table 23. Transceiver Specifications for Stratix V GX and GS Devices <sup>(1)</sup> (Part 5 of 7)

### Table 23. Transceiver Specifications for Stratix V GX and GS Devices <sup>(1)</sup> (Part 6 of 7)

Symbol/	Conditions	Trai	nsceive Grade	r Speed 1	Trar	isceive Grade	r Speed 2	Tran	isceive Grade	er Speed e 3	Unit
Description		Min	Тур	Max	Min	Тур	Max	Min	Тур	Max	
Inter-transceiver block transmitter channel-to- channel skew	xN PMA bonded mode	_	_	500	_	_	500	_	_	500	ps
CMU PLL	•										
Supported Data Range	_	600	_	12500	600	_	12500	600	_	8500/ 10312.5 (24)	Mbps
t <sub>pll_powerdown</sub> <sup>(15)</sup>	—	1			1			1			μs
t <sub>pll_lock</sub> <sup>(16)</sup>		—		10	—	_	10	—	_	10	μs
ATX PLL											
	VCO post-divider L=2	8000	_	14100	8000	_	12500	8000	_	8500/ 10312.5 (24)	Mbps
Supported Data	L=4	4000	_	7050	4000	_	6600	4000	—	6600	Mbps
Rate Range	L=8	2000		3525	2000		3300	2000		3300	Mbps
	L=8, Local/Central Clock Divider =2	1000	_	1762.5	1000	_	1762.5	1000	_	1762.5	Mbps
t <sub>pll_powerdown</sub> (15)	—	1	_	—	1	_	—	1	_	—	μs
t <sub>pll_lock</sub> (16)	—		—	10		—	10	—		10	μs
fPLL	•										
Supported Data Range	_	600	_	3250/ 3125 <sup>(25)</sup>	600	_	3250/ 3125 <sup>(25)</sup>	600	_	3250/ 3125 <sup>(25)</sup>	Mbps
t <sub>pll_powerdown</sub> <sup>(15)</sup>	_	1	—		1	—		1			μs

Symbol/	Conditions	s	Transceive peed Grade	r 2	S	Transceive peed Grade	r 3	Unit		
Description		Min	Тур	Max	Min	Тур	Max			
Reference Clock								1		
Supported I/O Standards	Dedicated reference clock pin	1.2-V PCN	IL, 1.4-V PC	ML, 1.5-V P(	CML, 2.5-V I and HCSL	PCML, Diffe	rential LVPE	ECL, LVDS,		
otanuarus	RX reference clock pin		1.4-V PCML, 1.5-V PCML, 2.5-V PCML, LVPECL, and LVDS							
Input Reference Clock Frequency (CMU PLL) <sup>(6)</sup>	_	40	_	710	40	_	710	MHz		
Input Reference Clock Frequency (ATX PLL) <sup>(6)</sup>	_	100	_	710	100	_	710	MHz		
Rise time	20% to 80%	_		400	_	_	400			
Fall time	80% to 20%			400	—	_	400	ps		
Duty cycle	—	45	_	55	45	_	55	%		
Spread-spectrum modulating clock frequency	PCI Express (PCIe)	30	_	33	30	_	33	kHz		
Spread-spectrum downspread	PCle	_	0 to -0.5	_	_	0 to -0.5	_	%		
On-chip termination resistors <sup>(19)</sup>	_	_	100	_	_	100	_	Ω		
Absolute V <sub>MAX</sub> <sup>(3)</sup>	Dedicated reference clock pin	_	_	1.6	_	_	1.6	V		
	RX reference clock pin	_	_	1.2	_	_	1.2			
Absolute V <sub>MIN</sub>	—	-0.4		—	-0.4	—		V		
Peak-to-peak differential input voltage	_	200	_	1600	200	_	1600	mV		
V <sub>ICM</sub> (AC coupled)	Dedicated reference clock pin		1050/1000 <sup>(,</sup>	2)	1	050/1000 (	2)	mV		
	RX reference clock pin	1	.0/0.9/0.85 (	22)	1.	0/0.9/0.85 (	(22)	V		
V <sub>ICM</sub> (DC coupled)	HCSL I/O standard for PCIe reference clock	250	_	550	250		550	mV		

#### Table 28. Transceiver Specifications for Stratix V GT Devices (Part 1 of 5)<sup>(1)</sup>

### Table 28. Transceiver Specifications for Stratix V GT Devices (Part 2 of 5)<sup>(1)</sup>

Symbol/	Conditions	S	Transceive peed Grade	r 2	SI	Fransceive Deed Grade	r 3	Unit
Description		Min	Тур	Max	Min	Тур	Max	
	100 Hz	—	—	-70			-70	
Transmitter REFCLK	1 kHz		_	-90	_	_	-90	
Phase Noise (622	10 kHz		—	-100	_		-100	dBc/Hz
MHz) <sup>(18)</sup>	100 kHz			-110			-110	
	$\geq$ 1 MHz	—	—	-120		_	-120	
Transmitter REFCLK Phase Jitter (100 MHz) <sup>(15)</sup>	10 kHz to 1.5 MHz (PCle)	_	_	3		_	3	ps (rms)
RREF <sup>(17)</sup>	_	_	1800 ± 1%	—	_	1800 ± 1%	_	Ω
Transceiver Clocks								
fixedclk clock frequency	PCIe Receiver Detect	_	100 or 125	_	_	100 or 125	_	MHz
Reconfiguration clock (mgmt_clk_clk) frequency	_	100	_	125	100	_	125	MHz
Receiver	•							
Supported I/O Standards	_		1.4-V PCML	., 1.5-V PCMI	L, 2.5-V PCI	VIL, LVPEC	L, and LVDS	6
Data rate (Standard PCS) <sup>(21)</sup>	GX channels	600	_	8500	600	_	8500	Mbps
Data rate (10G PCS) <sup>(21)</sup>	GX channels	600	_	12,500	600	_	12,500	Mbps
Data rate	GT channels	19,600	—	28,050	19,600		25,780	Mbps
Absolute V <sub>MAX</sub> for a receiver pin <sup>(3)</sup>	GT channels	_	_	1.2	_	_	1.2	V
Absolute V <sub>MIN</sub> for a receiver pin	GT channels	-0.4	_	—	-0.4	_	_	V
Maximum peak-to-peak	GT channels	_		1.6	—	_	1.6	V
differential input voltage V <sub>ID</sub> (diff p-p) before device configuration <sup>(20)</sup>	GX channels				(8)			
	GT channels							
Maximum peak-to-peak differential input voltage $V_{ID}$ (diff p-p) after device	V <sub>CCR_GTB</sub> = 1.05 V (V <sub>ICM</sub> = 0.65 V)	_	_	2.2	_	—	2.2	V
	GX channels		1	1 1	(8)			1
Minimum differential	GT channels	200	_	—	200		_	mV
eye opening at receiver serial input pins <sup>(4)</sup> , <sup>(20)</sup>	GX channels			·	(8)			

Table 28. Tra	nsceiver Specifi	cations for Stra	tix V GT Devices	(Part 5 of 5) <sup>(1)</sup>
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Symbol/ Description	Conditions	S	Transceivei peed Grade	2	ן Sr	Unit		
		Min	Тур	Max	Min	Тур	Max	
t <sub>pll_lock</sub> <sup>(14)</sup>	—	—	_	10	—	—	10	μs

#### Notes to Table 28:

- (1) Speed grades shown refer to the PMA Speed Grade in the device ordering code. The maximum data rate could be restricted by the Core/PCS speed grade. Contact your Altera Sales Representative for the maximum data rate specifications in each speed grade combination offered. For more information about device ordering codes, refer to the Stratix V Device Overview.
- (2) The reference clock common mode voltage is equal to the VCCR\_GXB power supply level.
- (3) The device cannot tolerate prolonged operation at this absolute maximum.
- (4) The differential eye opening specification at the receiver input pins assumes that receiver equalization is disabled. If you enable receiver equalization, the receiver circuitry can tolerate a lower minimum eye opening, depending on the equalization level.
- (5) Refer to Figure 5 for the GT channel AC gain curves. The total effective AC gain is the AC gain minus the DC gain.
- (6) Refer to Figure 6 for the GT channel DC gain curves.
- (7) CFP2 optical modules require the host interface to have the receiver data pins differentially terminated with 100 Ω. The internal OCT feature is available after the Stratix V FPGA configuration is completed. Altera recommends that FPGA configuration is completed before inserting the optical module. Otherwise, minimize unnecessary removal and insertion with unconfigured devices.
- (8) Specifications for this parameter are the same as for Stratix V GX and GS devices. See Table 23 for specifications.
- (9) t<sub>1 TR</sub> is the time required for the receive CDR to lock to the input reference clock frequency after coming out of reset.
- (10) t<sub>LTD</sub> is time required for the receiver CDR to start recovering valid data after the rx is lockedtodata signal goes high.
- (11)  $t_{LTD\_manual}$  is the time required for the receiver CDR to start recovering valid data after the rx\_is\_lockedtodata signal goes high when the CDR is functioning in the manual mode.
- (12) t<sub>LTR\_LTD\_manual</sub> is the time the receiver CDR must be kept in lock to reference (LTR) mode after the rx\_is\_lockedtoref signal goes high when the CDR is functioning in the manual mode.
- (13) tpll\_powerdown is the PLL powerdown minimum pulse width.
- (14) tpll lock is the time required for the transmitter CMU/ATX PLL to lock to the input reference clock frequency after coming out of reset.
- (15) To calculate the REFCLK rms phase jitter requirement for PCle at reference clock frequencies other than 100 MHz, use the following formula: REFCLK rms phase jitter at f(MHz) = REFCLK rms phase jitter at 100 MHz × 100/f.
- (16) The maximum peak to peak differential input voltage  $V_{ID}$  after device configuration is equal to 4 × (absolute  $V_{MAX}$  for receiver pin  $V_{ICM}$ ).
- (17) For ES devices, RREF is 2000  $\Omega \pm 1\%$ .
- (18) To calculate the REFCLK phase noise requirement at frequencies other than 622 MHz, use the following formula: REFCLK phase noise at f(MHz) = REFCLK phase noise at 622 MHz + 20\*log(f/622).
- (19) SFP/+ optical modules require the host interface to have RD+/- differentially terminated with 100 Ω. The internal OCT feature is available after the Stratix V FPGA configuration is completed. Altera recommends that FPGA configuration is completed before inserting the optical module. Otherwise, minimize unnecessary removal and insertion with unconfigured devices.
- (20) Refer to Figure 4.
- (21) For oversampling design to support data rates less than the minimum specification, the CDR needs to be in LTR mode only.
- (22) This supply follows VCCR\_GXB for both GX and GT channels.
- (23) When you use fPLL as a TXPLL of the transceiver.

Figure 4 shows the differential transmitter output waveform.





Figure 5 shows the Stratix V AC gain curves for GT channels.

Figure 5. AC Gain Curves for GT Channels

- XFI
- ASI
- HiGig/HiGig+
- HiGig2/HiGig2+
- Serial Data Converter (SDC)
- GPON
- SDI
- SONET
- Fibre Channel (FC)
- PCIe
- QPI
- SFF-8431

Download the Stratix V Characterization Report Tool to view the characterization report summary for these protocols.

### **Core Performance Specifications**

This section describes the clock tree, phase-locked loop (PLL), digital signal processing (DSP), memory blocks, configuration, and JTAG specifications.

### **Clock Tree Specifications**

Table 30 lists the clock tree specifications for Stratix V devices.

Table 30. Clock Tree Performance for Stratix V Devices (1)

Symbol	C1, C2, C2L, I2, and I2L	C3, I3, I3L, and I3YY	C4, I4	Unit
Global and Regional Clock	717	650	580	MHz
Periphery Clock	550	500	500	MHz

#### Note to Table 30:

(1) The Stratix V ES devices are limited to 600 MHz core clock tree performance.

Symbol	Parameter	Min	Тур	Max	Unit
+ (3) (4)	Input clock cycle-to-cycle jitter ( $f_{REF} \ge 100 \text{ MHz}$ )			0.15	UI (p-p)
LINCCJ (0), (1)	Input clock cycle-to-cycle jitter (f <sub>REF</sub> < 100 MHz)	-750		+750	ps (p-p)
+ (5)	Period Jitter for dedicated clock output (f_{OUT} $\geq$ 100 MHz)	_	_	175 <sup>(1)</sup>	ps (p-p)
CUTPJ_DC	Period Jitter for dedicated clock output (f <sub>OUT</sub> < 100 MHz)	_	_	17.5 <sup>(1)</sup>	mUI (p-p)
+ (5)	Period Jitter for dedicated clock output in fractional PLL ( $f_{OUT} \ge 100 \text{ MHz}$ )	_	_	250 <sup>(11)</sup> , 175 <sup>(12)</sup>	ps (p-p)
<sup>L</sup> FOUTPJ_DC	Period Jitter for dedicated clock output in fractional PLL (f <sub>OUT</sub> < 100 MHz)	_	_	25 <sup>(11)</sup> , 17.5 <sup>(12)</sup>	mUI (p-p)
+ (5)	Cycle-to-Cycle Jitter for a dedicated clock output ( $f_{\text{OUT}} \geq 100 \text{ MHz})$		_	175	ps (p-p)
COUTCCJ_DC	Cycle-to-Cycle Jitter for a dedicated clock output $(f_{OUT} < 100 \text{ MHz})$		_	17.5	mUI (p-p)
+ (5)	Cycle-to-cycle Jitter for a dedicated clock output in fractional PLL ( $f_{OUT} \ge 100 \text{ MHz}$ )		_	250 <sup>(11)</sup> , 175 <sup>(12)</sup>	ps (p-p)
FOUTCCJ_DC	Cycle-to-cycle Jitter for a dedicated clock output in fractional PLL ( $f_{OUT} < 100 \text{ MHz}$ )+		_	25 <sup>(11)</sup> , 17.5 <sup>(12)</sup>	mUI (p-p)
t <sub>outpj 10</sub> (5),	Period Jitter for a clock output on a regular I/O in integer PLL ( $f_{OUT} \ge 100 \text{ MHz}$ )		_	600	ps (p-p)
t <sub>OUTPJ_IO</sub> (5), (8)	Period Jitter for a clock output on a regular I/O $(f_{OUT} < 100 \text{ MHz})$		_	60	mUI (p-p)
t <sub>foutpj 10</sub> <sup>(5),</sup>	Period Jitter for a clock output on a regular I/O in fractional PLL ( $f_{OUT} \ge 100 \text{ MHz}$ )	_	_	600 <sup>(10)</sup>	ps (p-p)
(8), (11)	Period Jitter for a clock output on a regular I/O in fractional PLL (f <sub>OUT</sub> < 100 MHz)	_	_	60 <sup>(10)</sup>	mUI (p-p)
t <sub>outccj_io</sub> (5),	Cycle-to-cycle Jitter for a clock output on a regular I/O in integer PLL ( $f_{OUT} \geq 100 \mbox{ MHz})$	_	_	600	ps (p-p)
(8)	Cycle-to-cycle Jitter for a clock output on a regular I/O in integer PLL (f <sub>OUT</sub> < 100 MHz)	_	_	60 <sup>(10)</sup>	mUI (p-p)
t <sub>FOUTCCJ 10</sub> (5),	Cycle-to-cycle Jitter for a clock output on a regular I/O in fractional PLL ( $f_{OUT} \ge 100$ MHz)		_	600 <sup>(10)</sup>	ps (p-p)
(8), (11)	Cycle-to-cycle Jitter for a clock output on a regular I/O in fractional PLL (f <sub>OUT</sub> < 100 MHz)	_	_	60	mUI (p-p)
t <sub>CASC OUTPJ DC</sub>	Period Jitter for a dedicated clock output in cascaded PLLs ( $f_{OUT} \ge 100 \text{ MHz}$ )	_	_	175	ps (p-p)
(5), (6)	Period Jitter for a dedicated clock output in cascaded PLLs ( $f_{OUT}$ < 100 MHz)	_	_	17.5	mUI (p-p)
f <sub>DRIFT</sub>	Frequency drift after PFDENA is disabled for a duration of 100 $\mu s$		_	±10	%
dK <sub>BIT</sub>	Bit number of Delta Sigma Modulator (DSM)	8	24	32	Bits
k <sub>VALUE</sub>	Numerator of Fraction	128	8388608	2147483648	—

Table 31. PLL Specifications for Stratix V Devices (Part 2 of 3)

### **Periphery Performance**

This section describes periphery performance, including high-speed I/O and external memory interface.

I/O performance supports several system interfaces, such as the **LVDS** high-speed I/O interface, external memory interface, and the **PCI/PCI-X** bus interface. General-purpose I/O standards such as 3.3-, 2.5-, 1.8-, and 1.5-**LVTTL/LVCMOS** are capable of a typical 167 MHz and 1.2-**LVCMOS** at 100 MHz interfacing frequency with a 10 pF load.

The actual achievable frequency depends on design- and system-specific factors. Ensure proper timing closure in your design and perform HSPICE/IBIS simulations based on your specific design and system setup to determine the maximum achievable frequency in your system.

### **High-Speed I/O Specification**

Table 36 lists high-speed I/O timing for Stratix V devices.

Table 36. High-Speed I/O Specifications for Stratix V Devices (1), (2) (Part 1 of 4)

Cumbal	Conditions	C1		C2, C2L, I2, I2L		C3, I3, I3L, I3YY			C4,14			llni+		
Symbol		Min	Тур	Max	Min	Тур	Max	Min	Тур	Max	Min	Тур	Max	
f <sub>HSCLK_in</sub> (input clock frequency) True Differential I/O Standards	Clock boost factor W = 1 to 40 $^{(4)}$	5	_	800	5		800	5		625	5		525	MHz
f <sub>HSCLK_in</sub> (input clock frequency) Single Ended I/O Standards <sup>(3)</sup>	Clock boost factor W = 1 to 40 $^{(4)}$	5		800	5		800	5		625	5		525	MHz
f <sub>HSCLK_in</sub> (input clock frequency) Single Ended I/O Standards	Clock boost factor W = 1 to 40 $^{(4)}$	5	_	520	5		520	5	_	420	5	_	420	MHz
f <sub>HSCLK_OUT</sub> (output clock frequency)	_	5	_	800	5	_	800	5	_	625 (5)	5	_	525 (5)	MHz

	Conditions	C1			C2, C2L, I2, I2L			C3, I3, I3L, I3YY			C4,14			
Symbol		Min	Тур	Max	Min	Тур	Max	Min	Тур	Max	Min	Тур	Max	Unit
t <sub>duty</sub>	Transmitter output clock duty cycle for both True and Emulated Differential I/O Standards	45	50	55	45	50	55	45	50	55	45	50	55	%
	True Differential I/O Standards	_	_	160	_	_	160	_	_	200	_	_	200	ps
t <sub>rise</sub> & t <sub>fall</sub>	Emulated Differential I/O Standards with three external output resistor networks			250			250			250			300	ps
	True Differential I/O Standards	_	_	150	_	_	150	_	_	150	_	_	150	ps
TCCS	Emulated Differential I/O Standards			300			300	_		300			300	ps
Receiver														
	SERDES factor J = 3 to 10 (11), (12), (13), (14), (15), (16)	150		1434	150	_	1434	150	_	1250	150	_	1050	Mbps
True Differential 1/0 Standards	SERDES factor J ≥ 4 LVDS RX with DPA (12), (14), (15), (16)	150	_	1600	150	_	1600	150	_	1600	150	_	1250	Mbps
- f <sub>HSDRDPA</sub> (data rate)	SERDES factor J = 2, uses DDR Registers	(6)		(7)	(6)	_	(7)	(6)	_	(7)	(6)	_	(7)	Mbps
	SERDES factor J = 1, uses SDR Register	(6)	_	(7)	(6)	_	(7)	(6)	_	(7)	(6)		(7)	Mbps

### Table 36. High-Speed I/O Specifications for Stratix V Devices (1), (2) (Part 3 of 4)

Table 50 lists the timing parameters for Stratix V devices for FPP configuration when the DCLK-to-DATA[] ratio is 1.

Table 50. FPP Timing Parameters for Stratix V Devices (1)

Symbol	Parameter	Minimum	Maximum	Units
t <sub>CF2CD</sub>	nCONFIG low to CONF_DONE low		600	ns
t <sub>CF2ST0</sub>	nCONFIG low to nSTATUS low		600	ns
t <sub>CFG</sub>	nCONFIG low pulse width	2	_	μS
t <sub>status</sub>	nSTATUS low pulse width	268	1,506 <sup>(2)</sup>	μS
t <sub>CF2ST1</sub>	nCONFIG high to nSTATUS high		1,506 <sup>(3)</sup>	μS
t <sub>CF2CK</sub> (6)	nCONFIG high to first rising edge on DCLK	1,506		μS
t <sub>ST2CK</sub> (6)	nSTATUS high to first rising edge of DCLK	2		μS
t <sub>DSU</sub>	DATA [] setup time before rising edge on DCLK	5.5		ns
t <sub>DH</sub>	DATA [] hold time after rising edge on DCLK	0	_	ns
t <sub>CH</sub>	DCLK high time	$0.45\times1/f_{MAX}$		S
t <sub>CL</sub>	DCLK low time	$0.45\times 1/f_{MAX}$		S
t <sub>CLK</sub>	DCLK period	1/f <sub>MAX</sub>	_	S
£	DCLK frequency (FPP ×8/×16)	—	125	MHz
IMAX	DCLK frequency (FPP ×32)	—	100	MHz
t <sub>CD2UM</sub>	CONF_DONE high to user mode <sup>(4)</sup>	175	437	μS
+	CONTR DOWN high to Grund analysis	4 × maximum		
LCD2CU	CONF_DONE HIGH to CLEOSE enabled	DCLK period		_
t <sub>cd2uмc</sub>	CONF_DONE high to user mode with CLKUSR option on	$t_{CD2CU}$ + (8576 × CLKUSR period) <sup>(5)</sup>	_	

#### Notes to Table 50:

(1) Use these timing parameters when the decompression and design security features are disabled.

(2) This value is applicable if you do not delay configuration by extending the nCONFIG or nSTATUS low pulse width.

(3) This value is applicable if you do not delay configuration by externally holding the nSTATUS low.

- (4) The minimum and maximum numbers apply only if you chose the internal oscillator as the clock source for initializing the device.
- (5) To enable the CLKUSR pin as the initialization clock source and to obtain the maximum frequency specification on these pins, refer to the Initialization section of the "Configuration, Design Security, and Remote System Upgrades in Stratix V Devices" chapter.
- (6) If nSTATUS is monitored, follow the t<sub>ST2CK</sub> specification. If nSTATUS is not monitored, follow the t<sub>CF2CK</sub> specification.

### FPP Configuration Timing when DCLK-to-DATA [] > 1

Figure 13 shows the timing waveform for FPP configuration when using a MAX II device, MAX V device, or microprocessor as an external host. This waveform shows timing when the DCLK-to-DATA [] ratio is more than 1.



#### Figure 13. FPP Configuration Timing Waveform When the DCLK-to-DATA[] Ratio is >1 (1), (2)

#### Notes to Figure 13:

- (1) Use this timing waveform and parameters when the DCLK-to-DATA [] ratio is >1. To find out the DCLK-to-DATA [] ratio for your system, refer to Table 49 on page 55.
- (2) The beginning of this waveform shows the device in user mode. In user mode, nCONFIG, nSTATUS, and CONF\_DONE are at logic high levels. When nCONFIG is pulled low, a reconfiguration cycle begins.
- (3) After power-up, the Stratix V device holds nSTATUS low for the time as specified by the POR delay.
- (4) After power-up, before and during configuration, CONF\_DONE is low.
- (5) Do not leave DCLK floating after configuration. You can drive it high or low, whichever is more convenient.
- (6) "r" denotes the DCLK-to-DATA [] ratio. For the DCLK-to-DATA [] ratio based on the decompression and the design security feature enable settings, refer to Table 49 on page 55.
- (7) If needed, pause DCLK by holding it low. When DCLK restarts, the external host must provide data on the DATA [31..0] pins prior to sending the first DCLK rising edge.
- (8) To ensure a successful configuration, send the entire configuration data to the Stratix V device. CONF\_DONE is released high after the Stratix V device receives all the configuration data successfully. After CONF\_DONE goes high, send two additional falling edges on DCLK to begin initialization and enter user mode.
- (9) After the option bit to enable the INIT DONE pin is configured into the device, the INIT DONE goes low.

### **Remote System Upgrades**

Table 56 lists the timing parameter specifications for the remote system upgrade circuitry.

Table 56. Remote System Upgrade Circuitry Timing Specificatio
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Parameter	Minimum	Maximum	Unit
t <sub>RU_nCONFIG</sub> <sup>(1)</sup>	250	—	ns
t <sub>RU_nRSTIMER</sub> <sup>(2)</sup>	250	_	ns

#### Notes to Table 56:

- (1) This is equivalent to strobing the reconfiguration input of the ALTREMOTE\_UPDATE megafunction high for the minimum timing specification. For more information, refer to the Remote System Upgrade State Machine section of the "Configuration, Design Security, and Remote System Upgrades in Stratix V Devices" chapter.
- (2) This is equivalent to strobing the reset\_timer input of the ALTREMOTE\_UPDATE megafunction high for the minimum timing specification. For more information, refer to the User Watchdog Timer section of the "Configuration, Design Security, and Remote System Upgrades in Stratix V Devices" chapter.

### **User Watchdog Internal Circuitry Timing Specification**

Table 57 lists the operating range of the 12.5-MHz internal oscillator.

#### Table 57. 12.5-MHz Internal Oscillator Specifications

Minimum	Typical	Maximum	Units
5.3	7.9	12.5	MHz

# I/O Timing

Altera offers two ways to determine I/O timing—the Excel-based I/O Timing and the Quartus II Timing Analyzer.

Excel-based I/O timing provides pin timing performance for each device density and speed grade. The data is typically used prior to designing the FPGA to get an estimate of the timing budget as part of the link timing analysis. The Quartus II Timing Analyzer provides a more accurate and precise I/O timing data based on the specifics of the design after you complete place-and-route.

 You can download the Excel-based I/O Timing spreadsheet from the Stratix V Devices Documentation web page.

### **Programmable IOE Delay**

Table 58 lists the Stratix V IOE programmable delay settings.

Table 58. IOE Programmable Delay for Stratix V Devices (Part 1 of 2)

Deremeter	Paramatar Available		Fast	Model				Slow N	lodel			
(1)	Settings	<b>Offset</b> (2)	Industrial	Commercial	C1	C2	C3	C4	12	13, 13YY	14	Unit
D1	64	0	0.464	0.493	0.838	0.838	0.924	1.011	0.844	0.921	1.006	ns
D2	32	0	0.230	0.244	0.415	0.415	0.459	0.503	0.417	0.456	0.500	ns

Table 60.	Glossary	(Part 3 of 4)
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Letter	Subject	Definitions							
	SW (sampling window)	Timing Diagram—the period of time during which the data must be valid in order to capture it correctly. The setup and hold times determine the ideal strobe position within the sampling window, as shown:         Bit Time         0.5 x TCCS       RSKM         Sampling Window       RSKM         0.5 x TCCS       RSKM							
S	Single-ended voltage referenced I/O standard	(SW)         The JEDEC standard for SSTL and HSTL I/O defines both the AC and DC input signal values.         The AC values indicate the voltage levels at which the receiver must meet its timing specifications. The DC values indicate the voltage levels at which the final logic state of the receiver is unambiguously defined. After the receiver input has crossed the AC value, the receiver changes to the new logic state.         The new logic state is then maintained as long as the input stays beyond the DC threshold.         This approach is intended to provide predictable receiver timing in the presence of input waveform ringing:         Single-Ended Voltage Referenced I/O Standard							
	t <sub>C</sub>	High-speed receiver and transmitter input and output clock period.							
	TCCS (channel- to-channel-skew)	The timing difference between the fastest and slowest output edges, including t <sub>CO</sub> variation and clock skew, across channels driven by the same PLL. The clock is included in the TCCS measurement (refer to the <i>Timing Diagram</i> figure under <b>SW</b> in this table).							
		High-speed I/O block—Duty cycle on the high-speed transmitter output clock.							
т	t <sub>DUTY</sub>	<b>Timing Unit Interval (TUI)</b> The timing budget allowed for skew, propagation delays, and the data sampling window.							
		(TUI = 1/(receiver input clock frequency multiplication factor) = $t_c/w$ )							
	t <sub>FALL</sub>	Signal high-to-low transition time (80-20%)							
	t <sub>INCCJ</sub>	Cycle-to-cycle jitter tolerance on the PLL clock input.							
	t <sub>outpj_i0</sub>	Period jitter on the general purpose I/O driven by a PLL.							
	t <sub>outpj_dc</sub>	Period jitter on the dedicated clock output driven by a PLL.							
	<b>t</b> <sub>RISE</sub>	Signal low-to-high transition time (20-80%)							
U		_							