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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

| | |
|--------------------------------|---|
| Product Status | Obsolete |
| Number of LABs/CLBs | 185000 |
| Number of Logic Elements/Cells | 490000 |
| Total RAM Bits | 46080000 |
| Number of I/O | 432 |
| Number of Gates | - |
| Voltage - Supply | 0.82V ~ 0.88V |
| Mounting Type | Surface Mount |
| Operating Temperature | 0°C ~ 85°C (TJ) |
| Package / Case | 1152-BBGA, FCBGA |
| Supplier Device Package | 1152-FBGA (35x35) |
| Purchase URL | https://www.e-xfl.com/product-detail/intel/5sgxea5k3f35c4n |

Table 11. OCT Calibration Accuracy Specifications for Stratix V Devices ⁽¹⁾ (Part 2 of 2)

| Symbol | Description | Conditions | Calibration Accuracy | | | | Unit |
|--|--|---|----------------------|------------|----------------|------------|------|
| | | | C1 | C2,I2 | C3,I3, I3YY | C4,I4 | |
| 50-Ω R _S | Internal series termination with calibration (50-Ω setting) | V _{CCIO} = 3.0, 2.5, 1.8, 1.5, 1.2 V | ±15 | ±15 | ±15 | ±15 | % |
| 34-Ω and 40-Ω R _S | Internal series termination with calibration (34-Ω and 40-Ω setting) | V _{CCIO} = 1.5, 1.35, 1.25, 1.2 V | ±15 | ±15 | ±15 | ±15 | % |
| 48-Ω, 60-Ω, 80-Ω, and 240-Ω R _S | Internal series termination with calibration (48-Ω, 60-Ω, 80-Ω, and 240-Ω setting) | V _{CCIO} = 1.2 V | ±15 | ±15 | ±15 | ±15 | % |
| 50-Ω R _T | Internal parallel termination with calibration (50-Ω setting) | V _{CCIO} = 2.5, 1.8, 1.5, 1.2 V | -10 to +40 | -10 to +40 | -10 to +40 | -10 to +40 | % |
| 20-Ω, 30-Ω, 40-Ω, 60-Ω, and 120-Ω R _T | Internal parallel termination with calibration (20-Ω, 30-Ω, 40-Ω, 60-Ω, and 120-Ω setting) | V _{CCIO} = 1.5, 1.35, 1.25 V | -10 to +40 | -10 to +40 | -10 to +40 | -10 to +40 | % |
| 60-Ω and 120-Ω R _T | Internal parallel termination with calibration (60-Ω and 120-Ω setting) | V _{CCIO} = 1.2 | -10 to +40 | -10 to +40 | -10 to +40 | -10 to +40 | % |
| 25-Ω R _{S_left_shift} | Internal left shift series termination with calibration (25-Ω R _{S_left_shift} setting) | V _{CCIO} = 3.0, 2.5, 1.8, 1.5, 1.2 V | ±15 | ±15 | ±15 | ±15 | % |

Note to Table 11:

(1) OCT calibration accuracy is valid at the time of calibration only.

Table 12 lists the Stratix V OCT without calibration resistance tolerance to PVT changes.

Table 12. OCT Without Calibration Resistance Tolerance Specifications for Stratix V Devices (Part 1 of 2)

| Symbol | Description | Conditions | Resistance Tolerance | | | | Unit |
|-----------------------------|--|-----------------------------------|----------------------|-------|-----------------|--------|------|
| | | | C1 | C2,I2 | C3, I3, I3YY | C4, I4 | |
| 25-Ω R, 50-Ω R _S | Internal series termination without calibration (25-Ω setting) | V _{CCIO} = 3.0 and 2.5 V | ±30 | ±30 | ±40 | ±40 | % |
| 25-Ω R _S | Internal series termination without calibration (25-Ω setting) | V _{CCIO} = 1.8 and 1.5 V | ±30 | ±30 | ±40 | ±40 | % |
| 25-Ω R _S | Internal series termination without calibration (25-Ω setting) | V _{CCIO} = 1.2 V | ±35 | ±35 | ±50 | ±50 | % |

Table 12. OCT Without Calibration Resistance Tolerance Specifications for Stratix V Devices (Part 2 of 2)

| Symbol | Description | Conditions | Resistance Tolerance | | | | Unit |
|----------------------|--|-----------------------------------|----------------------|--------|--------------|--------|------|
| | | | C1 | C2, I2 | C3, I3, I3YY | C4, I4 | |
| 50-Ω R _S | Internal series termination without calibration (50-Ω setting) | V _{CCIO} = 1.8 and 1.5 V | ±30 | ±30 | ±40 | ±40 | % |
| 50-Ω R _S | Internal series termination without calibration (50-Ω setting) | V _{CCIO} = 1.2 V | ±35 | ±35 | ±50 | ±50 | % |
| 100-Ω R _D | Internal differential termination (100-Ω setting) | V _{CCPD} = 2.5 V | ±25 | ±25 | ±25 | ±25 | % |

Calibration accuracy for the calibrated series and parallel OCTs are applicable at the moment of calibration. When voltage and temperature conditions change after calibration, the tolerance may change.

OCT calibration is automatically performed at power-up for OCT-enabled I/Os. Table 13 lists the OCT variation with temperature and voltage after power-up calibration. Use Table 13 to determine the OCT variation after power-up calibration and Equation 1 to determine the OCT variation without recalibration.

Equation 1. OCT Variation Without Recalibration for Stratix V Devices ^{(1), (2), (3), (4), (5), (6)}

$$R_{OCT} = R_{SCAL} \left(1 + \left\langle \frac{dR}{dT} \times \Delta T \right\rangle \pm \left\langle \frac{dR}{dV} \times \Delta V \right\rangle \right)$$

Notes to Equation 1:

- (1) The R_{OCT} value shows the range of OCT resistance with the variation of temperature and V_{CCIO}.
- (2) R_{SCAL} is the OCT resistance value at power-up.
- (3) ΔT is the variation of temperature with respect to the temperature at power-up.
- (4) ΔV is the variation of voltage with respect to the V_{CCIO} at power-up.
- (5) dR/dT is the percentage change of R_{SCAL} with temperature.
- (6) dR/dV is the percentage change of R_{SCAL} with voltage.

Table 13 lists the on-chip termination variation after power-up calibration.

Table 13. OCT Variation after Power-Up Calibration for Stratix V Devices (Part 1 of 2) ⁽¹⁾

| Symbol | Description | V _{CCIO} (V) | Typical | Unit |
|--------|--|-----------------------|---------|------|
| dR/dV | OCT variation with voltage without recalibration | 3.0 | 0.0297 | %/mV |
| | | 2.5 | 0.0344 | |
| | | 1.8 | 0.0499 | |
| | | 1.5 | 0.0744 | |
| | | 1.2 | 0.1241 | |

Table 13. OCT Variation after Power-Up Calibration for Stratix V Devices (Part 2 of 2) ⁽¹⁾

| Symbol | Description | V _{CCIO} (V) | Typical | Unit |
|--------|--|-----------------------|---------|-------------------|
| dR/dT | OCT variation with temperature without recalibration | 3.0 | 0.189 | %/ ^o C |
| | | 2.5 | 0.208 | |
| | | 1.8 | 0.266 | |
| | | 1.5 | 0.273 | |
| | | 1.2 | 0.317 | |

Note to Table 13:

(1) Valid for a V_{CCIO} range of $\pm 5\%$ and a temperature range of 0° to 85°C.

Pin Capacitance

Table 14 lists the Stratix V device family pin capacitance.

Table 14. Pin Capacitance for Stratix V Devices

| Symbol | Description | Value | Unit |
|--------------------|--|-------|------|
| C _{IOTB} | Input capacitance on the top and bottom I/O pins | 6 | pF |
| C _{IOLR} | Input capacitance on the left and right I/O pins | 6 | pF |
| C _{OUTFB} | Input capacitance on dual-purpose clock output and feedback pins | 6 | pF |

Hot Socketing

Table 15 lists the hot socketing specifications for Stratix V devices.

Table 15. Hot Socketing Specifications for Stratix V Devices

| Symbol | Description | Maximum |
|---------------------------|--|---------------------|
| I _{IOPIN} (DC) | DC current per I/O pin | 300 μ A |
| I _{IOPIN} (AC) | AC current per I/O pin | 8 mA ⁽¹⁾ |
| I _{XCVR-TX} (DC) | DC current per transceiver transmitter pin | 100 mA |
| I _{XCVR-RX} (DC) | DC current per transceiver receiver pin | 50 mA |

Note to Table 15:

(1) The I/O ramp rate is 10 ns or more. For ramp rates faster than 10 ns, $|I_{IOPIN}| = C \, dv/dt$, in which C is the I/O pin capacitance and dv/dt is the slew rate.

Table 23. Transceiver Specifications for Stratix V GX and GS Devices ⁽¹⁾ (Part 2 of 7)

| Symbol/ Description | Conditions | Transceiver Speed Grade 1 | | | Transceiver Speed Grade 2 | | | Transceiver Speed Grade 3 | | | Unit |
|--|--|----------------------------------|-------------------|------|----------------------------------|-------------------|------|----------------------------------|-------------------|------|-------------|
| | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| Spread-spectrum downspread | PCIe | — | 0 to -0.5 | — | — | 0 to -0.5 | — | — | 0 to -0.5 | — | % |
| On-chip termination resistors ⁽²¹⁾ | — | — | 100 | — | — | 100 | — | — | 100 | — | Ω |
| Absolute V_{MAX} ⁽⁵⁾ | Dedicated reference clock pin | — | — | 1.6 | — | — | 1.6 | — | — | 1.6 | V |
| | RX reference clock pin | — | — | 1.2 | — | — | 1.2 | — | — | 1.2 | |
| Absolute V_{MIN} | — | -0.4 | — | — | -0.4 | — | — | -0.4 | — | — | V |
| Peak-to-peak differential input voltage | — | 200 | — | 1600 | 200 | — | 1600 | 200 | — | 1600 | mV |
| V_{ICM} (AC coupled) ⁽³⁾ | Dedicated reference clock pin | 1050/1000/900/850 ⁽²⁾ | | | 1050/1000/900/850 ⁽²⁾ | | | 1050/1000/900/850 ⁽²⁾ | | | mV |
| | RX reference clock pin | 1.0/0.9/0.85 ⁽⁴⁾ | | | 1.0/0.9/0.85 ⁽⁴⁾ | | | 1.0/0.9/0.85 ⁽⁴⁾ | | | V |
| V_{ICM} (DC coupled) | HCSL I/O standard for PCIe reference clock | 250 | — | 550 | 250 | — | 550 | 250 | — | 550 | mV |
| Transmitter REFCLK Phase Noise (622 MHz) ⁽²⁰⁾ | 100 Hz | — | — | -70 | — | — | -70 | — | — | -70 | dBc/Hz |
| | 1 kHz | — | — | -90 | — | — | -90 | — | — | -90 | dBc/Hz |
| | 10 kHz | — | — | -100 | — | — | -100 | — | — | -100 | dBc/Hz |
| | 100 kHz | — | — | -110 | — | — | -110 | — | — | -110 | dBc/Hz |
| | ≥ 1 MHz | — | — | -120 | — | — | -120 | — | — | -120 | dBc/Hz |
| Transmitter REFCLK Phase Jitter (100 MHz) ⁽¹⁷⁾ | 10 kHz to 1.5 MHz (PCIe) | — | — | 3 | — | — | 3 | — | — | 3 | ps (rms) |
| R_{REF} ⁽¹⁹⁾ | — | — | 1800 $\pm 1\%$ | — | — | 1800 $\pm 1\%$ | — | — | 1800 $\pm 1\%$ | — | Ω |
| Transceiver Clocks | | | | | | | | | | | |
| fixedclk clock frequency | PCIe Receiver Detect | — | 100 or 125 | — | — | 100 or 125 | — | — | 100 or 125 | — | MHz |

Table 23. Transceiver Specifications for Stratix V GX and GS Devices ⁽¹⁾ (Part 3 of 7)

| Symbol/ Description | Conditions | Transceiver Speed Grade 1 | | | Transceiver Speed Grade 2 | | | Transceiver Speed Grade 3 | | | Unit |
|---|--|--|-----|-------|------------------------------|-----|-------|------------------------------|-----|--------------------------|------|
| | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| Reconfiguration clock (<code>mgmt_clk_clk</code>) frequency | — | 100 | — | 125 | 100 | — | 125 | 100 | — | 125 | MHz |
| Receiver | | | | | | | | | | | |
| Supported I/O Standards | — | 1.4-V PCML, 1.5-V PCML, 2.5-V PCML, LVPECL, and LVDS | | | | | | | | | |
| Data rate (Standard PCS) (9), (23) | — | 600 | — | 12200 | 600 | — | 12200 | 600 | — | 8500/ 10312.5 (24) | Mbps |
| Data rate (10G PCS) (9), (23) | — | 600 | — | 14100 | 600 | — | 12500 | 600 | — | 8500/ 10312.5 (24) | Mbps |
| Absolute V_{MAX} for a receiver pin ⁽⁵⁾ | — | — | — | 1.2 | — | — | 1.2 | — | — | 1.2 | V |
| Absolute V_{MIN} for a receiver pin | — | −0.4 | — | — | −0.4 | — | — | −0.4 | — | — | V |
| Maximum peak- to-peak differential input voltage V_{ID} (diff p- p) before device configuration ⁽²²⁾ | — | — | — | 1.6 | — | — | 1.6 | — | — | 1.6 | V |
| Maximum peak- to-peak differential input voltage V_{ID} (diff p- p) after device configuration ⁽¹⁸⁾ , (22) | $V_{CCR_GXB} =$ 1.0 V/1.05 V ($V_{ICM} =$ 0.70 V) | — | — | 2.0 | — | — | 2.0 | — | — | 2.0 | V |
| | $V_{CCR_GXB} =$ 0.90 V ($V_{ICM} = 0.6$ V) | — | — | 2.4 | — | — | 2.4 | — | — | 2.4 | V |
| | $V_{CCR_GXB} =$ 0.85 V ($V_{ICM} = 0.6$ V) | — | — | 2.4 | — | — | 2.4 | — | — | 2.4 | V |
| Minimum differential eye opening at receiver serial input pins ⁽⁶⁾ , (22), (27) | — | 85 | — | — | 85 | — | — | 85 | — | — | mV |

Table 24 shows the maximum transmitter data rate for the clock network.

Table 24. Clock Network Maximum Data Rate Transmitter Specifications ⁽¹⁾

| Clock Network | ATX PLL | | | CMU PLL ⁽²⁾ | | | fPLL | | |
|--------------------------------|------------------------|--------------------|---------------------------------------|------------------------|--------------------|---------------------------------------|------------------------|--------------------|---------------------------------------|
| | Non-bonded Mode (Gbps) | Bonded Mode (Gbps) | Channel Span | Non-bonded Mode (Gbps) | Bonded Mode (Gbps) | Channel Span | Non-bonded Mode (Gbps) | Bonded Mode (Gbps) | Channel Span |
| x1 ⁽³⁾ | 14.1 | — | 6 | 12.5 | — | 6 | 3.125 | — | 3 |
| x6 ⁽³⁾ | — | 14.1 | 6 | — | 12.5 | 6 | — | 3.125 | 6 |
| x6 PLL Feedback ⁽⁴⁾ | — | 14.1 | Side-wide | — | 12.5 | Side-wide | — | — | — |
| xN (PCIe) | — | 8.0 | 8 | — | 5.0 | 8 | — | — | — |
| xN (Native PHY IP) | 8.0 | 8.0 | Up to 13 channels above and below PLL | 7.99 | 7.99 | Up to 13 channels above and below PLL | 3.125 | 3.125 | Up to 13 channels above and below PLL |
| | — | 8.01 to 9.8304 | Up to 7 channels above and below PLL | | | | | | |

Notes to Table 24:

- (1) Valid data rates below the maximum specified in this table depend on the reference clock frequency and the PLL counter settings. Check the MegaWizard message during the PHY IP instantiation.
- (2) ATX PLL is recommended at 8 Gbps and above data rates for improved jitter performance.
- (3) Channel span is within a transceiver bank.
- (4) Side-wide channel bonding is allowed up to the maximum supported by the PHY IP.

Table 25 shows the approximate maximum data rate using the standard PCS.

Table 25. Stratix V Standard PCS Approximate Maximum Date Rate ⁽¹⁾, ⁽³⁾

| Mode ⁽²⁾ | Transceiver Speed Grade | PMA Width | 20 | 20 | 16 | 16 | 10 | 10 | 8 | 8 |
|---------------------|-------------------------|---------------------------------------|---------|---------|---------|---------|-----|-----|------|------|
| | | PCS/Core Width | 40 | 20 | 32 | 16 | 20 | 10 | 16 | 8 |
| FIFO | 1 | C1, C2, C2L, I2, I2L core speed grade | 12.2 | 11.4 | 9.76 | 9.12 | 6.5 | 5.8 | 5.2 | 4.72 |
| | 2 | C1, C2, C2L, I2, I2L core speed grade | 12.2 | 11.4 | 9.76 | 9.12 | 6.5 | 5.8 | 5.2 | 4.72 |
| | | C3, I3, I3L core speed grade | 9.8 | 9.0 | 7.84 | 7.2 | 5.3 | 4.7 | 4.24 | 3.76 |
| | 3 | C1, C2, C2L, I2, I2L core speed grade | 8.5 | 8.5 | 8.5 | 8.5 | 6.5 | 5.8 | 5.2 | 4.72 |
| | | I3YY core speed grade | 10.3125 | 10.3125 | 7.84 | 7.2 | 5.3 | 4.7 | 4.24 | 3.76 |
| | | C3, I3, I3L core speed grade | 8.5 | 8.5 | 7.84 | 7.2 | 5.3 | 4.7 | 4.24 | 3.76 |
| | | C4, I4 core speed grade | 8.5 | 8.2 | 7.04 | 6.56 | 4.8 | 4.2 | 3.84 | 3.44 |
| Register | 1 | C1, C2, C2L, I2, I2L core speed grade | 12.2 | 11.4 | 9.76 | 9.12 | 6.1 | 5.7 | 4.88 | 4.56 |
| | 2 | C1, C2, C2L, I2, I2L core speed grade | 12.2 | 11.4 | 9.76 | 9.12 | 6.1 | 5.7 | 4.88 | 4.56 |
| | | C3, I3, I3L core speed grade | 9.8 | 9.0 | 7.92 | 7.2 | 4.9 | 4.5 | 3.96 | 3.6 |
| | 3 | C1, C2, C2L, I2, I2L core speed grade | 10.3125 | 10.3125 | 10.3125 | 10.3125 | 6.1 | 5.7 | 4.88 | 4.56 |
| | | I3YY core speed grade | 10.3125 | 10.3125 | 7.92 | 7.2 | 4.9 | 4.5 | 3.96 | 3.6 |
| | | C3, I3, I3L core speed grade | 8.5 | 8.5 | 7.92 | 7.2 | 4.9 | 4.5 | 3.96 | 3.6 |
| | | C4, I4 core speed grade | 8.5 | 8.2 | 7.04 | 6.56 | 4.4 | 4.1 | 3.52 | 3.28 |

Notes to Table 25:

- (1) The maximum data rate is in Gbps.
- (2) The Phase Compensation FIFO can be configured in FIFO mode or register mode. In the FIFO mode, the pointers are not fixed, and the latency can vary. In the register mode the pointers are fixed for low latency.
- (3) The maximum data rate is also constrained by the transceiver speed grade. Refer to Table 1 for the transceiver speed grade.

Table 26 shows the approximate maximum data rate using the 10G PCS.

Table 26. Stratix V 10G PCS Approximate Maximum Data Rate ⁽¹⁾

| Mode ⁽²⁾ | Transceiver Speed Grade | PMA Width | 64 | 40 | 40 | 40 | 32 | 32 |
|---------------------|-------------------------|---------------------------------------|--------------|-------|-------|------|----------|-------|
| | | PCS Width | 64 | 66/67 | 50 | 40 | 64/66/67 | 32 |
| FIFO or Register | 1 | C1, C2, C2L, I2, I2L core speed grade | 14.1 | 14.1 | 10.69 | 14.1 | 13.6 | 13.6 |
| | 2 | C1, C2, C2L, I2, I2L core speed grade | 12.5 | 12.5 | 10.69 | 12.5 | 12.5 | 12.5 |
| | | C3, I3, I3L core speed grade | 12.5 | 12.5 | 10.69 | 12.5 | 10.88 | 10.88 |
| | 3 | C1, C2, C2L, I2, I2L core speed grade | 8.5 Gbps | | | | | |
| | | C3, I3, I3L core speed grade | | | | | | |
| | | C4, I4 core speed grade | | | | | | |
| | | I3YY core speed grade | 10.3125 Gbps | | | | | |

Notes to Table 26:

- (1) The maximum data rate is in Gbps.
- (2) The Phase Compensation FIFO can be configured in FIFO mode or register mode. In the FIFO mode, the pointers are not fixed, and the latency can vary. In the register mode the pointers are fixed for low latency.

Table 27 shows the V_{OD} settings for the GX channel.

Table 27. Typical V_{OD} Setting for GX Channel, TX Termination = 100 Ω ⁽²⁾

| Symbol | V_{OD} Setting | V_{OD} Value (mV) | V_{OD} Setting | V_{OD} Value (mV) |
|---|------------------|---------------------|------------------|---------------------|
| V_{OD} differential peak to peak typical ⁽³⁾ | 0 ⁽¹⁾ | 0 | 32 | 640 |
| | 1 ⁽¹⁾ | 20 | 33 | 660 |
| | 2 ⁽¹⁾ | 40 | 34 | 680 |
| | 3 ⁽¹⁾ | 60 | 35 | 700 |
| | 4 ⁽¹⁾ | 80 | 36 | 720 |
| | 5 ⁽¹⁾ | 100 | 37 | 740 |
| | 6 | 120 | 38 | 760 |
| | 7 | 140 | 39 | 780 |
| | 8 | 160 | 40 | 800 |
| | 9 | 180 | 41 | 820 |
| | 10 | 200 | 42 | 840 |
| | 11 | 220 | 43 | 860 |
| | 12 | 240 | 44 | 880 |
| | 13 | 260 | 45 | 900 |
| | 14 | 280 | 46 | 920 |
| | 15 | 300 | 47 | 940 |
| | 16 | 320 | 48 | 960 |
| | 17 | 340 | 49 | 980 |
| | 18 | 360 | 50 | 1000 |
| | 19 | 380 | 51 | 1020 |
| | 20 | 400 | 52 | 1040 |
| | 21 | 420 | 53 | 1060 |
| | 22 | 440 | 54 | 1080 |
| | 23 | 460 | 55 | 1100 |
| | 24 | 480 | 56 | 1120 |
| | 25 | 500 | 57 | 1140 |
| | 26 | 520 | 58 | 1160 |
| | 27 | 540 | 59 | 1180 |
| | 28 | 560 | 60 | 1200 |
| | 29 | 580 | 61 | 1220 |
| | 30 | 600 | 62 | 1240 |
| | 31 | 620 | 63 | 1260 |

Note to Table 27:

- (1) If TX termination resistance = 100 Ω , this VOD setting is illegal.
- (2) The tolerance is +/-20% for all VOD settings except for settings 2 and below.
- (3) Refer to Figure 2.

Table 28. Transceiver Specifications for Stratix V GT Devices (Part 2 of 5) ⁽¹⁾

| Symbol/ Description | Conditions | Transceiver Speed Grade 2 | | | Transceiver Speed Grade 3 | | | Unit |
|---|---|--|---------------|--------|------------------------------|---------------|--------|----------|
| | | Min | Typ | Max | Min | Typ | Max | |
| Transmitter REFCLK Phase Noise (622 MHz) ⁽¹⁸⁾ | 100 Hz | — | — | -70 | — | — | -70 | dBc/Hz |
| | 1 kHz | — | — | -90 | — | — | -90 | |
| | 10 kHz | — | — | -100 | — | — | -100 | |
| | 100 kHz | — | — | -110 | — | — | -110 | |
| | ≥ 1 MHz | — | — | -120 | — | — | -120 | |
| Transmitter REFCLK Phase Jitter (100 MHz) ⁽¹⁵⁾ | 10 kHz to 1.5 MHz (PCIe) | — | — | 3 | — | — | 3 | ps (rms) |
| RREF ⁽¹⁷⁾ | — | — | 1800 ± 1% | — | — | 1800 ± 1% | — | Ω |
| Transceiver Clocks | | | | | | | | |
| fixedclk clock frequency | PCIe Receiver Detect | — | 100 or 125 | — | — | 100 or 125 | — | MHz |
| Reconfiguration clock (mgmt_clk_clk) frequency | — | 100 | — | 125 | 100 | — | 125 | MHz |
| Receiver | | | | | | | | |
| Supported I/O Standards | — | 1.4-V PCML, 1.5-V PCML, 2.5-V PCML, LVPECL, and LVDS | | | | | | |
| Data rate (Standard PCS) ⁽²¹⁾ | GX channels | 600 | — | 8500 | 600 | — | 8500 | Mbps |
| Data rate (10G PCS) ⁽²¹⁾ | GX channels | 600 | — | 12,500 | 600 | — | 12,500 | Mbps |
| Data rate | GT channels | 19,600 | — | 28,050 | 19,600 | — | 25,780 | Mbps |
| Absolute V _{MAX} for a receiver pin ⁽³⁾ | GT channels | — | — | 1.2 | — | — | 1.2 | V |
| Absolute V _{MIN} for a receiver pin | GT channels | -0.4 | — | — | -0.4 | — | — | V |
| Maximum peak-to-peak differential input voltage V _{ID} (diff p-p) before device configuration ⁽²⁰⁾ | GT channels | — | — | 1.6 | — | — | 1.6 | V |
| | GX channels | ⁽⁸⁾ | | | | | | |
| Maximum peak-to-peak differential input voltage V _{ID} (diff p-p) after device configuration ⁽¹⁶⁾ , ⁽²⁰⁾ | GT channels V _{CCR_GTB} = 1.05 V (V _{ICM} = 0.65 V) | — | — | 2.2 | — | — | 2.2 | V |
| | GX channels | ⁽⁸⁾ | | | | | | |
| Minimum differential eye opening at receiver serial input pins ⁽⁴⁾ , ⁽²⁰⁾ | GT channels | 200 | — | — | 200 | — | — | mV |
| | GX channels | ⁽⁸⁾ | | | | | | |

Table 28. Transceiver Specifications for Stratix V GT Devices (Part 5 of 5) ⁽¹⁾

| Symbol/ Description | Conditions | Transceiver Speed Grade 2 | | | Transceiver Speed Grade 3 | | | Unit |
|---------------------------------|------------|------------------------------|-----|-----|------------------------------|-----|-----|------|
| | | Min | Typ | Max | Min | Typ | Max | |
| t_{pll_lock} ⁽¹⁴⁾ | — | — | — | 10 | — | — | 10 | μs |

Notes to Table 28:

- (1) Speed grades shown refer to the PMA Speed Grade in the device ordering code. The maximum data rate could be restricted by the Core/PCS speed grade. Contact your Altera Sales Representative for the maximum data rate specifications in each speed grade combination offered. For more information about device ordering codes, refer to the *Stratix V Device Overview*.
- (2) The reference clock common mode voltage is equal to the VCCR_GXB power supply level.
- (3) The device cannot tolerate prolonged operation at this absolute maximum.
- (4) The differential eye opening specification at the receiver input pins assumes that receiver equalization is disabled. If you enable receiver equalization, the receiver circuitry can tolerate a lower minimum eye opening, depending on the equalization level.
- (5) Refer to Figure 5 for the GT channel AC gain curves. The total effective AC gain is the AC gain minus the DC gain.
- (6) Refer to Figure 6 for the GT channel DC gain curves.
- (7) CFP2 optical modules require the host interface to have the receiver data pins differentially terminated with 100 Ω. The internal OCT feature is available after the Stratix V FPGA configuration is completed. Altera recommends that FPGA configuration is completed before inserting the optical module. Otherwise, minimize unnecessary removal and insertion with unconfigured devices.
- (8) Specifications for this parameter are the same as for Stratix V GX and GS devices. See Table 23 for specifications.
- (9) t_{LTR} is the time required for the receive CDR to lock to the input reference clock frequency after coming out of reset.
- (10) t_{LTD} is time required for the receiver CDR to start recovering valid data after the $rx_is_lockedtodata$ signal goes high.
- (11) t_{LTD_manual} is the time required for the receiver CDR to start recovering valid data after the $rx_is_lockedtodata$ signal goes high when the CDR is functioning in the manual mode.
- (12) $t_{LTR_LTD_manual}$ is the time the receiver CDR must be kept in lock to reference (LTR) mode after the $rx_is_lockedtoref$ signal goes high when the CDR is functioning in the manual mode.
- (13) $tp11_powerdown$ is the PLL powerdown minimum pulse width.
- (14) $tp11_lock$ is the time required for the transmitter CMU/ATX PLL to lock to the input reference clock frequency after coming out of reset.
- (15) To calculate the REFCLK rms phase jitter requirement for PCIe at reference clock frequencies other than 100 MHz, use the following formula:
REFCLK rms phase jitter at f(MHz) = REFCLK rms phase jitter at 100 MHz × 100/f.
- (16) The maximum peak to peak differential input voltage V_{ID} after device configuration is equal to $4 \times (\text{absolute } V_{MAX} \text{ for receiver pin} - V_{ICM})$.
- (17) For ES devices, RREF is 2000 Ω ±1%.
- (18) To calculate the REFCLK phase noise requirement at frequencies other than 622 MHz, use the following formula: REFCLK phase noise at f(MHz) = REFCLK phase noise at 622 MHz + 20*log(f/622).
- (19) SFP/+ optical modules require the host interface to have RD+/- differentially terminated with 100 Ω. The internal OCT feature is available after the Stratix V FPGA configuration is completed. Altera recommends that FPGA configuration is completed before inserting the optical module. Otherwise, minimize unnecessary removal and insertion with unconfigured devices.
- (20) Refer to Figure 4.
- (21) For oversampling design to support data rates less than the minimum specification, the CDR needs to be in LTR mode only.
- (22) This supply follows VCCR_GXB for both GX and GT channels.
- (23) When you use fPLL as a TXPLL of the transceiver.

Table 31. PLL Specifications for Stratix V Devices (Part 3 of 3)

| Symbol | Parameter | Min | Typ | Max | Unit |
|-----------|--|--------|------|-------|------|
| f_{RES} | Resolution of VCO frequency ($f_{INPFD} = 100$ MHz) | 390625 | 5.96 | 0.023 | Hz |

Notes to Table 31:

- (1) This specification is limited in the Quartus II software by the I/O maximum frequency. The maximum I/O frequency is different for each I/O standard.
- (2) This specification is limited by the lower of the two: I/O f_{MAX} or f_{OUT} of the PLL.
- (3) A high input jitter directly affects the PLL output jitter. To have low PLL output clock jitter, you must provide a clean clock source < 120 ps.
- (4) f_{REF} is f_{IN}/N when $N = 1$.
- (5) Peak-to-peak jitter with a probability level of 10^{-12} (14 sigma, 99.9999999974404% confidence level). The output jitter specification applies to the intrinsic jitter of the PLL, when an input jitter of 30 ps is applied. The external memory interface clock output jitter specifications use a different measurement method and are available in Table 44 on page 52.
- (6) The cascaded PLL specification is only applicable with the following condition:
 - a. Upstream PLL: $0.59\text{MHz} \leq \text{Upstream PLL BW} < 1$ MHz
 - b. Downstream PLL: Downstream PLL BW > 2 MHz
- (7) High bandwidth PLL settings are not supported in external feedback mode.
- (8) The external memory interface clock output jitter specifications use a different measurement method, which is available in Table 42 on page 50.
- (9) The VCO frequency reported by the Quartus II software in the PLL Usage Summary section of the compilation report takes into consideration the VCO post-scale counter K value. Therefore, if the counter K has a value of 2, the frequency reported can be lower than the f_{VCO} specification.
- (10) This specification only covers fractional PLL for low bandwidth. The f_{VCO} for fractional value range 0.05 - 0.95 must be ≥ 1000 MHz, while f_{VCO} for fractional value range 0.20 - 0.80 must be ≥ 1200 MHz.
- (11) This specification only covered fractional PLL for low bandwidth. The f_{VCO} for fractional value range 0.05-0.95 must be ≥ 1000 MHz.
- (12) This specification only covered fractional PLL for low bandwidth. The f_{VCO} for fractional value range 0.20-0.80 must be ≥ 1200 MHz.

DSP Block Specifications

Table 32 lists the Stratix V DSP block performance specifications.

Table 32. Block Performance Specifications for Stratix V DSP Devices (Part 1 of 2)

| Mode | Peformance | | | | | | | Unit |
|--|------------|---------|---------|-----|---------------|-----|-----|------|
| | C1 | C2, C2L | I2, I2L | C3 | I3, I3L, I3YY | C4 | I4 | |
| Modes using one DSP | | | | | | | | |
| Three 9 x 9 | 600 | 600 | 600 | 480 | 480 | 420 | 420 | MHz |
| One 18 x 18 | 600 | 600 | 600 | 480 | 480 | 420 | 400 | MHz |
| Two partial 18 x 18 (or 16 x 16) | 600 | 600 | 600 | 480 | 480 | 420 | 400 | MHz |
| One 27 x 27 | 500 | 500 | 500 | 400 | 400 | 350 | 350 | MHz |
| One 36 x 18 | 500 | 500 | 500 | 400 | 400 | 350 | 350 | MHz |
| One sum of two 18 x 18(One sum of 2 16 x 16) | 500 | 500 | 500 | 400 | 400 | 350 | 350 | MHz |
| One sum of square | 500 | 500 | 500 | 400 | 400 | 350 | 350 | MHz |
| One 18 x 18 plus 36 (a x b) + c | 500 | 500 | 500 | 400 | 400 | 350 | 350 | MHz |
| Modes using two DSPs | | | | | | | | |
| Three 18 x 18 | 500 | 500 | 500 | 400 | 400 | 350 | 350 | MHz |
| One sum of four 18 x 18 | 475 | 475 | 475 | 380 | 380 | 300 | 300 | MHz |
| One sum of two 27 x 27 | 465 | 465 | 450 | 380 | 380 | 300 | 290 | MHz |
| One sum of two 36 x 18 | 475 | 475 | 475 | 380 | 380 | 300 | 300 | MHz |
| One complex 18 x 18 | 500 | 500 | 500 | 400 | 400 | 350 | 350 | MHz |
| One 36 x 36 | 475 | 475 | 475 | 380 | 380 | 300 | 300 | MHz |

Table 36. High-Speed I/O Specifications for Stratix V Devices ^{(1), (2)} (Part 2 of 4)

| Symbol | Conditions | C1 | | | C2, C2L, I2, I2L | | | C3, I3, I3L, I3YY | | | C4,I4 | | | Unit |
|--|---|-----|-----|------|------------------|-----|------|-------------------|-----|------|-------|-----|------|------|
| | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| Transmitter | | | | | | | | | | | | | | |
| True Differential I/O Standards - f _{HSDR} (data rate) | SERDES factor J = 3 to 10 ^{(9), (11), (12), (13), (14), (15), (16)} | (6) | — | 1600 | (6) | — | 1434 | (6) | — | 1250 | (6) | — | 1050 | Mbps |
| | SERDES factor J ≥ 4 LVDS TX with DPA ^{(12), (14), (15), (16)} | (6) | — | 1600 | (6) | — | 1600 | (6) | — | 1600 | (6) | — | 1250 | Mbps |
| | SERDES factor J = 2, uses DDR Registers | (6) | — | (7) | (6) | — | (7) | (6) | — | (7) | (6) | — | (7) | Mbps |
| | SERDES factor J = 1, uses SDR Register | (6) | — | (7) | (6) | — | (7) | (6) | — | (7) | (6) | — | (7) | Mbps |
| Emulated Differential I/O Standards with Three External Output Resistor Networks - f _{HSDR} (data rate) ⁽¹⁰⁾ | SERDES factor J = 4 to 10 ⁽¹⁷⁾ | (6) | — | 1100 | (6) | — | 1100 | (6) | — | 840 | (6) | — | 840 | Mbps |
| t _{x Jitter} - True Differential I/O Standards | Total Jitter for Data Rate 600 Mbps - 1.25 Gbps | — | — | 160 | — | — | 160 | — | — | 160 | — | — | 160 | ps |
| | Total Jitter for Data Rate < 600 Mbps | — | — | 0.1 | — | — | 0.1 | — | — | 0.1 | — | — | 0.1 | UI |
| t _{x Jitter} - Emulated Differential I/O Standards with Three External Output Resistor Network | Total Jitter for Data Rate 600 Mbps - 1.25 Gbps | — | — | 300 | — | — | 300 | — | — | 300 | — | — | 325 | ps |
| | Total Jitter for Data Rate < 600 Mbps | — | — | 0.2 | — | — | 0.2 | — | — | 0.2 | — | — | 0.25 | UI |

Figure 7 shows the dynamic phase alignment (DPA) lock time specifications with the DPA PLL calibration option enabled.

Figure 7. DPA Lock Time Specification with DPA PLL Calibration Enabled



Table 37 lists the DPA lock time specifications for Stratix V devices.

Table 37. DPA Lock Time Specifications for Stratix V GX Devices Only ^{(1), (2), (3)}

| Standard | Training Pattern | Number of Data Transitions in One Repetition of the Training Pattern | Number of Repetitions per 256 Data Transitions ⁽⁴⁾ | Maximum |
|--------------------|----------------------|--|---|----------------------|
| SPI-4 | 00000000001111111111 | 2 | 128 | 640 data transitions |
| Parallel Rapid I/O | 00001111 | 2 | 128 | 640 data transitions |
| | 10010000 | 4 | 64 | 640 data transitions |
| Miscellaneous | 10101010 | 8 | 32 | 640 data transitions |
| | 01010101 | 8 | 32 | 640 data transitions |

Notes to Table 37:

- (1) The DPA lock time is for one channel.
- (2) One data transition is defined as a 0-to-1 or 1-to-0 transition.
- (3) The DPA lock time stated in this table applies to both commercial and industrial grade.
- (4) This is the number of repetitions for the stated training pattern to achieve the 256 data transitions.

Figure 8 shows the LVDS soft-clock data recovery (CDR)/DPA sinusoidal jitter tolerance specification for a data rate ≥ 1.25 Gbps. Table 38 lists the LVDS soft-CDR/DPA sinusoidal jitter tolerance specification for a data rate ≥ 1.25 Gbps.

Figure 8. LVDS Soft-CDR/DPA Sinusoidal Jitter Tolerance Specification for a Data Rate ≥ 1.25 Gbps



Duty Cycle Distortion (DCD) Specifications

Table 44 lists the worst-case DCD for Stratix V devices.

Table 44. Worst-Case DCD on Stratix V I/O Pins ⁽¹⁾

| Symbol | C1 | | C2, C2L, I2, I2L | | C3, I3, I3L, I3YY | | C4, I4 | | Unit |
|-------------------|-----|-----|------------------|-----|-------------------|-----|--------|-----|------|
| | Min | Max | Min | Max | Min | Max | Min | Max | |
| Output Duty Cycle | 45 | 55 | 45 | 55 | 45 | 55 | 45 | 55 | % |

Note to Table 44:

(1) The DCD numbers do not cover the core clock network.

Configuration Specification

POR Delay Specification

Power-on reset (POR) delay is defined as the delay between the time when all the power supplies monitored by the POR circuitry reach the minimum recommended operating voltage to the time when the nSTATUS is released high and your device is ready to begin configuration.



For more information about the POR delay, refer to the *Hot Socketing and Power-On Reset in Stratix V Devices* chapter.

Table 45 lists the fast and standard POR delay specification.

Table 45. Fast and Standard POR Delay Specification ⁽¹⁾

| POR Delay | Minimum | Maximum |
|-----------|---------|---------|
| Fast | 4 ms | 12 ms |
| Standard | 100 ms | 300 ms |

Note to Table 45:

(1) You can select the POR delay based on the MSEL settings as described in the MSEL Pin Settings section of the “Configuration, Design Security, and Remote System Upgrades in Stratix V Devices” chapter.

JTAG Configuration Specifications

Table 46 lists the JTAG timing parameters and values for Stratix V devices.

Table 46. JTAG Timing Parameters and Values for Stratix V Devices

| Symbol | Description | Min | Max | Unit |
|-------------------------|------------------------------------|-----|-----|------|
| t _{JCP} | TCK clock period ⁽²⁾ | 30 | — | ns |
| t _{JCP} | TCK clock period ⁽²⁾ | 167 | — | ns |
| t _{JCH} | TCK clock high time ⁽²⁾ | 14 | — | ns |
| t _{JCL} | TCK clock low time ⁽²⁾ | 14 | — | ns |
| t _{JPSU (TDI)} | TDI JTAG port setup time | 2 | — | ns |
| t _{JPSU (TMS)} | TMS JTAG port setup time | 3 | — | ns |

Table 47. Uncompressed .rbf Sizes for Stratix V Devices

| Family | Device | Package | Configuration .rbf Size (bits) | IOCSR .rbf Size (bits) ^{(4), (5)} |
|----------------------------|--------|---------|--------------------------------|--|
| Stratix V E ⁽¹⁾ | 5SEE9 | — | 342,742,976 | 700,888 |
| | 5SEEB | — | 342,742,976 | 700,888 |

Notes to Table 47:

- (1) Stratix V E devices do not have PCI Express® (PCIe®) hard IP. Stratix V E devices do not support the CvP configuration scheme.
- (2) 36-transceiver devices.
- (3) 24-transceiver devices.
- (4) File size for the periphery image.
- (5) The IOCSR .rbf size is specifically for the CvP feature.

Use the data in Table 47 to estimate the file size before design compilation. Different configuration file formats, such as a hexadecimal (.hex) or tabular text file (.tff) format, have different file sizes. For the different types of configuration file and file sizes, refer to the Quartus II software. However, for a specific version of the Quartus II software, any design targeted for the same device has the same uncompressed configuration file size. If you are using compression, the file size can vary after each compilation because the compression ratio depends on your design.



For more information about setting device configuration options, refer to *Configuration, Design Security, and Remote System Upgrades in Stratix V Devices*. For creating configuration files, refer to the *Quartus II Help*.

Table 48 lists the minimum configuration time estimates for Stratix V devices.

Table 48. Minimum Configuration Time Estimation for Stratix V Devices

| Variant | Member Code | Active Serial ⁽¹⁾ | | | Fast Passive Parallel ⁽²⁾ | | |
|---------|-------------|------------------------------|------------|---------------------|--------------------------------------|------------|---------------------|
| | | Width | DCLK (MHz) | Min Config Time (s) | Width | DCLK (MHz) | Min Config Time (s) |
| GX | A3 | 4 | 100 | 0.534 | 32 | 100 | 0.067 |
| | | 4 | 100 | 0.344 | 32 | 100 | 0.043 |
| | A4 | 4 | 100 | 0.534 | 32 | 100 | 0.067 |
| | A5 | 4 | 100 | 0.675 | 32 | 100 | 0.084 |
| | A7 | 4 | 100 | 0.675 | 32 | 100 | 0.084 |
| | A9 | 4 | 100 | 0.857 | 32 | 100 | 0.107 |
| | AB | 4 | 100 | 0.857 | 32 | 100 | 0.107 |
| | B5 | 4 | 100 | 0.676 | 32 | 100 | 0.085 |
| | B6 | 4 | 100 | 0.676 | 32 | 100 | 0.085 |
| | B9 | 4 | 100 | 0.857 | 32 | 100 | 0.107 |
| | BB | 4 | 100 | 0.857 | 32 | 100 | 0.107 |
| GT | C5 | 4 | 100 | 0.675 | 32 | 100 | 0.084 |
| | C7 | 4 | 100 | 0.675 | 32 | 100 | 0.084 |

Table 48. Minimum Configuration Time Estimation for Stratix V Devices

| Variant | Member Code | Active Serial ⁽¹⁾ | | | Fast Passive Parallel ⁽²⁾ | | |
|---------|-------------|------------------------------|------------|---------------------|--------------------------------------|------------|---------------------|
| | | Width | DCLK (MHz) | Min Config Time (s) | Width | DCLK (MHz) | Min Config Time (s) |
| GS | D3 | 4 | 100 | 0.344 | 32 | 100 | 0.043 |
| | D4 | 4 | 100 | 0.534 | 32 | 100 | 0.067 |
| | | 4 | 100 | 0.344 | 32 | 100 | 0.043 |
| | D5 | 4 | 100 | 0.534 | 32 | 100 | 0.067 |
| | D6 | 4 | 100 | 0.741 | 32 | 100 | 0.093 |
| | D8 | 4 | 100 | 0.741 | 32 | 100 | 0.093 |
| E | E9 | 4 | 100 | 0.857 | 32 | 100 | 0.107 |
| | EB | 4 | 100 | 0.857 | 32 | 100 | 0.107 |

Notes to Table 48:

(1) DCLK frequency of 100 MHz using external CLKUSR.

(2) Max FPGA FPP bandwidth may exceed bandwidth available from some external storage or control logic.

Fast Passive Parallel Configuration Timing

This section describes the fast passive parallel (FPP) configuration timing parameters for Stratix V devices.

DCLK-to-DATA[] Ratio for FPP Configuration

FPP configuration requires a different DCLK-to-DATA [] ratio when you enable the design security, decompression, or both features. Table 49 lists the DCLK-to-DATA [] ratio for each combination.

Table 49. DCLK-to-DATA[] Ratio ⁽¹⁾ (Part 1 of 2)

| Configuration Scheme | Decompression | Design Security | DCLK-to-DATA[] Ratio |
|----------------------|---------------|-----------------|----------------------|
| FPP ×8 | Disabled | Disabled | 1 |
| | Disabled | Enabled | 1 |
| | Enabled | Disabled | 2 |
| | Enabled | Enabled | 2 |
| FPP ×16 | Disabled | Disabled | 1 |
| | Disabled | Enabled | 2 |
| | Enabled | Disabled | 4 |
| | Enabled | Enabled | 4 |

Figure 13. FPP Configuration Timing Waveform When the DCLK-to-DATA[] Ratio is >1 (1), (2)**Notes to Figure 13:**

- (1) Use this timing waveform and parameters when the DCLK-to-DATA[] ratio is >1. To find out the DCLK-to-DATA[] ratio for your system, refer to Table 49 on page 55.
- (2) The beginning of this waveform shows the device in user mode. In user mode, nCONFIG, nSTATUS, and CONF_DONE are at logic high levels. When nCONFIG is pulled low, a reconfiguration cycle begins.
- (3) After power-up, the Stratix V device holds nSTATUS low for the time as specified by the POR delay.
- (4) After power-up, before and during configuration, CONF_DONE is low.
- (5) Do not leave DCLK floating after configuration. You can drive it high or low, whichever is more convenient.
- (6) "r" denotes the DCLK-to-DATA[] ratio. For the DCLK-to-DATA[] ratio based on the decompression and the design security feature enable settings, refer to Table 49 on page 55.
- (7) If needed, pause DCLK by holding it low. When DCLK restarts, the external host must provide data on the DATA[31..0] pins prior to sending the first DCLK rising edge.
- (8) To ensure a successful configuration, send the entire configuration data to the Stratix V device. CONF_DONE is released high after the Stratix V device receives all the configuration data successfully. After CONF_DONE goes high, send two additional falling edges on DCLK to begin initialization and enter user mode.
- (9) After the option bit to enable the INIT_DONE pin is configured into the device, the INIT_DONE goes low.

Document Revision History

Table 61 lists the revision history for this chapter.

Table 61. Document Revision History (Part 1 of 3)

| Date | Version | Changes |
|---------------|---------|---|
| June 2018 | 3.9 | <ul style="list-style-type: none"> ■ Added the “Stratix V Device Overshoot Duration” figure. |
| April 2017 | 3.8 | <ul style="list-style-type: none"> ■ Added a footnote to the “High-Speed I/O Specifications for Stratix V Devices” table. ■ Changed the minimum value for t_{CD2UMC} in the “PS Timing Parameters for Stratix V Devices” table. ■ Changed the condition for $100\text{-}\Omega$ R_D in the “OCT Without Calibration Resistance Tolerance Specifications for Stratix V Devices” table. ■ Changed the minimum value for t_{CD2UMC} in the “AS Timing Parameters for AS ‘1 and AS ‘4 Configurations in Stratix V Devices” table ■ Changed the minimum value for t_{CD2UMC} in the “FPP Timing Parameters for Stratix V Devices When the DCLK-to-DATA[] Ratio is >1” table. ■ Changed the minimum value for t_{CD2UMC} in the “FPP Timing Parameters for Stratix V Devices When the DCLK-to-DATA[] Ratio is >1” table. ■ Changed the minimum number of clock cycles value in the “Initialization Clock Source Option and the Maximum Frequency” table. |
| June 2016 | 3.7 | <ul style="list-style-type: none"> ■ Added the V_{ID} minimum specification for LVPECL in the “Differential I/O Standard Specifications for Stratix V Devices” table ■ Added the I_{OUT} specification to the “Absolute Maximum Ratings for Stratix V Devices” table. |
| December 2015 | 3.6 | <ul style="list-style-type: none"> ■ Added a footnote to the “High-Speed I/O Specifications for Stratix V Devices” table. |
| December 2015 | 3.5 | <ul style="list-style-type: none"> ■ Changed the transmitter, receiver, and ATX PLL data rate specifications in the “Transceiver Specifications for Stratix V GX and GS Devices” table. ■ Changed the configuration .rbf sizes in the “Uncompressed .rbf Sizes for Stratix V Devices” table. |
| July 2015 | 3.4 | <ul style="list-style-type: none"> ■ Changed the data rate specification for transceiver speed grade 3 in the following tables: <ul style="list-style-type: none"> ■ “Transceiver Specifications for Stratix V GX and GS Devices” ■ “Stratix V Standard PCS Approximate Maximum Date Rate” ■ “Stratix V 10G PCS Approximate Maximum Data Rate” ■ Changed the conditions for reference clock rise and fall time, and added a note to the “Transceiver Specifications for Stratix V GX and GS Devices” table. ■ Added a note to the “Minimum differential eye opening at receiver serial input pins” specification in the “Transceiver Specifications for Stratix V GX and GS Devices” table. ■ Changed the t_{CO} maximum value in the “AS Timing Parameters for AS ‘1 and AS ‘4 Configurations in Stratix V Devices” table. ■ Removed the CDR ppm tolerance specification from the “Transceiver Specifications for Stratix V GX and GS Devices” table. |

Table 61. Document Revision History (Part 3 of 3)

| Date | Version | Changes |
|---------------|---------|--|
| May 2013 | 2.7 | <ul style="list-style-type: none"> ■ Updated Table 2, Table 6, Table 7, Table 20, Table 23, Table 27, Table 47, Table 60 ■ Added Table 24, Table 48 ■ Updated Figure 9, Figure 10, Figure 11, Figure 12 |
| February 2013 | 2.6 | <ul style="list-style-type: none"> ■ Updated Table 7, Table 9, Table 20, Table 23, Table 27, Table 30, Table 31, Table 35, Table 46 ■ Updated “Maximum Allowed Overshoot and Undershoot Voltage” |
| December 2012 | 2.5 | <ul style="list-style-type: none"> ■ Updated Table 3, Table 6, Table 7, Table 8, Table 23, Table 24, Table 25, Table 27, Table 30, Table 32, Table 35 ■ Added Table 33 ■ Added “Fast Passive Parallel Configuration Timing” ■ Added “Active Serial Configuration Timing” ■ Added “Passive Serial Configuration Timing” ■ Added “Remote System Upgrades” ■ Added “User Watchdog Internal Circuitry Timing Specification” ■ Added “Initialization” ■ Added “Raw Binary File Size” |
| June 2012 | 2.4 | <ul style="list-style-type: none"> ■ Added Figure 1, Figure 2, and Figure 3. ■ Updated Table 1, Table 2, Table 3, Table 6, Table 11, Table 22, Table 23, Table 27, Table 29, Table 30, Table 31, Table 32, Table 35, Table 38, Table 39, Table 40, Table 41, Table 43, Table 56, and Table 59. ■ Various edits throughout to fix bugs. ■ Changed title of document to <i>Stratix V Device Datasheet</i>. ■ Removed document from the Stratix V handbook and made it a separate document. |
| February 2012 | 2.3 | <ul style="list-style-type: none"> ■ Updated Table 1–22, Table 1–29, Table 1–31, and Table 1–31. |
| December 2011 | 2.2 | <ul style="list-style-type: none"> ■ Added Table 2–31. ■ Updated Table 2–28 and Table 2–34. |
| November 2011 | 2.1 | <ul style="list-style-type: none"> ■ Added Table 2–2 and Table 2–21 and updated Table 2–5 with information about Stratix V GT devices. ■ Updated Table 2–11, Table 2–13, Table 2–20, and Table 2–25. ■ Various edits throughout to fix SPRs. |
| May 2011 | 2.0 | <ul style="list-style-type: none"> ■ Updated Table 2–4, Table 2–18, Table 2–19, Table 2–21, Table 2–22, Table 2–23, and Table 2–24. ■ Updated the “DQ Logic Block and Memory Output Clock Jitter Specifications” title. ■ Chapter moved to Volume 1. ■ Minor text edits. |
| December 2010 | 1.1 | <ul style="list-style-type: none"> ■ Updated Table 1–2, Table 1–4, Table 1–19, and Table 1–23. ■ Converted chapter to the new template. ■ Minor text edits. |
| July 2010 | 1.0 | Initial release. |