# E·XFL

#### Intel - 5SGXEA5N3F40C3N Datasheet



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#### Understanding <u>Embedded - FPGAs (Field</u> <u>Programmable Gate Array)</u>

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

#### **Applications of Embedded - FPGAs**

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

#### Details

Product Status	Obsolete
Number of LABs/CLBs	185000
Number of Logic Elements/Cells	490000
Total RAM Bits	46080000
Number of I/O	600
Number of Gates	-
Voltage - Supply	0.82V ~ 0.88V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	1517-BBGA, FCBGA
Supplier Device Package	1517-FBGA (40x40)
Purchase URL	https://www.e-xfl.com/product-detail/intel/5sgxea5n3f40c3n

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

								·			
Transceiver Speed Grade	Core Speed Grade										
	C1	C2, C2L	C3	C4	<b>12, 12L</b>	13, 13L	<b>I</b> 3YY	14			
3 GX channel—8.5 Gbps	_	Yes	Yes	Yes	_	Yes	Yes <sup>(4)</sup>	Yes			

#### Table 1. Stratix V GX and GS Commercial and Industrial Speed Grade Offering <sup>(1), (2), (3)</sup> (Part 2 of 2)

Notes to Table 1:

(1) C = Commercial temperature grade; I = Industrial temperature grade.

(2) Lower number refers to faster speed grade.

(3) C2L, I2L, and I3L speed grades are for low-power devices.

(4) I3YY speed grades can achieve up to 10.3125 Gbps.

Table 2 lists the industrial and commercial speed grades for the Stratix V GT devices. **Table 2. Stratix V GT Commercial and Industrial Speed Grade Offering** <sup>(1)</sup>, <sup>(2)</sup>

Transseiver Speed Grade	Core Speed Grade						
Transceiver Speeu draue	C1	C2	12	13			
2 GX channel—12.5 Gbps GT channel—28.05 Gbps	Yes	Yes	_	_			
3 GX channel—12.5 Gbps GT channel—25.78 Gbps	Yes	Yes	Yes	Yes			

#### Notes to Table 2:

(1) C = Commercial temperature grade; I = Industrial temperature grade.

(2) Lower number refers to faster speed grade.

## **Absolute Maximum Ratings**

Absolute maximum ratings define the maximum operating conditions for Stratix V devices. The values are based on experiments conducted with the devices and theoretical modeling of breakdown and damage mechanisms. The functional operation of the device is not implied for these conditions.



Conditions other than those listed in Table 3 may cause permanent damage to the device. Additionally, device operation at the absolute maximum ratings for extended periods of time may have adverse effects on the device.

TANIC J. ANSULULC MAXIMUM NALINYS IVI SUALIX V DEVICES (FAIL I UI Z)	Table 3.	<b>Absolute Maximum</b>	Ratings	for Stratix \	/ Devices	(Part 1 of 2)
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Symbol	Description	Minimum	Maximum	Unit
V <sub>CC</sub>	Power supply for core voltage and periphery circuitry	-0.5	1.35	V
V <sub>CCPT</sub>	Power supply for programmable power technology	-0.5	1.8	V
V <sub>CCPGM</sub>	Power supply for configuration pins	-0.5	3.9	V
V <sub>CC_AUX</sub>	Auxiliary supply for the programmable power technology	-0.5	3.4	V
V <sub>CCBAT</sub>	Battery back-up power supply for design security volatile key register	-0.5	3.9	V
V <sub>CCPD</sub>	I/O pre-driver power supply	-0.5	3.9	V
V <sub>CCIO</sub>	I/O power supply	-0.5	3.9	V

This section lists the functional operating limits for the AC and DC parameters for Stratix V devices. Table 6 lists the steady-state voltage and current values expected from Stratix V devices. Power supply ramps must all be strictly monotonic, without plateaus.

Table 6. Recommended Operating Conditions for Stratix V Devices (Part 1 of 2)

Symbol	Description	Condition	Min <sup>(4)</sup>	Тур	Max <sup>(4)</sup>	Unit
	Core voltage and periphery circuitry power supply (C1, C2, I2, and I3YY speed grades)	_	0.87	0.9	0.93	V
V <sub>CC</sub>	Core voltage and periphery circuitry power supply (C2L, C3, C4, I2L, I3, I3L, and I4 speed grades) <sup>(3)</sup>		0.82	0.85	0.88	V
V <sub>CCPT</sub>	Power supply for programmable power technology	_	1.45	1.50	1.55	V
V <sub>CC_AUX</sub>	Auxiliary supply for the programmable power technology		2.375	2.5	2.625	V
VI (1)	I/O pre-driver (3.0 V) power supply	_	2.85	3.0	3.15	V
VCCPD	I/O pre-driver (2.5 V) power supply		2.375	2.5	2.625	V
	I/O buffers (3.0 V) power supply	_	2.85	3.0	3.15	V
V <sub>CCIO</sub>	I/O buffers (2.5 V) power supply		2.375	2.5	2.625	V
	I/O buffers (1.8 V) power supply	_	1.71	1.8	1.89	V
	I/O buffers (1.5 V) power supply	_	1.425	1.5	1.575	V
	I/O buffers (1.35 V) power supply		1.283	1.35	1.45	V
	I/O buffers (1.25 V) power supply	_	1.19	1.25	1.31	V
	I/O buffers (1.2 V) power supply	_	1.14	1.2	1.26	V
	Configuration pins (3.0 V) power supply		2.85	3.0	3.15	V
V <sub>CCPGM</sub>	Configuration pins (2.5 V) power supply	-	2.375	2.5	2.625	V
	Configuration pins (1.8 V) power supply	-	1.71	1.8	1.89	V
V <sub>CCA_FPLL</sub>	PLL analog voltage regulator power supply		2.375	2.5	2.625	V
V <sub>CCD_FPLL</sub>	PLL digital voltage regulator power supply	-	1.45	1.5	1.55	V
V <sub>CCBAT</sub> (2)	Battery back-up power supply (For design security volatile key register)	_	1.2	_	3.0	V
VI	DC input voltage	_	-0.5	—	3.6	V
V <sub>0</sub>	Output voltage		0	_	V <sub>CCIO</sub>	V
т	Operating junction temperature	Commercial	0	—	85	°C
IJ		Industrial	-40	_	100	°C

Symbol	Description	Condition	Min <sup>(4)</sup>	Тур	Max <sup>(4)</sup>	Unit
t <sub>RAMP</sub>	Power supply ramp time	Standard POR	200 µs	_	100 ms	—
		Fast POR	200 µs		4 ms	

#### Table 6. Recommended Operating Conditions for Stratix V Devices (Part 2 of 2)

#### Notes to Table 6:

(1)  $V_{CCPD}$  must be 2.5 V when  $V_{CCI0}$  is 2.5, 1.8, 1.5, 1.35, 1.25 or 1.2 V.  $V_{CCPD}$  must be 3.0 V when  $V_{CCI0}$  is 3.0 V.

(2) If you do not use the design security feature in Stratix V devices, connect V<sub>CCBAT</sub> to a 1.2- to 3.0-V power supply. Stratix V power-on-reset (POR) circuitry monitors V<sub>CCBAT</sub>. Stratix V devices will not exit POR if V<sub>CCBAT</sub> stays at logic low.

(3) C2L and I2L can also be run at 0.90 V for legacy boards that were designed for the C2 and I2 speed grades.

(4) The power supply value describes the budget for the DC (static) power supply tolerance and does not include the dynamic tolerance requirements. Refer to the PDN tool for the additional budget for the dynamic tolerance requirements.

Table 7 lists the transceiver power supply recommended operating conditions for Stratix V GX, GS, and GT devices.

## Table 7. Recommended Transceiver Power Supply Operating Conditions for Stratix V GX, GS, and GT Devices (Part 1 of 2)

Symbol	Description	Devices	Minimum <sup>(4)</sup>	Typical	Maximum <sup>(4)</sup>	Unit
V <sub>CCA GXBL</sub>	Transceiver channel PLL power supply (left		2.85	3.0	3.15	V
(1), (3)	side)	un, us, ui	2.375	2.5	2.625	v
V <sub>CCA_GXBR</sub>	Transceiver channel PLL power supply (right	CV CS	2.85	3.0	3.15	V
(1), (3)	side)	ux, us	2.375	2.5	2.625	v
V <sub>CCA_GTBR</sub>	Transceiver channel PLL power supply (right side)	GT	2.85	3.0	3.15	V
	Transceiver hard IP power supply (left side; C1, C2, I2, and I3YY speed grades)	GX, GS, GT	0.87	0.9	0.93	V
V <sub>CCHIP_L</sub>	Transceiver hard IP power supply (left side; C2L, C3, C4, I2L, I3, I3L, and I4 speed grades)	GX, GS, GT	0.82	0.85	0.88	V
	Transceiver hard IP power supply (right side; C1, C2, I2, and I3YY speed grades)	GX, GS, GT	0.87	0.9	0.93	V
V <sub>CCHIP_R</sub>	Transceiver hard IP power supply (right side; C2L, C3, C4, I2L, I3, I3L, and I4 speed grades)	GX, GS, GT	0.82	0.85	0.88	V
V <sub>CCHSSI_L</sub>	Transceiver PCS power supply (left side; C1, C2, I2, and I3YY speed grades)	GX, GS, GT	0.87	0.9	0.93	V
	Transceiver PCS power supply (left side; C2L, C3, C4, I2L, I3, I3L, and I4 speed grades)	GX, GS, GT	0.82	0.85	0.88	V
	Transceiver PCS power supply (right side; C1, C2, I2, and I3YY speed grades)	GX, GS, GT	0.87	0.9	0.93	V
V <sub>CCHSSI_R</sub>	Transceiver PCS power supply (right side; C2L, C3, C4, I2L, I3, I3L, and I4 speed grades)	GX, GS, GT	0.82	0.85	0.88	V
			0.82	0.85	0.88	
V <sub>CCR_GXBL</sub>	Receiver analog nower supply (left side)		0.87	0.90	0.93	V
(2) _	Therefore analog power supply (left Slue)	un, uo, ui	0.97	1.0	1.03	
			1.03	1.05	1.07	

Table 8 shows the transceiver power supply voltage requirements for various conditions.

**Table 8. Transceiver Power Supply Voltage Requirements** 

Conditions	Core Speed Grade	VCCR_GXB & VCCT_GXB <sup>(2)</sup>	VCCA_GXB	VCCH_GXB	Unit
If BOTH of the following conditions are true:	A11	1.05			
■ Data rate > 10.3 Gbps.	All	1.00			
<ul> <li>DFE is used.</li> </ul>					
If ANY of the following conditions are true <sup>(1)</sup> :			3.0		
<ul> <li>ATX PLL is used.</li> </ul>					
■ Data rate > 6.5Gbps.	All	1.0			
■ DFE (data rate ≤ 10.3 Gbps), AEQ, or EyeQ feature is used.				1.5	V
If ALL of the following	C1, C2, I2, and I3YY	0.90	2.5		
<ul> <li>ATX PLL is not used.</li> </ul>					
■ Data rate $\leq$ 6.5Gbps.	C2L, C3, C4, I2L, I3, I3L, and I4	0.85	2.5		
<ul> <li>DFE, AEQ, and EyeQ are not used.</li> </ul>					

#### Notes to Table 8:

(1) Choose this power supply voltage requirement option if you plan to upgrade your design later with any of the listed conditions.

(2) If the VCCR\_GXB and VCCT\_GXB supplies are set to 1.0 V or 1.05 V, they cannot be shared with the VCC core supply. If the VCCR\_GXB and VCCT\_GXB are set to either 0.90 V or 0.85 V, they can be shared with the VCC core supply.

#### **DC Characteristics**

This section lists the supply current, I/O pin leakage current, input pin capacitance, on-chip termination tolerance, and hot socketing specifications.

#### **Supply Current**

Supply current is the current drawn from the respective power rails used for power budgeting. Use the Excel-based Early Power Estimator (EPE) to get supply current estimates for your design because these currents vary greatly with the resources you use.

For more information about power estimation tools, refer to the *PowerPlay Early Power Estimator User Guide* and the *PowerPlay Power Analysis* chapter in the *Quartus II Handbook*.

## **Switching Characteristics**

This section provides performance characteristics of the Stratix V core and periphery blocks.

These characteristics can be designated as Preliminary or Final.

- Preliminary characteristics are created using simulation results, process data, and other known parameters. The title of these tables show the designation as "Preliminary."
- Final numbers are based on actual silicon characterization and testing. The numbers reflect the actual performance of the device under worst-case silicon process, voltage, and junction temperature conditions. There are no designations on finalized tables.

## **Transceiver Performance Specifications**

This section describes transceiver performance specifications.

Table 23 lists the Stratix V GX and GS transceiver specifications.

Table 23.	Transceiver 3	Specifications	for Stratix	V GX	and GS	Devices	(1)	(Part 1	nf 7	۱
Table 20.	TIANSUCIACI	opeonitionationa	IUI UIIAIIA	I UA	anu uu	DEVICES	• •	(1 61 6 1		

Symbol/	Conditions	Transceiver Speed Grade 1		Transceiver Speed Grade 2			Transceiver Speed Grade 3			Unit		
Description		Min	Тур	Max	Min	Тур	Max	Min	Тур	Max		
Reference Clock												
Supported I/O	Dedicated reference clock pin	1.2-V	PCML,	1.4-V PCM	IL, 1.5-∖	/ PCML	, 2.5-V PCN HCSL	1L, Diffe	rential	LVPECL, L\	/DS, and	
Standards	RX reference clock pin		1.4-V PCML, 1.5-V PCML, 2.5-V PCML, LVPECL, and LVDS									
Input Reference Clock Frequency (CMU PLL) <sup>(8)</sup>	_	40		710	40	_	710	40	_	710	MHz	
Input Reference Clock Frequency (ATX PLL) <sup>(8)</sup>		100		710	100		710	100		710	MHz	
Rise time	Measure at ±60 mV of differential signal <sup>(26)</sup>			400	_		400			400	ns	
Fall time	Measure at ±60 mV of differential signal <sup>(26)</sup>		_	400	_		400			400	– ps	
Duty cycle		45		55	45		55	45	—	55	%	
Spread-spectrum modulating clock frequency	PCI Express® (PCIe <sup>®</sup> )	30		33	30		33	30	_	33	kHz	

Table 24 shows the maximum transmitter data rate for the clock network.

Table 24. Clock Network Maximum Data Rate Transmitter Specifications (1)

	ATX PLL				CMU PLL <sup>(2)</sup>			fPLL			
Clock Network	Non- bonded Mode (Gbps)	Bonded Mode (Gbps)	Channel Span	Non- bonded Mode (Gbps)	Bonded Mode (Gbps)	Channel Span	Non- bonded Mode (Gbps)	Bonded Mode (Gbps)	Channel Span		
x1 <sup>(3)</sup>	14.1	_	6	12.5	_	6	3.125	—	3		
x6 <sup>(3)</sup>	_	14.1	6	—	12.5	6	—	3.125	6		
x6 PLL Feedback <sup>(4)</sup>	_	14.1	Side- wide	_	12.5	Side- wide	_	_	_		
xN (PCIe)	_	8.0	8	—	5.0	8	—	—	—		
xN (Native PHY IP)	8.0	8.0	Up to 13 channels above and below PLL	7 00	7 00	Up to 13 channels above	3 125	3 125	Up to 13 channels above		
	_	8.01 to 9.8304	Up to 7 channels above and below PLL	7.99	7.99	and below PLL	0.120	0.120	and below PLL		

Notes to Table 24:

(1) Valid data rates below the maximum specified in this table depend on the reference clock frequency and the PLL counter settings. Check the MegaWizard message during the PHY IP instantiation.

(2) ATX PLL is recommended at 8 Gbps and above data rates for improved jitter performance.

(3) Channel span is within a transceiver bank.

(4) Side-wide channel bonding is allowed up to the maximum supported by the PHY IP.

### Table 28. Transceiver Specifications for Stratix V GT Devices (Part 2 of 5)<sup>(1)</sup>

Symbol/	Conditions	S	Transceive peed Grade	r 2	SI	Unit		
Description		Min	Тур	Max	Min	Тур	Max	
	100 Hz	—	—	-70			-70	
Transmitter REFCLK	1 kHz		_	-90	_	_	-90	
Phase Noise (622	10 kHz		—	-100	_		-100	dBc/Hz
MHz) <sup>(18)</sup>	100 kHz			-110			-110	
	$\geq$ 1 MHz	—	—	-120	_	_	-120	
Transmitter REFCLK Phase Jitter (100 MHz) <sup>(15)</sup>	10 kHz to 1.5 MHz (PCle)	_	_	3		_	3	ps (rms)
RREF <sup>(17)</sup>	_	_	1800 ± 1%	—	_	1800 ± 1%	_	Ω
Transceiver Clocks								
fixedclk clock frequency	PCIe Receiver Detect	_	100 or 125	_	_	100 or 125	_	MHz
Reconfiguration clock (mgmt_clk_clk) frequency	_	100	_	125	100	_	125	MHz
Receiver	•							
Supported I/O Standards	_		1.4-V PCML	., 1.5-V PCMI	L, 2.5-V PCI	VIL, LVPEC	L, and LVDS	6
Data rate (Standard PCS) <sup>(21)</sup>	GX channels	600	_	8500	600	_	8500	Mbps
Data rate (10G PCS) <sup>(21)</sup>	GX channels	600	_	12,500	600	_	12,500	Mbps
Data rate	GT channels	19,600	—	28,050	19,600		25,780	Mbps
Absolute V <sub>MAX</sub> for a receiver pin <sup>(3)</sup>	GT channels	_	_	1.2	_	_	1.2	V
Absolute V <sub>MIN</sub> for a receiver pin	GT channels	-0.4	_	—	-0.4	_	_	V
Maximum peak-to-peak	GT channels	_		1.6	—	_	1.6	V
differential input voltage V <sub>ID</sub> (diff p-p) before device configuration <sup>(20)</sup>	GX channels				(8)			
	GT channels							
Maximum peak-to-peak differential input voltage $V_{ID}$ (diff p-p) after device	V <sub>CCR_GTB</sub> = 1.05 V (V <sub>ICM</sub> = 0.65 V)	_	_	2.2	_	—	2.2	V
	GX channels		1	1 1	(8)			1
Minimum differential	GT channels	200	_	—	200		_	mV
eye opening at receiver serial input pins <sup>(4)</sup> , <sup>(20)</sup>	GX channels			·	(8)			

Mode	C1	C2, C2L	12, 12L	C3	13, 13L, 13YY	C4	14	Unit	
		Modes us	ing Three	DSPs					
One complex 18 x 25	425	425	415	340	340	275	265	MHz	
Modes using Four DSPs									
One complex 27 x 27	465	465	465	380	380	300	290	MHz	

#### Table 32. Block Performance Specifications for Stratix V DSP Devices (Part 2 of 2)

## **Memory Block Specifications**

Table 33 lists the Stratix V memory block specifications.

### Table 33. Memory Block Performance Specifications for Stratix V Devices <sup>(1), (2)</sup> (Part 1 of 2)

		Resour	<b>Resources Used</b>		Performance							
Memory	Mode	ALUTS	Memory	C1	C2, C2L	C3	C4	12, 12L	13, 13L, 13YY	14	Unit	
	Single port, all supported widths	0	1	450	450	400	315	450	400	315	MHz	
MLAR	Simple dual-port, x32/x64 depth	0	1	450	450	400	315	450	400	315	MHz	
WILAD	Simple dual-port, x16 depth <sup>(3)</sup>	0	1	675	675	533	400	675	533	400	MHz	
	ROM, all supported widths	0	1	600	600	500	450	600	500	450	MHz	

Symbol	Conditiono		C1		C2,	C2L, I	2, I2L	C3,	13, 131	., <b>I</b> 3YY	C4,14			Ilait
Symbol	Conditions	Min	Тур	Max	Min	Тур	Max	Min	Тур	Max	Min	Тур	Max	Unit
Transmitter														
	SERDES factor J = 3 to 10 <sup>(9)</sup> , <sup>(11)</sup> , <sup>(12)</sup> , <sup>(13)</sup> , <sup>(14)</sup> , <sup>(15)</sup> , <sup>(16)</sup>	(6)	_	1600	(6)	_	1434	(6)	_	1250	(6)		1050	Mbps
True Differential I/O Standards	SERDES factor J $\geq 4$ LVDS TX with DPA (12), (14), (15), (16)	(6)		1600	(6)		1600	(6)		1600	(6)	_	1250	Mbps
- f <sub>HSDR</sub> (data rate)	SERDES factor J = 2, uses DDR Registers	(6)	_	(7)	(6)	_	(7)	(6)	_	(7)	(6)		(7)	Mbps
	SERDES factor J = 1, uses SDR Register	(6)	_	(7)	(6)	_	(7)	(6)	_	(7)	(6)		(7)	Mbps
Emulated Differential I/O Standards with Three External Output Resistor Networks - f <sub>HSDR</sub> (data rate) <sup>(10)</sup>	SERDES factor J = 4 to 10 $(17)$	(6)		1100	(6)		1100	(6)		840	(6)		840	Mbps
t <sub>x Jitter</sub> - True Differential	Total Jitter for Data Rate 600 Mbps - 1.25 Gbps		_	160		_	160		_	160		_	160	ps
I/O Standards	Total Jitter for Data Rate < 600 Mbps		_	0.1		_	0.1	_	_	0.1	_	_	0.1	UI
t <sub>x Jitter</sub> - Emulated Differential I/O Standards	Total Jitter for Data Rate 600 Mbps - 1.25 Gbps	_	_	300	_	_	300	_	_	300	_		325	ps
External Output Resistor Network	Total Jitter for Data Rate < 600 Mbps	_	_	0.2	_	_	0.2	_	_	0.2	_	_	0.25	UI

## Table 36. High-Speed I/O Specifications for Stratix V Devices <sup>(1), (2)</sup> (Part 2 of 4)

Figure 7 shows the dynamic phase alignment (DPA) lock time specifications with the DPA PLL calibration option enabled.

Figure 7. DPA Lock Time Specification with DPA PLL Calibration Enabled

rx_reset			
rx_dpa_locked			<u> </u>
			-

Table 37 lists the DPA lock time specifications for Stratix V devices.

Table 37. DPA Lock Time Specifications for Stratix V GX Devices Only (1), (2), (3)

Standard	Training Pattern	Number of Data Transitions in One Repetition of the Training Pattern	Number of Repetitions per 256 Data Transitions <sup>(4)</sup>	Maximum
SPI-4	00000000001111111111	2	128	640 data transitions
Parallel Rapid I/O	00001111	2	128	640 data transitions
	10010000	4	64	640 data transitions
Miscollanoous	10101010	8	32	640 data transitions
Wiscenareous	01010101	8	32	640 data transitions

#### Notes to Table 37:

(1) The DPA lock time is for one channel.

(2) One data transition is defined as a 0-to-1 or 1-to-0 transition.

(3) The DPA lock time stated in this table applies to both commercial and industrial grade.

(4) This is the number of repetitions for the stated training pattern to achieve the 256 data transitions.

Figure 8 shows the **LVDS** soft-clock data recovery (CDR)/DPA sinusoidal jitter tolerance specification for a data rate  $\geq$  1.25 Gbps. Table 38 lists the **LVDS** soft-CDR/DPA sinusoidal jitter tolerance specification for a data rate  $\geq$  1.25 Gbps.





Speed Grade	Min	Max	Unit
C4,I4	8	16	ps

#### Table 40. DQS Phase Offset Delay Per Setting for Stratix V Devices <sup>(1), (2)</sup> (Part 2 of 2)

#### Notes to Table 40:

(1) The typical value equals the average of the minimum and maximum values.

(2) The delay settings are linear with a cumulative delay variation of 40 ps for all speed grades. For example, when using a -2 speed grade and applying a 10-phase offset setting to a 90° phase shift at 400 MHz, the expected average cumulative delay is [625 ps + (10 × 10 ps) ± 20 ps] = 725 ps ± 20 ps.

Table 41 lists the DQS phase shift error for Stratix V devices.

Table 41. DQS Phase Shift Error Specification for DLL-Delayed Clock (t<sub>DQS\_PSERR</sub>) for Stratix V Devices <sup>(1)</sup>

Number of DQS Delay Buffers	C1	C2, C2L, I2, I2L	C3, I3, I3L, I3YY	C4,14	Unit
1	28	28	30	32	ps
2	56	56	60	64	ps
3	84	84	90	96	ps
4	112	112	120	128	ps

Notes to Table 41:

(1) This error specification is the absolute maximum and minimum error. For example, skew on three DQS delay buffers in a -2 speed grade is  $\pm 78$  ps or  $\pm 39$  ps.

Table 42 lists the memory output clock jitter specifications for Stratix V devices.

Table 42. Memory Output Clock Jitter Specification for Stratix V Devices (1	<sup>),</sup> (Part 1 of 2) <sup>(2), (3)</sup>
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Clock	Parameter	Symbol	C1		C2, C2L, I2, I2L		C3, I3, I3L, I3YY		C4,14		Unit
NELWURK		-	Min	Max	Min	Max	Min	Max	Min	Max	
	Clock period jitter	$t_{JIT(per)}$	-50	50	-50	50	-55	55	-55	55	ps
Regional	Cycle-to-cycle period jitter	$t_{\text{JIT(cc)}}$	-100	100	-100	100	-110	110	-110	110	ps
	Duty cycle jitter	t <sub>JIT(duty)</sub>	-50	50	-50	50	-82.5	82.5	-82.5	82.5	ps
	Clock period jitter	$t_{JIT(per)}$	-75	75	-75	75	-82.5	82.5	-82.5	82.5	ps
Global	Cycle-to-cycle period jitter	t <sub>JIT(cc)</sub>	-150	150	-150	150	-165	165	-165	165	ps
	Duty cycle jitter	$t_{\text{JIT}(\text{duty})}$	-75	75	-75	75	-90	90	-90	90	ps

## **Duty Cycle Distortion (DCD) Specifications**

Table 44 lists the worst-case DCD for Stratix V devices.

#### Table 44. Worst-Case DCD on Stratix V I/O Pins (1)

Symbol	C	C1 C2, C2L, I2, I2L		L, 12, 12L	C3, I3, I3L, I3YY		C4,14		Unit
-	Min	Max	Min	Max	Min	Max	Min	Max	
Output Duty Cycle	45	55	45	55	45	55	45	55	%

#### Note to Table 44:

(1) The DCD numbers do not cover the core clock network.

## **Configuration Specification**

## **POR Delay Specification**

Power-on reset (POR) delay is defined as the delay between the time when all the power supplies monitored by the POR circuitry reach the minimum recommended operating voltage to the time when the nSTATUS is released high and your device is ready to begin configuration.



For more information about the POR delay, refer to the *Hot Socketing and Power-On Reset in Stratix V Devices* chapter.

Table 45 lists the fast and standard POR delay specification.

#### Table 45. Fast and Standard POR Delay Specification (1)

POR Delay	Minimum	Maximum
Fast	4 ms	12 ms
Standard	100 ms	300 ms

#### Note to Table 45:

(1) You can select the POR delay based on the MSEL settings as described in the MSEL Pin Settings section of the "Configuration, Design Security, and Remote System Upgrades in Stratix V Devices" chapter.

## **JTAG Configuration Specifications**

Table 46 lists the JTAG timing parameters and values for Stratix V devices.

Table 46. JTAG Timing Parameters and Values for Stratix V Devices

Symbol	Description	Min	Max	Unit
t <sub>JCP</sub>	TCK clock period <sup>(2)</sup>	30		ns
t <sub>JCP</sub>	TCK clock period <sup>(2)</sup>	167	—	ns
t <sub>JCH</sub>	TCK clock high time <sup>(2)</sup>	14	—	ns
t <sub>JCL</sub>	TCK clock low time <sup>(2)</sup>	14		ns
t <sub>JPSU (TDI)</sub>	TDI JTAG port setup time	2	—	ns
t <sub>JPSU (TMS)</sub>	TMS JTAG port setup time	3	_	ns

Symbol	Description	Min	Max	Unit
t <sub>JPH</sub>	JTAG port hold time	5	—	ns
t <sub>JPCO</sub>	JTAG port clock to output	—	11 <sup>(1)</sup>	ns
t <sub>JPZX</sub>	JTAG port high impedance to valid output	—	14 <sup>(1)</sup>	ns
t <sub>JPXZ</sub>	JTAG port valid output to high impedance	—	<b>14</b> <sup>(1)</sup>	ns

Table 46. JTAG Timing Parameters and Values for Stratix V Devices

Notes to Table 46:

(1) A 1 ns adder is required for each V<sub>CCI0</sub> voltage step down from 3.0 V. For example,  $t_{JPC0} = 12$  ns if V<sub>CCI0</sub> of the TDO I/O bank = 2.5 V, or 13 ns if it equals 1.8 V.

(2) The minimum TCK clock period is 167 ns if VCCBAT is within the range 1.2V-1.5V when you perform the volatile key programming.

## **Raw Binary File Size**

For the POR delay specification, refer to the "POR Delay Specification" section of the "Configuration, Design Security, and Remote System Upgrades in Stratix V Devices".

Table 47 lists the uncompressed raw binary file (.rbf) sizes for Stratix V devices.

Family	Device Package		Configuration .rbf Size (bits)	IOCSR .rbf Size (bits) <sup>(4), (5)</sup>		
	500742	H35, F40, F35 <sup>(2)</sup>	213,798,880	562,392		
	JOUNAS	H29, F35 <sup>(3)</sup>	137,598,880	564,504		
	5SGXA4	—	213,798,880	563,672		
Stratix V GX	5SGXA5	—	269,979,008	562,392		
	5SGXA7	—	269,979,008	562,392		
	5SGXA9	—	342,742,976	700,888		
	5SGXAB	—	342,742,976	700,888		
	5SGXB5	—	270,528,640	584,344		
	5SGXB6	—	270,528,640	584,344		
	5SGXB9	_	342,742,976	700,888		
	5SGXBB	—	342,742,976	700,888		
Stratix V CT	5SGTC5	—	269,979,008	562,392		
	5SGTC7	—	269,979,008	562,392		
	5SGSD3	—	137,598,880	564,504		
	590904	F1517	213,798,880	563,672		
Stratix V GS	J303D4	_	137,598,880	564,504		
	5SGSD5		213,798,880	563,672		
	5SGSD6		293,441,888	565,528		
	5SGSD8	—	293,441,888	565,528		

Table 47. Uncompressed .rbf Sizes for Stratix V Devices

Family	Device	Package	Configuration .rbf Size (bits)	IOCSR .rbf Size (bits) <sup>(4), (5)</sup>
Stratix V E <sup>(1)</sup>	5SEE9	—	342,742,976	700,888
	5SEEB	—	342,742,976	700,888

#### Table 47. Uncompressed .rbf Sizes for Stratix V Devices

#### Notes to Table 47:

(1) Stratix V E devices do not have PCI Express® (PCIe®) hard IP. Stratix V E devices do not support the CvP configuration scheme.

(2) 36-transceiver devices.

(3) 24-transceiver devices.

(4) File size for the periphery image.

(5) The IOCSR .rbf size is specifically for the CvP feature.

Use the data in Table 47 to estimate the file size before design compilation. Different configuration file formats, such as a hexadecimal (.hex) or tabular text file (.ttf) format, have different file sizes. For the different types of configuration file and file sizes, refer to the Quartus II software. However, for a specific version of the Quartus II software, any design targeted for the same device has the same uncompressed configuration file size. If you are using compression, the file size can vary after each compilation because the compression ratio depends on your design.

• For more information about setting device configuration options, refer to *Configuration, Design Security, and Remote System Upgrades in Stratix V Devices.* For creating configuration files, refer to the *Quartus II Help.* 

Table 48 lists the minimum configuration time estimates for Stratix V devices.

Table 48. Minimum Configuration Time Estimation for Stratix V Devi
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Variant	Member Code		Active Serial (1)	)	Fast Passive Parallel <sup>(2)</sup>			
		Width	DCLK (MHz)	Min Config Time (s)	Width	DCLK (MHz)	Min Config Time (s)	
	٨٥	4	100	0.534	32	100	0.067	
	AJ	4	100	0.344	32	100	0.043	
	A4	4	100	0.534	32	100	0.067	
	A5	4	100	0.675	32	100	0.084	
	A7	4	100	0.675	32	100	0.084	
GX	A9	4	100	0.857	32	100	0.107	
	AB	4	100	0.857	32	100	0.107	
	B5	4	100	0.676	32	100	0.085	
	B6	4	100	0.676	32	100	0.085	
	B9	4	100	0.857	32	100	0.107	
	BB	4	100	0.857	32	100	0.107	
ст	C5	4	100	0.675	32	100	0.084	
GI	C7	4	100	0.675	32	100	0.084	

### FPP Configuration Timing when DCLK-to-DATA [] = 1

Figure 12 shows the timing waveform for FPP configuration when using a MAX II or MAX V device as an external host. This waveform shows timing when the DCLK-to-DATA[] ratio is 1.





#### Notes to Figure 12:

- (1) Use this timing waveform when the DCLK-to-DATA [] ratio is 1.
- (2) The beginning of this waveform shows the device in user mode. In user mode, nCONFIG, nSTATUS, and CONF\_DONE are at logic-high levels. When nCONFIG is pulled low, a reconfiguration cycle begins.
- (3) After power-up, the Stratix V device holds nstatus low for the time of the POR delay.
- (4) After power-up, before and during configuration, CONF\_DONE is low.
- (5) Do not leave DCLK floating after configuration. DCLK is ignored after configuration is complete. It can toggle high or low if required.
- (6) For FPP ×16, use DATA [15..0]. For FPP ×8, use DATA [7..0]. DATA [31..0] are available as a user I/O pin after configuration. The state of this pin depends on the dual-purpose pin settings.
- (7) To ensure a successful configuration, send the entire configuration data to the Stratix V device. CONF\_DONE is released high when the Stratix V device receives all the configuration data successfully. After CONF\_DONE goes high, send two additional falling edges on DCLK to begin initialization and enter user mode.
- (8) After the option bit to enable the INIT\_DONE pin is configured into the device, the INIT DONE goes low.

Table 54 lists the PS configuration timing parameters for Stratix V devices.

Table 54. PS Timing Parameters for Stratix V Devices

Symbol	Parameter	Minimum	Maximum	Units
t <sub>CF2CD</sub>	nCONFIG low to CONF_DONE low	—	600	ns
t <sub>CF2ST0</sub>	nCONFIG low to nSTATUS low	—	600	ns
t <sub>CFG</sub>	nCONFIG low pulse width	2	—	μS
t <sub>status</sub>	nSTATUS low pulse width	268	1,506 <sup>(1)</sup>	μS
t <sub>CF2ST1</sub>	nCONFIG high to nSTATUS high	—	1,506 <sup>(2)</sup>	μS
t <sub>CF2CK</sub> (5)	nCONFIG high to first rising edge on DCLK	1,506	—	μS
t <sub>ST2CK</sub> (5)	nSTATUS high to first rising edge of DCLK 2		—	μS
t <sub>DSU</sub>	DATA[] setup time before rising edge on DCLK	5.5	—	ns
t <sub>DH</sub>	DATA [] hold time after rising edge on DCLK	0	—	ns
t <sub>CH</sub>	DCLK high time	$0.45\times 1/f_{MAX}$	—	S
t <sub>CL</sub>	DCLK low time	$0.45\times 1/f_{MAX}$	—	S
t <sub>CLK</sub>	DCLK period	1/f <sub>MAX</sub>	—	S
f <sub>MAX</sub>	DCLK frequency	—	125	MHz
t <sub>CD2UM</sub>	CONF_DONE high to user mode <sup>(3)</sup>	175	437	μS
t <sub>CD2CU</sub>	CONF_DONE high to CLKUSR enabled	4 × maximum DCLK period	_	_
t <sub>cd2UMC</sub>	CONF_DONE high to user mode with CLKUSR option on	$t_{CD2CU}$ + (8576 × CLKUSR period) <sup>(4)</sup>	_	_

#### Notes to Table 54:

(1) This value is applicable if you do not delay configuration by extending the nCONFIG or nSTATUS low pulse width.

(2) This value is applicable if you do not delay configuration by externally holding the nSTATUS low.

(3) The minimum and maximum numbers apply only if you choose the internal oscillator as the clock source for initializing the device.

(4) To enable the CLKUSR pin as the initialization clock source and to obtain the maximum frequency specification on these pins, refer to the "Initialization" section.

(5) If nSTATUS is monitored, follow the t<sub>ST2CK</sub> specification. If nSTATUS is not monitored, follow the t<sub>CF2CK</sub> specification.

## Initialization

Table 55 lists the initialization clock source option, the applicable configuration schemes, and the maximum frequency.

Table 55.	Initialization	<b>Clock Source</b>	e Option	and the	Maximum	Frequency

Initialization Clock Source	Configuration Schemes	Maximum Frequency	Minimum Number of Clock Cycles <sup>(1)</sup>
Internal Oscillator	AS, PS, FPP	12.5 MHz	
CLKUSR	AS, PS, FPP (2)	125 MHz	8576
DCLK	PS, FPP	125 MHz	

#### Notes to Table 55:

(1) The minimum number of clock cycles required for device initialization.

(2) To enable CLKUSR as the initialization clock source, turn on the Enable user-supplied start-up clock (CLKUSR) option in the Quartus II software from the General panel of the Device and Pin Options dialog box.

Poromotor Available		Min	Fast Model		Slow Model							
(1)	<sup>(1)</sup> Settings	0ffset (2)	Industrial	Commercial	C1	C2	C3	C4	12	13, 13YY	14	Unit
D3	8	0	1.587	1.699	2.793	2.793	2.992	3.192	2.811	3.047	3.257	ns
D4	64	0	0.464	0.492	0.838	0.838	0.924	1.011	0.843	0.920	1.006	ns
D5	64	0	0.464	0.493	0.838	0.838	0.924	1.011	0.844	0.921	1.006	ns
D6	32	0	0.229	0.244	0.415	0.415	0.458	0.503	0.418	0.456	0.499	ns

Table 58.	IOE Pro	grammable De	lay for	Stratix V	V Devices	(Part 2 of 2	)
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#### Notes to Table 58:

(1) You can set this value in the Quartus II software by selecting D1, D2, D3, D5, and D6 in the Assignment Name column of Assignment Editor.

(2) Minimum offset does not include the intrinsic delay.

## **Programmable Output Buffer Delay**

Table 59 lists the delay chain settings that control the rising and falling edge delays of the output buffer. The default delay is 0 ps.

Symbol	Parameter	Typical	Unit
	Rising and/or falling edge delay	0 (default)	ps
Dauman		25	ps
DOUTBUF		50	ps
		75	ps

Note to Table 59:

(1) You can set the programmable output buffer delay in the Quartus II software by setting the Output Buffer Delay Control assignment to either positive, negative, or both edges, with the specific values stated here (in ps) for the Output Buffer Delay assignment.

## Glossary

Table 60 lists the glossary for this chapter.

Table 60. Glossary (Part 1 of 4)

Letter	Subject	Definitions	
Α			
В	—	—	
С			
D	—	_	
E	—	_	
F	f <sub>HSCLK</sub>	Left and right PLL input clock frequency.	
	f <sub>HSDR</sub>	High-speed I/O block—Maximum and minimum <b>LVDS</b> data transfer rate (f <sub>HSDR</sub> = 1/TUI), non-DPA.	
	f <sub>hsdrdpa</sub>	High-speed I/O block—Maximum and minimum <b>LVDS</b> data transfer rate (f <sub>HSDRDPA</sub> = 1/TUI), DPA.	

Letter	Subject	Definitions	
	V <sub>CM(DC)</sub>	DC common mode input voltage.	
	V <sub>ICM</sub>	Input common mode voltage—The common mode of the differential signal at the receiver.	
	V <sub>ID</sub>	Input differential voltage swing—The difference in voltage between the positive and complementary conductors of a differential transmission at the receiver.	
	V <sub>DIF(AC)</sub>	AC differential input voltage—Minimum AC input differential voltage required for switching.	
	V <sub>DIF(DC)</sub>	DC differential input voltage— Minimum DC input differential voltage required for switching.	
	V <sub>IH</sub>	Voltage input high—The minimum positive voltage applied to the input which is accepted by the device as a logic high.	
	V <sub>IH(AC)</sub>	High-level AC input voltage	
	V <sub>IH(DC)</sub>	High-level DC input voltage	
V	V <sub>IL</sub>	Voltage input low—The maximum positive voltage applied to the input which is accepted by the device as a logic low.	
	V <sub>IL(AC)</sub>	Low-level AC input voltage	
	V <sub>IL(DC)</sub>	Low-level DC input voltage	
	V <sub>OCM</sub>	Output common mode voltage—The common mode of the differential signal at the transmitter.	
	V <sub>OD</sub>	Output differential voltage swing—The difference in voltage between the positive and complementary conductors of a differential transmission at the transmitter.	
	V <sub>SWING</sub>	Differential input voltage	
	V <sub>X</sub>	Input differential cross point voltage	
	V <sub>OX</sub>	Output differential cross point voltage	
W	W	High-speed I/O block—clock boost factor	
X			
Y	—	—	
Z			

#### Table 60. Glossary (Part 4 of 4)

## **Document Revision History**

Table 61 lists the revision history for this chapter.

 Table 61. Document Revision History (Part 1 of 3)

Date	Version	Changes	
June 2018	3.9	<ul> <li>Added the "Stratix V Device Overshoot Duration" figure.</li> </ul>	
April 2017	3.8	Added a footnote to the "High-Speed I/O Specifications for Stratix V Devices" table.	
		<ul> <li>Changed the minimum value for t<sub>CD2UMC</sub> in the "PS Timing Parameters for Stratix V Devices" table.</li> </ul>	
		<ul> <li>Changed the condition for 100-Ω R<sub>D</sub> in the "OCT Without Calibration Resistance Tolerance Specifications for Stratix V Devices" table.</li> </ul>	
		<ul> <li>Changed the minimum value for t<sub>CD2UMC</sub> in the "AS Timing Parameters for AS '1 and AS '4 Configurations in Stratix V Devices" table</li> </ul>	
		<ul> <li>Changed the minimum value for t<sub>CD2UMC</sub> in the "FPP Timing Parameters for Stratix V Devices When the DCLK-to-DATA[] Ratio is &gt;1" table.</li> </ul>	
		<ul> <li>Changed the minimum value for t<sub>CD2UMC</sub> in the "FPP Timing Parameters for Stratix V Devices When the DCLK-to-DATA[] Ratio is &gt;1" table.</li> </ul>	
		<ul> <li>Changed the minimum number of clock cycles value in the "Initialization Clock Source Option and the Maximum Frequency" table.</li> </ul>	
June 2016	3.7	<ul> <li>Added the V<sub>ID</sub> minimum specification for LVPECL in the "Differential I/O Standard Specifications for Stratix V Devices" table</li> </ul>	
		<ul> <li>Added the I<sub>OUT</sub> specification to the "Absolute Maximum Ratings for Stratix V Devices" table.</li> </ul>	
December 2015	3.6	Added a footnote to the "High-Speed I/O Specifications for Stratix V Devices" table.	
December 2015	3.5	<ul> <li>Changed the transmitter, receiver, and ATX PLL data rate specifications in the "Transceiver Specifications for Stratix V GX and GS Devices" table.</li> </ul>	
		<ul> <li>Changed the configuration .rbf sizes in the "Uncompressed .rbf Sizes for Stratix V Devices" table.</li> </ul>	
	3.4	• Changed the data rate specification for transceiver speed grade 3 in the following tables:	
		<ul> <li>"Transceiver Specifications for Stratix V GX and GS Devices"</li> </ul>	
		<ul> <li>"Stratix V Standard PCS Approximate Maximum Date Rate"</li> </ul>	
		<ul> <li>"Stratix V 10G PCS Approximate Maximum Data Rate"</li> </ul>	
July 2015		<ul> <li>Changed the conditions for reference clock rise and fall time, and added a note to the "Transceiver Specifications for Stratix V GX and GS Devices" table.</li> </ul>	
		<ul> <li>Added a note to the "Minimum differential eye opening at receiver serial input pins" specification in the "Transceiver Specifications for Stratix V GX and GS Devices" table.</li> </ul>	
		<ul> <li>Changed the t<sub>c0</sub> maximum value in the "AS Timing Parameters for AS '1 and AS '4 Configurations in Stratix V Devices" table.</li> </ul>	
		<ul> <li>Removed the CDR ppm tolerance specification from the "Transceiver Specifications for Stratix V GX and GS Devices" table.</li> </ul>	

### Table 61. Document Revision History (Part 2 of 3)

Date	Version	Changes	
		<ul> <li>Added the I3YY speed grade and changed the data rates for the GX channel in Table 1.</li> </ul>	
		<ul> <li>Added the I3YY speed grade to the V<sub>CC</sub> description in Table 6.</li> </ul>	
	3.3	<ul> <li>Added the I3YY speed grade to V<sub>CCHIP_L</sub>, V<sub>CCHIP_R</sub>, V<sub>CCHSSI_L</sub>, and V<sub>CCHSSI_R</sub> descriptions in Table 7.</li> </ul>	
		■ Added 240-Ω to Table 11.	
		Changed CDR PPM tolerance in Table 23.	
		<ul> <li>Added additional max data rate for fPLL in Table 23.</li> </ul>	
		<ul> <li>Added the I3YY speed grade and changed the data rates for transceiver speed grade 3 in Table 25.</li> </ul>	
		<ul> <li>Added the I3YY speed grade and changed the data rates for transceiver speed grade 3 in Table 26.</li> </ul>	
		<ul> <li>Changed CDR PPM tolerance in Table 28.</li> </ul>	
November 2014		<ul> <li>Added additional max data rate for fPLL in Table 28.</li> </ul>	
		<ul> <li>Changed the mode descriptions for MLAB and M20K in Table 33.</li> </ul>	
		<ul> <li>Changed the Max value of f<sub>HSCLK_OUT</sub> for the C2, C2L, I2, I2L speed grades in Table 36.</li> </ul>	
		<ul> <li>Changed the frequency ranges for C1 and C2 in Table 39.</li> </ul>	
		<ul> <li>Changed the .rbf file sizes for 5SGSD6 and 5SGSD8 in Table 47.</li> </ul>	
		<ul> <li>Added note about nSTATUS to Table 50, Table 51, Table 54.</li> </ul>	
		<ul> <li>Changed the available settings in Table 58.</li> </ul>	
		<ul> <li>Changed the note in "Periphery Performance".</li> </ul>	
		<ul> <li>Updated the "I/O Standard Specifications" section.</li> </ul>	
		<ul> <li>Updated the "Raw Binary File Size" section.</li> </ul>	
		<ul> <li>Updated the receiver voltage input range in Table 22.</li> </ul>	
		<ul> <li>Updated the max frequency for the LVDS clock network in Table 36.</li> </ul>	
		■ Updated the DCLK note to Figure 11.	
		<ul> <li>Updated Table 23 VO<sub>CM</sub> (DC Coupled) condition.</li> </ul>	
		Updated Table 6 and Table 7.	
		<ul> <li>Added the DCLK specification to Table 55.</li> </ul>	
		Updated the notes for Table 47.	
		<ul> <li>Updated the list of parameters for Table 56.</li> </ul>	
November 2013	3.2	Updated Table 28	
November 2013	3.1	Updated Table 33	
November 2013	3.0	Updated Table 23 and Table 28	
October 2013	2.9	<ul> <li>Updated the "Transceiver Characterization" section</li> </ul>	
	2.8	<ul> <li>Updated Table 3, Table 12, Table 14, Table 19, Table 20, Table 23, Table 24, Table 28, Table 30, Table 31, Table 32, Table 33, Table 36, Table 39, Table 40, Table 41, Table 42, Table 47, Table 53, Table 58, and Table 59</li> </ul>	
Uctober 2013		<ul> <li>Added Figure 1 and Figure 3</li> </ul>	
		<ul> <li>Added the "Transceiver Characterization" section</li> </ul>	
		<ul> <li>Removed all "Preliminary" designations.</li> </ul>	