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Intel - 5SGXEA7K1F40C1N Datasheet



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Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Obsolete
Number of LABs/CLBs	234720
Number of Logic Elements/Cells	622000
Total RAM Bits	51200000
Number of I/O	696
Number of Gates	-
Voltage - Supply	0.87V ~ 0.93V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	1517-BBGA, FCBGA
Supplier Device Package	1517-FBGA (40x40)
Purchase URL	https://www.e-xfl.com/product-detail/intel/5sgxea7k1f40c1n

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This section lists the functional operating limits for the AC and DC parameters for Stratix V devices. Table 6 lists the steady-state voltage and current values expected from Stratix V devices. Power supply ramps must all be strictly monotonic, without plateaus.

Table 6. Recommended Operating Conditions for Stratix V Devices (Part 1 of 2)

Symbol	Description	Condition	Min ⁽⁴⁾	Тур	Max ⁽⁴⁾	Unit
	Core voltage and periphery circuitry power supply (C1, C2, I2, and I3YY speed grades)	_	0.87	0.9	0.93	V
V _{CC}	Core voltage and periphery circuitry power supply (C2L, C3, C4, I2L, I3, I3L, and I4 speed grades) ⁽³⁾		0.82	0.85	0.88	V
V _{CCPT}	Power supply for programmable power technology	_	1.45	1.50	1.55	V
V _{CC_AUX}	Auxiliary supply for the programmable power technology		2.375	2.5	2.625	V
VI (1)	I/O pre-driver (3.0 V) power supply	_	2.85	3.0	3.15	V
VCCPD	I/O pre-driver (2.5 V) power supply		2.375	2.5	2.625	V
	I/O buffers (3.0 V) power supply	_	2.85	3.0	3.15	V
	I/O buffers (2.5 V) power supply		2.375	2.5	2.625	V
	I/O buffers (1.8 V) power supply	_	1.71	1.8	1.89	V
V _{CCIO}	I/O buffers (1.5 V) power supply	_	1.425	1.5	1.575	V
	I/O buffers (1.35 V) power supply		1.283	1.35	1.45	V
	I/O buffers (1.25 V) power supply	_	1.19	1.25	1.31	V
	I/O buffers (1.2 V) power supply	_	1.14	1.2	1.26	V
	Configuration pins (3.0 V) power supply		2.85	3.0	3.15	V
V _{CCPGM}	Configuration pins (2.5 V) power supply	_	2.375	2.5	2.625	V
	Configuration pins (1.8 V) power supply	-	1.71	1.8	1.89	V
V _{CCA_FPLL}	PLL analog voltage regulator power supply		2.375	2.5	2.625	V
V _{CCD_FPLL}	PLL digital voltage regulator power supply	-	1.45	1.5	1.55	V
V _{CCBAT} (2)	Battery back-up power supply (For design security volatile key register)	_	1.2	_	3.0	V
VI	DC input voltage	_	-0.5	—	3.6	V
V ₀	Output voltage		0	_	V _{CCIO}	V
т	Operating junction temperature	Commercial	0	—	85	°C
IJ		Industrial	-40	_	100	°C

I/O Pin Leakage Current

Table 9 lists the Stratix V I/O pin leakage current specifications.

Table 9.	I/O Pin	Leakage	Current for	Stratix V	Devices (1)
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Symbol	Description	Conditions	Min	Тур	Max	Unit
I _I	Input pin	$V_I = 0 V \text{ to } V_{CCIOMAX}$	-30	_	30	μA
I _{OZ}	Tri-stated I/O pin	$V_0 = 0 V \text{ to } V_{\text{CCIOMAX}}$	-30		30	μA

Note to Table 9:

(1) If $V_0 = V_{CCI0}$ to $V_{CCI0Max}$, 100 μ A of leakage current per I/O is expected.

Bus Hold Specifications

Table 10 lists the Stratix V device family bus hold specifications.

Table 10. Bus Hold Parameters for Stratix V Devices

							Va	CI0					
Parameter	Symbol	Conditions	1.2	2 V	1.	5 V	1.8	B V	2.5	5 V	3.0	V	Unit
			Min	Max									
Low sustaining current	I _{SUSL}	V _{IN} > V _{IL} (maximum)	22.5	_	25.0	_	30.0	_	50.0	_	70.0	_	μA
High sustaining current	I _{SUSH}	V _{IN} < V _{IH} (minimum)	-22.5		-25.0	_	-30.0	_	-50.0	_	-70.0		μA
Low overdrive current	I _{odl}	$0V < V_{IN} < V_{CCIO}$		120		160		200	_	300		500	μA
High overdrive current	I _{odh}	$0V < V_{IN} < V_{CCIO}$		-120		-160		-200		-300		-500	μΑ
Bus-hold trip point	V _{TRIP}	_	0.45	0.95	0.50	1.00	0.68	1.07	0.70	1.70	0.80	2.00	۷

On-Chip Termination (OCT) Specifications

If you enable OCT calibration, calibration is automatically performed at power-up for I/Os connected to the calibration block. Table 11 lists the Stratix V OCT termination calibration accuracy specifications.

Table 11. OCT Calibration Accuracy Specifications for Stratix V Devices ⁽¹⁾ (Part 1 of 2)

				Calibratio	n Accuracy		
Symbol	Description	Conditions	C1	C2,12	C3,I3, I3YY	C4,14	Unit
25- $Ω$ R _S	Internal series termination with calibration (25- Ω setting)	V _{CCI0} = 3.0, 2.5, 1.8, 1.5, 1.2 V	±15	±15	±15	±15	%

				Calibratio	n Accuracy		
Symbol	Description	Conditions	C1	C2,I2	C3,I3, I3YY	C4,14	Unit
50-Ω R _S	Internal series termination with calibration (50- Ω setting)	V _{CCI0} = 3.0, 2.5, 1.8, 1.5, 1.2 V	±15	±15	±15	±15	%
34- Ω and 40- Ω R _S	Internal series termination with calibration (34- Ω and 40- Ω setting)	V _{CCI0} = 1.5, 1.35, 1.25, 1.2 V	±15	±15	±15	±15	%
48-Ω, 60-Ω, 80-Ω, and 240-Ω R _S	Internal series termination with calibration (48- Ω , 60- Ω , 80- Ω , and 240- Ω setting)	V _{CCI0} = 1.2 V	±15	±15	±15	±15	%
50-Ω R _T	Internal parallel termination with calibration (50-Ω setting)	V _{CCI0} = 2.5, 1.8, 1.5, 1.2 V	-10 to +40	-10 to +40	-10 to +40	-10 to +40	%
20-Ω, 30-Ω, 40-Ω,60-Ω, and 120-Ω R _T	Internal parallel termination with calibration ($20 - \Omega$, $30 - \Omega$, $40 - \Omega$, $60 - \Omega$, and $120 - \Omega$ setting)	V _{CCI0} = 1.5, 1.35, 1.25 V	-10 to +40	-10 to +40	-10 to +40	-10 to +40	%
60- $Ω$ and 120- $Ω$ R _T	Internal parallel termination with calibration (60-Ω and 120-Ω setting)	V _{CCI0} = 1.2	-10 to +40	-10 to +40	-10 to +40	-10 to +40	%
$25-\Omega \\ R_{S_left_shift}$	Internal left shift series termination with calibration ($25-\Omega$ R _{S_left_shift} setting)	V _{CCI0} = 3.0, 2.5, 1.8, 1.5, 1.2 V	±15	±15	±15	±15	%

Table II. OUI Valiblation Accuracy specifications for Stratix V Devices' / (Latt 2 OF	Table 11.	OCT Calibration A	ccuracy Specificati	ons for Stratix V D	Devices ⁽¹⁾ (Part 2 of
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Note to Table 11:

(1) OCT calibration accuracy is valid at the time of calibration only.

Table 12 lists the Stratix V OCT without calibration resistance to PVT changes.

Table 12.	OCT Without Calibration	Resistance 1	Tolerance	Specifications	for Stratix	V Devices	(Part 1	of 2)
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			Resistance Tolerance				
Symbol	Description	Conditions	C1	C2,I2	C3, I3, I3YY	C4, I4	Unit
25-Ω R, 50-Ω R _S	Internal series termination without calibration (25-Ω setting)	$V_{CCIO} = 3.0$ and 2.5 V	±30	±30	±40	±40	%
25-Ω R _S	Internal series termination without calibration (25-Ω setting)	V _{CCI0} = 1.8 and 1.5 V	±30	±30	±40	±40	%
25-Ω R _S	Internal series termination without calibration (25-Ω setting)	V _{CCI0} = 1.2 V	±35	±35	±50	±50	%

Symbol	Description	V _{CCIO} (V)	Typical	Unit
dR/dT		3.0	0.189	
	OCT variation with temperature without recalibration	2.5	0.208	
		1.8	0.266	%/°C
		1.5	0.273	
		1.2	0.317	

Table 13. OCT Variation after Power-Up Calibration for Stratix V Devices (Part 2 of 2)⁽¹⁾

Note to Table 13:

(1) Valid for a V_{CCIO} range of $\pm 5\%$ and a temperature range of 0° to 85°C.

Pin Capacitance

Table 14 lists the Stratix V device family pin capacitance.

Table 14. Pin Capacitance for Stratix V Devices

Symbol	Description	Value	Unit
CIOTB	Input capacitance on the top and bottom I/O pins	6	pF
C _{IOLR}	Input capacitance on the left and right I/O pins	6	рF
C _{OUTFB}	Input capacitance on dual-purpose clock output and feedback pins	6	pF

Hot Socketing

Table 15 lists the hot socketing specifications for Stratix V devices.

Symbol	Description	Maximum
I _{IOPIN (DC)}	DC current per I/O pin	300 μA
I _{IOPIN (AC)}	AC current per I/O pin	8 mA ⁽¹⁾
IXCVR-TX (DC)	DC current per transceiver transmitter pin	100 mA
IXCVR-RX (DC)	DC current per transceiver receiver pin	50 mA

Note to Table 15:

(1) The I/O ramp rate is 10 ns or more. For ramp rates faster than 10 ns, $|I_{10PIN}| = C dv/dt$, in which C is the I/O pin capacitance and dv/dt is the slew rate.

I/O Standard	ndard V _{IL(DC)} (V) Min Max		V _{IH(D}	_{C)} (V)	V _{IL(AC)} (V)	V _{IH(AC)} (V)	V _{ol} (V)	V _{oh} (V)	I (mA)	l _{oh}
i/U Stanuaru			Min Max		Max Min		Max	Min	1 ₀₁ (11174)	(mA)
HSTL-18 Class I	—	V _{REF} – 0.1	V _{REF} + 0.1	_	$V_{REF} - 0.2$	V _{REF} + 0.2	0.4	V _{CCI0} – 0.4	8	-8
HSTL-18 Class II	_	V _{REF} – 0.1	V _{REF} + 0.1	_	V _{REF} - 0.2	V _{REF} + 0.2	0.4	V _{CCI0} – 0.4	16	-16
HSTL-15 Class I	_	V _{REF} – 0.1	V _{REF} + 0.1	_	V _{REF} - 0.2	V _{REF} + 0.2	0.4	V _{CCI0} – 0.4	8	-8
HSTL-15 Class II	_	V _{REF} – 0.1	V _{REF} + 0.1	_	V _{REF} - 0.2	V _{REF} + 0.2	0.4	V _{CCI0} – 0.4	16	-16
HSTL-12 Class I	-0.15	V _{REF} - 0.08	V _{REF} + 0.08	V _{CCIO} + 0.15	V _{REF} – 0.15	V _{REF} + 0.15	0.25* V _{CCI0}	0.75* V _{CCI0}	8	-8
HSTL-12 Class II	-0.15	V _{REF} - 0.08	V _{REF} + 0.08	V _{CCIO} + 0.15	V _{REF} – 0.15	V _{REF} + 0.15	0.25* V _{CCI0}	0.75* V _{CCI0}	16	-16
HSUL-12	—	V _{REF} – 0.13	V _{REF} + 0.13	_	V _{REF} – 0.22	V _{REF} + 0.22	0.1* V _{CCIO}	0.9* V _{CCI0}	_	

Table 19. Single-Ended SSTL, HSTL, and HSUL I/O Standards Signal Specifications for Stratix V Devices (Part 2 of 2)

Table 20. Differential SSTL I/O Standards for Stratix V Devices

1/0 Standard	V _{CCIO} (V)			V _{SWING(DC)} (V)			V _{X(AC)} (V)	V _{SWING(AC)} (V)		
ijo Stanuaru	Min	Тур	Max	Min	Max	Min	Тур	Max	Min	Max
SSTL-2 Class I, II	2.375	2.5	2.625	0.3	V _{CCI0} + 0.6	V _{CCI0} /2- 0.2	_	V _{CCI0} /2 + 0.2	0.62	V _{CCI0} + 0.6
SSTL-18 Class I, II	1.71	1.8	1.89	0.25	V _{CCIO} + 0.6	V _{CCI0} /2- 0.175	_	V _{CCI0} /2 + 0.175	0.5	V _{CCI0} + 0.6
SSTL-15 Class I, II	1.425	1.5	1.575	0.2	(1)	V _{CCI0} /2- 0.15	_	V _{CCI0} /2 + 0.15	0.35	_
SSTL-135 Class I, II	1.283	1.35	1.45	0.2	(1)	V _{CCI0} /2- 0.15	V _{CCI0} /2	V _{CCI0} /2 + 0.15	2(V _{IH(AC)} - V _{REF})	2(V _{IL(AC)} - V _{REF})
SSTL-125 Class I, II	1.19	1.25	1.31	0.18	(1)	V _{CCI0} /2- 0.15	V _{CCI0} /2	V _{CCI0} /2 + 0.15	2(V _{IH(AC)} - V _{REF})	_
SSTL-12 Class I, II	1.14	1.2	1.26	0.18	_	V _{REF} 0.15	V _{CCI0} /2	V _{REF} + 0.15	-0.30	0.30

Note to Table 20:

(1) The maximum value for $V_{SWING(DC)}$ is not defined. However, each single-ended signal needs to be within the respective single-ended limits $(V_{IH(DC)} \text{ and } V_{IL(DC)})$.

I/O	V _{CCIO} (V)			V _{DIF(DC)} (V)			V _{X(AC)} (V)			V _{CM(DC)} (V)			V _{DIF(AC)} (V)	
Standard	Min	Тур	Max	Min	Max	Min	Тур	Max	Min	Тур	Max	Min	Max	
HSTL-18 Class I, II	1.71	1.8	1.89	0.2	_	0.78	_	1.12	0.78	_	1.12	0.4	_	
HSTL-15 Class I, II	1.425	1.5	1.575	0.2	_	0.68	_	0.9	0.68		0.9	0.4	_	

Table 24 shows the maximum transmitter data rate for the clock network.

Table 24. Clock Network Maximum Data Rate Transmitter Specifications (1)

		ATX PLL			CMU PLL ⁽²⁾)	fPLL			
Clock Network	Non- bonded Mode (Gbps)	Bonded Mode (Gbps)	Channel Span	Non- bonded Mode (Gbps)	Bonded Mode (Gbps)	Channel Span	Non- bonded Mode (Gbps)	Bonded Mode (Gbps)	Channel Span	
x1 ⁽³⁾	14.1	_	6	12.5	_	6	3.125	—	3	
x6 ⁽³⁾	_	14.1	6	—	12.5	6	—	3.125	6	
x6 PLL Feedback ⁽⁴⁾	_	14.1	Side- wide	_	12.5	Side- wide	_	_	_	
xN (PCIe)	_	8.0	8	—	5.0	8	—	—	—	
xN (Native PHY IP)	8.0	8.0	Up to 13 channels above and below PLL	7 00	7 00	Up to 13 channels above	3 125	3 125	Up to 13 channels above	
	_	8.01 to 9.8304	Up to 7 channels above and below PLL	7.99	7.99	and below PLL	J. 120	3.125	and below PLL	

Notes to Table 24:

(1) Valid data rates below the maximum specified in this table depend on the reference clock frequency and the PLL counter settings. Check the MegaWizard message during the PHY IP instantiation.

(2) ATX PLL is recommended at 8 Gbps and above data rates for improved jitter performance.

(3) Channel span is within a transceiver bank.

(4) Side-wide channel bonding is allowed up to the maximum supported by the PHY IP.

Mode ⁽²⁾	Transceiver	PMA Width	20	20	16	16	10	10	8	8
	Speed Grade	PCS/Core Width	40	20	32	16	20	10	16	8
FIFO	1	C1, C2, C2L, I2, I2L core speed grade	12.2	11.4	9.76	9.12	6.5	5.8	5.2	4.72
	ŋ	C1, C2, C2L, I2, I2L core speed grade	12.2	11.4	9.76	9.12	6.5	5.8	5.2	4.72
	2	C3, I3, I3L core speed grade	9.8	9.0	7.84	7.2	5.3	4.7	4.24	3.76
		C1, C2, C2L, I2, I2L core speed grade	8.5	8.5	8.5	8.5	6.5	5.8	5.2	4.72
	3	I3YY core speed grade	10.3125	10.3125	7.84	7.2	5.3	4.7	4.24	3.76
		C3, I3, I3L core speed grade	8.5	8.5	7.84	7.2	5.3	4.7	4.24	3.76
		C4, I4 core speed grade	8.5	8.2	7.04	6.56	4.8	4.2	3.84	3.44
	1	C1, C2, C2L, I2, I2L core speed grade	12.2	11.4	9.76	9.12	6.1	5.7	4.88	4.56
	ŋ	C1, C2, C2L, I2, I2L core speed grade	12.2	11.4	9.76	9.12	6.1	5.7	4.88	4.56
	۷	C3, I3, I3L core speed grade	9.8	9.0	7.92	7.2	4.9	4.5	3.96	3.6
Register		C1, C2, C2L, I2, I2L core speed grade	10.3125	10.3125	10.3125	10.3125	6.1	5.7	4.88	4.56
	3	I3YY core speed grade	10.3125	10.3125	7.92	7.2	4.9	4.5	3.96	3.6
	J	C3, I3, I3L core speed grade	8.5	8.5	7.92	7.2	4.9	4.5	3.96	3.6
		C4, I4 core speed grade	8.5	8.2	7.04	6.56	4.4	4.1	3.52	3.28

Table 25 shows the approximate maximum data rate using the standard PCS.

Table 25. Stratix V Standard PCS Approximate Maximum Date Rate (1), (3)

Notes to Table 25:

(1) The maximum data rate is in Gbps.

(2) The Phase Compensation FIFO can be configured in FIFO mode or register mode. In the FIFO mode, the pointers are not fixed, and the latency can vary. In the register mode the pointers are fixed for low latency.

(3) The maximum data rate is also constrained by the transceiver speed grade. Refer to Table 1 for the transceiver speed grade.

Table 26 shows the approximate maximum data rate using the 10G PCS.

Mada (2)	Transceiver	PMA Width	64	40	40	40	32	32		
mode ""	Speed Grade	PCS Width	64	66/67	50	40	64/66/67	32		
	1	C1, C2, C2L, I2, I2L core speed grade	14.1	14.1	10.69	14.1	13.6	13.6		
	2	C1, C2, C2L, I2, I2L core speed grade	12.5	12.5	10.69	12.5	12.5	12.5		
	2	C3, I3, I3L core speed grade	12.5	12.5	10.69	12.5	10.88	10.88		
FIFO or Register		C1, C2, C2L, I2, I2L core speed grade	8.5 Gbps							
	0	C3, I3, I3L core speed grade								
	5	C4, I4 core speed grade								
		I3YY core speed grade	10.3125 Gbps							

Notes to Table 26:

(1) The maximum data rate is in Gbps.

(2) The Phase Compensation FIFO can be configured in FIFO mode or register mode. In the FIFO mode, the pointers are not fixed, and the latency can vary. In the register mode the pointers are fixed for low latency.





Figure 3 shows the Stratix V AC gain curves for GX channels.

Figure 3. AC Gain Curves for GX Channels (full bandwidth)

Stratix V GT devices contain both GX and GT channels. All transceiver specifications for the GX channels not listed in Table 28 are the same as those listed in Table 23.

Table 28 lists the Stratix V GT transceiver specifications.

Symbol/ Description	Conditions	s	Transceive peed Grade	r 2	S	r 3	Unit			
Description		Min	Тур	Max	Min	Тур	Max			
Reference Clock								1		
Supported I/O Standards	Dedicated reference clock pin	1.2-V PCN	IL, 1.4-V PC	ML, 1.5-V P(CML, 2.5-V I and HCSL	PCML, Diffe	rential LVPE	ECL, LVDS,		
otanuarus	RX reference clock pin		1.4-V PCML, 1.5-V PCML, 2.5-V PCML, LVPECL, and LVDS							
Input Reference Clock Frequency (CMU PLL) ⁽⁶⁾	_	40	_	710	40	_	710	MHz		
Input Reference Clock Frequency (ATX PLL) ⁽⁶⁾	_	100	_	710	100	_	710	MHz		
Rise time	20% to 80%	_		400	_	_	400			
Fall time	80% to 20%			400	—	_	400	ps		
Duty cycle	—	45	_	55	45	_	55	%		
Spread-spectrum modulating clock frequency	PCI Express (PCIe)	30	_	33	30	_	33	kHz		
Spread-spectrum downspread	PCle	_	0 to -0.5	_	_	0 to -0.5	_	%		
On-chip termination resistors ⁽¹⁹⁾	_	_	100	_	_	100	_	Ω		
Absolute V _{MAX} ⁽³⁾	Dedicated reference clock pin	_	_	1.6	_	_	1.6	V		
	RX reference clock pin	_	_	1.2	_	_	1.2			
Absolute V _{MIN}	—	-0.4		—	-0.4	—		V		
Peak-to-peak differential input voltage	_	200	_	1600	200	_	1600	mV		
V _{ICM} (AC coupled)	Dedicated reference clock pin		1050/1000 ^{(,}	2)	1	1050/1000 ⁽²⁾				
	RX reference clock pin	1	.0/0.9/0.85 (22)	1.	1.0/0.9/0.85 (22)				
V _{ICM} (DC coupled)	HCSL I/O standard for PCIe reference clock	250	_	550	250		550	mV		

Table 28. Transceiver Specifications for Stratix V GT Devices (Part 1 of 5)⁽¹⁾

Table 29 shows the V_{OD} settings for the GT channel.

Symbol	V _{OD} Setting	V _{od} Value (mV)
	0	0
	1	200
V., differential neak to neak typical (1)	2	400
The fine contrar hear to hear the field to	3	600
	4	800
	5	1000

Note:

(1) Refer to Figure 4.

Figure 4 shows the differential transmitter output waveform.





Figure 5 shows the Stratix V AC gain curves for GT channels.

Figure 5. AC Gain Curves for GT Channels

Figure 7 shows the dynamic phase alignment (DPA) lock time specifications with the DPA PLL calibration option enabled.

Figure 7. DPA Lock Time Specification with DPA PLL Calibration Enabled

rx_reset			
rx_dpa_locked			<u> </u>
			-

Table 37 lists the DPA lock time specifications for Stratix V devices.

Table 37. DPA Lock Time Specifications for Stratix V GX Devices Only (1), (2), (3)

Standard	Training Pattern	Number of Data Transitions in One Repetition of the Training Pattern	Number of Repetitions per 256 Data Transitions ⁽⁴⁾	Maximum
SPI-4	00000000001111111111	2	128	640 data transitions
Parallel Rapid I/O	00001111	2	128	640 data transitions
	10010000	4	64	640 data transitions
Miscellaneous	10101010	8	32	640 data transitions
Wiscenareous	01010101	8	32	640 data transitions

Notes to Table 37:

(1) The DPA lock time is for one channel.

(2) One data transition is defined as a 0-to-1 or 1-to-0 transition.

(3) The DPA lock time stated in this table applies to both commercial and industrial grade.

(4) This is the number of repetitions for the stated training pattern to achieve the 256 data transitions.

Figure 8 shows the **LVDS** soft-clock data recovery (CDR)/DPA sinusoidal jitter tolerance specification for a data rate \geq 1.25 Gbps. Table 38 lists the **LVDS** soft-CDR/DPA sinusoidal jitter tolerance specification for a data rate \geq 1.25 Gbps.





Jitter Free	quency (Hz)	Sinusoidal Jitter (UI)
F1	10,000	25.000
F2	17,565	25.000
F3	1,493,000	0.350
F4	50,000,000	0.350

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Figure 9 shows the **LVDS** soft-CDR/DPA sinusoidal jitter tolerance specification for a data rate < 1.25 Gbps.





DLL Range, DQS Logic Block, and Memory Output Clock Jitter Specifications

Table 39 lists the DLL range specification for Stratix V devices. The DLL is always in 8-tap mode in Stratix V devices.

Table 39. DLL Range Specifications for Stratix V Devices (1)

C1	C2, C2L, I2, I2L	C3, I3, I3L, I3YY	C4,I4	Unit
300-933	300-933	300-890	300-890	MHz

Note to Table 39:

(1) Stratix V devices support memory interface frequencies lower than 300 MHz, although the reference clock that feeds the DLL must be at least 300 MHz. To support interfaces below 300 MHz, multiply the reference clock feeding the DLL to ensure the frequency is within the supported range of the DLL.

Table 40 lists the DQS phase offset delay per stage for Stratix V devices.

Table 40. DQS Phase Offset Delay Per Setting for Stratix V Devices ^{(1), (2)} (Part 1 of 2)

Speed Grade	Min	Max	Unit
C1	8	14	ps
C2, C2L, I2, I2L	8	14	ps
C3,I3, I3L, I3YY	8	15	ps

Clock	Parameter	Symbol	C	1	C2, C2L	, 12, 12L	C3, I3 I3	8, 13L , YY	C4	,14	Unit
NELWUIK		-	Min	Max	Min	Max	Min	Max	Min	Max	
	Clock period jitter	$t_{JIT(per)}$	-25	25	-25	25	-30	30	-35	35	ps
PHY Clock	Cycle-to-cycle period jitter	$t_{\rm JIT(cc)}$	-50	50	-50	50	-60	60	-70	70	ps
	Duty cycle jitter	$t_{JIT(duty)}$	-37.5	37.5	-37.5	37.5	-45	45	-56	56	ps

Table 42. Memory Output Clock Jitter Specification for Stratix V Devices (1), (Part 2 of 2) (2), (3)

Notes to Table 42:

(1) The clock jitter specification applies to the memory output clock pins generated using differential signal-splitter and DDIO circuits clocked by a PLL output routed on a PHY, regional, or global clock network as specified. Altera recommends using PHY clock networks whenever possible.

(2) The clock jitter specification applies to the memory output clock pins clocked by an integer PLL.

(3) The memory output clock jitter is applicable when an input jitter of 30 ps peak-to-peak is applied with bit error rate (BER) -12, equivalent to 14 sigma.

OCT Calibration Block Specifications

Table 43 lists the OCT calibration block specifications for Stratix V devices.

Table 43. OCT Calibration Block Specifications for Stratix V Devices

Symbol	Description	Min	Тур	Max	Unit
OCTUSRCLK	Clock required by the OCT calibration blocks	—	_	20	MHz
T _{OCTCAL}	Number of OCTUSRCLK clock cycles required for OCT $\rm R_S/R_T$ calibration		1000	_	Cycles
T _{OCTSHIFT}	Number of OCTUSRCLK clock cycles required for the OCT code to shift out	_	32	_	Cycles
T _{RS_RT}	Time required between the dyn_term_ctrl and oe signal transitions in a bidirectional I/O buffer to dynamically switch between OCT R_S and R_T (Figure 10)		2.5		ns

Figure 10 shows the timing diagram for the oe and dyn_term_ctrl signals.

Figure 10. Timing Diagram for oe and dyn_term_ctrl Signals



Symbol	Description	Min	Max	Unit
t _{JPH}	JTAG port hold time	5	—	ns
t _{JPCO}	JTAG port clock to output	—	11 ⁽¹⁾	ns
t _{JPZX}	JTAG port high impedance to valid output	—	14 ⁽¹⁾	ns
t _{JPXZ}	JTAG port valid output to high impedance	—	14 ⁽¹⁾	ns

Table 46. JTAG Timing Parameters and Values for Stratix V Devices

Notes to Table 46:

(1) A 1 ns adder is required for each V_{CCI0} voltage step down from 3.0 V. For example, $t_{JPC0} = 12$ ns if V_{CCI0} of the TDO I/O bank = 2.5 V, or 13 ns if it equals 1.8 V.

(2) The minimum TCK clock period is 167 ns if VCCBAT is within the range 1.2V-1.5V when you perform the volatile key programming.

Raw Binary File Size

For the POR delay specification, refer to the "POR Delay Specification" section of the "Configuration, Design Security, and Remote System Upgrades in Stratix V Devices".

Table 47 lists the uncompressed raw binary file (.rbf) sizes for Stratix V devices.

Family	Device	Package	Configuration .rbf Size (bits)	IOCSR .rbf Size (bits) ^{(4), (5)}
	500742	H35, F40, F35 ⁽²⁾	213,798,880	562,392
	JOUNAS	H29, F35 ⁽³⁾	137,598,880	564,504
	5SGXA4	—	213,798,880	563,672
	5SGXA5	—	269,979,008	562,392
	5SGXA7	—	269,979,008	562,392
Stratix V GX	5SGXA9	—	342,742,976	700,888
	5SGXAB	—	342,742,976	700,888
	5SGXB5	—	270,528,640	584,344
	5SGXB6	—	270,528,640	584,344
	5SGXB9	_	342,742,976	700,888
	5SGXBB	—	342,742,976	700,888
Stratix V CT	5SGTC5	—	269,979,008	562,392
	5SGTC7	_	269,979,008	562,392
	5SGSD3	—	137,598,880	564,504
	590904	F1517	213,798,880	563,672
Stratix V GS	J303D4		137,598,880	564,504
	5SGSD5		213,798,880	563,672
	5SGSD6		293,441,888	565,528
	5SGSD8	—	293,441,888	565,528

Table 47. Uncompressed .rbf Sizes for Stratix V Devices

FPP Configuration Timing when DCLK-to-DATA [] = 1

Figure 12 shows the timing waveform for FPP configuration when using a MAX II or MAX V device as an external host. This waveform shows timing when the DCLK-to-DATA[] ratio is 1.





Notes to Figure 12:

- (1) Use this timing waveform when the DCLK-to-DATA [] ratio is 1.
- (2) The beginning of this waveform shows the device in user mode. In user mode, nCONFIG, nSTATUS, and CONF_DONE are at logic-high levels. When nCONFIG is pulled low, a reconfiguration cycle begins.
- (3) After power-up, the Stratix V device holds nstatus low for the time of the POR delay.
- (4) After power-up, before and during configuration, CONF_DONE is low.
- (5) Do not leave DCLK floating after configuration. DCLK is ignored after configuration is complete. It can toggle high or low if required.
- (6) For FPP ×16, use DATA [15..0]. For FPP ×8, use DATA [7..0]. DATA [31..0] are available as a user I/O pin after configuration. The state of this pin depends on the dual-purpose pin settings.
- (7) To ensure a successful configuration, send the entire configuration data to the Stratix V device. CONF_DONE is released high when the Stratix V device receives all the configuration data successfully. After CONF_DONE goes high, send two additional falling edges on DCLK to begin initialization and enter user mode.
- (8) After the option bit to enable the INIT_DONE pin is configured into the device, the INIT DONE goes low.

Table 50 lists the timing parameters for Stratix V devices for FPP configuration when the DCLK-to-DATA[] ratio is 1.

Table 50. FPP Timing Parameters for Stratix V Devices (1)

Symbol	Parameter	Minimum	Maximum	Units
t _{CF2CD}	nCONFIG low to CONF_DONE low	—	600	ns
t _{CF2ST0}	nCONFIG low to nSTATUS low		600	ns
t _{CFG}	nCONFIG low pulse width	2		μS
t _{status}	nSTATUS low pulse width	268	1,506 ⁽²⁾	μS
t _{CF2ST1}	nCONFIG high to nSTATUS high	—	1,506 ⁽³⁾	μS
t _{CF2CK} (6)	nCONFIG high to first rising edge on DCLK	1,506		μS
t _{ST2CK} (6)	nSTATUS high to first rising edge of DCLK	2		μS
t _{DSU}	DATA [] setup time before rising edge on DCLK	5.5	_	ns
t _{DH}	DATA [] hold time after rising edge on DCLK	0	_	ns
t _{CH}	DCLK high time	$0.45\times1/f_{MAX}$		S
t _{CL}	DCLK low time	$0.45\times1/f_{MAX}$	_	S
t _{CLK}	DCLK period	1/f _{MAX}		S
4	DCLK frequency (FPP ×8/×16)	—	125	MHz
IMAX	DCLK frequency (FPP ×32)	—	100	MHz
t _{CD2UM}	CONF_DONE high to user mode ⁽⁴⁾	175	437	μS
+	CONTR DOWN high to CT WARD analysis	4 × maximum		
LCD2CU	CONF_DONE HIGH to CLEOSE enabled	DCLK period	—	_
t _{cD2UMC}	CONF_DONE high to user mode with CLKUSR option on	$\begin{array}{c} t_{\text{CD2CU}} + \\ (8576 \times \text{CLKUSR} \\ \text{period}) \ ^{(5)} \end{array}$		_

Notes to Table 50:

(1) Use these timing parameters when the decompression and design security features are disabled.

(2) This value is applicable if you do not delay configuration by extending the nCONFIG or nSTATUS low pulse width.

(3) This value is applicable if you do not delay configuration by externally holding the nSTATUS low.

- (4) The minimum and maximum numbers apply only if you chose the internal oscillator as the clock source for initializing the device.
- (5) To enable the CLKUSR pin as the initialization clock source and to obtain the maximum frequency specification on these pins, refer to the Initialization section of the "Configuration, Design Security, and Remote System Upgrades in Stratix V Devices" chapter.
- (6) If nSTATUS is monitored, follow the t_{ST2CK} specification. If nSTATUS is not monitored, follow the t_{CF2CK} specification.

FPP Configuration Timing when DCLK-to-DATA [] > 1

Figure 13 shows the timing waveform for FPP configuration when using a MAX II device, MAX V device, or microprocessor as an external host. This waveform shows timing when the DCLK-to-DATA [] ratio is more than 1.

Symbol	Parameter	Minimum	Maximum	Units
t _{CD2UM}	CONF_DONE high to user mode (3)	175	437	μS
t _{CD2CU}	CONF_DONE high to CLKUSR enabled	4 × maximum DCLK period	-	—
t _{CD2UMC}	CONF_DONE high to user mode with CLKUSR option on	t _{cd2cu} + (8576 × clkusr period)	-	—

Table 53. AS Timing Parameters for AS \times 1 and AS \times 4 Configurations in Stratix V Devices ^{(1), (2)} (Part 2 of 2)

Notes to Table 53:

(1) The minimum and maximum numbers apply only if you choose the internal oscillator as the clock source for initializing the device.

(2) t_{CF2CD}, t_{CF2ST0}, t_{CF2ST0}, t_{CF6}, t_{STATUS}, and t_{CF2ST1} timing parameters are identical to the timing parameters for PS mode listed in Table 54 on page 63.

(3) To enable the CLKUSR pin as the initialization clock source and to obtain the maximum frequency specification on this pin, refer to the Initialization section of the "Configuration, Design Security, and Remote System Upgrades in Stratix V Devices" chapter.

Passive Serial Configuration Timing

Figure 15 shows the timing waveform for a passive serial (PS) configuration when using a MAX II device, MAX V device, or microprocessor as an external host.

Figure 15. PS Configuration Timing Waveform ⁽¹⁾



Notes to Figure 15:

- (1) The beginning of this waveform shows the device in user mode. In user mode, nCONFIG, nSTATUS, and CONF_DONE are at logic high levels. When nCONFIG is pulled low, a reconfiguration cycle begins.
- (2) After power-up, the Stratix V device holds nSTATUS low for the time of the POR delay.
- (3) After power-up, before and during configuration, CONF DONE is low.
- (4) Do not leave DCLK floating after configuration. You can drive it high or low, whichever is more convenient.
- (5) DATAO is available as a user I/O pin after configuration. The state of this pin depends on the dual-purpose pin settings in the **Device and Pins Option**.
- (6) To ensure a successful configuration, send the entire configuration data to the Stratix V device. CONF_DONE is released high after the Stratix V device receives all the configuration data successfully. After CONF_DONE goes high, send two additional falling edges on DCLK to begin initialization and enter user mode.
- (7) After the option bit to enable the INIT DONE pin is configured into the device, the INIT DONE goes low.

Table 61. Document Revision History (Part 2 of 3)

Date	Version	Changes		
		 Added the I3YY speed grade and changed the data rates for the GX channel in Table 1. 		
		 Added the I3YY speed grade to the V_{CC} description in Table 6. 		
		 Added the I3YY speed grade to V_{CCHIP_L}, V_{CCHIP_R}, V_{CCHSSI_L}, and V_{CCHSSI_R} descriptions in Table 7. 		
		■ Added 240-Ω to Table 11.		
		Changed CDR PPM tolerance in Table 23.		
		 Added additional max data rate for fPLL in Table 23. 		
		 Added the I3YY speed grade and changed the data rates for transceiver speed grade 3 in Table 25. 		
		 Added the I3YY speed grade and changed the data rates for transceiver speed grade 3 in Table 26. 		
		 Changed CDR PPM tolerance in Table 28. 		
		 Added additional max data rate for fPLL in Table 28. 		
		 Changed the mode descriptions for MLAB and M20K in Table 33. 		
		 Changed the Max value of f_{HSCLK_OUT} for the C2, C2L, I2, I2L speed grades in Table 36. 		
November 2014	3.3	 Changed the frequency ranges for C1 and C2 in Table 39. 		
		 Changed the .rbf file sizes for 5SGSD6 and 5SGSD8 in Table 47. 		
		 Added note about nSTATUS to Table 50, Table 51, Table 54. 		
		 Changed the available settings in Table 58. 		
		 Changed the note in "Periphery Performance". 		
		 Updated the "I/O Standard Specifications" section. 		
		 Updated the "Raw Binary File Size" section. 		
		 Updated the receiver voltage input range in Table 22. 		
		 Updated the max frequency for the LVDS clock network in Table 36. 		
		■ Updated the DCLK note to Figure 11.		
		 Updated Table 23 VO_{CM} (DC Coupled) condition. 		
		Updated Table 6 and Table 7.		
		 Added the DCLK specification to Table 55. 		
		Updated the notes for Table 47.		
		 Updated the list of parameters for Table 56. 		
November 2013	3.2	Updated Table 28		
November 2013	3.1	Updated Table 33		
November 2013	3.0	Updated Table 23 and Table 28		
October 2013	2.9	 Updated the "Transceiver Characterization" section 		
	2.8	 Updated Table 3, Table 12, Table 14, Table 19, Table 20, Table 23, Table 24, Table 28, Table 30, Table 31, Table 32, Table 33, Table 36, Table 39, Table 40, Table 41, Table 42, Table 47, Table 53, Table 58, and Table 59 		
Uctober 2013		 Added Figure 1 and Figure 3 		
		 Added the "Transceiver Characterization" section 		
		 Removed all "Preliminary" designations. 		