# E·XFL

# Intel - 5SGXEA7K1F40C2L Datasheet



Welcome to E-XFL.COM

#### Understanding <u>Embedded - FPGAs (Field</u> <u>Programmable Gate Array)</u>

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

#### **Applications of Embedded - FPGAs**

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

#### Details

Product Status	Obsolete
Number of LABs/CLBs	234720
Number of Logic Elements/Cells	622000
Total RAM Bits	51200000
Number of I/O	696
Number of Gates	-
Voltage - Supply	0.82V ~ 0.88V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	1517-BBGA, FCBGA
Supplier Device Package	1517-FBGA (40x40)
Purchase URL	https://www.e-xfl.com/product-detail/intel/5sgxea7k1f40c2l

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

		Conditions		Calibratio	n Accuracy		
Symbol	Description	Conditions	C1	C2,I2	C3,I3, I3YY	C4,14	Unit
50-Ω R <sub>S</sub>	Internal series termination with calibration (50- $\Omega$ setting)	V <sub>CCI0</sub> = 3.0, 2.5, 1.8, 1.5, 1.2 V	±15	±15	±15	±15	%
34- $\Omega$ and 40- $\Omega$ R <sub>S</sub>	Internal series termination with calibration (34- $\Omega$ and 40- $\Omega$ setting)	V <sub>CCI0</sub> = 1.5, 1.35, 1.25, 1.2 V	±15	±15	±15	±15	%
48-Ω, 60-Ω, 80-Ω, and 240-Ω R <sub>S</sub>	Internal series termination with calibration (48- $\Omega$ , 60- $\Omega$ , 80- $\Omega$ , and 240- $\Omega$ setting)	V <sub>CCI0</sub> = 1.2 V	±15	±15	±15	±15	%
50-Ω R <sub>T</sub>	Internal parallel termination with calibration (50-Ω setting)	V <sub>CCI0</sub> = 2.5, 1.8, 1.5, 1.2 V	-10 to +40	-10 to +40	-10 to +40	-10 to +40	%
20-Ω, 30-Ω, 40-Ω,60-Ω, and 120-Ω R <sub>T</sub>	Internal parallel termination with calibration ( $20 - \Omega$ , $30 - \Omega$ , $40 - \Omega$ , $60 - \Omega$ , and $120 - \Omega$ setting)	V <sub>CCI0</sub> = 1.5, 1.35, 1.25 V	-10 to +40	-10 to +40	-10 to +40	-10 to +40	%
60- $Ω$ and 120- $Ω$ R <sub>T</sub>	Internal parallel termination with calibration (60-Ω and 120-Ω setting)	V <sub>CCI0</sub> = 1.2	-10 to +40	-10 to +40	-10 to +40	-10 to +40	%
$25-\Omega \\ R_{S\_left\_shift}$	Internal left shift series termination with calibration ( $25-\Omega$ R <sub>S_left_shift</sub> setting)	V <sub>CCI0</sub> = 3.0, 2.5, 1.8, 1.5, 1.2 V	±15	±15	±15	±15	%

Table II. OUI Valiblation Accuracy specifications for Stratix V Devices' / (I all 2 of	Table 11.	<b>OCT Calibration A</b>	ccuracy Specificati	ons for Stratix V D	Devices <sup>(1)</sup> (	Part 2 of
--	-----------	--------------------------	---------------------	---------------------	--------------------------	-----------

# Note to Table 11:

(1) OCT calibration accuracy is valid at the time of calibration only.

Table 12 lists the Stratix V OCT without calibration resistance to PVT changes.

Table 12.	OCT Without Calibration	<b>Resistance</b> 1	<b>Tolerance</b>	<b>Specifications</b>	for Stratix	V Devices	(Part 1	of 2)
-----------	-------------------------	---------------------	------------------	-----------------------	-------------	-----------	---------	-------

			<b>Resistance Tolerance</b>				
Symbol	Description	Description Conditions		C2,I2	C3, I3, I3YY	C4, I4	Unit
25-Ω R, 50-Ω R <sub>S</sub>	Internal series termination without calibration (25-Ω setting)	$V_{CCIO} = 3.0$ and 2.5 V	±30	±30	±40	±40	%
25-Ω R <sub>S</sub>	Internal series termination without calibration (25-Ω setting)	V <sub>CCI0</sub> = 1.8 and 1.5 V	±30	±30	±40	±40	%
25-Ω R <sub>S</sub>	Internal series termination without calibration (25-Ω setting)	V <sub>CCI0</sub> = 1.2 V	±35	±35	±50	±50	%

Symbol/	Conditions	Trai	nsceive Grade	r Speed 1	Trai	Transceiver Speed Grade 2			Transceiver Speed Grade 3			
Description		Min	Тур	Max	Min	Тур	Max	Min	Тур	Max		
Reconfiguration clock (mgmt_clk_clk) frequency	_	100		125	100		125	100	_	125	MHz	
Receiver	Receiver											
Supported I/O Standards	_			1.4-V PCMI	L, 1.5-V	PCML,	2.5-V PCM	L, LVPE	CL, and	d LVDS		
Data rate (Standard PCS) (9), (23)	_	600	_	12200	600	_	12200	600	_	8500/ 10312.5 (24)	Mbps	
Data rate (10G PCS) <sup>(9),</sup> <sup>(23)</sup>	_	600	_	14100	600	_	12500	600	_	8500/ 10312.5 (24)	Mbps	
Absolute V <sub>MAX</sub> for a receiver pin <sup>(5)</sup>	_	_	_	1.2	_	_	1.2	_	_	1.2	V	
Absolute V <sub>MIN</sub> for a receiver pin	_	-0.4	_	_	-0.4	_	_	-0.4	_	_	V	
Maximum peak- to-peak differential input voltage V <sub>ID</sub> (diff p- p) before device configuration <sup>(22)</sup>	_	_	_	1.6	_	_	1.6	_		1.6	V	
Maximum peak- to-peak	V <sub>CCR_GXB</sub> = 1.0 V/1.05 V (V <sub>ICM</sub> = 0.70 V)	_	_	2.0	_	_	2.0	_	_	2.0	V	
voltage $V_{ID}$ (diff p- p) after device configuration <sup>(18)</sup> .	V <sub>CCR_GXB</sub> = 0.90 V (V <sub>ICM</sub> = 0.6 V)			2.4			2.4			2.4	V	
(22)	$V_{CCR_GXB} = 0.85 V$ (V <sub>ICM</sub> = 0.6 V)			2.4			2.4		_	2.4	V	
Minimum differential eye opening at receiver serial input pins <sup>(6), (22),</sup> (27)	_	85			85			85	_	_	mV	

# Table 23. Transceiver Specifications for Stratix V GX and GS Devices <sup>(1)</sup> (Part 3 of 7)

Symbol/	Conditions	Trai	nsceive Grade	r Speed 1	Transceiver Speed Grade 2			Trai	Unit		
Description		Min	Тур	Max	Min	Тур	Max	Min	Тур	Max	
	DC Gain Setting = 0		0	_	_	0	_	_	0	—	dB
	DC Gain Setting = 1	_	2		_	2	_	_	2	_	dB
Programmable DC gain	DC Gain Setting = 2	_	4	_	_	4	_	_	4	_	dB
	DC Gain Setting = 3	_	6	_	_	6	_	_	6	_	dB
	DC Gain Setting = 4		8			8	_		8	_	dB
Transmitter											
Supported I/O Standards	_		1.4-V and 1.5-V PCML								
Data rate (Standard PCS)	_	600	_	12200	600	_	12200	600	_	8500/ 10312.5 (24)	Mbps
Data rate (10G PCS)	_	600	_	14100	600	_	12500	600	_	8500/ 10312.5 (24)	Mbps
	85-Ω setting	_	85 ± 20%	_	_	85 ± 20%	_	_	85 ± 20%	—	Ω
Differential on-	100-Ω setting	_	100 ± 20%	_	_	100 ± 20%	_	_	100 ± 20%	_	Ω
chip termination resistors	120-Ω setting		120 ± 20%	_		120 ± 20%	_		120 ± 20%	_	Ω
	150-Ω setting	_	150 ± 20%			150 ± 20%	_		150 ± 20%	_	Ω
V <sub>OCM</sub> (AC coupled)	0.65-V setting	_	650		_	650	_	_	650	—	mV
V <sub>OCM</sub> (DC coupled)	_	_	650	_	_	650		_	650	_	mV
Rise time <sup>(7)</sup>	20% to 80%	30	—	160	30	—	160	30	—	160	ps
Fall time <sup>(7)</sup>	80% to 20%	30		160	30		160	30	—	160	ps
Intra-differential pair skew	Tx V <sub>CM</sub> = 0.5 V and slew rate of 15 ps	_	_	15			15		_	15	ps
Intra-transceiver block transmitter channel-to- channel skew	x6 PMA bonded mode	_	_	120	_	_	120	_		120	ps

# Table 23. Transceiver Specifications for Stratix V GX and GS Devices <sup>(1)</sup> (Part 5 of 7)

# Table 23. Transceiver Specifications for Stratix V GX and GS Devices <sup>(1)</sup> (Part 6 of 7)

Symbol/	Conditions	Trai	nsceive Grade	r Speed 1	Transceiver Speed Grade 2			Tran	Unit		
Description		Min	Тур	Max	Min	Тур	Max	Min	Тур	Max	
Inter-transceiver block transmitter channel-to- channel skew	xN PMA bonded mode	_	_	500	_	_	500	_	_	500	ps
CMU PLL	•										
Supported Data Range	_	600	_	12500	600	_	12500	600	_	8500/ 10312.5 (24)	Mbps
t <sub>pll_powerdown</sub> <sup>(15)</sup>	—	1			1			1			μs
t <sub>pll_lock</sub> <sup>(16)</sup>		—		10	—	_	10	—	_	10	μs
ATX PLL											
	VCO post-divider L=2	8000	_	14100	8000	_	12500	8000	_	8500/ 10312.5 (24)	Mbps
Supported Data	L=4	4000	_	7050	4000	_	6600	4000	—	6600	Mbps
Rate Range	L=8	2000		3525	2000		3300	2000		3300	Mbps
Rate Range	L=8, Local/Central Clock Divider =2	1000	_	1762.5	1000	_	1762.5	1000	_	1762.5	Mbps
t <sub>pll_powerdown</sub> (15)	—	1	_	—	1	_	—	1	_	—	μs
t <sub>pll_lock</sub> (16)	—		—	10		—	10	—		10	μs
fPLL	•										
Supported Data Range	_	600	_	3250/ 3125 <sup>(25)</sup>	600	_	3250/ 3125 <sup>(25)</sup>	600	_	3250/ 3125 <sup>(25)</sup>	Mbps
t <sub>pll_powerdown</sub> <sup>(15)</sup>	_	1	—		1	—		1			μs

Table 27 shows the  $V_{\text{OD}}$  settings for the GX channel.

Symbol	V <sub>op</sub> Setting	V <sub>od</sub> Value (mV)	V <sub>op</sub> Setting	V <sub>op</sub> Value (mV)
	0 (1)	0	32	640
	1 (1)	20	33	660
	2 (1)	40	34	680
	3 (1)	60	35	700
	4 (1)	80	36	720
	5 <sup>(1)</sup>	100	37	740
	6	120	38	760
	7	140	39	780
	8	160	40	800
	9	180	41	820
	10	200	42	840
	11	220	43	860
	12	240	44	880
	13	260	45	900
	14	280	46	920
$V_{0D}$ differential peak to peak	15	300	47	940
typical <sup>(3)</sup>	16	320	48	960
	17	340	49	980
	18	360	50	1000
	19	380	51	1020
	20	400	52	1040
	21	420	53	1060
	22	440	54	1080
	23	460	55	1100
	24	480	56	1120
	25	500	57	1140
	26	520	58	1160
	27	540	59	1180
	28	560	60	1200
	29	580	61	1220
	30	600	62	1240
	31	620	63	1260

Table 27. Typical V\_{0D} Setting for GX Channel, TX Termination = 100  $\Omega^{\left(2\right)}$ 

#### Note to Table 27:

(1) If TX termination resistance =  $100\Omega$ , this VOD setting is illegal.

(2) The tolerance is +/-20% for all VOD settings except for settings 2 and below.

(3) Refer to Figure 2.

Symbol/	Conditions	S	Transceive peed Grade	2	S	Fransceive Deed Grade	r 3	Unit
Description		Min	Тур	Max	Min	Тур	Max	
Differential on-chip termination resistors <sup>(7)</sup>	GT channels		100	_	_	100	_	Ω
	85- $\Omega$ setting	_	85 ± 30%	_	_	85 ± 30%	_	Ω
Differential on-chip	100-Ω setting	_	100 ± 30%	_	_	100 ± 30%	_	Ω
for GX channels <sup>(19)</sup>	120-Ω setting	_	120 ± 30%	_	—	120 ± 30%	—	Ω
	150-Ω setting		150 ± 30%	_	_	150 ± 30%	_	Ω
V <sub>ICM</sub> (AC coupled)	GT channels	_	650	_	—	650	—	mV
	VCCR_GXB = 0.85 V or 0.9 V	_	600	_	_	600	_	mV
VICM (AC and DC coupled) for GX Channels	VCCR_GXB = 1.0 V full bandwidth	_	700		_	700	_	mV
	VCCR_GXB = 1.0 V half bandwidth	_	750	_	_	750	_	mV
t <sub>LTR</sub> <sup>(9)</sup>	—	_	—	10	—	—	10	μs
t <sub>LTD</sub> <sup>(10)</sup>		4			4	_	_	μs
t <sub>LTD_manual</sub> <sup>(11)</sup>		4	_		4	_	_	μs
t <sub>LTR_LTD_manual</sub> <sup>(12)</sup>	—	15	—	_	15	—	—	μs
Run Lenath	GT channels		—	72	—	—	72	CID
	GX channels				(8)			
CDR PPM	GT channels	_	—	1000	—	—	1000	± PPM
	GX channels				(8)			
Programmable	GT channels	_		14		_	14	dB
(AC Gain) <sup>(5)</sup>	GX channels				(8)			
Programmable	GT channels	_		7.5	_		7.5	dB
DC gain <sup>(6)</sup>	GX channels				(8)			
Differential on-chip termination resistors <sup>(7)</sup>	GT channels	_	100	—	_	100	_	Ω
Transmitter								
Supported I/O Standards	_			1.4-V	and 1.5-V P	CML		
Data rate (Standard PCS)	GX channels	600	_	8500	600		8500	Mbps
Data rate (10G PCS)	GX channels	600		12,500	600		12,500	Mbps

# Table 28. Transceiver Specifications for Stratix V GT Devices (Part 3 of 5)<sup>(1)</sup>

Table 29 shows the  $V_{\text{OD}}$  settings for the GT channel.

Symbol	V <sub>OD</sub> Setting	V <sub>od</sub> Value (mV)
	0	0
	1	200
V., differential neak to neak typical $(1)$	2	400
The american hear to hear thicat to	3	600
	4	800
	5	1000

## Note:

(1) Refer to Figure 4.

Figure 4 shows the differential transmitter output waveform.





Figure 5 shows the Stratix V AC gain curves for GT channels.

Figure 5. AC Gain Curves for GT Channels

Symbol	Parameter	Min	Тур	Max	Unit
+ (3) (4)	Input clock cycle-to-cycle jitter ( $f_{REF} \ge 100 \text{ MHz}$ )			0.15	UI (p-p)
LINCCJ (0), (1)	Input clock cycle-to-cycle jitter (f <sub>REF</sub> < 100 MHz)	-750		+750	ps (p-p)
+ (5)	Period Jitter for dedicated clock output (f_{OUT} $\geq$ 100 MHz)	_	_	175 <sup>(1)</sup>	ps (p-p)
CUTPJ_DC	Period Jitter for dedicated clock output (f <sub>OUT</sub> < 100 MHz)	_	_	17.5 <sup>(1)</sup>	mUI (p-p)
+ (5)	Period Jitter for dedicated clock output in fractional PLL ( $f_{OUT} \ge 100$ MHz)	_	_	250 <sup>(11)</sup> , 175 <sup>(12)</sup>	ps (p-p)
<sup>L</sup> FOUTPJ_DC	Period Jitter for dedicated clock output in fractional PLL (f <sub>OUT</sub> < 100 MHz)	_	_	25 <sup>(11)</sup> , 17.5 <sup>(12)</sup>	mUI (p-p)
+ (5)	Cycle-to-Cycle Jitter for a dedicated clock output ( $f_{\text{OUT}} \geq 100 \text{ MHz})$		_	175	ps (p-p)
COUTCCJ_DC	Cycle-to-Cycle Jitter for a dedicated clock output $(f_{OUT} < 100 \text{ MHz})$		_	17.5	mUI (p-p)
+ (5)	Cycle-to-cycle Jitter for a dedicated clock output in fractional PLL ( $f_{OUT} \ge 100 \text{ MHz}$ )		_	250 <sup>(11)</sup> , 175 <sup>(12)</sup>	ps (p-p)
FOUTCCJ_DC	Cycle-to-cycle Jitter for a dedicated clock output in fractional PLL ( $f_{OUT} < 100 \text{ MHz}$ )+		_	25 <sup>(11)</sup> , 17.5 <sup>(12)</sup>	mUI (p-p)
t <sub>outpj 10</sub> (5),	Period Jitter for a clock output on a regular I/O in integer PLL ( $f_{OUT} \ge 100 \text{ MHz}$ )		_	600	ps (p-p)
(8)	Period Jitter for a clock output on a regular I/O $(f_{OUT} < 100 \text{ MHz})$		_	60	mUI (p-p)
t <sub>foutpj 10</sub> <sup>(5),</sup>	Period Jitter for a clock output on a regular I/O in fractional PLL ( $f_{OUT} \ge 100 \text{ MHz}$ )	_	_	600 <sup>(10)</sup>	ps (p-p)
(8), (11)	Period Jitter for a clock output on a regular I/O in fractional PLL (f <sub>OUT</sub> < 100 MHz)	_	_	60 <sup>(10)</sup>	mUI (p-p)
t <sub>outccj_io</sub> (5),	Cycle-to-cycle Jitter for a clock output on a regular I/O in integer PLL ( $f_{OUT} \geq 100 \mbox{ MHz})$	_	_	600	ps (p-p)
(8)	Cycle-to-cycle Jitter for a clock output on a regular I/O in integer PLL (f <sub>OUT</sub> < 100 MHz)	_	_	60 <sup>(10)</sup>	mUI (p-p)
t <sub>FOUTCCJ 10</sub> (5),	Cycle-to-cycle Jitter for a clock output on a regular I/O in fractional PLL ( $f_{OUT} \ge 100$ MHz)		_	600 <sup>(10)</sup>	ps (p-p)
(8), (11)	Cycle-to-cycle Jitter for a clock output on a regular I/O in fractional PLL (f <sub>OUT</sub> < 100 MHz)	_	_	60	mUI (p-p)
t <sub>CASC OUTPJ DC</sub>	Period Jitter for a dedicated clock output in cascaded PLLs ( $f_{OUT} \ge 100 \text{ MHz}$ )	_	_	175	ps (p-p)
(5), (6)	Period Jitter for a dedicated clock output in cascaded PLLs ( $f_{OUT}$ < 100 MHz)	_	_	17.5	mUI (p-p)
f <sub>DRIFT</sub>	Frequency drift after PFDENA is disabled for a duration of 100 $\mu s$		_	±10	%
dK <sub>BIT</sub>	Bit number of Delta Sigma Modulator (DSM)	8	24	32	Bits
k <sub>VALUE</sub>	Numerator of Fraction	128	8388608	2147483648	—

Table 31. PLL Specifications for Stratix V Devices (Part 2 of 3)

## Table 31. PLL Specifications for Stratix V Devices (Part 3 of 3)

Symbol	Parameter	Min	Тур	Max	Unit
f <sub>RES</sub>	Resolution of VCO frequency ( $f_{INPFD} = 100 \text{ MHz}$ )	390625	5.96	0.023	Hz

#### Notes to Table 31:

(1) This specification is limited in the Quartus II software by the I/O maximum frequency. The maximum I/O frequency is different for each I/O standard.

(2) This specification is limited by the lower of the two: I/O  $f_{MAX}$  or  $f_{OUT}$  of the PLL.

- (3) A high input jitter directly affects the PLL output jitter. To have low PLL output clock jitter, you must provide a clean clock source < 120 ps.
- (4)  $f_{REF}$  is fIN/N when N = 1.
- (5) Peak-to-peak jitter with a probability level of 10<sup>-12</sup> (14 sigma, 99.9999999974404% confidence level). The output jitter specification applies to the intrinsic jitter of the PLL, when an input jitter of 30 ps is applied. The external memory interface clock output jitter specifications use a different measurement method and are available in Table 44 on page 52.
- (6) The cascaded PLL specification is only applicable with the following condition: a. Upstream PLL: 0.59Mhz ≤ Upstream PLL BW < 1 MHz b. Downstream PLL: Downstream PLL BW > 2 MHz
- (7) High bandwidth PLL settings are not supported in external feedback mode.
- (8) The external memory interface clock output jitter specifications use a different measurement method, which is available in Table 42 on page 50.
- (9) The VCO frequency reported by the Quartus II software in the PLL Usage Summary section of the compilation report takes into consideration the VCO post-scale counter K value. Therefore, if the counter K has a value of 2, the frequency reported can be lower than the f<sub>VCO</sub> specification.
- (10) This specification only covers fractional PLL for low bandwidth. The  $f_{VCO}$  for fractional value range 0.05 0.95 must be  $\geq$  1000 MHz, while  $f_{VCO}$  for fractional value range 0.20 0.80 must be  $\geq$  1200 MHz.
- (11) This specification only covered fractional PLL for low bandwidth. The  $f_{VC0}$  for fractional value range 0.05-0.95 must be  $\geq$  1000 MHz.
- (12) This specification only covered fractional PLL for low bandwidth. The  $f_{VC0}$  for fractional value range 0.20-0.80 must be  $\geq$  1200 MHz.

# **DSP Block Specifications**

Table 32 lists the Stratix V DSP block performance specifications.

			F	Peformanc	e			
Mode	C1	C2, C2L	12, 12L	C3	13, 13L, 13YY	C4	14	Unit
		Modes ı	using one	DSP				
Three 9 x 9	600	600	600	480	480	420	420	MHz
One 18 x 18	600	600	600	480	480	420	400	MHz
Two partial 18 x 18 (or 16 x 16)	600	600	600	480	480	420	400	MHz
One 27 x 27	500	500	500	400	400	350	350	MHz
One 36 x 18	500	500	500	400	400	350	350	MHz
One sum of two 18 x 18(One sum of 2 16 x 16)	500	500	500	400	400	350	350	MHz
One sum of square	500	500	500	400	400	350	350	MHz
One 18 x 18 plus 36 (a x b) + c	500	500	500	400	400	350	350	MHz
		Modes u	sing two l	DSPs				
Three 18 x 18	500	500	500	400	400	350	350	MHz
One sum of four 18 x 18	475	475	475	380	380	300	300	MHz
One sum of two 27 x 27	465	465	450	380	380	300	290	MHz
One sum of two 36 x 18	475	475	475	380	380	300	300	MHz
One complex 18 x 18	500	500	500	400	400	350	350	MHz
One 36 x 36	475	475	475	380	380	300	300	MHz

## Table 32. Block Performance Specifications for Stratix V DSP Devices (Part 1 of 2)

		Resour	ces Used			Pe	erforman	ce			
Memory	Mode	ALUTS	Memory	C1	C2, C2L	C3	C4	12, 12L	13, 13L, 13YY	14	Unit
	Single-port, all supported widths	0	1	700	700	650	550	700	500	450	MHz
	Simple dual-port, all supported widths	0	1	700	700	650	550	700	500	450	MHz
	Simple dual-port with the read-during-write option set to <b>Old Data</b> , all supported widths	0	1	525	525	455	400	525	455	400	MHz
M20K Block	Simple dual-port with ECC enabled, 512 × 32	0	1	450	450	400	350	450	400	350	MHz
	Simple dual-port with ECC and optional pipeline registers enabled, 512 × 32	0	1	600	600	500	450	600	500	450	MHz
	True dual port, all supported widths	0	1	700	700	650	550	700	500	450	MHz
	ROM, all supported widths	0	1	700	700	650	550	700	500	450	MHz

# Table 33. Memory Block Performance Specifications for Stratix V Devices <sup>(1), (2)</sup> (Part 2 of 2)

## Notes to Table 33:

(1) To achieve the maximum memory block performance, use a memory block clock that comes through global clock routing from an on-chip PLL set to **50**% output duty cycle. Use the Quartus II software to report timing for this and other memory block clocking schemes.

(2) When you use the error detection cyclical redundancy check (CRC) feature, there is no degradation in F<sub>MAX</sub>.

(3) The F<sub>MAX</sub> specification is only achievable with Fitter options, MLAB Implementation In 16-Bit Deep Mode enabled.

# **Temperature Sensing Diode Specifications**

Table 34 lists the internal TSD specification.

#### **Table 34. Internal Temperature Sensing Diode Specification**

Temperature Range	Accuracy	Offset Calibrated Option	Sampling Rate	Conversion Time	Resolution	Minimum Resolution with no Missing Codes
-40°C to 100°C	±8°C	No	1 MHz, 500 KHz	< 100 ms	8 bits	8 bits

Table 35 lists the specifications for the Stratix V external temperature sensing diode.

Table 35.	External	Temperature	<b>Sensing D</b>	iode Speci	fications f	for Stratix V	Devices
-----------	----------	-------------	------------------	------------	-------------	---------------	---------

Description	Min	Тур	Max	Unit
I <sub>bias</sub> , diode source current	8	—	200	μA
V <sub>bias,</sub> voltage across diode	0.3	—	0.9	V
Series resistance	—	_	< 1	Ω
Diode ideality factor	1.006	1.008	1.010	_

# **Periphery Performance**

This section describes periphery performance, including high-speed I/O and external memory interface.

I/O performance supports several system interfaces, such as the **LVDS** high-speed I/O interface, external memory interface, and the **PCI/PCI-X** bus interface. General-purpose I/O standards such as 3.3-, 2.5-, 1.8-, and 1.5-**LVTTL/LVCMOS** are capable of a typical 167 MHz and 1.2-**LVCMOS** at 100 MHz interfacing frequency with a 10 pF load.

The actual achievable frequency depends on design- and system-specific factors. Ensure proper timing closure in your design and perform HSPICE/IBIS simulations based on your specific design and system setup to determine the maximum achievable frequency in your system.

# **High-Speed I/O Specification**

Table 36 lists high-speed I/O timing for Stratix V devices.

Table 36. High-Speed I/O Specifications for Stratix V Devices (1), (2) (Part 1 of 4)

Sumbol	Conditions		C1		C2,	C2L, I	2, I2L	C3,	<b>13, 13</b> 1	., I3YY		C4,I	4	11
Symbol	Conditions	Min	Тур	Max	Min	Тур	Max	Min	Тур	Max	Min	Тур	Max	UNIT
f <sub>HSCLK_in</sub> (input clock frequency) True Differential I/O Standards	Clock boost factor W = 1 to 40 $^{(4)}$	5	_	800	5		800	5		625	5		525	MHz
f <sub>HSCLK_in</sub> (input clock frequency) Single Ended I/O Standards <sup>(3)</sup>	Clock boost factor W = 1 to 40 $^{(4)}$	5		800	5		800	5		625	5		525	MHz
f <sub>HSCLK_in</sub> (input clock frequency) Single Ended I/O Standards	Clock boost factor W = 1 to 40 $^{(4)}$	5	_	520	5		520	5	_	420	5	_	420	MHz
f <sub>HSCLK_OUT</sub> (output clock frequency)	_	5	_	800	5	_	800	5	_	625 (5)	5	_	525 (5)	MHz

Symbol	Conditiono		C1		C2,	C2L, I	2, I2L	C3,	13, 131	., I3YY	C4,14			Unit
Symbol	Conditions	Min	Тур	Max	Min	Тур	Max	Min	Тур	Max	Min	Тур	Max	UIIIL
Transmitter														
	SERDES factor J = 3 to 10 <sup>(9)</sup> , <sup>(11)</sup> , <sup>(12)</sup> , <sup>(13)</sup> , <sup>(14)</sup> , <sup>(15)</sup> , <sup>(16)</sup>	(6)	_	1600	(6)	_	1434	(6)	_	1250	(6)	_	1050	Mbps
True Differential I/O Standards	SERDES factor J $\geq 4$ LVDS TX with DPA (12), (14), (15), (16)	(6)		1600	(6)		1600	(6)		1600	(6)	_	1250	Mbps
- f <sub>HSDR</sub> (data rate)	SERDES factor J = 2, uses DDR Registers	(6)	_	(7)	(6)	_	(7)	(6)	_	(7)	(6)		(7)	Mbps
	SERDES factor J = 1, uses SDR Register	(6)	_	(7)	(6)	_	(7)	(6)	_	(7)	(6)	_	(7)	Mbps
Emulated Differential I/O Standards with Three External Output Resistor Networks - f <sub>HSDR</sub> (data rate) <sup>(10)</sup>	SERDES factor J = 4 to 10 $(^{17})$	(6)		1100	(6)		1100	(6)		840	(6)		840	Mbps
t <sub>x Jitter</sub> - True Differential	Total Jitter for Data Rate 600 Mbps - 1.25 Gbps		_	160		_	160		_	160			160	ps
I/O Standards	Total Jitter for Data Rate < 600 Mbps	_	_	0.1			0.1			0.1		_	0.1	UI
t <sub>x Jitter</sub> - Emulated Differential I/O Standards	Total Jitter for Data Rate 600 Mbps - 1.25 Gbps	_	_	300	_	_	300	_	_	300	_		325	ps
with Three External Output Resistor Network	Total Jitter for Data Rate < 600 Mbps	_	_	0.2	_	_	0.2	_	_	0.2	_	_	0.25	UI

# Table 36. High-Speed I/O Specifications for Stratix V Devices (1), (2) (Part 2 of 4)

Symbol	Conditiono		C1		C2, C2L, I2, I2L		C3, I3, I3L, I3YY		C4,I4			Unit		
əyiinuu	Conultions	Min	Тур	Max	Min	Тур	Max	Min	Тур	Max	Min	Тур	Max	Umt
	SERDES factor J = 3 to 10	(6)		(8)	(6)	_	(8)	(6)		(8)	(6)		(8)	Mbps
f <sub>HSDR</sub> (data rate)	SERDES factor J = 2, uses DDR Registers	(6)		(7)	(6)	_	(7)	(6)	_	(7)	(6)		(7)	Mbps
	SERDES factor J = 1, uses SDR Register	(6)	_	(7)	(6)	_	(7)	(6)	_	(7)	(6)	_	(7)	Mbps
DPA Mode														
DPA run length	_			1000 0		_	1000 0	_		1000 0	_		1000 0	UI
Soft CDR mode														
Soft-CDR PPM tolerance	_	_	_	300	_	_	300	_	_	300	_	_	300	± PPM
Non DPA Mode														
Sampling Window	_			300			300			300			300	ps

## Table 36. High-Speed I/O Specifications for Stratix V Devices (1), (2) (Part 4 of 4)

Notes to Table 36:

(1) When J = 3 to 10, use the serializer/deserializer (SERDES) block.

(2) When J = 1 or 2, bypass the SERDES block.

(3) This only applies to DPA and soft-CDR modes.

(4) Clock Boost Factor (W) is the ratio between the input data rate to the input clock rate.

(5) This is achieved by using the **LVDS** clock network.

(6) The minimum specification depends on the clock source (for example, the PLL and clock pin) and the clock routing resource (global, regional, or local) that you use. The I/O differential buffer and input register do not have a minimum toggle rate.

(7) The maximum ideal frequency is the SERDES factor (J) x the PLL maximum output frequency (fOUT) provided you can close the design timing and the signal integrity simulation is clean.

(8) You can estimate the achievable maximum data rate for non-DPA mode by performing link timing closure analysis. You must consider the board skew margin, transmitter delay margin, and receiver sampling margin to determine the maximum data rate supported.

(9) If the receiver with DPA enabled and transmitter are using shared PLLs, the minimum data rate is 150 Mbps.

(10) You must calculate the leftover timing margin in the receiver by performing link timing closure analysis. You must consider the board skew margin, transmitter channel-to-channel skew, and receiver sampling margin to determine leftover timing margin.

(11) The F<sub>MAX</sub> specification is based on the fast clock used for serial data. The interface F<sub>MAX</sub> is also dependent on the parallel clock domain which is design-dependent and requires timing analysis.

(12) Stratix V RX LVDS will need DPA. For Stratix V TX LVDS, the receiver side component must have DPA.

(13) Stratix V LVDS serialization and de-serialization factor needs to be x4 and above.

(14) Requires package skew compensation with PCB trace length.

(15) Do not mix single-ended I/O buffer within LVDS I/O bank.

(16) Chip-to-chip communication only with a maximum load of 5 pF.

(17) When using True LVDS RX channels for emulated LVDS TX channel, only serialization factors 1 and 2 are supported.

Figure 7 shows the dynamic phase alignment (DPA) lock time specifications with the DPA PLL calibration option enabled.

Figure 7. DPA Lock Time Specification with DPA PLL Calibration Enabled

rx_reset			
rx_dpa_locked			<u> </u>
			-

Table 37 lists the DPA lock time specifications for Stratix V devices.

Table 37. DPA Lock Time Specifications for Stratix V GX Devices Only (1), (2), (3)

Standard	Training Pattern	Number of Data Transitions in One Repetition of the Training Pattern	Number of Repetitions per 256 Data Transitions <sup>(4)</sup>	Maximum
SPI-4	00000000001111111111	2	128	640 data transitions
Parallel Rapid I/O	00001111	2	128	640 data transitions
	10010000	4	64	640 data transitions
Miscellaneous	10101010	8	32	640 data transitions
Wiscenareous	01010101	8	32	640 data transitions

#### Notes to Table 37:

(1) The DPA lock time is for one channel.

(2) One data transition is defined as a 0-to-1 or 1-to-0 transition.

(3) The DPA lock time stated in this table applies to both commercial and industrial grade.

(4) This is the number of repetitions for the stated training pattern to achieve the 256 data transitions.

Figure 8 shows the **LVDS** soft-clock data recovery (CDR)/DPA sinusoidal jitter tolerance specification for a data rate  $\geq$  1.25 Gbps. Table 38 lists the **LVDS** soft-CDR/DPA sinusoidal jitter tolerance specification for a data rate  $\geq$  1.25 Gbps.





Jitter Free	quency (Hz)	Sinusoidal Jitter (UI)
F1	10,000	25.000
F2	17,565	25.000
F3	1,493,000	0.350
F4	50,000,000	0.350

iadie 38. lvus sott-luk/upa sinusoidai jitter mask vaiues tor a uata kate > 1.2	25 G	.2	1.	1	>	>		Ì	e	F	Ł	đ	a	2	1	R	P							Ľ	I.		I.	Ì	1	3	a	3	a	2	2	2	ŀ	t	t	t	ſ	ľ	3	2	2	2	2	2	1	)	D		I		Ľ	1	2	2	ź	â	i		۴	ŕ	r	r		I	I	Ì	1	Π	٥	٢	i	F	f	f	1	1		5	S	S	S	2	2	e	E	I	U	h	I	۱	a	ŀ	I	V	۱			ľ	٢	k	k	s	S	S	1	a	2	2		И	V	N			•	۴	r	r	1	1	1	2	2	2	2	e	e	e	E	t	t	i	ŀ	t	ľ	i	i	f	f	ŀ	ŀ	li
---	------	----	----	---	---	---	--	---	---	---	---	---	---	---	---	---	---	--	--	--	--	--	--	---	----	--	----	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---	--	---	--	---	---	---	---	---	---	---	--	---	---	---	---	--	---	---	---	---	---	---	---	---	---	---	---	---	---	--	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---	--	--	---	---	---	---	---	---	---	---	---	---	---	--	---	---	---	--	--	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---	----

Figure 9 shows the **LVDS** soft-CDR/DPA sinusoidal jitter tolerance specification for a data rate < 1.25 Gbps.





# **DLL Range, DQS Logic Block, and Memory Output Clock Jitter Specifications**

Table 39 lists the DLL range specification for Stratix V devices. The DLL is always in 8-tap mode in Stratix V devices.

Table 39. DLL Range Specifications for Stratix V Devices (1)

C1	C2, C2L, I2, I2L	C3, I3, I3L, I3YY	C4,I4	Unit
300-933	300-933	300-890	300-890	MHz

#### Note to Table 39:

(1) Stratix V devices support memory interface frequencies lower than 300 MHz, although the reference clock that feeds the DLL must be at least 300 MHz. To support interfaces below 300 MHz, multiply the reference clock feeding the DLL to ensure the frequency is within the supported range of the DLL.

Table 40 lists the DQS phase offset delay per stage for Stratix V devices.

Table 40. DQS Phase Offset Delay Per Setting for Stratix V Devices <sup>(1), (2)</sup> (Part 1 of 2)

Speed Grade	Min	Max	Unit
C1	8	14	ps
C2, C2L, I2, I2L	8	14	ps
C3,I3, I3L, I3YY	8	15	ps

Clock	Parameter	Symbol	C	1	C2, C2L	, 12, 12L	C3, I3 I3	8, <b>13L</b> , YY	C4	,14	Unit
NELWUIK		-	Min	Max	Min	Max	Min	Max	Min	Max	
	Clock period jitter	$t_{JIT(per)}$	-25	25	-25	25	-30	30	-35	35	ps
PHY Clock	Cycle-to-cycle period jitter	$t_{\rm JIT(cc)}$	-50	50	-50	50	-60	60	-70	70	ps
	Duty cycle jitter	$t_{JIT(duty)}$	-37.5	37.5	-37.5	37.5	-45	45	-56	56	ps

## Table 42. Memory Output Clock Jitter Specification for Stratix V Devices (1), (Part 2 of 2) (2), (3)

## Notes to Table 42:

(1) The clock jitter specification applies to the memory output clock pins generated using differential signal-splitter and DDIO circuits clocked by a PLL output routed on a PHY, regional, or global clock network as specified. Altera recommends using PHY clock networks whenever possible.

(2) The clock jitter specification applies to the memory output clock pins clocked by an integer PLL.

(3) The memory output clock jitter is applicable when an input jitter of 30 ps peak-to-peak is applied with bit error rate (BER) -12, equivalent to 14 sigma.

# **OCT Calibration Block Specifications**

Table 43 lists the OCT calibration block specifications for Stratix V devices.

# Table 43. OCT Calibration Block Specifications for Stratix V Devices

Symbol	Description	Min	Тур	Max	Unit
OCTUSRCLK	Clock required by the OCT calibration blocks	—	—	20	MHz
T <sub>OCTCAL</sub>	Number of OCTUSRCLK clock cycles required for OCT $\rm R_S/R_T$ calibration		1000	_	Cycles
T <sub>OCTSHIFT</sub>	Number of OCTUSRCLK clock cycles required for the OCT code to shift out	_	32	_	Cycles
T <sub>RS_RT</sub>	Time required between the dyn_term_ctrl and oe signal transitions in a bidirectional I/O buffer to dynamically switch between OCT $R_S$ and $R_T$ (Figure 10)		2.5		ns

Figure 10 shows the timing diagram for the oe and dyn\_term\_ctrl signals.

#### Figure 10. Timing Diagram for oe and dyn\_term\_ctrl Signals



# **Duty Cycle Distortion (DCD) Specifications**

Table 44 lists the worst-case DCD for Stratix V devices.

# Table 44. Worst-Case DCD on Stratix V I/O Pins (1)

Symbol	C	1	C2, C2	L, 12, 12L	C3, I I3	3, I3L, IYY	C4	4,14	Unit
-	Min	Max	Min	Max	Min	Max	Min	Max	
Output Duty Cycle	45	55	45	55	45	55	45	55	%

# Note to Table 44:

(1) The DCD numbers do not cover the core clock network.

# **Configuration Specification**

# **POR Delay Specification**

Power-on reset (POR) delay is defined as the delay between the time when all the power supplies monitored by the POR circuitry reach the minimum recommended operating voltage to the time when the nSTATUS is released high and your device is ready to begin configuration.



For more information about the POR delay, refer to the *Hot Socketing and Power-On Reset in Stratix V Devices* chapter.

Table 45 lists the fast and standard POR delay specification.

#### Table 45. Fast and Standard POR Delay Specification (1)

POR Delay	Minimum	Maximum
Fast	4 ms	12 ms
Standard	100 ms	300 ms

## Note to Table 45:

(1) You can select the POR delay based on the MSEL settings as described in the MSEL Pin Settings section of the "Configuration, Design Security, and Remote System Upgrades in Stratix V Devices" chapter.

# **JTAG Configuration Specifications**

Table 46 lists the JTAG timing parameters and values for Stratix V devices.

Table 46. JTAG Timing Parameters and Values for Stratix V Devices

Symbol	Description	Min	Max	Unit
t <sub>JCP</sub>	TCK clock period <sup>(2)</sup>	30		ns
t <sub>JCP</sub>	TCK clock period <sup>(2)</sup>	167	—	ns
t <sub>JCH</sub>	TCK clock high time <sup>(2)</sup>	14	—	ns
t <sub>JCL</sub>	TCK clock low time <sup>(2)</sup>	14		ns
t <sub>JPSU (TDI)</sub>	TDI JTAG port setup time	2	—	ns
t <sub>JPSU (TMS)</sub>	TMS JTAG port setup time	3	_	ns

# **Remote System Upgrades**

Table 56 lists the timing parameter specifications for the remote system upgrade circuitry.

Table 56. Remote System Upgrade Circuitry Timing Specificatio
---

Parameter	Minimum	Maximum	Unit
t <sub>RU_nCONFIG</sub> <sup>(1)</sup>	250	—	ns
t <sub>RU_nRSTIMER</sub> <sup>(2)</sup>	250	_	ns

#### Notes to Table 56:

- (1) This is equivalent to strobing the reconfiguration input of the ALTREMOTE\_UPDATE megafunction high for the minimum timing specification. For more information, refer to the Remote System Upgrade State Machine section of the "Configuration, Design Security, and Remote System Upgrades in Stratix V Devices" chapter.
- (2) This is equivalent to strobing the reset\_timer input of the ALTREMOTE\_UPDATE megafunction high for the minimum timing specification. For more information, refer to the User Watchdog Timer section of the "Configuration, Design Security, and Remote System Upgrades in Stratix V Devices" chapter.

# **User Watchdog Internal Circuitry Timing Specification**

Table 57 lists the operating range of the 12.5-MHz internal oscillator.

#### Table 57. 12.5-MHz Internal Oscillator Specifications

Minimum	Typical	Maximum	Units
5.3	7.9	12.5	MHz

# I/O Timing

Altera offers two ways to determine I/O timing—the Excel-based I/O Timing and the Quartus II Timing Analyzer.

Excel-based I/O timing provides pin timing performance for each device density and speed grade. The data is typically used prior to designing the FPGA to get an estimate of the timing budget as part of the link timing analysis. The Quartus II Timing Analyzer provides a more accurate and precise I/O timing data based on the specifics of the design after you complete place-and-route.

 You can download the Excel-based I/O Timing spreadsheet from the Stratix V Devices Documentation web page.

# **Programmable IOE Delay**

Table 58 lists the Stratix V IOE programmable delay settings.

Table 58. IOE Programmable Delay for Stratix V Devices (Part 1 of 2)

Parameter	Available Settings	Min Offset (2)	Fast Model		Slow Model							
			Industrial	Commercial	C1	C2	C3	C4	12	13, 13YY	14	Unit
D1	64	0	0.464	0.493	0.838	0.838	0.924	1.011	0.844	0.921	1.006	ns
D2	32	0	0.230	0.244	0.415	0.415	0.459	0.503	0.417	0.456	0.500	ns