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Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Obsolete
Number of LABs/CLBs	234720
Number of Logic Elements/Cells	622000
Total RAM Bits	51200000
Number of I/O	696
Number of Gates	-
Voltage - Supply	0.82V ~ 0.88V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	1517-BBGA, FCBGA
Supplier Device Package	1517-FBGA (40x40)
Purchase URL	https://www.e-xfl.com/product-detail/intel/5sgxea7k1f40c2ln

I/O Pin Leakage Current

Table 9 lists the Stratix V I/O pin leakage current specifications.

Table 9. I/O Pin Leakage Current for Stratix V Devices ⁽¹⁾

Symbol	Description	Conditions	Min	Typ	Max	Unit
I_I	Input pin	$V_I = 0 \text{ V to } V_{CCIO\text{MAX}}$	-30	—	30	μA
I_{OZ}	Tri-stated I/O pin	$V_O = 0 \text{ V to } V_{CCIO\text{MAX}}$	-30	—	30	μA

Note to Table 9:

(1) If $V_O = V_{CCIO}$ to $V_{CCIO\text{MAX}}$, 100 μA of leakage current per I/O is expected.

Bus Hold Specifications

Table 10 lists the Stratix V device family bus hold specifications.

Table 10. Bus Hold Parameters for Stratix V Devices

Parameter	Symbol	Conditions	V _{CCIO}										Unit
			1.2 V		1.5 V		1.8 V		2.5 V		3.0 V		
			Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Low sustaining current	I _{SUSL}	V _{IN} > V _{IL} (maximum)	22.5	—	25.0	—	30.0	—	50.0	—	70.0	—	μA
High sustaining current	I _{SUSH}	V _{IN} < V _{IH} (minimum)	−22.5	—	−25.0	—	−30.0	—	−50.0	—	−70.0	—	μA
Low overdrive current	I _{ODL}	0V < V _{IN} < V _{CCIO}	—	120	—	160	—	200	—	300	—	500	μA
High overdrive current	I _{ODH}	0V < V _{IN} < V _{CCIO}	—	−120	—	−160	—	−200	—	−300	—	−500	μA
Bus-hold trip point	V _{TRIP}	—	0.45	0.95	0.50	1.00	0.68	1.07	0.70	1.70	0.80	2.00	V

On-Chip Termination (OCT) Specifications

If you enable OCT calibration, calibration is automatically performed at power-up for I/Os connected to the calibration block. Table 11 lists the Stratix V OCT termination calibration accuracy specifications.

Table 11. OCT Calibration Accuracy Specifications for Stratix V Devices ⁽¹⁾ (Part 1 of 2)

Symbol	Description	Conditions	Calibration Accuracy				Unit
			C1	C2,I2	C3,I3, I3YY	C4,I4	
25- Ω R_S	Internal series termination with calibration (25- Ω setting)	$V_{\text{CCIO}} = 3.0, 2.5, 1.8, 1.5, 1.2 \text{ V}$	± 15	± 15	± 15	± 15	%

Table 11. OCT Calibration Accuracy Specifications for Stratix V Devices ⁽¹⁾ (Part 2 of 2)

Symbol	Description	Conditions	Calibration Accuracy				Unit
			C1	C2,I2	C3,I3, I3YY	C4,I4	
50-Ω R _S	Internal series termination with calibration (50-Ω setting)	V _{CCIO} = 3.0, 2.5, 1.8, 1.5, 1.2 V	±15	±15	±15	±15	%
34-Ω and 40-Ω R _S	Internal series termination with calibration (34-Ω and 40-Ω setting)	V _{CCIO} = 1.5, 1.35, 1.25, 1.2 V	±15	±15	±15	±15	%
48-Ω, 60-Ω, 80-Ω, and 240-Ω R _S	Internal series termination with calibration (48-Ω, 60-Ω, 80-Ω, and 240-Ω setting)	V _{CCIO} = 1.2 V	±15	±15	±15	±15	%
50-Ω R _T	Internal parallel termination with calibration (50-Ω setting)	V _{CCIO} = 2.5, 1.8, 1.5, 1.2 V	-10 to +40	-10 to +40	-10 to +40	-10 to +40	%
20-Ω, 30-Ω, 40-Ω, 60-Ω, and 120-Ω R _T	Internal parallel termination with calibration (20-Ω, 30-Ω, 40-Ω, 60-Ω, and 120-Ω setting)	V _{CCIO} = 1.5, 1.35, 1.25 V	-10 to +40	-10 to +40	-10 to +40	-10 to +40	%
60-Ω and 120-Ω R _T	Internal parallel termination with calibration (60-Ω and 120-Ω setting)	V _{CCIO} = 1.2	-10 to +40	-10 to +40	-10 to +40	-10 to +40	%
25-Ω R _{S_left_shift}	Internal left shift series termination with calibration (25-Ω R _{S_left_shift} setting)	V _{CCIO} = 3.0, 2.5, 1.8, 1.5, 1.2 V	±15	±15	±15	±15	%

Note to Table 11:

(1) OCT calibration accuracy is valid at the time of calibration only.

Table 12 lists the Stratix V OCT without calibration resistance tolerance to PVT changes.

Table 12. OCT Without Calibration Resistance Tolerance Specifications for Stratix V Devices (Part 1 of 2)

Symbol	Description	Conditions	Resistance Tolerance				Unit
			C1	C2,I2	C3, I3, I3YY	C4, I4	
25-Ω R, 50-Ω R _S	Internal series termination without calibration (25-Ω setting)	V _{CCIO} = 3.0 and 2.5 V	±30	±30	±40	±40	%
25-Ω R _S	Internal series termination without calibration (25-Ω setting)	V _{CCIO} = 1.8 and 1.5 V	±30	±30	±40	±40	%
25-Ω R _S	Internal series termination without calibration (25-Ω setting)	V _{CCIO} = 1.2 V	±35	±35	±50	±50	%

Table 13. OCT Variation after Power-Up Calibration for Stratix V Devices (Part 2 of 2) ⁽¹⁾

Symbol	Description	V _{CCIO} (V)	Typical	Unit
dR/dT	OCT variation with temperature without recalibration	3.0	0.189	%/ ^o C
		2.5	0.208	
		1.8	0.266	
		1.5	0.273	
		1.2	0.317	

Note to Table 13:

(1) Valid for a V_{CCIO} range of $\pm 5\%$ and a temperature range of 0° to 85°C.

Pin Capacitance

Table 14 lists the Stratix V device family pin capacitance.

Table 14. Pin Capacitance for Stratix V Devices

Symbol	Description	Value	Unit
C _{IOTB}	Input capacitance on the top and bottom I/O pins	6	pF
C _{IOLR}	Input capacitance on the left and right I/O pins	6	pF
C _{OUTFB}	Input capacitance on dual-purpose clock output and feedback pins	6	pF

Hot Socketing

Table 15 lists the hot socketing specifications for Stratix V devices.

Table 15. Hot Socketing Specifications for Stratix V Devices

Symbol	Description	Maximum
I _{IOPIN} (DC)	DC current per I/O pin	300 μ A
I _{IOPIN} (AC)	AC current per I/O pin	8 mA ⁽¹⁾
I _{XCVR-TX} (DC)	DC current per transceiver transmitter pin	100 mA
I _{XCVR-RX} (DC)	DC current per transceiver receiver pin	50 mA

Note to Table 15:

(1) The I/O ramp rate is 10 ns or more. For ramp rates faster than 10 ns, $|I_{IOPIN}| = C \, dv/dt$, in which C is the I/O pin capacitance and dv/dt is the slew rate.

Internal Weak Pull-Up Resistor

Table 16 lists the weak pull-up resistor values for Stratix V devices.

Table 16. Internal Weak Pull-Up Resistor for Stratix V Devices ^{(1), (2)}

Symbol	Description	V _{CCIO} Conditions (V) ⁽³⁾	Value ⁽⁴⁾	Unit
R _{PU}	Value of the I/O pin pull-up resistor before and during configuration, as well as user mode if you enable the programmable pull-up resistor option.	3.0 ±5%	25	kΩ
		2.5 ±5%	25	kΩ
		1.8 ±5%	25	kΩ
		1.5 ±5%	25	kΩ
		1.35 ±5%	25	kΩ
		1.25 ±5%	25	kΩ
		1.2 ±5%	25	kΩ

Notes to Table 16:

- (1) All I/O pins have an option to enable the weak pull-up resistor except the configuration, test, and JTAG pins.
- (2) The internal weak pull-down feature is only available for the JTAG TCK pin. The typical value for this internal weak pull-down resistor is approximately 25 kΩ.
- (3) The pin pull-up resistance values may be lower if an external source drives the pin higher than V_{CCIO}.
- (4) These specifications are valid with a ±10% tolerance to cover changes over PVT.

I/O Standard Specifications

Table 17 through Table 22 list the input voltage (V_{IH} and V_{IL}), output voltage (V_{OH} and V_{OL}), and current drive characteristics (I_{OH} and I_{OL}) for various I/O standards supported by Stratix V devices. These tables also show the Stratix V device family I/O standard specifications. The V_{OL} and V_{OH} values are valid at the corresponding I_{OH} and I_{OL}, respectively.

For an explanation of the terms used in Table 17 through Table 22, refer to “Glossary” on page 65. For tolerance calculations across all SSTL and HSTL I/O standards, refer to Altera knowledge base solution rd07262012_486.

Table 17. Single-Ended I/O Standards for Stratix V Devices

I/O Standard	V _{CCIO} (V)			V _{IL} (V)		V _{IH} (V)		V _{OL} (V)	V _{OH} (V)	I _{OL} (mA)	I _{OH} (mA)
	Min	Typ	Max	Min	Max	Min	Max	Max	Min		
LVTTTL	2.85	3	3.15	−0.3	0.8	1.7	3.6	0.4	2.4	2	−2
LVC MOS	2.85	3	3.15	−0.3	0.8	1.7	3.6	0.2	V _{CCIO} − 0.2	0.1	−0.1
2.5 V	2.375	2.5	2.625	−0.3	0.7	1.7	3.6	0.4	2	1	−1
1.8 V	1.71	1.8	1.89	−0.3	0.35 * V _{CCIO}	0.65 * V _{CCIO}	V _{CCIO} + 0.3	0.45	V _{CCIO} − 0.45	2	−2
1.5 V	1.425	1.5	1.575	−0.3	0.35 * V _{CCIO}	0.65 * V _{CCIO}	V _{CCIO} + 0.3	0.25 * V _{CCIO}	0.75 * V _{CCIO}	2	−2
1.2 V	1.14	1.2	1.26	−0.3	0.35 * V _{CCIO}	0.65 * V _{CCIO}	V _{CCIO} + 0.3	0.25 * V _{CCIO}	0.75 * V _{CCIO}	2	−2

Table 18. Single-Ended SSTL, HSTL, and HSUL I/O Reference Voltage Specifications for Stratix V Devices

I/O Standard	V_{CCIO} (V)			V_{REF} (V)			V_{TT} (V)		
	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max
SSTL-2 Class I, II	2.375	2.5	2.625	$0.49 * V_{CCIO}$	$0.5 * V_{CCIO}$	$0.51 * V_{CCIO}$	$V_{REF} - 0.04$	V_{REF}	$V_{REF} + 0.04$
SSTL-18 Class I, II	1.71	1.8	1.89	0.833	0.9	0.969	$V_{REF} - 0.04$	V_{REF}	$V_{REF} + 0.04$
SSTL-15 Class I, II	1.425	1.5	1.575	$0.49 * V_{CCIO}$	$0.5 * V_{CCIO}$	$0.51 * V_{CCIO}$	$0.49 * V_{CCIO}$	$0.5 * V_{CCIO}$	$0.51 * V_{CCIO}$
SSTL-135 Class I, II	1.283	1.35	1.418	$0.49 * V_{CCIO}$	$0.5 * V_{CCIO}$	$0.51 * V_{CCIO}$	$0.49 * V_{CCIO}$	$0.5 * V_{CCIO}$	$0.51 * V_{CCIO}$
SSTL-125 Class I, II	1.19	1.25	1.26	$0.49 * V_{CCIO}$	$0.5 * V_{CCIO}$	$0.51 * V_{CCIO}$	$0.49 * V_{CCIO}$	$0.5 * V_{CCIO}$	$0.51 * V_{CCIO}$
SSTL-12 Class I, II	1.14	1.20	1.26	$0.49 * V_{CCIO}$	$0.5 * V_{CCIO}$	$0.51 * V_{CCIO}$	$0.49 * V_{CCIO}$	$0.5 * V_{CCIO}$	$0.51 * V_{CCIO}$
HSTL-18 Class I, II	1.71	1.8	1.89	0.85	0.9	0.95	—	$V_{CCIO}/2$	—
HSTL-15 Class I, II	1.425	1.5	1.575	0.68	0.75	0.9	—	$V_{CCIO}/2$	—
HSTL-12 Class I, II	1.14	1.2	1.26	$0.47 * V_{CCIO}$	$0.5 * V_{CCIO}$	$0.53 * V_{CCIO}$	—	$V_{CCIO}/2$	—
HSUL-12	1.14	1.2	1.3	$0.49 * V_{CCIO}$	$0.5 * V_{CCIO}$	$0.51 * V_{CCIO}$	—	—	—

Table 19. Single-Ended SSTL, HSTL, and HSUL I/O Standards Signal Specifications for Stratix V Devices (Part 1 of 2)

I/O Standard	$V_{IL(DC)}$ (V)		$V_{IH(DC)}$ (V)		$V_{IL(AC)}$ (V)	$V_{IH(AC)}$ (V)	V_{OL} (V)	V_{OH} (V)	I_{OI} (mA)	I_{OH} (mA)
	Min	Max	Min	Max	Max	Min	Max	Min		
SSTL-2 Class I	-0.3	$V_{REF} - 0.15$	$V_{REF} + 0.15$	$V_{CCIO} + 0.3$	$V_{REF} - 0.31$	$V_{REF} + 0.31$	$V_{TT} - 0.608$	$V_{TT} + 0.608$	8.1	-8.1
SSTL-2 Class II	-0.3	$V_{REF} - 0.15$	$V_{REF} + 0.15$	$V_{CCIO} + 0.3$	$V_{REF} - 0.31$	$V_{REF} + 0.31$	$V_{TT} - 0.81$	$V_{TT} + 0.81$	16.2	-16.2
SSTL-18 Class I	-0.3	$V_{REF} - 0.125$	$V_{REF} + 0.125$	$V_{CCIO} + 0.3$	$V_{REF} - 0.25$	$V_{REF} + 0.25$	$V_{TT} - 0.603$	$V_{TT} + 0.603$	6.7	-6.7
SSTL-18 Class II	-0.3	$V_{REF} - 0.125$	$V_{REF} + 0.125$	$V_{CCIO} + 0.3$	$V_{REF} - 0.25$	$V_{REF} + 0.25$	0.28	$V_{CCIO} - 0.28$	13.4	-13.4
SSTL-15 Class I	—	$V_{REF} - 0.1$	$V_{REF} + 0.1$	—	$V_{REF} - 0.175$	$V_{REF} + 0.175$	$0.2 * V_{CCIO}$	$0.8 * V_{CCIO}$	8	-8
SSTL-15 Class II	—	$V_{REF} - 0.1$	$V_{REF} + 0.1$	—	$V_{REF} - 0.175$	$V_{REF} + 0.175$	$0.2 * V_{CCIO}$	$0.8 * V_{CCIO}$	16	-16
SSTL-135 Class I, II	—	$V_{REF} - 0.09$	$V_{REF} + 0.09$	—	$V_{REF} - 0.16$	$V_{REF} + 0.16$	$0.2 * V_{CCIO}$	$0.8 * V_{CCIO}$	—	—
SSTL-125 Class I, II	—	$V_{REF} - 0.85$	$V_{REF} + 0.85$	—	$V_{REF} - 0.15$	$V_{REF} + 0.15$	$0.2 * V_{CCIO}$	$0.8 * V_{CCIO}$	—	—
SSTL-12 Class I, II	—	$V_{REF} - 0.1$	$V_{REF} + 0.1$	—	$V_{REF} - 0.15$	$V_{REF} + 0.15$	$0.2 * V_{CCIO}$	$0.8 * V_{CCIO}$	—	—

Switching Characteristics

This section provides performance characteristics of the Stratix V core and periphery blocks.

These characteristics can be designated as Preliminary or Final.

- Preliminary characteristics are created using simulation results, process data, and other known parameters. The title of these tables show the designation as “Preliminary.”
- Final numbers are based on actual silicon characterization and testing. The numbers reflect the actual performance of the device under worst-case silicon process, voltage, and junction temperature conditions. There are no designations on finalized tables.

Transceiver Performance Specifications

This section describes transceiver performance specifications.

Table 23 lists the Stratix V GX and GS transceiver specifications.

Table 23. Transceiver Specifications for Stratix V GX and GS Devices ⁽¹⁾ (Part 1 of 7)

Symbol/ Description	Conditions	Transceiver Speed Grade 1			Transceiver Speed Grade 2			Transceiver Speed Grade 3			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Reference Clock											
Supported I/O Standards	Dedicated reference clock pin	1.2-V PCML, 1.4-V PCML, 1.5-V PCML, 2.5-V PCML, Differential LVPECL, LVDS, and HCSL									
	RX reference clock pin	1.4-V PCML, 1.5-V PCML, 2.5-V PCML, LVPECL, and LVDS									
Input Reference Clock Frequency (CMU PLL) ⁽⁸⁾	—	40	—	710	40	—	710	40	—	710	MHz
Input Reference Clock Frequency (ATX PLL) ⁽⁸⁾	—	100	—	710	100	—	710	100	—	710	MHz
Rise time	Measure at ±60 mV of differential signal ⁽²⁶⁾	—	—	400	—	—	400	—	—	400	ps
Fall time	Measure at ±60 mV of differential signal ⁽²⁶⁾	—	—	400	—	—	400	—	—	400	
Duty cycle	—	45	—	55	45	—	55	45	—	55	%
Spread-spectrum modulating clock frequency	PCI Express® (PCIe®)	30	—	33	30	—	33	30	—	33	kHz

Table 23. Transceiver Specifications for Stratix V GX and GS Devices ⁽¹⁾ (Part 4 of 7)

Symbol/ Description	Conditions	Transceiver Speed Grade 1			Transceiver Speed Grade 2			Transceiver Speed Grade 3			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Differential on-chip termination resistors ⁽²¹⁾	85- Ω setting	—	85 \pm 30%	—	—	85 \pm 30%	—	—	85 \pm 30%	—	Ω
	100- Ω setting	—	100 \pm 30%	—	—	100 \pm 30%	—	—	100 \pm 30%	—	Ω
	120- Ω setting	—	120 \pm 30%	—	—	120 \pm 30%	—	—	120 \pm 30%	—	Ω
	150- Ω setting	—	150 \pm 30%	—	—	150 \pm 30%	—	—	150 \pm 30%	—	Ω
V_{ICM} (AC and DC coupled)	$V_{CCR_GXB} = 0.85\text{ V}$ or 0.9 V full bandwidth	—	600	—	—	600	—	—	600	—	mV
	$V_{CCR_GXB} = 0.85\text{ V}$ or 0.9 V half bandwidth	—	600	—	—	600	—	—	600	—	mV
	$V_{CCR_GXB} = 1.0\text{ V}/1.05\text{ V}$ full bandwidth	—	700	—	—	700	—	—	700	—	mV
	$V_{CCR_GXB} = 1.0\text{ V}$ half bandwidth	—	750	—	—	750	—	—	750	—	mV
t_{LTR} ⁽¹¹⁾	—	—	—	10	—	—	10	—	—	10	μs
t_{LTD} ⁽¹²⁾	—	4	—	—	4	—	—	4	—	—	μs
t_{LTD_manual} ⁽¹³⁾	—	4	—	—	4	—	—	4	—	—	μs
$t_{LTR_LTD_manual}$ ⁽¹⁴⁾	—	15	—	—	15	—	—	15	—	—	μs
Run Length	—	—	—	200	—	—	200	—	—	200	UI
Programmable equalization (AC Gain) ⁽¹⁰⁾	Full bandwidth (6.25 GHz) Half bandwidth (3.125 GHz)	—	—	16	—	—	16	—	—	16	dB

Table 23. Transceiver Specifications for Stratix V GX and GS Devices ⁽¹⁾ (Part 6 of 7)

Symbol/ Description	Conditions	Transceiver Speed Grade 1			Transceiver Speed Grade 2			Transceiver Speed Grade 3			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Inter-transceiver block transmitter channel-to- channel skew	xN PMA bonded mode	—	—	500	—	—	500	—	—	500	ps
CMU PLL											
Supported Data Range	—	600	—	12500	600	—	12500	600	—	8500/ 10312.5 (24)	Mbps
$t_{\text{pll_powerdown}}$ ⁽¹⁵⁾	—	1	—	—	1	—	—	1	—	—	μs
$t_{\text{pll_lock}}$ ⁽¹⁶⁾	—	—	—	10	—	—	10	—	—	10	μs
ATX PLL											
Supported Data Rate Range	VCO post-divider L=2	8000	—	14100	8000	—	12500	8000	—	8500/ 10312.5 (24)	Mbps
	L=4	4000	—	7050	4000	—	6600	4000	—	6600	Mbps
	L=8	2000	—	3525	2000	—	3300	2000	—	3300	Mbps
	L=8, Local/Central Clock Divider =2	1000	—	1762.5	1000	—	1762.5	1000	—	1762.5	Mbps
$t_{\text{pll_powerdown}}$ ⁽¹⁵⁾	—	1	—	—	1	—	—	1	—	—	μs
$t_{\text{pll_lock}}$ ⁽¹⁶⁾	—	—	—	10	—	—	10	—	—	10	μs
fPLL											
Supported Data Range	—	600	—	3250/ 3125 ⁽²⁵⁾	600	—	3250/ 3125 ⁽²⁵⁾	600	—	3250/ 3125 ⁽²⁵⁾	Mbps
$t_{\text{pll_powerdown}}$ ⁽¹⁵⁾	—	1	—	—	1	—	—	1	—	—	μs

Table 23. Transceiver Specifications for Stratix V GX and GS Devices ⁽¹⁾ (Part 7 of 7)

Symbol/ Description	Conditions	Transceiver Speed Grade 1			Transceiver Speed Grade 2			Transceiver Speed Grade 3			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
$t_{pll_lock}^{(16)}$	—	—	—	10	—	—	10	—	—	10	μs

Notes to Table 23:

- (1) Speed grades shown in Table 23 refer to the PMA Speed Grade in the device ordering code. The maximum data rate could be restricted by the Core/PCS speed grade. Contact your Altera Sales Representative for the maximum data rate specifications in each speed grade combination offered. For more information about device ordering codes, refer to the *Stratix V Device Overview*.
- (2) The reference clock common mode voltage is equal to the V_{CCR_GXB} power supply level.
- (3) This supply must be connected to 1.0 V if the transceiver is configured at a data rate > 6.5 Gbps, and to 1.05 V if configured at a data rate > 10.3 Gbps when DFE is used. For data rates up to 6.5 Gbps, you can connect this supply to 0.85 V.
- (4) This supply follows V_{CCR_GXB} .
- (5) The device cannot tolerate prolonged operation at this absolute maximum.
- (6) The differential eye opening specification at the receiver input pins assumes that **Receiver Equalization** is disabled. If you enable **Receiver Equalization**, the receiver circuitry can tolerate a lower minimum eye opening, depending on the equalization level.
- (7) The Quartus II software automatically selects the appropriate slew rate depending on the configured data rate or functional mode.
- (8) The input reference clock frequency options depend on the data rate and the device speed grade.
- (9) The line data rate may be limited by PCS-FPGA interface speed grade.
- (10) Refer to Figure 1 for the GX channel AC gain curves. The total effective AC gain is the AC gain minus the DC gain.
- (11) t_{LTR} is the time required for the receive CDR to lock to the input reference clock frequency after coming out of reset.
- (12) t_{LTD} is time required for the receiver CDR to start recovering valid data after the rx_is_lockedtodata signal goes high.
- (13) t_{LTD_manual} is the time required for the receiver CDR to start recovering valid data after the rx_is_lockedtodata signal goes high when the CDR is functioning in the manual mode.
- (14) $t_{LTR_LTD_manual}$ is the time the receiver CDR must be kept in lock to reference (LTR) mode after the rx_is_lockedtoref signal goes high when the CDR is functioning in the manual mode.
- (15) $t_{pll_powerdown}$ is the PLL powerdown minimum pulse width.
- (16) t_{pll_lock} is the time required for the transmitter CMU/ATX PLL to lock to the input reference clock frequency after coming out of reset.
- (17) To calculate the REFCLK rms phase jitter requirement for PCIe at reference clock frequencies other than 100 MHz, use the following formula: REFCLK rms phase jitter at f(MHz) = REFCLK rms phase jitter at 100 MHz \times 100/f.
- (18) The maximum peak to peak differential input voltage V_{ID} after device configuration is equal to $4 \times (\text{absolute } V_{MAX} \text{ for receiver pin} - V_{ICM})$.
- (19) For ES devices, R_{REF} is $2000 \Omega \pm 1\%$.
- (20) To calculate the REFCLK phase noise requirement at frequencies other than 622 MHz, use the following formula: REFCLK phase noise at f(MHz) = REFCLK phase noise at 622 MHz + $20 \times \log(f/622)$.
- (21) SFP/+ optical modules require the host interface to have RD+/- differentially terminated with 100Ω . The internal OCT feature is available after the Stratix V FPGA configuration is completed. Altera recommends that FPGA configuration is completed before inserting the optical module. Otherwise, minimize unnecessary removal and insertion with unconfigured devices.
- (22) Refer to Figure 2.
- (23) For oversampling designs to support data rates less than the minimum specification, the CDR needs to be in LTR mode only.
- (24) I3YY devices can achieve data rates up to 10.3125 Gbps.
- (25) When you use fPLL as a TXPLL of the transceiver.
- (26) REFCLK performance requires to meet transmitter REFCLK phase noise specification.
- (27) Minimum eye opening of 85 mV is only for the unstressed input eye condition.

Table 25 shows the approximate maximum data rate using the standard PCS.

Table 25. Stratix V Standard PCS Approximate Maximum Date Rate ⁽¹⁾, ⁽³⁾

Mode ⁽²⁾	Transceiver Speed Grade	PMA Width	20	20	16	16	10	10	8	8
		PCS/Core Width	40	20	32	16	20	10	16	8
FIFO	1	C1, C2, C2L, I2, I2L core speed grade	12.2	11.4	9.76	9.12	6.5	5.8	5.2	4.72
	2	C1, C2, C2L, I2, I2L core speed grade	12.2	11.4	9.76	9.12	6.5	5.8	5.2	4.72
		C3, I3, I3L core speed grade	9.8	9.0	7.84	7.2	5.3	4.7	4.24	3.76
	3	C1, C2, C2L, I2, I2L core speed grade	8.5	8.5	8.5	8.5	6.5	5.8	5.2	4.72
		I3YY core speed grade	10.3125	10.3125	7.84	7.2	5.3	4.7	4.24	3.76
		C3, I3, I3L core speed grade	8.5	8.5	7.84	7.2	5.3	4.7	4.24	3.76
		C4, I4 core speed grade	8.5	8.2	7.04	6.56	4.8	4.2	3.84	3.44
Register	1	C1, C2, C2L, I2, I2L core speed grade	12.2	11.4	9.76	9.12	6.1	5.7	4.88	4.56
	2	C1, C2, C2L, I2, I2L core speed grade	12.2	11.4	9.76	9.12	6.1	5.7	4.88	4.56
		C3, I3, I3L core speed grade	9.8	9.0	7.92	7.2	4.9	4.5	3.96	3.6
	3	C1, C2, C2L, I2, I2L core speed grade	10.3125	10.3125	10.3125	10.3125	6.1	5.7	4.88	4.56
		I3YY core speed grade	10.3125	10.3125	7.92	7.2	4.9	4.5	3.96	3.6
		C3, I3, I3L core speed grade	8.5	8.5	7.92	7.2	4.9	4.5	3.96	3.6
		C4, I4 core speed grade	8.5	8.2	7.04	6.56	4.4	4.1	3.52	3.28

Notes to Table 25:

- (1) The maximum data rate is in Gbps.
- (2) The Phase Compensation FIFO can be configured in FIFO mode or register mode. In the FIFO mode, the pointers are not fixed, and the latency can vary. In the register mode the pointers are fixed for low latency.
- (3) The maximum data rate is also constrained by the transceiver speed grade. Refer to Table 1 for the transceiver speed grade.

Figure 2 shows the differential transmitter output waveform.

Figure 2. Differential Transmitter Output Waveform

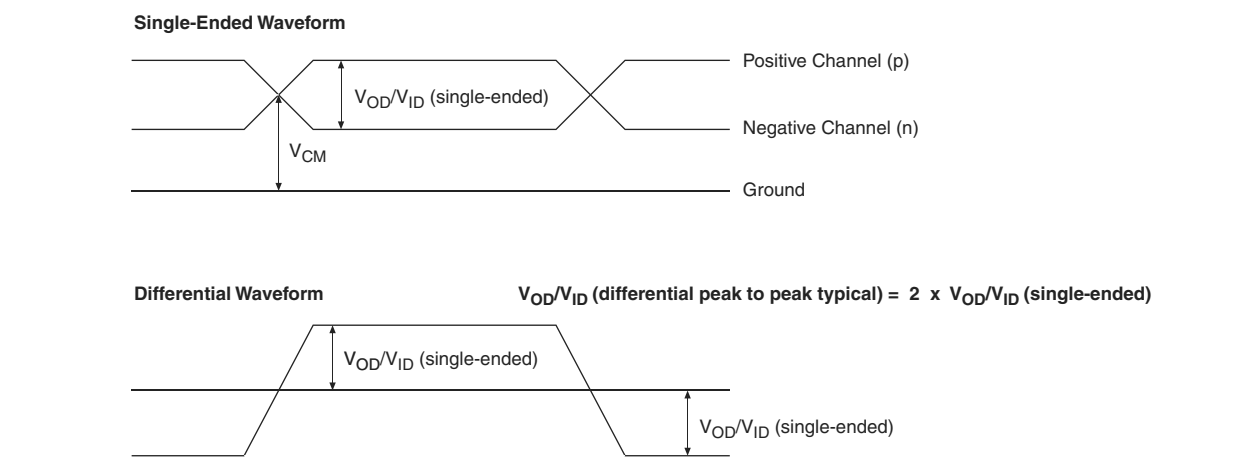


Figure 3 shows the Stratix V AC gain curves for GX channels.

Figure 3. AC Gain Curves for GX Channels (full bandwidth)



Stratix V GT devices contain both GX and GT channels. All transceiver specifications for the GX channels not listed in Table 28 are the same as those listed in Table 23.

Table 28 lists the Stratix V GT transceiver specifications.

Table 28. Transceiver Specifications for Stratix V GT Devices (Part 4 of 5) ⁽¹⁾

Symbol/ Description	Conditions	Transceiver Speed Grade 2			Transceiver Speed Grade 3			Unit
		Min	Typ	Max	Min	Typ	Max	
Data rate	GT channels	19,600	—	28,050	19,600	—	25,780	Mbps
Differential on-chip termination resistors	GT channels	—	100	—	—	100	—	Ω
	GX channels	(8)						
V _{OCM} (AC coupled)	GT channels	—	500	—	—	500	—	mV
	GX channels	(8)						
Rise/Fall time	GT channels	—	15	—	—	15	—	ps
	GX channels	(8)						
Intra-differential pair skew	GX channels	(8)						
Intra-transceiver block transmitter channel-to- channel skew	GX channels	(8)						
Inter-transceiver block transmitter channel-to- channel skew	GX channels	(8)						
CMU PLL								
Supported Data Range	—	600	—	12500	600	—	8500	Mbps
t _{pll_powerdown} ⁽¹³⁾	—	1	—	—	1	—	—	μs
t _{pll_lock} ⁽¹⁴⁾	—	—	—	10	—	—	10	μs
ATX PLL								
Supported Data Rate Range for GX Channels	VCO post- divider L=2	8000	—	12500	8000	—	8500	Mbps
	L=4	4000	—	6600	4000	—	6600	Mbps
	L=8	2000	—	3300	2000	—	3300	Mbps
	L=8, Local/Central Clock Divider =2	1000	—	1762.5	1000	—	1762.5	Mbps
Supported Data Rate Range for GT Channels	VCO post- divider L=2	9800	—	14025	9800	—	12890	Mbps
t _{pll_powerdown} ⁽¹³⁾	—	1	—	—	1	—	—	μs
t _{pll_lock} ⁽¹⁴⁾	—	—	—	10	—	—	10	μs
fPLL								
Supported Data Range	—	600	—	3250/ 3.125 ⁽²³⁾	600	—	3250/ 3.125 ⁽²³⁾	Mbps
t _{pll_powerdown} ⁽¹³⁾	—	1	—	—	1	—	—	μs

Figure 6 shows the Stratix V DC gain curves for GT channels.

Figure 6. DC Gain Curves for GT Channels

Transceiver Characterization

This section summarizes the Stratix V transceiver characterization results for compliance with the following protocols:

- Interlaken
- 40G (XLAUI)/100G (CAUI)
- 10GBase-KR
- QSGMII
- XAUI
- SFI
- Gigabit Ethernet (Gbe / GIGE)
- SPAUI
- Serial Rapid IO (SRIO)
- CPRI
- OBSAI
- Hyper Transport (HT)
- SATA
- SAS
- CEI

- XFI
- ASI
- HiGig/HiGig+
- HiGig2/HiGig2+
- Serial Data Converter (SDC)
- GPON
- SDI
- SONET
- Fibre Channel (FC)
- PCIe
- QPI
- SFF-8431

Download the Stratix V Characterization Report Tool to view the characterization report summary for these protocols.

Core Performance Specifications

This section describes the clock tree, phase-locked loop (PLL), digital signal processing (DSP), memory blocks, configuration, and JTAG specifications.

Clock Tree Specifications

Table 30 lists the clock tree specifications for Stratix V devices.

Table 30. Clock Tree Performance for Stratix V Devices ⁽¹⁾

Symbol	Performance			Unit
	C1, C2, C2L, I2, and I2L	C3, I3, I3L, and I3YY	C4, I4	
Global and Regional Clock	717	650	580	MHz
Periphery Clock	550	500	500	MHz

Note to Table 30:

(1) The Stratix V ES devices are limited to 600 MHz core clock tree performance.

Table 31. PLL Specifications for Stratix V Devices (Part 2 of 3)

Symbol	Parameter	Min	Typ	Max	Unit
t_{INCCJ} ^{(3), (4)}	Input clock cycle-to-cycle jitter ($f_{\text{REF}} \geq 100$ MHz)	—	—	0.15	UI (p-p)
	Input clock cycle-to-cycle jitter ($f_{\text{REF}} < 100$ MHz)	−750	—	+750	ps (p-p)
$t_{\text{OUTPJ_DC}}$ ⁽⁵⁾	Period Jitter for dedicated clock output ($f_{\text{OUT}} \geq 100$ MHz)	—	—	175 ⁽¹⁾	ps (p-p)
	Period Jitter for dedicated clock output ($f_{\text{OUT}} < 100$ MHz)	—	—	17.5 ⁽¹⁾	mUI (p-p)
$t_{\text{FOUTPJ_DC}}$ ⁽⁵⁾	Period Jitter for dedicated clock output in fractional PLL ($f_{\text{OUT}} \geq 100$ MHz)	—	—	250 ⁽¹¹⁾ , 175 ⁽¹²⁾	ps (p-p)
	Period Jitter for dedicated clock output in fractional PLL ($f_{\text{OUT}} < 100$ MHz)	—	—	25 ⁽¹¹⁾ , 17.5 ⁽¹²⁾	mUI (p-p)
$t_{\text{OUTCCJ_DC}}$ ⁽⁵⁾	Cycle-to-Cycle Jitter for a dedicated clock output ($f_{\text{OUT}} \geq 100$ MHz)	—	—	175	ps (p-p)
	Cycle-to-Cycle Jitter for a dedicated clock output ($f_{\text{OUT}} < 100$ MHz)	—	—	17.5	mUI (p-p)
$t_{\text{FOUTCCJ_DC}}$ ⁽⁵⁾	Cycle-to-cycle Jitter for a dedicated clock output in fractional PLL ($f_{\text{OUT}} \geq 100$ MHz)	—	—	250 ⁽¹¹⁾ , 175 ⁽¹²⁾	ps (p-p)
	Cycle-to-cycle Jitter for a dedicated clock output in fractional PLL ($f_{\text{OUT}} < 100$ MHz)+	—	—	25 ⁽¹¹⁾ , 17.5 ⁽¹²⁾	mUI (p-p)
$t_{\text{OUTPJ_IO}}$ ^{(5), (8)}	Period Jitter for a clock output on a regular I/O in integer PLL ($f_{\text{OUT}} \geq 100$ MHz)	—	—	600	ps (p-p)
	Period Jitter for a clock output on a regular I/O ($f_{\text{OUT}} < 100$ MHz)	—	—	60	mUI (p-p)
$t_{\text{FOUTPJ_IO}}$ ^{(5), (8), (11)}	Period Jitter for a clock output on a regular I/O in fractional PLL ($f_{\text{OUT}} \geq 100$ MHz)	—	—	600 ⁽¹⁰⁾	ps (p-p)
	Period Jitter for a clock output on a regular I/O in fractional PLL ($f_{\text{OUT}} < 100$ MHz)	—	—	60 ⁽¹⁰⁾	mUI (p-p)
$t_{\text{OUTCCJ_IO}}$ ^{(5), (8)}	Cycle-to-cycle Jitter for a clock output on a regular I/O in integer PLL ($f_{\text{OUT}} \geq 100$ MHz)	—	—	600	ps (p-p)
	Cycle-to-cycle Jitter for a clock output on a regular I/O in integer PLL ($f_{\text{OUT}} < 100$ MHz)	—	—	60 ⁽¹⁰⁾	mUI (p-p)
$t_{\text{FOUTCCJ_IO}}$ ^{(5), (8), (11)}	Cycle-to-cycle Jitter for a clock output on a regular I/O in fractional PLL ($f_{\text{OUT}} \geq 100$ MHz)	—	—	600 ⁽¹⁰⁾	ps (p-p)
	Cycle-to-cycle Jitter for a clock output on a regular I/O in fractional PLL ($f_{\text{OUT}} < 100$ MHz)	—	—	60	mUI (p-p)
$t_{\text{CASC_OUTPJ_DC}}$ ^{(5), (6)}	Period Jitter for a dedicated clock output in cascaded PLLs ($f_{\text{OUT}} \geq 100$ MHz)	—	—	175	ps (p-p)
	Period Jitter for a dedicated clock output in cascaded PLLs ($f_{\text{OUT}} < 100$ MHz)	—	—	17.5	mUI (p-p)
f_{DRIFT}	Frequency drift after PFDENA is disabled for a duration of 100 μ s	—	—	± 10	%
dK_{BIT}	Bit number of Delta Sigma Modulator (DSM)	8	24	32	Bits
K_{VALUE}	Numerator of Fraction	128	8388608	2147483648	—

Table 31. PLL Specifications for Stratix V Devices (Part 3 of 3)

Symbol	Parameter	Min	Typ	Max	Unit
f_{RES}	Resolution of VCO frequency ($f_{INPFD} = 100$ MHz)	390625	5.96	0.023	Hz

Notes to Table 31:

- (1) This specification is limited in the Quartus II software by the I/O maximum frequency. The maximum I/O frequency is different for each I/O standard.
- (2) This specification is limited by the lower of the two: I/O f_{MAX} or f_{OUT} of the PLL.
- (3) A high input jitter directly affects the PLL output jitter. To have low PLL output clock jitter, you must provide a clean clock source < 120 ps.
- (4) f_{REF} is f_{IN}/N when $N = 1$.
- (5) Peak-to-peak jitter with a probability level of 10^{-12} (14 sigma, 99.9999999974404% confidence level). The output jitter specification applies to the intrinsic jitter of the PLL, when an input jitter of 30 ps is applied. The external memory interface clock output jitter specifications use a different measurement method and are available in Table 44 on page 52.
- (6) The cascaded PLL specification is only applicable with the following condition:
 - a. Upstream PLL: $0.59\text{MHz} \leq \text{Upstream PLL BW} < 1$ MHz
 - b. Downstream PLL: Downstream PLL BW > 2 MHz
- (7) High bandwidth PLL settings are not supported in external feedback mode.
- (8) The external memory interface clock output jitter specifications use a different measurement method, which is available in Table 42 on page 50.
- (9) The VCO frequency reported by the Quartus II software in the PLL Usage Summary section of the compilation report takes into consideration the VCO post-scale counter K value. Therefore, if the counter K has a value of 2, the frequency reported can be lower than the f_{VCO} specification.
- (10) This specification only covers fractional PLL for low bandwidth. The f_{VCO} for fractional value range 0.05 - 0.95 must be ≥ 1000 MHz, while f_{VCO} for fractional value range 0.20 - 0.80 must be ≥ 1200 MHz.
- (11) This specification only covered fractional PLL for low bandwidth. The f_{VCO} for fractional value range 0.05-0.95 must be ≥ 1000 MHz.
- (12) This specification only covered fractional PLL for low bandwidth. The f_{VCO} for fractional value range 0.20-0.80 must be ≥ 1200 MHz.

DSP Block Specifications

Table 32 lists the Stratix V DSP block performance specifications.

Table 32. Block Performance Specifications for Stratix V DSP Devices (Part 1 of 2)

Mode	Peformance							Unit
	C1	C2, C2L	I2, I2L	C3	I3, I3L, I3YY	C4	I4	
Modes using one DSP								
Three 9 x 9	600	600	600	480	480	420	420	MHz
One 18 x 18	600	600	600	480	480	420	400	MHz
Two partial 18 x 18 (or 16 x 16)	600	600	600	480	480	420	400	MHz
One 27 x 27	500	500	500	400	400	350	350	MHz
One 36 x 18	500	500	500	400	400	350	350	MHz
One sum of two 18 x 18(One sum of 2 16 x 16)	500	500	500	400	400	350	350	MHz
One sum of square	500	500	500	400	400	350	350	MHz
One 18 x 18 plus 36 (a x b) + c	500	500	500	400	400	350	350	MHz
Modes using two DSPs								
Three 18 x 18	500	500	500	400	400	350	350	MHz
One sum of four 18 x 18	475	475	475	380	380	300	300	MHz
One sum of two 27 x 27	465	465	450	380	380	300	290	MHz
One sum of two 36 x 18	475	475	475	380	380	300	300	MHz
One complex 18 x 18	500	500	500	400	400	350	350	MHz
One 36 x 36	475	475	475	380	380	300	300	MHz

Figure 7 shows the dynamic phase alignment (DPA) lock time specifications with the DPA PLL calibration option enabled.

Figure 7. DPA Lock Time Specification with DPA PLL Calibration Enabled

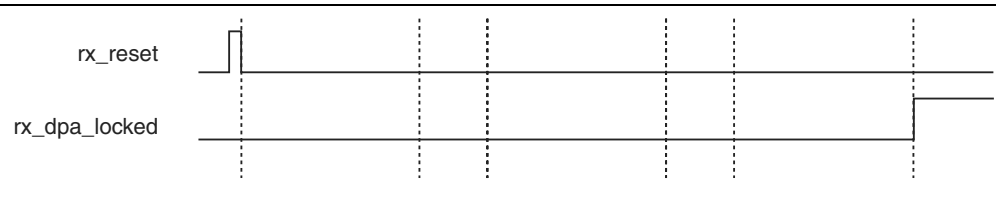


Table 37 lists the DPA lock time specifications for Stratix V devices.

Table 37. DPA Lock Time Specifications for Stratix V GX Devices Only ^{(1), (2), (3)}

Standard	Training Pattern	Number of Data Transitions in One Repetition of the Training Pattern	Number of Repetitions per 256 Data Transitions ⁽⁴⁾	Maximum
SPI-4	00000000001111111111	2	128	640 data transitions
Parallel Rapid I/O	00001111	2	128	640 data transitions
	10010000	4	64	640 data transitions
Miscellaneous	10101010	8	32	640 data transitions
	01010101	8	32	640 data transitions

Notes to Table 37:

- (1) The DPA lock time is for one channel.
- (2) One data transition is defined as a 0-to-1 or 1-to-0 transition.
- (3) The DPA lock time stated in this table applies to both commercial and industrial grade.
- (4) This is the number of repetitions for the stated training pattern to achieve the 256 data transitions.

Figure 8 shows the LVDS soft-clock data recovery (CDR)/DPA sinusoidal jitter tolerance specification for a data rate ≥ 1.25 Gbps. Table 38 lists the LVDS soft-CDR/DPA sinusoidal jitter tolerance specification for a data rate ≥ 1.25 Gbps.

Figure 8. LVDS Soft-CDR/DPA Sinusoidal Jitter Tolerance Specification for a Data Rate ≥ 1.25 Gbps

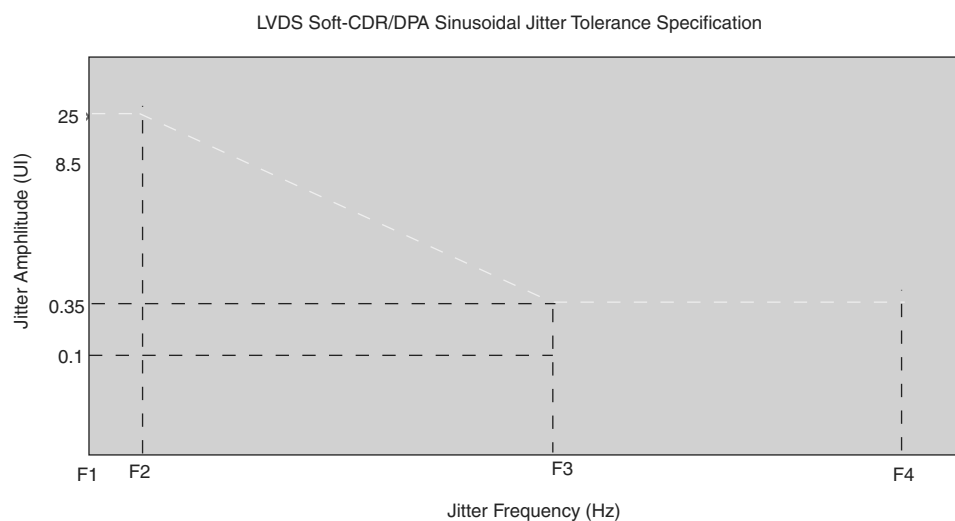


Table 42. Memory Output Clock Jitter Specification for Stratix V Devices ⁽¹⁾, (Part 2 of 2) ⁽²⁾, ⁽³⁾

Clock Network	Parameter	Symbol	C1		C2, C2L, I2, I2L		C3, I3, I3L, I3YY		C4,I4		Unit
			Min	Max	Min	Max	Min	Max	Min	Max	
PHY Clock	Clock period jitter	$t_{JIT(per)}$	-25	25	-25	25	-30	30	-35	35	ps
	Cycle-to-cycle period jitter	$t_{JIT(cc)}$	-50	50	-50	50	-60	60	-70	70	ps
	Duty cycle jitter	$t_{JIT(duty)}$	-37.5	37.5	-37.5	37.5	-45	45	-56	56	ps

Notes to Table 42:

- (1) The clock jitter specification applies to the memory output clock pins generated using differential signal-splitter and DDIO circuits clocked by a PLL output routed on a PHY, regional, or global clock network as specified. Altera recommends using PHY clock networks whenever possible.
- (2) The clock jitter specification applies to the memory output clock pins clocked by an integer PLL.
- (3) The memory output clock jitter is applicable when an input jitter of 30 ps peak-to-peak is applied with bit error rate (BER) -12, equivalent to 14 sigma.

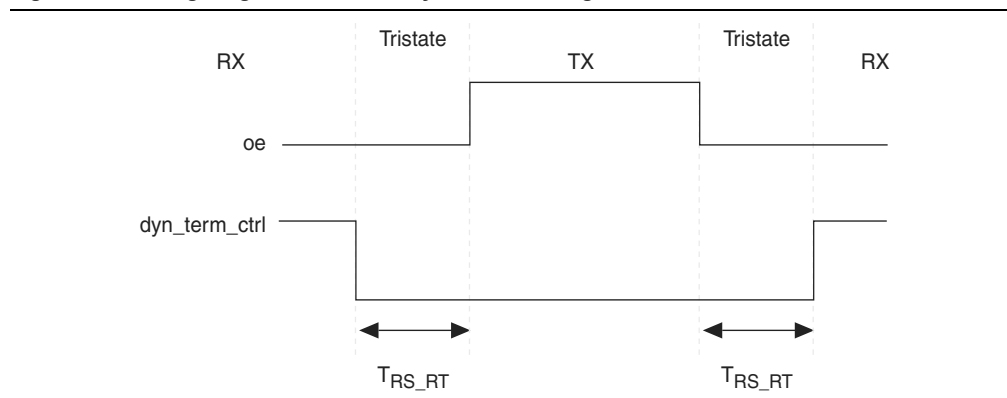
OCT Calibration Block Specifications

Table 43 lists the OCT calibration block specifications for Stratix V devices.

Table 43. OCT Calibration Block Specifications for Stratix V Devices

Symbol	Description	Min	Typ	Max	Unit
OCTUSRCLK	Clock required by the OCT calibration blocks	—	—	20	MHz
T_{OCTCAL}	Number of OCTUSRCLK clock cycles required for OCT R_S/R_T calibration	—	1000	—	Cycles
$T_{OCTSHIFT}$	Number of OCTUSRCLK clock cycles required for the OCT code to shift out	—	32	—	Cycles
T_{RS_RT}	Time required between the <code>dyn_term_ctrl</code> and <code>oe</code> signal transitions in a bidirectional I/O buffer to dynamically switch between OCT R_S and R_T (Figure 10)	—	2.5	—	ns

Figure 10 shows the timing diagram for the `oe` and `dyn_term_ctrl` signals.

Figure 10. Timing Diagram for `oe` and `dyn_term_ctrl` Signals

Duty Cycle Distortion (DCD) Specifications

Table 44 lists the worst-case DCD for Stratix V devices.

Table 44. Worst-Case DCD on Stratix V I/O Pins ⁽¹⁾

Symbol	C1		C2, C2L, I2, I2L		C3, I3, I3L, I3YY		C4, I4		Unit
	Min	Max	Min	Max	Min	Max	Min	Max	
Output Duty Cycle	45	55	45	55	45	55	45	55	%

Note to Table 44:

(1) The DCD numbers do not cover the core clock network.

Configuration Specification

POR Delay Specification

Power-on reset (POR) delay is defined as the delay between the time when all the power supplies monitored by the POR circuitry reach the minimum recommended operating voltage to the time when the nSTATUS is released high and your device is ready to begin configuration.



For more information about the POR delay, refer to the *Hot Socketing and Power-On Reset in Stratix V Devices* chapter.

Table 45 lists the fast and standard POR delay specification.

Table 45. Fast and Standard POR Delay Specification ⁽¹⁾

POR Delay	Minimum	Maximum
Fast	4 ms	12 ms
Standard	100 ms	300 ms

Note to Table 45:

(1) You can select the POR delay based on the MSEL settings as described in the MSEL Pin Settings section of the “Configuration, Design Security, and Remote System Upgrades in Stratix V Devices” chapter.

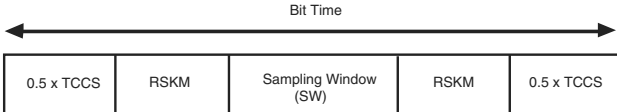
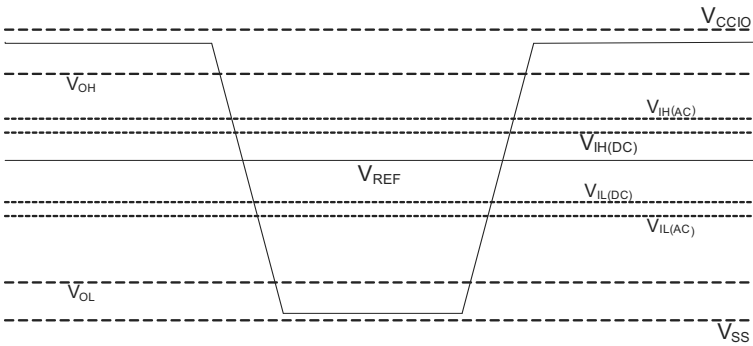
JTAG Configuration Specifications

Table 46 lists the JTAG timing parameters and values for Stratix V devices.

Table 46. JTAG Timing Parameters and Values for Stratix V Devices

Symbol	Description	Min	Max	Unit
t _{JCP}	TCK clock period ⁽²⁾	30	—	ns
t _{JCP}	TCK clock period ⁽²⁾	167	—	ns
t _{JCH}	TCK clock high time ⁽²⁾	14	—	ns
t _{JCL}	TCK clock low time ⁽²⁾	14	—	ns
t _{JPSU (TDI)}	TDI JTAG port setup time	2	—	ns
t _{JPSU (TMS)}	TMS JTAG port setup time	3	—	ns

Table 60. Glossary (Part 3 of 4)

Letter	Subject	Definitions
S	SW (sampling window)	<p>Timing Diagram—the period of time during which the data must be valid in order to capture it correctly. The setup and hold times determine the ideal strobe position within the sampling window, as shown:</p> 
	Single-ended voltage referenced I/O standard	<p>The JEDEC standard for SSTL and HSTL I/O defines both the AC and DC input signal values. The AC values indicate the voltage levels at which the receiver must meet its timing specifications. The DC values indicate the voltage levels at which the final logic state of the receiver is unambiguously defined. After the receiver input has crossed the AC value, the receiver changes to the new logic state.</p> <p>The new logic state is then maintained as long as the input stays beyond the DC threshold. This approach is intended to provide predictable receiver timing in the presence of input waveform ringing:</p> <p><i>Single-Ended Voltage Referenced I/O Standard</i></p> 
T	t_c	High-speed receiver and transmitter input and output clock period.
	TCCS (channel-to-channel-skew)	The timing difference between the fastest and slowest output edges, including t_{CO} variation and clock skew, across channels driven by the same PLL. The clock is included in the TCCS measurement (refer to the <i>Timing Diagram</i> figure under SW in this table).
	t_{DUTY}	<p>High-speed I/O block—Duty cycle on the high-speed transmitter output clock.</p> <p>Timing Unit Interval (TUI)</p> <p>The timing budget allowed for skew, propagation delays, and the data sampling window. (TUI = $1/(\text{receiver input clock frequency multiplication factor}) = t_c/w$)</p>
	t_{FALL}	Signal high-to-low transition time (80-20%)
	t_{INCCJ}	Cycle-to-cycle jitter tolerance on the PLL clock input.
	t_{OUTPJ_IO}	Period jitter on the general purpose I/O driven by a PLL.
	t_{OUTPJ_DC}	Period jitter on the dedicated clock output driven by a PLL.
	t_{RISE}	Signal low-to-high transition time (20-80%)
U	—	—