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### Understanding [Embedded - FPGAs \(Field Programmable Gate Array\)](#)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

### Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

#### Details

|                                |                                                                                                                                     |
|--------------------------------|-------------------------------------------------------------------------------------------------------------------------------------|
| Product Status                 | Obsolete                                                                                                                            |
| Number of LABs/CLBs            | 234720                                                                                                                              |
| Number of Logic Elements/Cells | 622000                                                                                                                              |
| Total RAM Bits                 | 51200000                                                                                                                            |
| Number of I/O                  | 696                                                                                                                                 |
| Number of Gates                | -                                                                                                                                   |
| Voltage - Supply               | 0.82V ~ 0.88V                                                                                                                       |
| Mounting Type                  | Surface Mount                                                                                                                       |
| Operating Temperature          | 0°C ~ 85°C (TJ)                                                                                                                     |
| Package / Case                 | 1517-BBGA, FCBGA                                                                                                                    |
| Supplier Device Package        | 1517-FBGA (40x40)                                                                                                                   |
| Purchase URL                   | <a href="https://www.e-xfl.com/product-detail/intel/5sgxea7k2f40c2l">https://www.e-xfl.com/product-detail/intel/5sgxea7k2f40c2l</a> |

## Recommended Operating Conditions

This section lists the functional operating limits for the AC and DC parameters for Stratix V devices. Table 6 lists the steady-state voltage and current values expected from Stratix V devices. Power supply ramps must all be strictly monotonic, without plateaus.

**Table 6. Recommended Operating Conditions for Stratix V Devices (Part 1 of 2)**

| Symbol                            | Description                                                                                                       | Condition  | Min <sup>(4)</sup> | Typ  | Max <sup>(4)</sup> | Unit |
|-----------------------------------|-------------------------------------------------------------------------------------------------------------------|------------|--------------------|------|--------------------|------|
| V <sub>CC</sub>                   | Core voltage and periphery circuitry power supply (C1, C2, I2, and I3YY speed grades)                             | —          | 0.87               | 0.9  | 0.93               | V    |
|                                   | Core voltage and periphery circuitry power supply (C2L, C3, C4, I2L, I3, I3L, and I4 speed grades) <sup>(3)</sup> | —          | 0.82               | 0.85 | 0.88               | V    |
| V <sub>CCPT</sub>                 | Power supply for programmable power technology                                                                    | —          | 1.45               | 1.50 | 1.55               | V    |
| V <sub>CC_AUX</sub>               | Auxiliary supply for the programmable power technology                                                            | —          | 2.375              | 2.5  | 2.625              | V    |
| V <sub>CCPD</sub> <sup>(1)</sup>  | I/O pre-driver (3.0 V) power supply                                                                               | —          | 2.85               | 3.0  | 3.15               | V    |
|                                   | I/O pre-driver (2.5 V) power supply                                                                               | —          | 2.375              | 2.5  | 2.625              | V    |
| V <sub>CCIO</sub>                 | I/O buffers (3.0 V) power supply                                                                                  | —          | 2.85               | 3.0  | 3.15               | V    |
|                                   | I/O buffers (2.5 V) power supply                                                                                  | —          | 2.375              | 2.5  | 2.625              | V    |
|                                   | I/O buffers (1.8 V) power supply                                                                                  | —          | 1.71               | 1.8  | 1.89               | V    |
|                                   | I/O buffers (1.5 V) power supply                                                                                  | —          | 1.425              | 1.5  | 1.575              | V    |
|                                   | I/O buffers (1.35 V) power supply                                                                                 | —          | 1.283              | 1.35 | 1.45               | V    |
|                                   | I/O buffers (1.25 V) power supply                                                                                 | —          | 1.19               | 1.25 | 1.31               | V    |
|                                   | I/O buffers (1.2 V) power supply                                                                                  | —          | 1.14               | 1.2  | 1.26               | V    |
| V <sub>CCPGM</sub>                | Configuration pins (3.0 V) power supply                                                                           | —          | 2.85               | 3.0  | 3.15               | V    |
|                                   | Configuration pins (2.5 V) power supply                                                                           | —          | 2.375              | 2.5  | 2.625              | V    |
|                                   | Configuration pins (1.8 V) power supply                                                                           | —          | 1.71               | 1.8  | 1.89               | V    |
| V <sub>CCA_FPLL</sub>             | PLL analog voltage regulator power supply                                                                         | —          | 2.375              | 2.5  | 2.625              | V    |
| V <sub>CCD_FPLL</sub>             | PLL digital voltage regulator power supply                                                                        | —          | 1.45               | 1.5  | 1.55               | V    |
| V <sub>CCBAT</sub> <sup>(2)</sup> | Battery back-up power supply (For design security volatile key register)                                          | —          | 1.2                | —    | 3.0                | V    |
| V <sub>I</sub>                    | DC input voltage                                                                                                  | —          | −0.5               | —    | 3.6                | V    |
| V <sub>O</sub>                    | Output voltage                                                                                                    | —          | 0                  | —    | V <sub>CCIO</sub>  | V    |
| T <sub>J</sub>                    | Operating junction temperature                                                                                    | Commercial | 0                  | —    | 85                 | °C   |
|                                   |                                                                                                                   | Industrial | −40                | —    | 100                | °C   |

**Table 6. Recommended Operating Conditions for Stratix V Devices (Part 2 of 2)**

| Symbol            | Description            | Condition    | Min <sup>(4)</sup> | Typ | Max <sup>(4)</sup> | Unit |
|-------------------|------------------------|--------------|--------------------|-----|--------------------|------|
| $t_{\text{RAMP}}$ | Power supply ramp time | Standard POR | 200 $\mu\text{s}$  | —   | 100 ms             | —    |
|                   |                        | Fast POR     | 200 $\mu\text{s}$  | —   | 4 ms               | —    |

**Notes to Table 6:**

- (1)  $V_{\text{CCPD}}$  must be 2.5 V when  $V_{\text{CCIO}}$  is 2.5, 1.8, 1.5, 1.35, 1.25 or 1.2 V.  $V_{\text{CCPD}}$  must be 3.0 V when  $V_{\text{CCIO}}$  is 3.0 V.
- (2) If you do not use the design security feature in Stratix V devices, connect  $V_{\text{CCBAT}}$  to a 1.2- to 3.0-V power supply. Stratix V power-on-reset (POR) circuitry monitors  $V_{\text{CCBAT}}$ . Stratix V devices will not exit POR if  $V_{\text{CCBAT}}$  stays at logic low.
- (3) C2L and I2L can also be run at 0.90 V for legacy boards that were designed for the C2 and I2 speed grades.
- (4) The power supply value describes the budget for the DC (static) power supply tolerance and does not include the dynamic tolerance requirements. Refer to the PDN tool for the additional budget for the dynamic tolerance requirements.

Table 7 lists the transceiver power supply recommended operating conditions for Stratix V GX, GS, and GT devices.

**Table 7. Recommended Transceiver Power Supply Operating Conditions for Stratix V GX, GS, and GT Devices (Part 1 of 2)**

| Symbol                             | Description                                                                                   | Devices    | Minimum <sup>(4)</sup> | Typical | Maximum <sup>(4)</sup> | Unit |
|------------------------------------|-----------------------------------------------------------------------------------------------|------------|------------------------|---------|------------------------|------|
| $V_{\text{CCA\_GXBL}}$<br>(1), (3) | Transceiver channel PLL power supply (left side)                                              | GX, GS, GT | 2.85                   | 3.0     | 3.15                   | V    |
|                                    |                                                                                               |            | 2.375                  | 2.5     | 2.625                  |      |
| $V_{\text{CCA\_GXBR}}$<br>(1), (3) | Transceiver channel PLL power supply (right side)                                             | GX, GS     | 2.85                   | 3.0     | 3.15                   | V    |
|                                    |                                                                                               |            | 2.375                  | 2.5     | 2.625                  |      |
| $V_{\text{CCA\_GTBR}}$             | Transceiver channel PLL power supply (right side)                                             | GT         | 2.85                   | 3.0     | 3.15                   | V    |
| $V_{\text{CCHIP\_L}}$              | Transceiver hard IP power supply (left side; C1, C2, I2, and I3YY speed grades)               | GX, GS, GT | 0.87                   | 0.9     | 0.93                   | V    |
|                                    | Transceiver hard IP power supply (left side; C2L, C3, C4, I2L, I3, I3L, and I4 speed grades)  | GX, GS, GT | 0.82                   | 0.85    | 0.88                   | V    |
| $V_{\text{CCHIP\_R}}$              | Transceiver hard IP power supply (right side; C1, C2, I2, and I3YY speed grades)              | GX, GS, GT | 0.87                   | 0.9     | 0.93                   | V    |
|                                    | Transceiver hard IP power supply (right side; C2L, C3, C4, I2L, I3, I3L, and I4 speed grades) | GX, GS, GT | 0.82                   | 0.85    | 0.88                   | V    |
| $V_{\text{CCHSSI\_L}}$             | Transceiver PCS power supply (left side; C1, C2, I2, and I3YY speed grades)                   | GX, GS, GT | 0.87                   | 0.9     | 0.93                   | V    |
|                                    | Transceiver PCS power supply (left side; C2L, C3, C4, I2L, I3, I3L, and I4 speed grades)      | GX, GS, GT | 0.82                   | 0.85    | 0.88                   | V    |
| $V_{\text{CCHSSI\_R}}$             | Transceiver PCS power supply (right side; C1, C2, I2, and I3YY speed grades)                  | GX, GS, GT | 0.87                   | 0.9     | 0.93                   | V    |
|                                    | Transceiver PCS power supply (right side; C2L, C3, C4, I2L, I3, I3L, and I4 speed grades)     | GX, GS, GT | 0.82                   | 0.85    | 0.88                   | V    |
| $V_{\text{CCR\_GXBL}}$<br>(2)      | Receiver analog power supply (left side)                                                      | GX, GS, GT | 0.82                   | 0.85    | 0.88                   | V    |
|                                    |                                                                                               |            | 0.87                   | 0.90    | 0.93                   |      |
|                                    |                                                                                               |            | 0.97                   | 1.0     | 1.03                   |      |
|                                    |                                                                                               |            | 1.03                   | 1.05    | 1.07                   |      |

## Internal Weak Pull-Up Resistor

Table 16 lists the weak pull-up resistor values for Stratix V devices.

**Table 16. Internal Weak Pull-Up Resistor for Stratix V Devices <sup>(1), (2)</sup>**

| Symbol          | Description                                                                                                                                         | V <sub>CCIO</sub> Conditions (V) <sup>(3)</sup> | Value <sup>(4)</sup> | Unit |
|-----------------|-----------------------------------------------------------------------------------------------------------------------------------------------------|-------------------------------------------------|----------------------|------|
| R <sub>PU</sub> | Value of the I/O pin pull-up resistor before and during configuration, as well as user mode if you enable the programmable pull-up resistor option. | 3.0 ±5%                                         | 25                   | kΩ   |
|                 |                                                                                                                                                     | 2.5 ±5%                                         | 25                   | kΩ   |
|                 |                                                                                                                                                     | 1.8 ±5%                                         | 25                   | kΩ   |
|                 |                                                                                                                                                     | 1.5 ±5%                                         | 25                   | kΩ   |
|                 |                                                                                                                                                     | 1.35 ±5%                                        | 25                   | kΩ   |
|                 |                                                                                                                                                     | 1.25 ±5%                                        | 25                   | kΩ   |
|                 |                                                                                                                                                     | 1.2 ±5%                                         | 25                   | kΩ   |

### Notes to Table 16:

- (1) All I/O pins have an option to enable the weak pull-up resistor except the configuration, test, and JTAG pins.
- (2) The internal weak pull-down feature is only available for the JTAG TCK pin. The typical value for this internal weak pull-down resistor is approximately 25 kΩ.
- (3) The pin pull-up resistance values may be lower if an external source drives the pin higher than V<sub>CCIO</sub>.
- (4) These specifications are valid with a ±10% tolerance to cover changes over PVT.

## I/O Standard Specifications

Table 17 through Table 22 list the input voltage (V<sub>IH</sub> and V<sub>IL</sub>), output voltage (V<sub>OH</sub> and V<sub>OL</sub>), and current drive characteristics (I<sub>OH</sub> and I<sub>OL</sub>) for various I/O standards supported by Stratix V devices. These tables also show the Stratix V device family I/O standard specifications. The V<sub>OL</sub> and V<sub>OH</sub> values are valid at the corresponding I<sub>OH</sub> and I<sub>OL</sub>, respectively.

For an explanation of the terms used in Table 17 through Table 22, refer to “Glossary” on page 65. For tolerance calculations across all SSTL and HSTL I/O standards, refer to Altera knowledge base solution rd07262012\_486.

**Table 17. Single-Ended I/O Standards for Stratix V Devices**

| I/O Standard | V <sub>CCIO</sub> (V) |     |       | V <sub>IL</sub> (V) |                             | V <sub>IH</sub> (V)         |                         | V <sub>OL</sub> (V)         | V <sub>OH</sub> (V)         | I <sub>OL</sub> (mA) | I <sub>OH</sub> (mA) |
|--------------|-----------------------|-----|-------|---------------------|-----------------------------|-----------------------------|-------------------------|-----------------------------|-----------------------------|----------------------|----------------------|
|              | Min                   | Typ | Max   | Min                 | Max                         | Min                         | Max                     | Max                         | Min                         |                      |                      |
| LVTTTL       | 2.85                  | 3   | 3.15  | −0.3                | 0.8                         | 1.7                         | 3.6                     | 0.4                         | 2.4                         | 2                    | −2                   |
| LVC MOS      | 2.85                  | 3   | 3.15  | −0.3                | 0.8                         | 1.7                         | 3.6                     | 0.2                         | V <sub>CCIO</sub> − 0.2     | 0.1                  | −0.1                 |
| 2.5 V        | 2.375                 | 2.5 | 2.625 | −0.3                | 0.7                         | 1.7                         | 3.6                     | 0.4                         | 2                           | 1                    | −1                   |
| 1.8 V        | 1.71                  | 1.8 | 1.89  | −0.3                | 0.35 *<br>V <sub>CCIO</sub> | 0.65 *<br>V <sub>CCIO</sub> | V <sub>CCIO</sub> + 0.3 | 0.45                        | V <sub>CCIO</sub> − 0.45    | 2                    | −2                   |
| 1.5 V        | 1.425                 | 1.5 | 1.575 | −0.3                | 0.35 *<br>V <sub>CCIO</sub> | 0.65 *<br>V <sub>CCIO</sub> | V <sub>CCIO</sub> + 0.3 | 0.25 *<br>V <sub>CCIO</sub> | 0.75 *<br>V <sub>CCIO</sub> | 2                    | −2                   |
| 1.2 V        | 1.14                  | 1.2 | 1.26  | −0.3                | 0.35 *<br>V <sub>CCIO</sub> | 0.65 *<br>V <sub>CCIO</sub> | V <sub>CCIO</sub> + 0.3 | 0.25 *<br>V <sub>CCIO</sub> | 0.75 *<br>V <sub>CCIO</sub> | 2                    | −2                   |

**Table 18. Single-Ended SSTL, HSTL, and HSUL I/O Reference Voltage Specifications for Stratix V Devices**

| I/O Standard            | $V_{CCIO}$ (V) |      |       | $V_{REF}$ (V)     |                  |                   | $V_{TT}$ (V)      |                  |                   |
|-------------------------|----------------|------|-------|-------------------|------------------|-------------------|-------------------|------------------|-------------------|
|                         | Min            | Typ  | Max   | Min               | Typ              | Max               | Min               | Typ              | Max               |
| SSTL-2<br>Class I, II   | 2.375          | 2.5  | 2.625 | $0.49 * V_{CCIO}$ | $0.5 * V_{CCIO}$ | $0.51 * V_{CCIO}$ | $V_{REF} - 0.04$  | $V_{REF}$        | $V_{REF} + 0.04$  |
| SSTL-18<br>Class I, II  | 1.71           | 1.8  | 1.89  | 0.833             | 0.9              | 0.969             | $V_{REF} - 0.04$  | $V_{REF}$        | $V_{REF} + 0.04$  |
| SSTL-15<br>Class I, II  | 1.425          | 1.5  | 1.575 | $0.49 * V_{CCIO}$ | $0.5 * V_{CCIO}$ | $0.51 * V_{CCIO}$ | $0.49 * V_{CCIO}$ | $0.5 * V_{CCIO}$ | $0.51 * V_{CCIO}$ |
| SSTL-135<br>Class I, II | 1.283          | 1.35 | 1.418 | $0.49 * V_{CCIO}$ | $0.5 * V_{CCIO}$ | $0.51 * V_{CCIO}$ | $0.49 * V_{CCIO}$ | $0.5 * V_{CCIO}$ | $0.51 * V_{CCIO}$ |
| SSTL-125<br>Class I, II | 1.19           | 1.25 | 1.26  | $0.49 * V_{CCIO}$ | $0.5 * V_{CCIO}$ | $0.51 * V_{CCIO}$ | $0.49 * V_{CCIO}$ | $0.5 * V_{CCIO}$ | $0.51 * V_{CCIO}$ |
| SSTL-12<br>Class I, II  | 1.14           | 1.20 | 1.26  | $0.49 * V_{CCIO}$ | $0.5 * V_{CCIO}$ | $0.51 * V_{CCIO}$ | $0.49 * V_{CCIO}$ | $0.5 * V_{CCIO}$ | $0.51 * V_{CCIO}$ |
| HSTL-18<br>Class I, II  | 1.71           | 1.8  | 1.89  | 0.85              | 0.9              | 0.95              | —                 | $V_{CCIO}/2$     | —                 |
| HSTL-15<br>Class I, II  | 1.425          | 1.5  | 1.575 | 0.68              | 0.75             | 0.9               | —                 | $V_{CCIO}/2$     | —                 |
| HSTL-12<br>Class I, II  | 1.14           | 1.2  | 1.26  | $0.47 * V_{CCIO}$ | $0.5 * V_{CCIO}$ | $0.53 * V_{CCIO}$ | —                 | $V_{CCIO}/2$     | —                 |
| HSUL-12                 | 1.14           | 1.2  | 1.3   | $0.49 * V_{CCIO}$ | $0.5 * V_{CCIO}$ | $0.51 * V_{CCIO}$ | —                 | —                | —                 |

**Table 19. Single-Ended SSTL, HSTL, and HSUL I/O Standards Signal Specifications for Stratix V Devices (Part 1 of 2)**

| I/O Standard            | $V_{IL(DC)}$ (V) |                   | $V_{IH(DC)}$ (V)  |                  | $V_{IL(AC)}$ (V)  | $V_{IH(AC)}$ (V)  | $V_{OL}$ (V)     | $V_{OH}$ (V)      | $I_{OI}$ (mA) | $I_{OH}$ (mA) |
|-------------------------|------------------|-------------------|-------------------|------------------|-------------------|-------------------|------------------|-------------------|---------------|---------------|
|                         | Min              | Max               | Min               | Max              | Max               | Min               | Max              | Min               |               |               |
| SSTL-2<br>Class I       | -0.3             | $V_{REF} - 0.15$  | $V_{REF} + 0.15$  | $V_{CCIO} + 0.3$ | $V_{REF} - 0.31$  | $V_{REF} + 0.31$  | $V_{TT} - 0.608$ | $V_{TT} + 0.608$  | 8.1           | -8.1          |
| SSTL-2<br>Class II      | -0.3             | $V_{REF} - 0.15$  | $V_{REF} + 0.15$  | $V_{CCIO} + 0.3$ | $V_{REF} - 0.31$  | $V_{REF} + 0.31$  | $V_{TT} - 0.81$  | $V_{TT} + 0.81$   | 16.2          | -16.2         |
| SSTL-18<br>Class I      | -0.3             | $V_{REF} - 0.125$ | $V_{REF} + 0.125$ | $V_{CCIO} + 0.3$ | $V_{REF} - 0.25$  | $V_{REF} + 0.25$  | $V_{TT} - 0.603$ | $V_{TT} + 0.603$  | 6.7           | -6.7          |
| SSTL-18<br>Class II     | -0.3             | $V_{REF} - 0.125$ | $V_{REF} + 0.125$ | $V_{CCIO} + 0.3$ | $V_{REF} - 0.25$  | $V_{REF} + 0.25$  | 0.28             | $V_{CCIO} - 0.28$ | 13.4          | -13.4         |
| SSTL-15<br>Class I      | —                | $V_{REF} - 0.1$   | $V_{REF} + 0.1$   | —                | $V_{REF} - 0.175$ | $V_{REF} + 0.175$ | $0.2 * V_{CCIO}$ | $0.8 * V_{CCIO}$  | 8             | -8            |
| SSTL-15<br>Class II     | —                | $V_{REF} - 0.1$   | $V_{REF} + 0.1$   | —                | $V_{REF} - 0.175$ | $V_{REF} + 0.175$ | $0.2 * V_{CCIO}$ | $0.8 * V_{CCIO}$  | 16            | -16           |
| SSTL-135<br>Class I, II | —                | $V_{REF} - 0.09$  | $V_{REF} + 0.09$  | —                | $V_{REF} - 0.16$  | $V_{REF} + 0.16$  | $0.2 * V_{CCIO}$ | $0.8 * V_{CCIO}$  | —             | —             |
| SSTL-125<br>Class I, II | —                | $V_{REF} - 0.85$  | $V_{REF} + 0.85$  | —                | $V_{REF} - 0.15$  | $V_{REF} + 0.15$  | $0.2 * V_{CCIO}$ | $0.8 * V_{CCIO}$  | —             | —             |
| SSTL-12<br>Class I, II  | —                | $V_{REF} - 0.1$   | $V_{REF} + 0.1$   | —                | $V_{REF} - 0.15$  | $V_{REF} + 0.15$  | $0.2 * V_{CCIO}$ | $0.8 * V_{CCIO}$  | —             | —             |

**Table 19. Single-Ended SSTL, HSTL, and HSUL I/O Standards Signal Specifications for Stratix V Devices (Part 2 of 2)**

| I/O Standard     | $V_{IL(DC)}$ (V) |                  | $V_{IH(DC)}$ (V) |                   | $V_{IL(AC)}$ (V) | $V_{IH(AC)}$ (V) | $V_{OL}$ (V)      | $V_{OH}$ (V)      | $I_{ol}$ (mA) | $I_{oh}$ (mA) |
|------------------|------------------|------------------|------------------|-------------------|------------------|------------------|-------------------|-------------------|---------------|---------------|
|                  | Min              | Max              | Min              | Max               | Max              | Min              | Max               | Min               |               |               |
| HSTL-18 Class I  | —                | $V_{REF} - 0.1$  | $V_{REF} + 0.1$  | —                 | $V_{REF} - 0.2$  | $V_{REF} + 0.2$  | 0.4               | $V_{CCIO} - 0.4$  | 8             | -8            |
| HSTL-18 Class II | —                | $V_{REF} - 0.1$  | $V_{REF} + 0.1$  | —                 | $V_{REF} - 0.2$  | $V_{REF} + 0.2$  | 0.4               | $V_{CCIO} - 0.4$  | 16            | -16           |
| HSTL-15 Class I  | —                | $V_{REF} - 0.1$  | $V_{REF} + 0.1$  | —                 | $V_{REF} - 0.2$  | $V_{REF} + 0.2$  | 0.4               | $V_{CCIO} - 0.4$  | 8             | -8            |
| HSTL-15 Class II | —                | $V_{REF} - 0.1$  | $V_{REF} + 0.1$  | —                 | $V_{REF} - 0.2$  | $V_{REF} + 0.2$  | 0.4               | $V_{CCIO} - 0.4$  | 16            | -16           |
| HSTL-12 Class I  | -0.15            | $V_{REF} - 0.08$ | $V_{REF} + 0.08$ | $V_{CCIO} + 0.15$ | $V_{REF} - 0.15$ | $V_{REF} + 0.15$ | $0.25^* V_{CCIO}$ | $0.75^* V_{CCIO}$ | 8             | -8            |
| HSTL-12 Class II | -0.15            | $V_{REF} - 0.08$ | $V_{REF} + 0.08$ | $V_{CCIO} + 0.15$ | $V_{REF} - 0.15$ | $V_{REF} + 0.15$ | $0.25^* V_{CCIO}$ | $0.75^* V_{CCIO}$ | 16            | -16           |
| HSUL-12          | —                | $V_{REF} - 0.13$ | $V_{REF} + 0.13$ | —                 | $V_{REF} - 0.22$ | $V_{REF} + 0.22$ | $0.1^* V_{CCIO}$  | $0.9^* V_{CCIO}$  | —             | —             |

**Table 20. Differential SSTL I/O Standards for Stratix V Devices**

| I/O Standard         | $V_{CCIO}$ (V) |      |       | $V_{SWING(DC)}$ (V) |                  | $V_{X(AC)}$ (V)      |              |                      | $V_{SWING(AC)}$ (V)       |                           |
|----------------------|----------------|------|-------|---------------------|------------------|----------------------|--------------|----------------------|---------------------------|---------------------------|
|                      | Min            | Typ  | Max   | Min                 | Max              | Min                  | Typ          | Max                  | Min                       | Max                       |
| SSTL-2 Class I, II   | 2.375          | 2.5  | 2.625 | 0.3                 | $V_{CCIO} + 0.6$ | $V_{CCIO}/2 - 0.2$   | —            | $V_{CCIO}/2 + 0.2$   | 0.62                      | $V_{CCIO} + 0.6$          |
| SSTL-18 Class I, II  | 1.71           | 1.8  | 1.89  | 0.25                | $V_{CCIO} + 0.6$ | $V_{CCIO}/2 - 0.175$ | —            | $V_{CCIO}/2 + 0.175$ | 0.5                       | $V_{CCIO} + 0.6$          |
| SSTL-15 Class I, II  | 1.425          | 1.5  | 1.575 | 0.2                 | (1)              | $V_{CCIO}/2 - 0.15$  | —            | $V_{CCIO}/2 + 0.15$  | 0.35                      | —                         |
| SSTL-135 Class I, II | 1.283          | 1.35 | 1.45  | 0.2                 | (1)              | $V_{CCIO}/2 - 0.15$  | $V_{CCIO}/2$ | $V_{CCIO}/2 + 0.15$  | $2(V_{IH(AC)} - V_{REF})$ | $2(V_{IL(AC)} - V_{REF})$ |
| SSTL-125 Class I, II | 1.19           | 1.25 | 1.31  | 0.18                | (1)              | $V_{CCIO}/2 - 0.15$  | $V_{CCIO}/2$ | $V_{CCIO}/2 + 0.15$  | $2(V_{IH(AC)} - V_{REF})$ | —                         |
| SSTL-12 Class I, II  | 1.14           | 1.2  | 1.26  | 0.18                | —                | $V_{REF} - 0.15$     | $V_{CCIO}/2$ | $V_{REF} + 0.15$     | -0.30                     | 0.30                      |

**Note to Table 20:**

(1) The maximum value for  $V_{SWING(DC)}$  is not defined. However, each single-ended signal needs to be within the respective single-ended limits ( $V_{IH(DC)}$  and  $V_{IL(DC)}$ ).

**Table 21. Differential HSTL and HSUL I/O Standards for Stratix V Devices (Part 1 of 2)**

| I/O Standard        | $V_{CCIO}$ (V) |     |       | $V_{DIF(DC)}$ (V) |     | $V_{X(AC)}$ (V) |     |      | $V_{CM(DC)}$ (V) |     |      | $V_{DIF(AC)}$ (V) |     |
|---------------------|----------------|-----|-------|-------------------|-----|-----------------|-----|------|------------------|-----|------|-------------------|-----|
|                     | Min            | Typ | Max   | Min               | Max | Min             | Typ | Max  | Min              | Typ | Max  | Min               | Max |
| HSTL-18 Class I, II | 1.71           | 1.8 | 1.89  | 0.2               | —   | 0.78            | —   | 1.12 | 0.78             | —   | 1.12 | 0.4               | —   |
| HSTL-15 Class I, II | 1.425          | 1.5 | 1.575 | 0.2               | —   | 0.68            | —   | 0.9  | 0.68             | —   | 0.9  | 0.4               | —   |

**Table 21. Differential HSTL and HSUL I/O Standards for Stratix V Devices (Part 2 of 2)**

| I/O Standard        | $V_{CCIO}$ (V) |     |      | $V_{DIF(DC)}$ (V) |                  | $V_{X(AC)}$ (V)         |                  |                         | $V_{CM(DC)}$ (V) |                  |                  | $V_{DIF(AC)}$ (V) |                   |
|---------------------|----------------|-----|------|-------------------|------------------|-------------------------|------------------|-------------------------|------------------|------------------|------------------|-------------------|-------------------|
|                     | Min            | Typ | Max  | Min               | Max              | Min                     | Typ              | Max                     | Min              | Typ              | Max              | Min               | Max               |
| HSTL-12 Class I, II | 1.14           | 1.2 | 1.26 | 0.16              | $V_{CCIO} + 0.3$ | —                       | $0.5^* V_{CCIO}$ | —                       | $0.4^* V_{CCIO}$ | $0.5^* V_{CCIO}$ | $0.6^* V_{CCIO}$ | 0.3               | $V_{CCIO} + 0.48$ |
| HSUL-12             | 1.14           | 1.2 | 1.3  | 0.26              | 0.26             | $0.5^* V_{CCIO} - 0.12$ | $0.5^* V_{CCIO}$ | $0.5^* V_{CCIO} + 0.12$ | $0.4^* V_{CCIO}$ | $0.5^* V_{CCIO}$ | $0.6^* V_{CCIO}$ | 0.44              | 0.44              |

**Table 22. Differential I/O Standard Specifications for Stratix V Devices <sup>(7)</sup>**

| I/O Standard                   | $V_{CCIO}$ (V) <sup>(10)</sup>                                                                                                                                                                                       |     |       | $V_{ID}$ (mV) <sup>(8)</sup> |                   |     | $V_{ICM(DC)}$ (V) |                         |       | $V_{OD}$ (V) <sup>(6)</sup> |     |     | $V_{OCM}$ (V) <sup>(6)</sup> |      |       |
|--------------------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----|-------|------------------------------|-------------------|-----|-------------------|-------------------------|-------|-----------------------------|-----|-----|------------------------------|------|-------|
|                                | Min                                                                                                                                                                                                                  | Typ | Max   | Min                          | Condition         | Max | Min               | Condition               | Max   | Min                         | Typ | Max | Min                          | Typ  | Max   |
| PCML                           | Transmitter, receiver, and input reference clock pins of the high-speed transceivers use the PCML I/O standard. For transmitter, receiver, and reference clock I/O pin specifications, refer to Table 23 on page 18. |     |       |                              |                   |     |                   |                         |       |                             |     |     |                              |      |       |
| 2.5 V LVDS <sup>(1)</sup>      | 2.375                                                                                                                                                                                                                | 2.5 | 2.625 | 100                          | $V_{CM} = 1.25$ V | —   | 0.05              | $D_{MAX} \leq 700$ Mbps | 1.8   | 0.247                       | —   | 0.6 | 1.125                        | 1.25 | 1.375 |
|                                |                                                                                                                                                                                                                      |     |       |                              |                   | —   | 1.05              | $D_{MAX} > 700$ Mbps    | 1.55  | 0.247                       | —   | 0.6 | 1.125                        | 1.25 | 1.375 |
| BLVDS <sup>(5)</sup>           | 2.375                                                                                                                                                                                                                | 2.5 | 2.625 | 100                          | —                 | —   | —                 | —                       | —     | —                           | —   | —   | —                            | —    | —     |
| RSDS (HIO) <sup>(2)</sup>      | 2.375                                                                                                                                                                                                                | 2.5 | 2.625 | 100                          | $V_{CM} = 1.25$ V | —   | 0.3               | —                       | 1.4   | 0.1                         | 0.2 | 0.6 | 0.5                          | 1.2  | 1.4   |
| Mini-LVDS (HIO) <sup>(3)</sup> | 2.375                                                                                                                                                                                                                | 2.5 | 2.625 | 200                          | —                 | 600 | 0.4               | —                       | 1.325 | 0.25                        | —   | 0.6 | 1                            | 1.2  | 1.4   |
| LVPECL <sup>(4), (9)</sup>     | —                                                                                                                                                                                                                    | —   | —     | 300                          | —                 | —   | 0.6               | $D_{MAX} \leq 700$ Mbps | 1.8   | —                           | —   | —   | —                            | —    | —     |
|                                | —                                                                                                                                                                                                                    | —   | —     | 300                          | —                 | —   | 1                 | $D_{MAX} > 700$ Mbps    | 1.6   | —                           | —   | —   | —                            | —    | —     |

**Notes to Table 22:**

- (1) For optimized LVDS receiver performance, the receiver voltage input range must be between 1.0 V to 1.6 V for data rates above 700 Mbps, and 0 V to 1.85 V for data rates below 700 Mbps.
- (2) For optimized RSDS receiver performance, the receiver voltage input range must be between 0.25 V to 1.45 V.
- (3) For optimized Mini-LVDS receiver performance, the receiver voltage input range must be between 0.3 V to 1.425 V.
- (4) For optimized LVPECL receiver performance, the receiver voltage input range must be between 0.85 V to 1.75 V for data rate above 700 Mbps and 0.45 V to 1.95 V for data rate below 700 Mbps.
- (5) There are no fixed  $V_{ICM}$ ,  $V_{OD}$ , and  $V_{OCM}$  specifications for BLVDS. They depend on the system topology.
- (6) RL range:  $90 \leq RL \leq 110 \Omega$ .
- (7) The 1.4-V and 1.5-V PCML transceiver I/O standard specifications are described in "Transceiver Performance Specifications" on page 18.
- (8) The minimum  $V_{ID}$  value is applicable over the entire common mode range,  $V_{CM}$ .
- (9) LVPECL is only supported on dedicated clock input pins.
- (10) Differential inputs are powered by VCCPD which requires 2.5 V.

## Power Consumption

Altera offers two ways to estimate power consumption for a design—the Excel-based Early Power Estimator and the Quartus® II PowerPlay Power Analyzer feature.

Table 24 shows the maximum transmitter data rate for the clock network.

**Table 24. Clock Network Maximum Data Rate Transmitter Specifications <sup>(1)</sup>**

| Clock Network                  | ATX PLL                |                    |                                       | CMU PLL <sup>(2)</sup> |                    |                                       | fPLL                   |                    |                                       |
|--------------------------------|------------------------|--------------------|---------------------------------------|------------------------|--------------------|---------------------------------------|------------------------|--------------------|---------------------------------------|
|                                | Non-bonded Mode (Gbps) | Bonded Mode (Gbps) | Channel Span                          | Non-bonded Mode (Gbps) | Bonded Mode (Gbps) | Channel Span                          | Non-bonded Mode (Gbps) | Bonded Mode (Gbps) | Channel Span                          |
| x1 <sup>(3)</sup>              | 14.1                   | —                  | 6                                     | 12.5                   | —                  | 6                                     | 3.125                  | —                  | 3                                     |
| x6 <sup>(3)</sup>              | —                      | 14.1               | 6                                     | —                      | 12.5               | 6                                     | —                      | 3.125              | 6                                     |
| x6 PLL Feedback <sup>(4)</sup> | —                      | 14.1               | Side-wide                             | —                      | 12.5               | Side-wide                             | —                      | —                  | —                                     |
| xN (PCIe)                      | —                      | 8.0                | 8                                     | —                      | 5.0                | 8                                     | —                      | —                  | —                                     |
| xN (Native PHY IP)             | 8.0                    | 8.0                | Up to 13 channels above and below PLL | 7.99                   | 7.99               | Up to 13 channels above and below PLL | 3.125                  | 3.125              | Up to 13 channels above and below PLL |
|                                | —                      | 8.01 to 9.8304     | Up to 7 channels above and below PLL  |                        |                    |                                       |                        |                    |                                       |

**Notes to Table 24:**

- (1) Valid data rates below the maximum specified in this table depend on the reference clock frequency and the PLL counter settings. Check the MegaWizard message during the PHY IP instantiation.
- (2) ATX PLL is recommended at 8 Gbps and above data rates for improved jitter performance.
- (3) Channel span is within a transceiver bank.
- (4) Side-wide channel bonding is allowed up to the maximum supported by the PHY IP.

Table 26 shows the approximate maximum data rate using the 10G PCS.

**Table 26. Stratix V 10G PCS Approximate Maximum Data Rate <sup>(1)</sup>**

| Mode <sup>(2)</sup> | Transceiver Speed Grade | PMA Width                             | 64           | 40    | 40    | 40   | 32       | 32    |
|---------------------|-------------------------|---------------------------------------|--------------|-------|-------|------|----------|-------|
|                     |                         | PCS Width                             | 64           | 66/67 | 50    | 40   | 64/66/67 | 32    |
| FIFO or Register    | 1                       | C1, C2, C2L, I2, I2L core speed grade | 14.1         | 14.1  | 10.69 | 14.1 | 13.6     | 13.6  |
|                     | 2                       | C1, C2, C2L, I2, I2L core speed grade | 12.5         | 12.5  | 10.69 | 12.5 | 12.5     | 12.5  |
|                     |                         | C3, I3, I3L core speed grade          | 12.5         | 12.5  | 10.69 | 12.5 | 10.88    | 10.88 |
|                     | 3                       | C1, C2, C2L, I2, I2L core speed grade | 8.5 Gbps     |       |       |      |          |       |
|                     |                         | C3, I3, I3L core speed grade          |              |       |       |      |          |       |
|                     |                         | C4, I4 core speed grade               |              |       |       |      |          |       |
|                     |                         | I3YY core speed grade                 | 10.3125 Gbps |       |       |      |          |       |

**Notes to Table 26:**

- (1) The maximum data rate is in Gbps.
- (2) The Phase Compensation FIFO can be configured in FIFO mode or register mode. In the FIFO mode, the pointers are not fixed, and the latency can vary. In the register mode the pointers are fixed for low latency.

**Table 28. Transceiver Specifications for Stratix V GT Devices (Part 2 of 5) <sup>(1)</sup>**

| Symbol/<br>Description                                                                                                                              | Conditions                                                                        | Transceiver<br>Speed Grade 2                         |               |        | Transceiver<br>Speed Grade 3 |               |        | Unit     |
|-----------------------------------------------------------------------------------------------------------------------------------------------------|-----------------------------------------------------------------------------------|------------------------------------------------------|---------------|--------|------------------------------|---------------|--------|----------|
|                                                                                                                                                     |                                                                                   | Min                                                  | Typ           | Max    | Min                          | Typ           | Max    |          |
| Transmitter REFCLK<br>Phase Noise (622<br>MHz) <sup>(18)</sup>                                                                                      | 100 Hz                                                                            | —                                                    | —             | -70    | —                            | —             | -70    | dBc/Hz   |
|                                                                                                                                                     | 1 kHz                                                                             | —                                                    | —             | -90    | —                            | —             | -90    |          |
|                                                                                                                                                     | 10 kHz                                                                            | —                                                    | —             | -100   | —                            | —             | -100   |          |
|                                                                                                                                                     | 100 kHz                                                                           | —                                                    | —             | -110   | —                            | —             | -110   |          |
|                                                                                                                                                     | ≥ 1 MHz                                                                           | —                                                    | —             | -120   | —                            | —             | -120   |          |
| Transmitter REFCLK<br>Phase Jitter (100<br>MHz) <sup>(15)</sup>                                                                                     | 10 kHz to<br>1.5 MHz<br>(PCIe)                                                    | —                                                    | —             | 3      | —                            | —             | 3      | ps (rms) |
| RREF <sup>(17)</sup>                                                                                                                                | —                                                                                 | —                                                    | 1800<br>± 1%  | —      | —                            | 1800<br>± 1%  | —      | Ω        |
| <b>Transceiver Clocks</b>                                                                                                                           |                                                                                   |                                                      |               |        |                              |               |        |          |
| fixedclk clock<br>frequency                                                                                                                         | PCIe<br>Receiver<br>Detect                                                        | —                                                    | 100 or<br>125 | —      | —                            | 100 or<br>125 | —      | MHz      |
| Reconfiguration clock<br>(mgmt_clk_clk)<br>frequency                                                                                                | —                                                                                 | 100                                                  | —             | 125    | 100                          | —             | 125    | MHz      |
| <b>Receiver</b>                                                                                                                                     |                                                                                   |                                                      |               |        |                              |               |        |          |
| Supported I/O<br>Standards                                                                                                                          | —                                                                                 | 1.4-V PCML, 1.5-V PCML, 2.5-V PCML, LVPECL, and LVDS |               |        |                              |               |        |          |
| Data rate<br>(Standard PCS) <sup>(21)</sup>                                                                                                         | GX channels                                                                       | 600                                                  | —             | 8500   | 600                          | —             | 8500   | Mbps     |
| Data rate<br>(10G PCS) <sup>(21)</sup>                                                                                                              | GX channels                                                                       | 600                                                  | —             | 12,500 | 600                          | —             | 12,500 | Mbps     |
| Data rate                                                                                                                                           | GT channels                                                                       | 19,600                                               | —             | 28,050 | 19,600                       | —             | 25,780 | Mbps     |
| Absolute V <sub>MAX</sub> for a<br>receiver pin <sup>(3)</sup>                                                                                      | GT channels                                                                       | —                                                    | —             | 1.2    | —                            | —             | 1.2    | V        |
| Absolute V <sub>MIN</sub> for a<br>receiver pin                                                                                                     | GT channels                                                                       | -0.4                                                 | —             | —      | -0.4                         | —             | —      | V        |
| Maximum peak-to-peak<br>differential input<br>voltage V <sub>ID</sub> (diff p-p)<br>before device<br>configuration <sup>(20)</sup>                  | GT channels                                                                       | —                                                    | —             | 1.6    | —                            | —             | 1.6    | V        |
|                                                                                                                                                     | GX channels                                                                       | <sup>(8)</sup>                                       |               |        |                              |               |        |          |
| Maximum peak-to-peak<br>differential input<br>voltage V <sub>ID</sub> (diff p-p)<br>after device<br>configuration <sup>(16)</sup> , <sup>(20)</sup> | GT channels<br>V <sub>CCR_GTB</sub> =<br>1.05 V<br>(V <sub>ICM</sub> =<br>0.65 V) | —                                                    | —             | 2.2    | —                            | —             | 2.2    | V        |
|                                                                                                                                                     | GX channels                                                                       | <sup>(8)</sup>                                       |               |        |                              |               |        |          |
| Minimum differential<br>eye opening at receiver<br>serial input pins <sup>(4)</sup> , <sup>(20)</sup>                                               | GT channels                                                                       | 200                                                  | —             | —      | 200                          | —             | —      | mV       |
|                                                                                                                                                     | GX channels                                                                       | <sup>(8)</sup>                                       |               |        |                              |               |        |          |

Table 29 shows the  $V_{OD}$  settings for the GT channel.

**Table 29. Typical  $V_{OD}$  Setting for GT Channel, TX Termination = 100  $\Omega$**

| Symbol                                                                      | $V_{OD}$ Setting | $V_{OD}$ Value (mV) |
|-----------------------------------------------------------------------------|------------------|---------------------|
| <b><math>V_{OD}</math> differential peak to peak typical <sup>(1)</sup></b> | 0                | 0                   |
|                                                                             | 1                | 200                 |
|                                                                             | 2                | 400                 |
|                                                                             | 3                | 600                 |
|                                                                             | 4                | 800                 |
|                                                                             | 5                | 1000                |

**Note:**

(1) Refer to Figure 4.

- XFI
- ASI
- HiGig/HiGig+
- HiGig2/HiGig2+
- Serial Data Converter (SDC)
- GPON
- SDI
- SONET
- Fibre Channel (FC)
- PCIe
- QPI
- SFF-8431

Download the Stratix V Characterization Report Tool to view the characterization report summary for these protocols.

## Core Performance Specifications

This section describes the clock tree, phase-locked loop (PLL), digital signal processing (DSP), memory blocks, configuration, and JTAG specifications.

### Clock Tree Specifications

Table 30 lists the clock tree specifications for Stratix V devices.

**Table 30. Clock Tree Performance for Stratix V Devices <sup>(1)</sup>**

| Symbol                    | Performance              |                       |        | Unit |
|---------------------------|--------------------------|-----------------------|--------|------|
|                           | C1, C2, C2L, I2, and I2L | C3, I3, I3L, and I3YY | C4, I4 |      |
| Global and Regional Clock | 717                      | 650                   | 580    | MHz  |
| Periphery Clock           | 550                      | 500                   | 500    | MHz  |

**Note to Table 30:**

(1) The Stratix V ES devices are limited to 600 MHz core clock tree performance.

## PLL Specifications

Table 31 lists the Stratix V PLL specifications when operating in both the commercial junction temperature range (0° to 85°C) and the industrial junction temperature range (–40° to 100°C).

**Table 31. PLL Specifications for Stratix V Devices (Part 1 of 3)**

| Symbol                   | Parameter                                                                                                | Min | Typ | Max                | Unit |
|--------------------------|----------------------------------------------------------------------------------------------------------|-----|-----|--------------------|------|
| $f_{IN}$                 | Input clock frequency (C1, C2, C2L, I2, and I2L speed grades)                                            | 5   | —   | 800 <sup>(1)</sup> | MHz  |
|                          | Input clock frequency (C3, I3, I3L, and I3YY speed grades)                                               | 5   | —   | 800 <sup>(1)</sup> | MHz  |
|                          | Input clock frequency (C4, I4 speed grades)                                                              | 5   | —   | 650 <sup>(1)</sup> | MHz  |
| $f_{INPFD}$              | Input frequency to the PFD                                                                               | 5   | —   | 325                | MHz  |
| $f_{FINPFD}$             | Fractional Input clock frequency to the PFD                                                              | 50  | —   | 160                | MHz  |
| $f_{VCO}$ <sup>(9)</sup> | PLL VCO operating range (C1, C2, C2L, I2, I2L speed grades)                                              | 600 | —   | 1600               | MHz  |
|                          | PLL VCO operating range (C3, I3, I3L, I3YY speed grades)                                                 | 600 | —   | 1600               | MHz  |
|                          | PLL VCO operating range (C4, I4 speed grades)                                                            | 600 | —   | 1300               | MHz  |
| $t_{EINDUTY}$            | Input clock or external feedback clock input duty cycle                                                  | 40  | —   | 60                 | %    |
| $f_{OUT}$                | Output frequency for an internal global or regional clock (C1, C2, C2L, I2, I2L speed grades)            | —   | —   | 717 <sup>(2)</sup> | MHz  |
|                          | Output frequency for an internal global or regional clock (C3, I3, I3L speed grades)                     | —   | —   | 650 <sup>(2)</sup> | MHz  |
|                          | Output frequency for an internal global or regional clock (C4, I4 speed grades)                          | —   | —   | 580 <sup>(2)</sup> | MHz  |
| $f_{OUT\_EXT}$           | Output frequency for an external clock output (C1, C2, C2L, I2, I2L speed grades)                        | —   | —   | 800 <sup>(2)</sup> | MHz  |
|                          | Output frequency for an external clock output (C3, I3, I3L speed grades)                                 | —   | —   | 667 <sup>(2)</sup> | MHz  |
|                          | Output frequency for an external clock output (C4, I4 speed grades)                                      | —   | —   | 553 <sup>(2)</sup> | MHz  |
| $t_{OUTDUTY}$            | Duty cycle for a dedicated external clock output (when set to 50%)                                       | 45  | 50  | 55                 | %    |
| $t_{FCOMP}$              | External feedback clock compensation time                                                                | —   | —   | 10                 | ns   |
| $f_{DYCONFIGCLK}$        | Dynamic Configuration Clock used for <code>mgmt_clk</code> and <code>scanclk</code>                      | —   | —   | 100                | MHz  |
| $t_{LOCK}$               | Time required to lock from the end-of-device configuration or deassertion of <code>areset</code>         | —   | —   | 1                  | ms   |
| $t_{DLOCK}$              | Time required to lock dynamically (after switchover or reconfiguring any non-post-scale counters/delays) | —   | —   | 1                  | ms   |
| $f_{CLBW}$               | PLL closed-loop low bandwidth                                                                            | —   | 0.3 | —                  | MHz  |
|                          | PLL closed-loop medium bandwidth                                                                         | —   | 1.5 | —                  | MHz  |
|                          | PLL closed-loop high bandwidth <sup>(7)</sup>                                                            | —   | 4   | —                  | MHz  |
| $t_{PLL\_PSERR}$         | Accuracy of PLL phase shift                                                                              | —   | —   | ±50                | ps   |
| $t_{ARESET}$             | Minimum pulse width on the <code>areset</code> signal                                                    | 10  | —   | —                  | ns   |

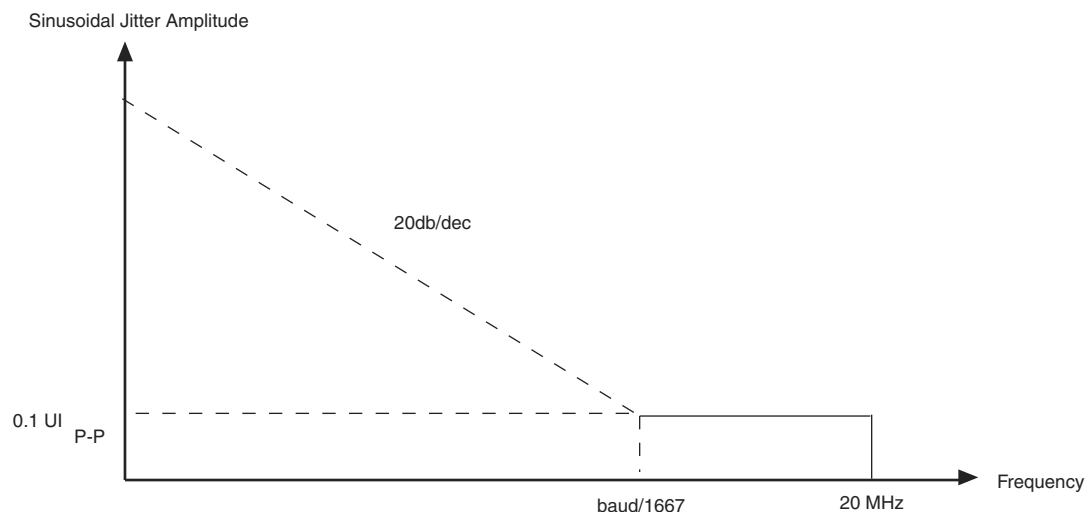
**Table 36. High-Speed I/O Specifications for Stratix V Devices <sup>(1)</sup>, <sup>(2)</sup> (Part 3 of 4)**

| Symbol                                                     | Conditions                                                                                                                          | C1             |     |                | C2, C2L, I2, I2L |     |                | C3, I3, I3L, I3YY |     |                | C4, I4         |     |                | Unit |
|------------------------------------------------------------|-------------------------------------------------------------------------------------------------------------------------------------|----------------|-----|----------------|------------------|-----|----------------|-------------------|-----|----------------|----------------|-----|----------------|------|
|                                                            |                                                                                                                                     | Min            | Typ | Max            | Min              | Typ | Max            | Min               | Typ | Max            | Min            | Typ | Max            |      |
| $t_{DUTY}$                                                 | Transmitter output clock duty cycle for both True and Emulated Differential I/O Standards                                           | 45             | 50  | 55             | 45               | 50  | 55             | 45                | 50  | 55             | 45             | 50  | 55             | %    |
| $t_{RISE}$ & $t_{FALL}$                                    | True Differential I/O Standards                                                                                                     | —              | —   | 160            | —                | —   | 160            | —                 | —   | 200            | —              | —   | 200            | ps   |
|                                                            | Emulated Differential I/O Standards with three external output resistor networks                                                    | —              | —   | 250            | —                | —   | 250            | —                 | —   | 250            | —              | —   | 300            | ps   |
| TCCS                                                       | True Differential I/O Standards                                                                                                     | —              | —   | 150            | —                | —   | 150            | —                 | —   | 150            | —              | —   | 150            | ps   |
|                                                            | Emulated Differential I/O Standards                                                                                                 | —              | —   | 300            | —                | —   | 300            | —                 | —   | 300            | —              | —   | 300            | ps   |
| <b>Receiver</b>                                            |                                                                                                                                     |                |     |                |                  |     |                |                   |     |                |                |     |                |      |
| True Differential I/O Standards - $f_{HSDRDP}$ (data rate) | SERDES factor J = 3 to 10 <sup>(11)</sup> , <sup>(12)</sup> , <sup>(13)</sup> , <sup>(14)</sup> , <sup>(15)</sup> , <sup>(16)</sup> | 150            | —   | 1434           | 150              | —   | 1434           | 150               | —   | 1250           | 150            | —   | 1050           | Mbps |
|                                                            | SERDES factor J $\geq 4$                                                                                                            | 150            | —   | 1600           | 150              | —   | 1600           | 150               | —   | 1600           | 150            | —   | 1250           | Mbps |
|                                                            | LVDS RX with DPA <sup>(12)</sup> , <sup>(14)</sup> , <sup>(15)</sup> , <sup>(16)</sup>                                              | 150            | —   | 1600           | 150              | —   | 1600           | 150               | —   | 1600           | 150            | —   | 1250           | Mbps |
|                                                            | SERDES factor J = 2, uses DDR Registers                                                                                             | <sup>(6)</sup> | —   | <sup>(7)</sup> | <sup>(6)</sup>   | —   | <sup>(7)</sup> | <sup>(6)</sup>    | —   | <sup>(7)</sup> | <sup>(6)</sup> | —   | <sup>(7)</sup> | Mbps |
|                                                            | SERDES factor J = 1, uses SDR Register                                                                                              | <sup>(6)</sup> | —   | <sup>(7)</sup> | <sup>(6)</sup>   | —   | <sup>(7)</sup> | <sup>(6)</sup>    | —   | <sup>(7)</sup> | <sup>(6)</sup> | —   | <sup>(7)</sup> | Mbps |

**Table 38. LVDS Soft-CDR/DPA Sinusoidal Jitter Mask Values for a Data Rate  $\geq 1.25$  Gbps**

| Jitter Frequency (Hz) |            | Sinusoidal Jitter (UI) |
|-----------------------|------------|------------------------|
| F1                    | 10,000     | 25.000                 |
| F2                    | 17,565     | 25.000                 |
| F3                    | 1,493,000  | 0.350                  |
| F4                    | 50,000,000 | 0.350                  |

Figure 9 shows the LVDS soft-CDR/DPA sinusoidal jitter tolerance specification for a data rate  $< 1.25$  Gbps.

**Figure 9. LVDS Soft-CDR/DPA Sinusoidal Jitter Tolerance Specification for a Data Rate  $< 1.25$  Gbps**

### DLL Range, DQS Logic Block, and Memory Output Clock Jitter Specifications

Table 39 lists the DLL range specification for Stratix V devices. The DLL is always in 8-tap mode in Stratix V devices.

**Table 39. DLL Range Specifications for Stratix V Devices <sup>(1)</sup>**

| C1      | C2, C2L, I2, I2L | C3, I3, I3L, I3YY | C4,I4   | Unit |
|---------|------------------|-------------------|---------|------|
| 300-933 | 300-933          | 300-890           | 300-890 | MHz  |

**Note to Table 39:**

- (1) Stratix V devices support memory interface frequencies lower than 300 MHz, although the reference clock that feeds the DLL must be at least 300 MHz. To support interfaces below 300 MHz, multiply the reference clock feeding the DLL to ensure the frequency is within the supported range of the DLL.

Table 40 lists the DQS phase offset delay per stage for Stratix V devices.

**Table 40. DQS Phase Offset Delay Per Setting for Stratix V Devices <sup>(1), (2)</sup> (Part 1 of 2)**

| Speed Grade      | Min | Max | Unit |
|------------------|-----|-----|------|
| C1               | 8   | 14  | ps   |
| C2, C2L, I2, I2L | 8   | 14  | ps   |
| C3,I3, I3L, I3YY | 8   | 15  | ps   |

**Table 46. JTAG Timing Parameters and Values for Stratix V Devices**

| Symbol     | Description                              | Min | Max               | Unit |
|------------|------------------------------------------|-----|-------------------|------|
| $t_{JPH}$  | JTAG port hold time                      | 5   | —                 | ns   |
| $t_{JPCO}$ | JTAG port clock to output                | —   | 11 <sup>(1)</sup> | ns   |
| $t_{JPZX}$ | JTAG port high impedance to valid output | —   | 14 <sup>(1)</sup> | ns   |
| $t_{JPXZ}$ | JTAG port valid output to high impedance | —   | 14 <sup>(1)</sup> | ns   |

**Notes to Table 46:**

- (1) A 1 ns adder is required for each  $V_{CCIO}$  voltage step down from 3.0 V. For example,  $t_{JPCO}$  = 12 ns if  $V_{CCIO}$  of the TDO I/O bank = 2.5 V, or 13 ns if it equals 1.8 V.
- (2) The minimum TCK clock period is 167 ns if VCCBAT is within the range 1.2V-1.5V when you perform the volatile key programming.

## Raw Binary File Size

For the POR delay specification, refer to the “POR Delay Specification” section of the “Configuration, Design Security, and Remote System Upgrades in Stratix V Devices”.

Table 47 lists the uncompressed raw binary file (.rbf) sizes for Stratix V devices.

**Table 47. Uncompressed .rbf Sizes for Stratix V Devices**

| Family       | Device | Package                      | Configuration .rbf Size (bits) | IOCSR .rbf Size (bits) <sup>(4), (5)</sup> |
|--------------|--------|------------------------------|--------------------------------|--------------------------------------------|
| Stratix V GX | 5SGXA3 | H35, F40, F35 <sup>(2)</sup> | 213,798,880                    | 562,392                                    |
|              |        | H29, F35 <sup>(3)</sup>      | 137,598,880                    | 564,504                                    |
|              | 5SGXA4 | —                            | 213,798,880                    | 563,672                                    |
|              | 5SGXA5 | —                            | 269,979,008                    | 562,392                                    |
|              | 5SGXA7 | —                            | 269,979,008                    | 562,392                                    |
|              | 5SGXA9 | —                            | 342,742,976                    | 700,888                                    |
|              | 5SGXAB | —                            | 342,742,976                    | 700,888                                    |
|              | 5SGXB5 | —                            | 270,528,640                    | 584,344                                    |
|              | 5SGXB6 | —                            | 270,528,640                    | 584,344                                    |
|              | 5SGXB9 | —                            | 342,742,976                    | 700,888                                    |
|              | 5SGXBB | —                            | 342,742,976                    | 700,888                                    |
| Stratix V GT | 5SGTC5 | —                            | 269,979,008                    | 562,392                                    |
|              | 5SGTC7 | —                            | 269,979,008                    | 562,392                                    |
| Stratix V GS | 5SGSD3 | —                            | 137,598,880                    | 564,504                                    |
|              | 5SGSD4 | F1517                        | 213,798,880                    | 563,672                                    |
|              |        | —                            | 137,598,880                    | 564,504                                    |
|              | 5SGSD5 | —                            | 213,798,880                    | 563,672                                    |
|              | 5SGSD6 | —                            | 293,441,888                    | 565,528                                    |
|              | 5SGSD8 | —                            | 293,441,888                    | 565,528                                    |

Table 51 lists the timing parameters for Stratix V devices for FPP configuration when the DCLK-to-DATA [ ] ratio is more than 1.

**Table 51. FPP Timing Parameters for Stratix V Devices When the DCLK-to-DATA[ ] Ratio is >1 <sup>(1)</sup>**

| Symbol                     | Parameter                                         | Minimum                                                         | Maximum              | Units   |
|----------------------------|---------------------------------------------------|-----------------------------------------------------------------|----------------------|---------|
| $t_{CF2CD}$                | nCONFIG low to CONF_DONE low                      | —                                                               | 600                  | ns      |
| $t_{CF2ST0}$               | nCONFIG low to nSTATUS low                        | —                                                               | 600                  | ns      |
| $t_{CFG}$                  | nCONFIG low pulse width                           | 2                                                               | —                    | $\mu$ s |
| $t_{STATUS}$               | nSTATUS low pulse width                           | 268                                                             | 1,506 <sup>(2)</sup> | $\mu$ s |
| $t_{CF2ST1}$               | nCONFIG high to nSTATUS high                      | —                                                               | 1,506 <sup>(2)</sup> | $\mu$ s |
| $t_{CF2CK}$ <sup>(5)</sup> | nCONFIG high to first rising edge on DCLK         | 1,506                                                           | —                    | $\mu$ s |
| $t_{ST2CK}$ <sup>(5)</sup> | nSTATUS high to first rising edge of DCLK         | 2                                                               | —                    | $\mu$ s |
| $t_{DSU}$                  | DATA [ ] setup time before rising edge on DCLK    | 5.5                                                             | —                    | ns      |
| $t_{DH}$                   | DATA [ ] hold time after rising edge on DCLK      | $N-1/f_{DCLK}$ <sup>(5)</sup>                                   | —                    | s       |
| $t_{CH}$                   | DCLK high time                                    | $0.45 \times 1/f_{MAX}$                                         | —                    | s       |
| $t_{CL}$                   | DCLK low time                                     | $0.45 \times 1/f_{MAX}$                                         | —                    | s       |
| $t_{CLK}$                  | DCLK period                                       | $1/f_{MAX}$                                                     | —                    | s       |
| $f_{MAX}$                  | DCLK frequency (FPP $\times 8/\times 16$ )        | —                                                               | 125                  | MHz     |
|                            | DCLK frequency (FPP $\times 32$ )                 | —                                                               | 100                  | MHz     |
| $t_R$                      | Input rise time                                   | —                                                               | 40                   | ns      |
| $t_F$                      | Input fall time                                   | —                                                               | 40                   | ns      |
| $t_{CD2UM}$                | CONF_DONE high to user mode <sup>(3)</sup>        | 175                                                             | 437                  | $\mu$ s |
| $t_{CD2CU}$                | CONF_DONE high to CLKUSR enabled                  | $4 \times$ maximum DCLK period                                  | —                    | —       |
| $t_{CD2UMC}$               | CONF_DONE high to user mode with CLKUSR option on | $t_{CD2CU} + (8576 \times \text{CLKUSR period})$ <sup>(4)</sup> | —                    | —       |

**Notes to Table 51:**

- (1) Use these timing parameters when you use the decompression and design security features.
- (2) You can obtain this value if you do not delay configuration by extending the nCONFIG or nSTATUS low pulse width.
- (3) The minimum and maximum numbers apply only if you use the internal oscillator as the clock source for initializing the device.
- (4) To enable the CLKUSR pin as the initialization clock source and to obtain the maximum frequency specification on these pins, refer to the Initialization section of the “Configuration, Design Security, and Remote System Upgrades in Stratix V Devices” chapter.
- (5) N is the DCLK-to-DATA ratio and  $f_{DCLK}$  is the DCLK frequency the system is operating.
- (6) If nSTATUS is monitored, follow the  $t_{ST2CK}$  specification. If nSTATUS is not monitored, follow the  $t_{CF2CK}$  specification.

## Active Serial Configuration Timing

Table 52 lists the DCLK frequency specification in the AS configuration scheme.

**Table 52. DCLK Frequency Specification in the AS Configuration Scheme <sup>(1), (2)</sup>**

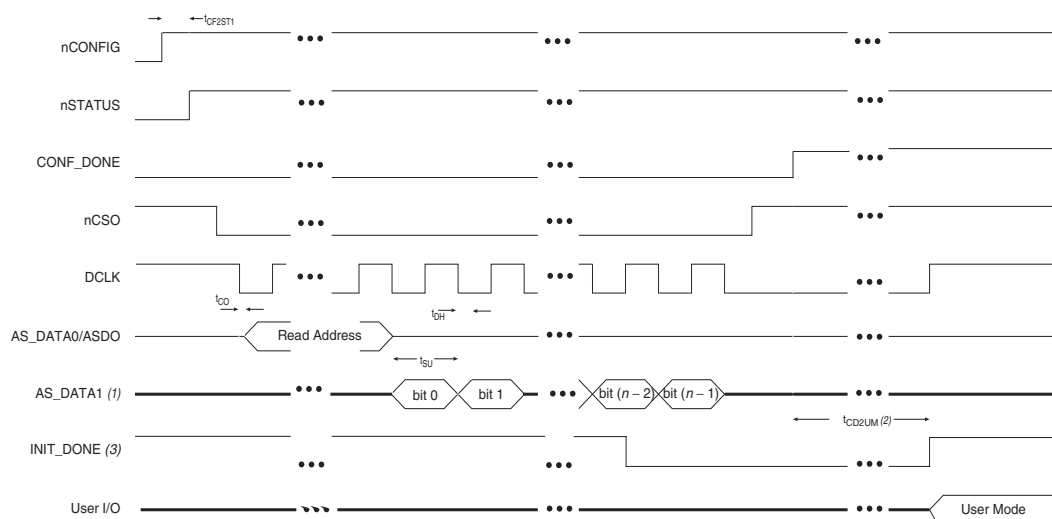
| Minimum | Typical | Maximum | Unit |
|---------|---------|---------|------|
| 5.3     | 7.9     | 12.5    | MHz  |
| 10.6    | 15.7    | 25.0    | MHz  |
| 21.3    | 31.4    | 50.0    | MHz  |
| 42.6    | 62.9    | 100.0   | MHz  |

**Notes to Table 52:**

- (1) This applies to the DCLK frequency specification when using the internal oscillator as the configuration clock source.
- (2) The AS multi-device configuration scheme does not support DCLK frequency of 100 MHz.

Figure 14 shows the single-device configuration setup for an AS ×1 mode.

**Figure 14. AS Configuration Timing**



**Notes to Figure 14:**

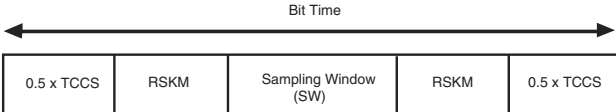
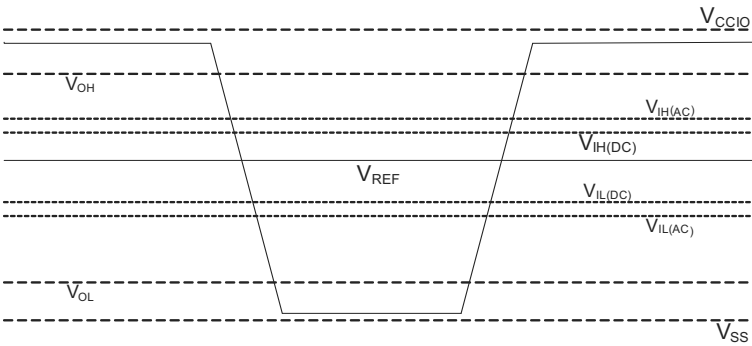
- (1) If you are using AS ×4 mode, this signal represents the AS\_DATA [3 : 0] and EPCQ sends in 4-bits of data for each DCLK cycle.
- (2) The initialization clock can be from internal oscillator or CLKUSR pin.
- (3) After the option bit to enable the INIT\_DONE pin is configured into the device, the INIT\_DONE goes low.

Table 53 lists the timing parameters for AS ×1 and AS ×4 configurations in Stratix V devices.

**Table 53. AS Timing Parameters for AS ×1 and AS ×4 Configurations in Stratix V Devices <sup>(1), (2)</sup> (Part 1 of 2)**

| Symbol   | Parameter                                   | Minimum | Maximum | Units |
|----------|---------------------------------------------|---------|---------|-------|
| $t_{CO}$ | DCLK falling edge to AS_DATA0/ASDO output   | —       | 2       | ns    |
| $t_{SU}$ | Data setup time before falling edge on DCLK | 1.5     | —       | ns    |
| $t_H$    | Data hold time after falling edge on DCLK   | 0       | —       | ns    |

Table 60. Glossary (Part 3 of 4)

| Letter | Subject                                      | Definitions                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        |
|--------|----------------------------------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| S      | SW (sampling window)                         | <p>Timing Diagram—the period of time during which the data must be valid in order to capture it correctly. The setup and hold times determine the ideal strobe position within the sampling window, as shown:</p>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |
|        | Single-ended voltage referenced I/O standard | <p>The JEDEC standard for <b>SSTL</b> and <b>HSTL</b> I/O defines both the AC and DC input signal values. The AC values indicate the voltage levels at which the receiver must meet its timing specifications. The DC values indicate the voltage levels at which the final logic state of the receiver is unambiguously defined. After the receiver input has crossed the AC value, the receiver changes to the new logic state.</p> <p>The new logic state is then maintained as long as the input stays beyond the DC threshold. This approach is intended to provide predictable receiver timing in the presence of input waveform ringing:</p> <p><i>Single-Ended Voltage Referenced I/O Standard</i></p>  |
| T      | $t_c$                                        | High-speed receiver and transmitter input and output clock period.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 |
|        | TCCS (channel-to-channel-skew)               | The timing difference between the fastest and slowest output edges, including $t_{CO}$ variation and clock skew, across channels driven by the same PLL. The clock is included in the TCCS measurement (refer to the <i>Timing Diagram</i> figure under <b>SW</b> in this table).                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  |
|        | $t_{DUTY}$                                   | <p>High-speed I/O block—Duty cycle on the high-speed transmitter output clock.</p> <p><b>Timing Unit Interval (TUI)</b></p> <p>The timing budget allowed for skew, propagation delays, and the data sampling window. (TUI = <math>1/(\text{receiver input clock frequency multiplication factor}) = t_c/w</math>)</p>                                                                                                                                                                                                                                                                                                                                                                                                                                                                              |
|        | $t_{FALL}$                                   | Signal high-to-low transition time (80-20%)                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        |
|        | $t_{INCCJ}$                                  | Cycle-to-cycle jitter tolerance on the PLL clock input.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            |
|        | $t_{OUTPJ\_IO}$                              | Period jitter on the general purpose I/O driven by a PLL.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          |
|        | $t_{OUTPJ\_DC}$                              | Period jitter on the dedicated clock output driven by a PLL.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       |
|        | $t_{RISE}$                                   | Signal low-to-high transition time (20-80%)                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        |
| U      | —                                            | —                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  |

**Table 61. Document Revision History (Part 3 of 3)**

| Date          | Version | Changes                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |
|---------------|---------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| May 2013      | 2.7     | <ul style="list-style-type: none"> <li>■ Updated Table 2, Table 6, Table 7, Table 20, Table 23, Table 27, Table 47, Table 60</li> <li>■ Added Table 24, Table 48</li> <li>■ Updated Figure 9, Figure 10, Figure 11, Figure 12</li> </ul>                                                                                                                                                                                                                                                                                                                               |
| February 2013 | 2.6     | <ul style="list-style-type: none"> <li>■ Updated Table 7, Table 9, Table 20, Table 23, Table 27, Table 30, Table 31, Table 35, Table 46</li> <li>■ Updated “Maximum Allowed Overshoot and Undershoot Voltage”</li> </ul>                                                                                                                                                                                                                                                                                                                                               |
| December 2012 | 2.5     | <ul style="list-style-type: none"> <li>■ Updated Table 3, Table 6, Table 7, Table 8, Table 23, Table 24, Table 25, Table 27, Table 30, Table 32, Table 35</li> <li>■ Added Table 33</li> <li>■ Added “Fast Passive Parallel Configuration Timing”</li> <li>■ Added “Active Serial Configuration Timing”</li> <li>■ Added “Passive Serial Configuration Timing”</li> <li>■ Added “Remote System Upgrades”</li> <li>■ Added “User Watchdog Internal Circuitry Timing Specification”</li> <li>■ Added “Initialization”</li> <li>■ Added “Raw Binary File Size”</li> </ul> |
| June 2012     | 2.4     | <ul style="list-style-type: none"> <li>■ Added Figure 1, Figure 2, and Figure 3.</li> <li>■ Updated Table 1, Table 2, Table 3, Table 6, Table 11, Table 22, Table 23, Table 27, Table 29, Table 30, Table 31, Table 32, Table 35, Table 38, Table 39, Table 40, Table 41, Table 43, Table 56, and Table 59.</li> <li>■ Various edits throughout to fix bugs.</li> <li>■ Changed title of document to <i>Stratix V Device Datasheet</i>.</li> <li>■ Removed document from the Stratix V handbook and made it a separate document.</li> </ul>                            |
| February 2012 | 2.3     | <ul style="list-style-type: none"> <li>■ Updated Table 1–22, Table 1–29, Table 1–31, and Table 1–31.</li> </ul>                                                                                                                                                                                                                                                                                                                                                                                                                                                        |
| December 2011 | 2.2     | <ul style="list-style-type: none"> <li>■ Added Table 2–31.</li> <li>■ Updated Table 2–28 and Table 2–34.</li> </ul>                                                                                                                                                                                                                                                                                                                                                                                                                                                    |
| November 2011 | 2.1     | <ul style="list-style-type: none"> <li>■ Added Table 2–2 and Table 2–21 and updated Table 2–5 with information about Stratix V GT devices.</li> <li>■ Updated Table 2–11, Table 2–13, Table 2–20, and Table 2–25.</li> <li>■ Various edits throughout to fix SPRs.</li> </ul>                                                                                                                                                                                                                                                                                          |
| May 2011      | 2.0     | <ul style="list-style-type: none"> <li>■ Updated Table 2–4, Table 2–18, Table 2–19, Table 2–21, Table 2–22, Table 2–23, and Table 2–24.</li> <li>■ Updated the “DQ Logic Block and Memory Output Clock Jitter Specifications” title.</li> <li>■ Chapter moved to Volume 1.</li> <li>■ Minor text edits.</li> </ul>                                                                                                                                                                                                                                                     |
| December 2010 | 1.1     | <ul style="list-style-type: none"> <li>■ Updated Table 1–2, Table 1–4, Table 1–19, and Table 1–23.</li> <li>■ Converted chapter to the new template.</li> <li>■ Minor text edits.</li> </ul>                                                                                                                                                                                                                                                                                                                                                                           |
| July 2010     | 1.0     | Initial release.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       |

