Intel - 5SGXEA7K3F40I4N Datasheet





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Details

Product Status	Obsolete
Number of LABs/CLBs	234720
Number of Logic Elements/Cells	622000
Total RAM Bits	51200000
Number of I/O	696
Number of Gates	-
Voltage - Supply	0.82V ~ 0.88V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	1517-BBGA, FCBGA
Supplier Device Package	1517-FBGA (40x40)
Purchase URL	https://www.e-xfl.com/product-detail/intel/5sgxea7k3f40i4n

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This section lists the functional operating limits for the AC and DC parameters for Stratix V devices. Table 6 lists the steady-state voltage and current values expected from Stratix V devices. Power supply ramps must all be strictly monotonic, without plateaus.

Table 6. Recommended Operating Conditions for Stratix V Devices (Part 1 of 2)

Symbol	Description	Condition	Min ⁽⁴⁾	Тур	Max ⁽⁴⁾	Unit
	Core voltage and periphery circuitry power supply (C1, C2, I2, and I3YY speed grades)	_	0.87	0.9	0.93	V
V _{CC}	Core voltage and periphery circuitry power supply (C2L, C3, C4, I2L, I3, I3L, and I4 speed grades) ⁽³⁾		0.82	0.85	0.88	V
V _{CCPT}	Power supply for programmable power technology	_	1.45	1.50	1.55	V
V _{CC_AUX}	Auxiliary supply for the programmable power technology		2.375	2.5	2.625	V
VI (1)	I/O pre-driver (3.0 V) power supply	_	2.85	3.0	3.15	V
VCCPD	I/O pre-driver (2.5 V) power supply		2.375	2.5	2.625	V
	I/O buffers (3.0 V) power supply	_	2.85	3.0	3.15	V
	I/O buffers (2.5 V) power supply		2.375	2.5	2.625	V
	I/O buffers (1.8 V) power supply	_	1.71	1.8	1.89	V
V _{CCIO}	I/O buffers (1.5 V) power supply	_	1.425	1.5	1.575	V
	I/O buffers (1.35 V) power supply		1.283	1.35	1.45	V
	I/O buffers (1.25 V) power supply	_	1.19	1.25	1.31	V
	I/O buffers (1.2 V) power supply	_	1.14	1.2	1.26	V
	Configuration pins (3.0 V) power supply		2.85	3.0	3.15	V
V _{CCPGM}	Configuration pins (2.5 V) power supply	-	2.375	2.5	2.625	V
	Configuration pins (1.8 V) power supply	-	1.71	1.8	1.89	V
V _{CCA_FPLL}	PLL analog voltage regulator power supply		2.375	2.5	2.625	V
V _{CCD_FPLL}	PLL digital voltage regulator power supply	-	1.45	1.5	1.55	V
V _{CCBAT} (2)	Battery back-up power supply (For design security volatile key register)	_	1.2	_	3.0	V
VI	DC input voltage	_	-0.5	—	3.6	V
V ₀	Output voltage		0	_	V _{CCIO}	V
т	Operating junction temperature	Commercial	0	—	85	°C
IJ		Industrial	-40	_	100	°C

Symbol	Description	Devices	Minimum ⁽⁴⁾	Typical	Maximum ⁽⁴⁾	Unit
			0.82	0.85	0.88	V
V _{CCR_GXBR}	Receiver analog power supply (right side)	GX, GS, GT	0.87	0.90	0.93	
(2)	neceiver analog power supply (right side)		0.97	1.0	1.03	
			1.03	1.05	1.07	
V _{CCR_GTBR}	Receiver analog power supply for GT channels (right side)	GT	1.02	1.05	1.08	V
			0.82	0.85	0.88	
V _{CCT_GXBL}	Transmitter analog newer supply (left side)		0.87	0.90	0.93	v
	Transmitter analog power supply (left side)	un, uo, ui	0.97	1.0	1.03	v
			1.03	1.05	1.07	
		GX, GS, GT	0.82	0.85	0.88	V
V _{CCT GXBR}	Transmitter analog newer supply (right side)		0.87	0.90	0.93	
(2) _	Transmitter analog power supply (light side)		0.97	1.0	1.03	
			1.03	1.05	1.07	
V_{CCT_GTBR}	Transmitter analog power supply for GT channels (right side)	GT	1.02	1.05	1.08	V
V_{CCL_GTBR}	Transmitter clock network power supply	GT	1.02	1.05	1.08	V
V _{CCH_GXBL}	Transmitter output buffer power supply (left side)	GX, GS, GT	1.425	1.5	1.575	V
V _{CCH_GXBR}	Transmitter output buffer power supply (right side)	GX, GS, GT	1.425	1.5	1.575	V

Table 7.	Recommended Transceiver Power Supply Operating Conditions for Stratix V GX ,	GS , and GT Devices
(Part 2	of 2)	

Notes to Table 7:

(1) This supply must be connected to 3.0 V if the CMU PLL, receiver CDR, or both, are configured at a base data rate > 6.5 Gbps. Up to 6.5 Gbps, you can connect this supply to either 3.0 V or 2.5 V.

(2) Refer to Table 8 to select the correct power supply level for your design.

(3) When using ATX PLLs, the supply must be 3.0 V.

(4) This value describes the budget for the DC (static) power supply tolerance and does not include the dynamic tolerance requirements. Refer to the PDN tool for the additional budget for the dynamic tolerance requirements.

				Calibratio	n Accuracy		
Symbol	Description	Conditions	C1	C2,I2	C3,I3, I3YY	C4,14	Unit
50-Ω R _S	Internal series termination with calibration (50- Ω setting)	V _{CCI0} = 3.0, 2.5, 1.8, 1.5, 1.2 V	±15	±15	±15	±15	%
34- Ω and 40- Ω R _S	Internal series termination with calibration (34- Ω and 40- Ω setting)	V _{CCI0} = 1.5, 1.35, 1.25, 1.2 V	±15	±15	±15	±15	%
48-Ω, 60-Ω, 80-Ω, and 240-Ω R _S	Internal series termination with calibration (48- Ω , 60- Ω , 80- Ω , and 240- Ω setting)	V _{CCI0} = 1.2 V	±15	±15	±15	±15	%
50-Ω R _T	Internal parallel termination with calibration (50-Ω setting)	V _{CCI0} = 2.5, 1.8, 1.5, 1.2 V	-10 to +40	-10 to +40	-10 to +40	-10 to +40	%
20-Ω, 30-Ω, 40-Ω,60-Ω, and 120-Ω R _T	Internal parallel termination with calibration ($20 - \Omega$, $30 - \Omega$, $40 - \Omega$, $60 - \Omega$, and $120 - \Omega$ setting)	V _{CCI0} = 1.5, 1.35, 1.25 V	-10 to +40	-10 to +40	-10 to +40	-10 to +40	%
60- Ω and 120- Ω R _T	Internal parallel termination with calibration (60-Ω and 120-Ω setting)	V _{CCI0} = 1.2	-10 to +40	-10 to +40	-10 to +40	-10 to +40	%
$25-\Omega \\ R_{S_left_shift}$	Internal left shift series termination with calibration ($25-\Omega$ R _{S_left_shift} setting)	V _{CCI0} = 3.0, 2.5, 1.8, 1.5, 1.2 V	±15	±15	±15	±15	%

Table II. OUI Valiblation Accuracy specifications for Stratix V Devices' / (Latt 2 OF	Table 11.	OCT Calibration A	ccuracy Specificati	ons for Stratix V D	Devices ⁽¹⁾ (Part 2 of
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Note to Table 11:

(1) OCT calibration accuracy is valid at the time of calibration only.

Table 12 lists the Stratix V OCT without calibration resistance to PVT changes.

Table 12.	OCT Without Calibration	Resistance 1	Tolerance	Specifications	for Stratix	V Devices	(Part 1	of 2)
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			Resistance Tolerance					
Symbol	Description	Conditions	C1	C2,I2	C3, I3, I3YY	C4, I4	Unit	
25-Ω R, 50-Ω R _S	Internal series termination without calibration (25-Ω setting)	$V_{CCIO} = 3.0$ and 2.5 V	±30	±30	±40	±40	%	
25-Ω R _S	Internal series termination without calibration (25-Ω setting)	V _{CCI0} = 1.8 and 1.5 V	±30	±30	±40	±40	%	
25-Ω R _S	Internal series termination without calibration (25-Ω setting)	V _{CCI0} = 1.2 V	±35	±35	±50	±50	%	

Internal Weak Pull-Up Resistor

Table 16 lists the weak pull-up resistor values for Stratix V devices.

Symbol	Description	V _{CCIO} Conditions (V) ⁽³⁾	Value ⁽⁴⁾	Unit
		3.0 ±5%	25	kΩ
		2.5 ±5%	25	kΩ
R _{PU}	Value of the I/O pin pull-up resistor before	1.8 ±5%	25	kΩ
	and during configuration, as well as user mode if you enable the programmable	1.5 ±5%	25	kΩ
	pull-up resistor option.	1.35 ±5%	25	kΩ
		1.25 ±5%	25	kΩ
		1.2 ±5%	25	kΩ

Table 16. Internal Weak Pull-Up Resistor for Stratix V Devices (1), (2)

Notes to Table 16:

(1) All I/O pins have an option to enable the weak pull-up resistor except the configuration, test, and JTAG pins.

(2) The internal weak pull-down feature is only available for the JTAG TCK pin. The typical value for this internal weak pull-down resistor is approximately 25 k Ω .

- (3) The pin pull-up resistance values may be lower if an external source drives the pin higher than V_{CCIO}.
- (4) These specifications are valid with a $\pm 10\%$ tolerance to cover changes over PVT.

I/O Standard Specifications

Table 17 through Table 22 list the input voltage (V_{IH} and V_{IL}), output voltage (V_{OH} and V_{OL}), and current drive characteristics (I_{OH} and I_{OL}) for various I/O standards supported by Stratix V devices. These tables also show the Stratix V device family I/O standard specifications. The V_{OL} and V_{OH} values are valid at the corresponding I_{OH} and I_{OL}, respectively.

For an explanation of the terms used in Table 17 through Table 22, refer to "Glossary" on page 65. For tolerance calculations across all SSTL and HSTL I/O standards, refer to Altera knowledge base solution rd07262012_486.

I/O		V _{CCIO} (V)		VII	∟ (V)	VIH	(V)	V _{OL} (V)	V _{OH} (V)	I _{OL}	I _{oh}
Standard	Min	Тур	Max	Min	Max	Min	Max	Max	Min	(mA)	(mA)
LVTTL	2.85	3	3.15	-0.3	0.8	1.7	3.6	0.4	2.4	2	-2
LVCMOS	2.85	3	3.15	-0.3	0.8	1.7	3.6	0.2	$V_{CCIO} - 0.2$	0.1	-0.1
2.5 V	2.375	2.5	2.625	-0.3	0.7	1.7	3.6	0.4	2	1	-1
1.8 V	1.71	1.8	1.89	-0.3	0.35 * V _{CCIO}	0.65 * V _{CCIO}	V _{CCI0} + 0.3	0.45	V _{CCI0} – 0.45	2	-2
1.5 V	1.425	1.5	1.575	-0.3	0.35 * V _{CCI0}	0.65 * V _{CCI0}	V _{CCI0} + 0.3	0.25 * V _{CCIO}	0.75 * V _{CCIO}	2	-2
1.2 V	1.14	1.2	1.26	-0.3	0.35 * V _{CCI0}	0.65 * V _{CCI0}	V _{CCI0} + 0.3	0.25 * V _{CCIO}	0.75 * V _{CCIO}	2	-2

Table 17. Single-Ended I/O Standards for Stratix V Devices

- You typically use the interactive Excel-based Early Power Estimator before designing the FPGA to get a magnitude estimate of the device power. The Quartus II PowerPlay Power Analyzer provides better quality estimates based on the specifics of the design after you complete place-and-route. The PowerPlay Power Analyzer can apply a combination of user-entered, simulation-derived, and estimated signal activities that, when combined with detailed circuit models, yields very accurate power estimates.
- ***** For more information about power estimation tools, refer to the *PowerPlay Early Power Estimator User Guide* and the *PowerPlay Power Analysis* chapter in the *Quartus II Handbook*.

Table 23. Transceiver Specifications for Stratix V GX and GS Devices ⁽¹⁾ (Part 6 of 7)

Symbol/	Conditions	Trai	nsceive Grade	r Speed 1	Trar	isceive Grade	r Speed 2	Tran	isceive Grade	er Speed e 3	Unit
Description		Min	Тур	Max	Min	Тур	Max	Min	Тур	Max	
Inter-transceiver block transmitter channel-to- channel skew	xN PMA bonded mode	_	_	500	_	_	500	_	_	500	ps
CMU PLL	•									•	
Supported Data Range	_	600	_	12500	600	_	12500	600	_	8500/ 10312.5 (24)	Mbps
t _{pll_powerdown} ⁽¹⁵⁾	—	1			1			1			μs
t _{pll_lock} ⁽¹⁶⁾		—		10	—	_	10	—	_	10	μs
ATX PLL											
	VCO post-divider L=2	8000	_	14100	8000	_	12500	8000	_	8500/ 10312.5 (24)	Mbps
Supported Data	L=4	4000	_	7050	4000	_	6600	4000	—	6600	Mbps
Rate Range	L=8	2000		3525	2000		3300	2000		3300	Mbps
Rate Range	L=8, Local/Central Clock Divider =2	1000	_	1762.5	1000	_	1762.5	1000	_	1762.5	Mbps
t _{pll_powerdown} (15)	—	1	_	—	1	_	—	1	_	—	μs
t _{pll_lock} (16)	—		—	10		—	10	—		10	μs
fPLL	•										
Supported Data Range	_	600	_	3250/ 3125 ⁽²⁵⁾	600	_	3250/ 3125 ⁽²⁵⁾	600	_	3250/ 3125 ⁽²⁵⁾	Mbps
t _{pll_powerdown} ⁽¹⁵⁾	_	1	—		1	—		1			μs

Symbol/ Description	Conditions	Transceiver Speed Grade 1			Transceiver Speed Grade 2			Transceiver Speed Grade 3			Unit
		Min	Тур	Max	Min	Тур	Max	Min	Тур	Max	
t _{pll_lock} (16)	_			10			10		_	10	μs

Table 23. Transceiver Specifications for Stratix V GX and GS Devices ⁽¹⁾ (Part 7 of 7)

Notes to Table 23:

(2) The reference clock common mode voltage is equal to the V_{CCR_GXB} power supply level.

(3) This supply must be connected to 1.0 V if the transceiver is configured at a data rate > 6.5 Gbps, and to 1.05 V if configured at a data rate > 10.3 Gbps when DFE is used. For data rates up to 6.5 Gbps, you can connect this supply to 0.85 V.

- (4) This supply follows VCCR_GXB.
- (5) The device cannot tolerate prolonged operation at this absolute maximum.
- (6) The differential eye opening specification at the receiver input pins assumes that **Receiver Equalization** is disabled. If you enable **Receiver Equalization**, the receiver circuitry can tolerate a lower minimum eye opening, depending on the equalization level.
- (7) The Quartus II software automatically selects the appropriate slew rate depending on the configured data rate or functional mode.
- (8) The input reference clock frequency options depend on the data rate and the device speed grade.
- (9) The line data rate may be limited by PCS-FPGA interface speed grade.
- (10) Refer to Figure 1 for the GX channel AC gain curves. The total effective AC gain is the AC gain minus the DC gain.
- (11) t_{LTR} is the time required for the receive CDR to lock to the input reference clock frequency after coming out of reset.
- (12) t_{LTD} is time required for the receiver CDR to start recovering valid data after the rx_is_lockedtodata signal goes high.
- (13) t_{LTD_manual} is the time required for the receiver CDR to start recovering valid data after the rx_is_lockedtodata signal goes high when the CDR is functioning in the manual mode.
- (14) $t_{LTR_LTD_manual}$ is the time the receiver CDR must be kept in lock to reference (LTR) mode after the rx_is_lockedtoref signal goes high when the CDR is functioning in the manual mode.
- (15) $t_{pll_powerdown}$ is the PLL powerdown minimum pulse width.
- (16) t_{pll lock} is the time required for the transmitter CMU/ATX PLL to lock to the input reference clock frequency after coming out of reset.
- (17) To calculate the REFCLK rms phase jitter requirement for PCIe at reference clock frequencies other than 100 MHz, use the following formula: REFCLK rms phase jitter at f(MHz) = REFCLK rms phase jitter at 100 MHz × 100/f.
- (18) The maximum peak to peak differential input voltage V_{ID} after device configuration is equal to 4 × (absolute V_{MAX} for receiver pin V_{ICM}).
- (19) For ES devices, R_{BEF} is 2000 $\Omega \pm 1\%$.
- (20) To calculate the REFCLK phase noise requirement at frequencies other than 622 MHz, use the following formula: REFCLK phase noise at f(MHz) = REFCLK phase noise at 622 MHz + 20*log(f/622).
- (21) SFP/+ optical modules require the host interface to have RD+/- differentially terminated with 100 Ω. The internal OCT feature is available after the Stratix V FPGA configuration is completed. Altera recommends that FPGA configuration is completed before inserting the optical module. Otherwise, minimize unnecessary removal and insertion with unconfigured devices.
- (22) Refer to Figure 2.
- (23) For oversampling designs to support data rates less than the minimum specification, the CDR needs to be in LTR mode only.
- (24) I3YY devices can achieve data rates up to 10.3125 Gbps.
- (25) When you use fPLL as a TXPLL of the transceiver.
- (26) REFCLK performance requires to meet transmitter REFCLK phase noise specification.
- (27) Minimum eye opening of 85 mV is only for the unstressed input eye condition.

⁽¹⁾ Speed grades shown in Table 23 refer to the PMA Speed Grade in the device ordering code. The maximum data rate could be restricted by the Core/PCS speed grade. Contact your Altera Sales Representative for the maximum data rate specifications in each speed grade combination offered. For more information about device ordering codes, refer to the Stratix V Device Overview.

Table 27 shows the V_{OD} settings for the GX channel.

Symbol	V _{op} Setting	V _{od} Value (mV)	V _{op} Setting	V _{op} Value (mV)
	0 (1)	0	32	640
	1 (1)	20	33	660
	2 (1)	40	34	680
	3 (1)	60	35	700
	4 (1)	80	36	720
	5 ⁽¹⁾	100	37	740
	6	120	38	760
	7	140	39	780
	8	160	40	800
	9	180	41	820
	10	200	42	840
	11	220	43	860
	12	240	44	880
	13	260	45	900
	14	280	46	920
V_{0D} differential peak to peak	15	300	47	940
typical ⁽³⁾	16	320	48	960
	17	340	49	980
	18	360	50	1000
	19	380	51	1020
	20	400	52	1040
	21	420	53	1060
	22	440	54	1080
	23	460	55	1100
	24	480	56	1120
	25	500	57	1140
	26	520	58	1160
	27	540	59	1180
	28	560	60	1200
	29	580	61	1220
	30	600	62	1240
	31	620	63	1260

Table 27. Typical V_{0D} Setting for GX Channel, TX Termination = 100 $\Omega^{\left(2\right)}$

Note to Table 27:

(1) If TX termination resistance = 100Ω , this VOD setting is illegal.

(2) The tolerance is +/-20% for all VOD settings except for settings 2 and below.

(3) Refer to Figure 2.

Table 28. Tra	nsceiver Specifi	cations for Stra	tix V GT Devices	(Part 5 of 5) ⁽¹⁾
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Symbol/ Description	Conditions	S	Transceivei peed Grade	2	ן Sr	Unit		
		Min	Тур	Max	Min	Тур	Max	
t _{pll_lock} ⁽¹⁴⁾	—	—	_	10	—	—	10	μs

Notes to Table 28:

- (1) Speed grades shown refer to the PMA Speed Grade in the device ordering code. The maximum data rate could be restricted by the Core/PCS speed grade. Contact your Altera Sales Representative for the maximum data rate specifications in each speed grade combination offered. For more information about device ordering codes, refer to the Stratix V Device Overview.
- (2) The reference clock common mode voltage is equal to the VCCR_GXB power supply level.
- (3) The device cannot tolerate prolonged operation at this absolute maximum.
- (4) The differential eye opening specification at the receiver input pins assumes that receiver equalization is disabled. If you enable receiver equalization, the receiver circuitry can tolerate a lower minimum eye opening, depending on the equalization level.
- (5) Refer to Figure 5 for the GT channel AC gain curves. The total effective AC gain is the AC gain minus the DC gain.
- (6) Refer to Figure 6 for the GT channel DC gain curves.
- (7) CFP2 optical modules require the host interface to have the receiver data pins differentially terminated with 100 Ω. The internal OCT feature is available after the Stratix V FPGA configuration is completed. Altera recommends that FPGA configuration is completed before inserting the optical module. Otherwise, minimize unnecessary removal and insertion with unconfigured devices.
- (8) Specifications for this parameter are the same as for Stratix V GX and GS devices. See Table 23 for specifications.
- (9) t_{1 TR} is the time required for the receive CDR to lock to the input reference clock frequency after coming out of reset.
- (10) t_{LTD} is time required for the receiver CDR to start recovering valid data after the rx is lockedtodata signal goes high.
- (11) t_{LTD_manual} is the time required for the receiver CDR to start recovering valid data after the rx_is_lockedtodata signal goes high when the CDR is functioning in the manual mode.
- (12) t_{LTR_LTD_manual} is the time the receiver CDR must be kept in lock to reference (LTR) mode after the rx_is_lockedtoref signal goes high when the CDR is functioning in the manual mode.
- (13) tpll_powerdown is the PLL powerdown minimum pulse width.
- (14) tpll lock is the time required for the transmitter CMU/ATX PLL to lock to the input reference clock frequency after coming out of reset.
- (15) To calculate the REFCLK rms phase jitter requirement for PCle at reference clock frequencies other than 100 MHz, use the following formula: REFCLK rms phase jitter at f(MHz) = REFCLK rms phase jitter at 100 MHz × 100/f.
- (16) The maximum peak to peak differential input voltage V_{ID} after device configuration is equal to 4 × (absolute V_{MAX} for receiver pin V_{ICM}).
- (17) For ES devices, RREF is 2000 $\Omega \pm 1\%$.
- (18) To calculate the REFCLK phase noise requirement at frequencies other than 622 MHz, use the following formula: REFCLK phase noise at f(MHz) = REFCLK phase noise at 622 MHz + 20*log(f/622).
- (19) SFP/+ optical modules require the host interface to have RD+/- differentially terminated with 100 Ω. The internal OCT feature is available after the Stratix V FPGA configuration is completed. Altera recommends that FPGA configuration is completed before inserting the optical module. Otherwise, minimize unnecessary removal and insertion with unconfigured devices.
- (20) Refer to Figure 4.
- (21) For oversampling design to support data rates less than the minimum specification, the CDR needs to be in LTR mode only.
- (22) This supply follows VCCR_GXB for both GX and GT channels.
- (23) When you use fPLL as a TXPLL of the transceiver.

- XFI
- ASI
- HiGig/HiGig+
- HiGig2/HiGig2+
- Serial Data Converter (SDC)
- GPON
- SDI
- SONET
- Fibre Channel (FC)
- PCIe
- QPI
- SFF-8431

Download the Stratix V Characterization Report Tool to view the characterization report summary for these protocols.

Core Performance Specifications

This section describes the clock tree, phase-locked loop (PLL), digital signal processing (DSP), memory blocks, configuration, and JTAG specifications.

Clock Tree Specifications

Table 30 lists the clock tree specifications for Stratix V devices.

Table 30. Clock Tree Performance for Stratix V Devices (1)

	Performance								
Symbol	C1, C2, C2L, I2, and I2L	C3, I3, I3L, and I3YY	C4, I4	Unit					
Global and Regional Clock	717	650	580	MHz					
Periphery Clock	550	500	500	MHz					

Note to Table 30:

(1) The Stratix V ES devices are limited to 600 MHz core clock tree performance.

PLL Specifications

Table 31 lists the Stratix V PLL specifications when operating in both the commercial junction temperature range (0° to 85° C) and the industrial junction temperature range (-40° to 100° C).

Table 31. PLL Specifications for Stratix V Devices (Part 1 of 3)

Symbol	Parameter	Min	Тур	Max	Unit
	Input clock frequency (C1, C2, C2L, I2, and I2L speed grades)	5		800 (1)	MHz
f _{IN}	Input clock frequency (C3, I3, I3L, and I3YY speed grades)	5		800 (1)	MHz
	Input clock frequency (C4, I4 speed grades)	5	—	650 ⁽¹⁾	MHz
f _{INPFD}	Input frequency to the PFD	5	—	325	MHz
f _{FINPFD}	Fractional Input clock frequency to the PFD	50	—	160	MHz
	PLL VCO operating range (C1, C2, C2L, I2, I2L speed grades)	600	_	1600	MHz
f _{VCO} (9)	PLL VCO operating range (C3, I3, I3L, I3YY speed grades)	600		1600	MHz
	PLL VCO operating range (C4, I4 speed grades)	600	—	1300	MHz
t _{einduty}	Input clock or external feedback clock input duty cycle	40	—	60	%
	Output frequency for an internal global or regional clock (C1, C2, C2L, I2, I2L speed grades)	_	_	717 ⁽²⁾	MHz
f _{out}	Output frequency for an internal global or regional clock (C3, I3, I3L speed grades)			650 ⁽²⁾	MHz
	Output frequency for an internal global or regional clock (C4, I4 speed grades)			580 ⁽²⁾	MHz
	Output frequency for an external clock output (C1, C2, C2L, I2, I2L speed grades)			800 ⁽²⁾	MHz
f _{OUT_EXT}	Output frequency for an external clock output (C3, I3, I3L speed grades)			667 ⁽²⁾	MHz
	Output frequency for an external clock output (C4, I4 speed grades)			553 ⁽²⁾	MHz
t _{outduty}	Duty cycle for a dedicated external clock output (when set to 50%)	45	50	55	%
t _{FCOMP}	External feedback clock compensation time	_		10	ns
f _{dyconfigclk}	Dynamic Configuration Clock used for mgmt_clk and scanclk		_	100	MHz
t _{LOCK}	Time required to lock from the end-of-device configuration or deassertion of areset			1	ms
t _{DLOCK}	Time required to lock dynamically (after switchover or reconfiguring any non-post-scale counters/delays)			1	ms
	PLL closed-loop low bandwidth	—	0.3	—	MHz
f _{CLBW}	PLL closed-loop medium bandwidth	—	1.5	—	MHz
	PLL closed-loop high bandwidth (7)	—	4	-	MHz
t _{PLL_PSERR}	Accuracy of PLL phase shift	—	—	±50	ps
t _{ARESET}	Minimum pulse width on the areset signal	10	—	_	ns

Symbol	Parameter	Min	Тур	Max	Unit
+ (3) (4)	Input clock cycle-to-cycle jitter ($f_{REF} \ge 100 \text{ MHz}$)			0.15	UI (p-p)
LINCCJ (0), (1)	Input clock cycle-to-cycle jitter (f _{REF} < 100 MHz)	-750		+750	ps (p-p)
+ (5)	Period Jitter for dedicated clock output (f_{OUT} \geq 100 MHz)	_	_	175 ⁽¹⁾	ps (p-p)
CUTPJ_DC	Period Jitter for dedicated clock output (f _{OUT} < 100 MHz)	_	_	17.5 ⁽¹⁾	mUI (p-p)
+ (5)	Period Jitter for dedicated clock output in fractional PLL ($f_{OUT} \ge 100 \text{ MHz}$)	_	_	250 ⁽¹¹⁾ , 175 ⁽¹²⁾	ps (p-p)
^L FOUTPJ_DC	Period Jitter for dedicated clock output in fractional PLL (f _{OUT} < 100 MHz)	ParameterMincycle-to-cycle jitter ($f_{REF} < 100 \text{ MHz}$)	_	25 ⁽¹¹⁾ , 17.5 ⁽¹²⁾	mUI (p-p)
+ (5)	Cycle-to-Cycle Jitter for a dedicated clock output ($f_{\text{OUT}} \geq 100 \text{ MHz})$		_	175	ps (p-p)
COUTCCJ_DC	Cycle-to-Cycle Jitter for a dedicated clock output $(f_{OUT} < 100 \text{ MHz})$		_	17.5	mUI (p-p)
+ (5)	Cycle-to-cycle Jitter for a dedicated clock output in fractional PLL ($f_{OUT} \ge 100 \text{ MHz}$)		_	250 ⁽¹¹⁾ , 175 ⁽¹²⁾	ps (p-p)
FOUTCCJ_DC	Cycle-to-cycle Jitter for a dedicated clock output in fractional PLL ($f_{OUT} < 100 \text{ MHz}$)+		_	25 ⁽¹¹⁾ , 17.5 ⁽¹²⁾	mUI (p-p)
t _{outpj 10} (5),	Period Jitter for a clock output on a regular I/O in integer PLL ($f_{OUT} \ge 100 \text{ MHz}$)		_	600	ps (p-p)
(8)	Period Jitter for a clock output on a regular I/O $(f_{OUT} < 100 \text{ MHz})$	edicated clock output	60	mUI (p-p)	
t _{foutpj 10} ^{(5),}	Period Jitter for a clock output on a regular I/O in fractional PLL ($f_{OUT} \ge 100 \text{ MHz}$)	_	_	600 ⁽¹⁰⁾	ps (p-p)
(8), (11)	Period Jitter for a clock output on a regular I/O in fractional PLL (f _{OUT} < 100 MHz)	_	_	60 ⁽¹⁰⁾	mUI (p-p)
t _{outccj_io} (5),	Cycle-to-cycle Jitter for a clock output on a regular I/O in integer PLL ($f_{OUT} \geq 100 \mbox{ MHz})$	_	_	600	ps (p-p)
(8)	Cycle-to-cycle Jitter for a clock output on a regular I/O in integer PLL (f _{OUT} < 100 MHz)	_	_	60 ⁽¹⁰⁾	mUI (p-p)
t _{FOUTCCJ 10} (5),	Cycle-to-cycle Jitter for a clock output on a regular I/O in fractional PLL ($f_{OUT} \ge 100$ MHz)		_	600 ⁽¹⁰⁾	ps (p-p)
(8), (11)	Cycle-to-cycle Jitter for a clock output on a regular I/O in fractional PLL (f _{OUT} < 100 MHz)	_	_	60	mUI (p-p)
t _{CASC OUTPJ DC}	Period Jitter for a dedicated clock output in cascaded PLLs ($f_{OUT} \ge 100 \text{ MHz}$)	_	_	175	ps (p-p)
(5), (6)	Period Jitter for a dedicated clock output in cascaded PLLs (f_{OUT} < 100 MHz)	_	_	17.5	mUI (p-p)
f _{DRIFT}	Frequency drift after PFDENA is disabled for a duration of 100 μs		_	±10	%
dK _{BIT}	Bit number of Delta Sigma Modulator (DSM)	8	24	32	Bits
k _{VALUE}	Numerator of Fraction	128	8388608	2147483648	—

Table 31. PLL Specifications for Stratix V Devices (Part 2 of 3)

	Ocuditions		C1		C2,	C2L, I	2, I2L	C3,	13, 131	., I 3YY	C4,I4			
Symbol	Conditions	Min	Тур	Max	Min	Тур	Max	Min	Тур	Max	Min	Тур	Max	Unit
t _{duty}	Transmitter output clock duty cycle for both True and Emulated Differential I/O Standards	45	50	55	45	50	55	45	50	55	45	50	55	%
	True Differential I/O Standards	_	_	160	_	_	160	_	_	200	_	_	200	ps
t _{rise} & t _{fall}	Emulated Differential I/O Standards with three external output resistor networks			250			250			250			300	ps
	True Differential I/O Standards	_	_	150	_	_	150	_	_	150	_	_	150	ps
TCCS	Emulated Differential I/O Standards			300			300	_		300			300	ps
Receiver														
	SERDES factor J = 3 to 10 (11), (12), (13), (14), (15), (16)	150		1434	150	_	1434	150	_	1250	150	_	1050	Mbps
True Differential	SERDES factor J ≥ 4 LVDS RX with DPA (12), (14), (15), (16)	150	_	1600	150	_	1600	150	_	1600	150	_	1250	Mbps
- f _{HSDRDPA} (data rate)	SERDES factor J = 2, uses DDR Registers	(6)		(7)	(6)	_	(7)	(6)	_	(7)	(6)	_	(7)	Mbps
	SERDES factor J = 1, uses SDR Register	(6)	_	(7)	(6)	_	(7)	(6)	_	(7)	(6)		(7)	Mbps

Table 36. High-Speed I/O Specifications for Stratix V Devices (1), (2) (Part 3 of 4)

Figure 7 shows the dynamic phase alignment (DPA) lock time specifications with the DPA PLL calibration option enabled.

Figure 7. DPA Lock Time Specification with DPA PLL Calibration Enabled

rx_reset			
rx_dpa_locked			<u> </u>
···			-

Table 37 lists the DPA lock time specifications for Stratix V devices.

Table 37. DPA Lock Time Specifications for Stratix V GX Devices Only (1), (2), (3)

Standard	Training Pattern	Number of Data Transitions in One Repetition of the Training Pattern	Number of Repetitions per 256 Data Transitions ⁽⁴⁾	Maximum
SPI-4	00000000001111111111	2	128	640 data transitions
Parallel Rapid I/O	00001111	2	128	640 data transitions
	10010000	4	64	640 data transitions
Miscellaneous	10101010	8	32	640 data transitions
Wiscenareous	01010101	8	32	640 data transitions

Notes to Table 37:

(1) The DPA lock time is for one channel.

(2) One data transition is defined as a 0-to-1 or 1-to-0 transition.

(3) The DPA lock time stated in this table applies to both commercial and industrial grade.

(4) This is the number of repetitions for the stated training pattern to achieve the 256 data transitions.

Figure 8 shows the **LVDS** soft-clock data recovery (CDR)/DPA sinusoidal jitter tolerance specification for a data rate \geq 1.25 Gbps. Table 38 lists the **LVDS** soft-CDR/DPA sinusoidal jitter tolerance specification for a data rate \geq 1.25 Gbps.





Clock Network	Parameter	Symbol	C1		C2, C2L, I2, I2L		C3, I3, I3L, I3YY		C4,14		Unit
			Min	Max	Min	Max	Min	Max	Min	Max	
	Clock period jitter	$t_{JIT(per)}$	-25	25	-25	25	-30	30	-35	35	ps
PHY Clock	Cycle-to-cycle period jitter	$t_{\rm JIT(cc)}$	-50	50	-50	50	-60	60	-70	70	ps
	Duty cycle jitter	$t_{JIT(duty)}$	-37.5	37.5	-37.5	37.5	-45	45	-56	56	ps

Table 42. Memory Output Clock Jitter Specification for Stratix V Devices (1), (Part 2 of 2) (2), (3)

Notes to Table 42:

(1) The clock jitter specification applies to the memory output clock pins generated using differential signal-splitter and DDIO circuits clocked by a PLL output routed on a PHY, regional, or global clock network as specified. Altera recommends using PHY clock networks whenever possible.

(2) The clock jitter specification applies to the memory output clock pins clocked by an integer PLL.

(3) The memory output clock jitter is applicable when an input jitter of 30 ps peak-to-peak is applied with bit error rate (BER) -12, equivalent to 14 sigma.

OCT Calibration Block Specifications

Table 43 lists the OCT calibration block specifications for Stratix V devices.

Table 43. OCT Calibration Block Specifications for Stratix V Devices

Symbol	Description	Min	Тур	Max	Unit
OCTUSRCLK	Clock required by the OCT calibration blocks	—	—	20	MHz
T _{OCTCAL}	Number of OCTUSRCLK clock cycles required for OCT $\rm R_S/R_T$ calibration		1000	_	Cycles
T _{OCTSHIFT}	Number of OCTUSRCLK clock cycles required for the OCT code to shift out	_	32	_	Cycles
T _{RS_RT}	Time required between the dyn_term_ctrl and oe signal transitions in a bidirectional I/O buffer to dynamically switch between OCT R_S and R_T (Figure 10)		2.5		ns

Figure 10 shows the timing diagram for the oe and dyn_term_ctrl signals.

Figure 10. Timing Diagram for oe and dyn_term_ctrl Signals



Duty Cycle Distortion (DCD) Specifications

Table 44 lists the worst-case DCD for Stratix V devices.

Table 44. Worst-Case DCD on Stratix V I/O Pins (1)

Symbol	C1 C2, C2L			L, 12, 12L	, I2, I2L C3, I3, I3L, I3YY			4,14	Unit
	Min	Max	Min	Max	Min	Max	Min	Max	
Output Duty Cycle	45	55	45	55	45	55	45	55	%

Note to Table 44:

(1) The DCD numbers do not cover the core clock network.

Configuration Specification

POR Delay Specification

Power-on reset (POR) delay is defined as the delay between the time when all the power supplies monitored by the POR circuitry reach the minimum recommended operating voltage to the time when the nSTATUS is released high and your device is ready to begin configuration.



For more information about the POR delay, refer to the *Hot Socketing and Power-On Reset in Stratix V Devices* chapter.

Table 45 lists the fast and standard POR delay specification.

Table 45. Fast and Standard POR Delay Specification (1)

POR Delay	Minimum	Maximum	
Fast	4 ms	12 ms	
Standard	100 ms	300 ms	

Note to Table 45:

(1) You can select the POR delay based on the MSEL settings as described in the MSEL Pin Settings section of the "Configuration, Design Security, and Remote System Upgrades in Stratix V Devices" chapter.

JTAG Configuration Specifications

Table 46 lists the JTAG timing parameters and values for Stratix V devices.

Table 46. JTAG Timing Parameters and Values for Stratix V Devices

Symbol	Description	Min	Max	Unit
t _{JCP}	TCK clock period ⁽²⁾	30		ns
t _{JCP}	TCK clock period ⁽²⁾	167	—	ns
t _{JCH}	TCK clock high time ⁽²⁾	14	—	ns
t _{JCL}	TCK clock low time ⁽²⁾	14		ns
t _{JPSU (TDI)}	TDI JTAG port setup time	2	—	ns
t _{JPSU (TMS)}	TMS JTAG port setup time	3	_	ns

Symbol	Description	Min	Max	Unit
t _{JPH}	JTAG port hold time	5	—	ns
t _{JPCO}	JTAG port clock to output	—	11 ⁽¹⁾	ns
t _{JPZX}	JTAG port high impedance to valid output	—	14 ⁽¹⁾	ns
t _{JPXZ}	JTAG port valid output to high impedance	—	14 ⁽¹⁾	ns

Table 46. JTAG Timing Parameters and Values for Stratix V Devices

Notes to Table 46:

(1) A 1 ns adder is required for each V_{CCI0} voltage step down from 3.0 V. For example, $t_{JPC0} = 12$ ns if V_{CCI0} of the TDO I/O bank = 2.5 V, or 13 ns if it equals 1.8 V.

(2) The minimum TCK clock period is 167 ns if VCCBAT is within the range 1.2V-1.5V when you perform the volatile key programming.

Raw Binary File Size

For the POR delay specification, refer to the "POR Delay Specification" section of the "Configuration, Design Security, and Remote System Upgrades in Stratix V Devices".

Table 47 lists the uncompressed raw binary file (.rbf) sizes for Stratix V devices.

Family	Family Device Package		Configuration .rbf Size (bits)	IOCSR .rbf Size (bits) ^{(4), (5)}
	500742	H35, F40, F35 ⁽²⁾	213,798,880	562,392
	JOUNAS	H29, F35 ⁽³⁾	137,598,880	564,504
	5SGXA4	—	213,798,880	563,672
	5SGXA5	—	269,979,008	562,392
	5SGXA7	—	269,979,008	562,392
Stratix V GX	5SGXA9	—	342,742,976	700,888
	5SGXAB	—	342,742,976	700,888
	5SGXB5	—	270,528,640	584,344
	5SGXB6	—	270,528,640	584,344
	5SGXB9	—	342,742,976	700,888
	5SGXBB	—	342,742,976	700,888
Strativ V CT	5SGTC5	—	269,979,008	562,392
	5SGTC7	—	269,979,008	562,392
	5SGSD3	—	137,598,880	564,504
	500004	F1517	213,798,880	563,672
Strativ V CS	J303D4		137,598,880	564,504
	5SGSD5	—	213,798,880	563,672
	5SGSD6		293,441,888	565,528
	5SGSD8	—	293,441,888	565,528

Table 47. Uncompressed .rbf Sizes for Stratix V Devices

Family	Device	Package	Configuration .rbf Size (bits)	IOCSR .rbf Size (bits) ^{(4), (5)}
Stratix $V \in (1)$	5SEE9	—	342,742,976	700,888
	5SEEB	—	342,742,976	700,888

Table 47. Uncompressed .rbf Sizes for Stratix V Devices

Notes to Table 47:

(1) Stratix V E devices do not have PCI Express® (PCIe®) hard IP. Stratix V E devices do not support the CvP configuration scheme.

(2) 36-transceiver devices.

(3) 24-transceiver devices.

(4) File size for the periphery image.

(5) The IOCSR .rbf size is specifically for the CvP feature.

Use the data in Table 47 to estimate the file size before design compilation. Different configuration file formats, such as a hexadecimal (.hex) or tabular text file (.ttf) format, have different file sizes. For the different types of configuration file and file sizes, refer to the Quartus II software. However, for a specific version of the Quartus II software, any design targeted for the same device has the same uncompressed configuration file size. If you are using compression, the file size can vary after each compilation because the compression ratio depends on your design.

• For more information about setting device configuration options, refer to *Configuration, Design Security, and Remote System Upgrades in Stratix V Devices.* For creating configuration files, refer to the *Quartus II Help.*

Table 48 lists the minimum configuration time estimates for Stratix V devices.

Table 48. Minimum Configuration Time Estimation for Stratix V Devi
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Variant	Marchar	Active Serial ⁽¹⁾		Fast Passive Parallel ⁽²⁾			
	Code	Width	DCLK (MHz)	Min Config Time (s)	Width	DCLK (MHz)	Min Config Time (s)
	٨٥	4	100	0.534	32	100	0.067
	AJ	4	100	0.344	32	100	0.043
	A4	4	100	0.534	32	100	0.067
	A5	4	100	0.675	32	100	0.084
	A7	4	100	0.675	32	100	0.084
GX	A9	4	100	0.857	32	100	0.107
	AB	4	100	0.857	32	100	0.107
	B5	4	100	0.676	32	100	0.085
	B6	4	100	0.676	32	100	0.085
	B9	4	100	0.857	32	100	0.107
	BB	4	100	0.857	32	100	0.107
ст	C5	4	100	0.675	32	100	0.084
GI	C7	4	100	0.675	32	100	0.084

Table 51 lists the timing parameters for Stratix V devices for FPP configuration when the DCLK-to-DATA [] ratio is more than 1.

Table 51.	FPP Timing	Parameters fo	r Stratix V	Devices When	the DCLK-	to-DATA[] Rati	o is >1 ((1)
							• • • •	

Symbol	Parameter	Minimum	Maximum	Units
t _{CF2CD}	nCONFIG low to CONF_DONE low	—	600	ns
t _{CF2ST0}	nCONFIG low to nSTATUS low	—	600	ns
t _{CFG}	nCONFIG low pulse width	2		μS
t _{STATUS}	nSTATUS low pulse width	268	1,506 ⁽²⁾	μS
t _{CF2ST1}	nCONFIG high to nSTATUS high	—	1,506 ⁽²⁾	μS
t _{CF2CK} (5)	nCONFIG high to first rising edge on DCLK	1,506		μS
t _{ST2CK} (5)	nSTATUS high to first rising edge of DCLK	2		μS
t _{DSU}	DATA [] setup time before rising edge on DCLK	5.5		ns
t _{DH}	DATA [] hold time after rising edge on DCLK	N-1/f _{DCLK} (5)		S
t _{CH}	DCLK high time	$0.45\times 1/f_{MAX}$		S
t _{CL}	DCLK low time	$0.45\times 1/f_{MAX}$		S
t _{CLK}	DCLK period	1/f _{MAX}		S
f	DCLK frequency (FPP ×8/×16)	—	125	MHz
IMAX	DCLK frequency (FPP ×32)	—	100	MHz
t _R	Input rise time	—	40	ns
t _F	Input fall time	—	40	ns
t _{CD2UM}	CONF_DONE high to user mode ⁽³⁾	175	437	μS
t _{CD2CU}	CONF_DONE high to CLKUSR enabled	4 × maximum DCLK period	_	_
t _{CD2UMC}	CONF_DONE high to user mode with CLKUSR option on	t _{CD2CU} + (8576 × CLKUSR period) ⁽⁴⁾	_	_

Notes to Table 51:

- (1) Use these timing parameters when you use the decompression and design security features.
- (2) You can obtain this value if you do not delay configuration by extending the nCONFIG or nSTATUS low pulse width.
- (3) The minimum and maximum numbers apply only if you use the internal oscillator as the clock source for initializing the device.
- (4) To enable the CLKUSR pin as the initialization clock source and to obtain the maximum frequency specification on these pins, refer to the Initialization section of the "Configuration, Design Security, and Remote System Upgrades in Stratix V Devices" chapter.
- (5) N is the DCLK-to-DATA ratio and f_{DCLK} is the DCLK frequency the system is operating.
- (6) If nSTATUS is monitored, follow the t_{ST2CK} specification. If nSTATUS is not monitored, follow the t_{CF2CK} specification.

Table 60. Glossary (Part 2 of 4)

Letter	Subject	Definitions
G H I	JTAG Timing Specifications	High-speed I/O block—Deserialization factor (width of parallel data bus). JTAG Timing Specifications: TMS
K L M N O		
Ρ	PLL Specifications	Diagram of PLL Specifications (1)
Q	_	—
R	RL	Receiver differential input discrete resistor (external to the Stratix V device).