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#### Intel - 5SGXEA7N2F40C2 Datasheet



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#### Understanding <u>Embedded - FPGAs (Field</u> <u>Programmable Gate Array)</u>

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

#### **Applications of Embedded - FPGAs**

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

#### Details

Product Status	Obsolete
Number of LABs/CLBs	234720
Number of Logic Elements/Cells	622000
Total RAM Bits	51200000
Number of I/O	600
Number of Gates	-
Voltage - Supply	0.87V ~ 0.93V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	1517-BBGA, FCBGA
Supplier Device Package	1517-FBGA (40x40)
Purchase URL	https://www.e-xfl.com/product-detail/intel/5sgxea7n2f40c2

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

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<b>Transceiver Speed</b>				Core Spe	ed Grade			
Grade	C1	C2, C2L	C3	C4	<b>12, 12L</b>	13, 13L	<b>I</b> 3YY	14
3 GX channel—8.5 Gbps	_	Yes	Yes	Yes	_	Yes	Yes <sup>(4)</sup>	Yes

#### Table 1. Stratix V GX and GS Commercial and Industrial Speed Grade Offering <sup>(1), (2), (3)</sup> (Part 2 of 2)

Notes to Table 1:

(1) C = Commercial temperature grade; I = Industrial temperature grade.

(2) Lower number refers to faster speed grade.

(3) C2L, I2L, and I3L speed grades are for low-power devices.

(4) I3YY speed grades can achieve up to 10.3125 Gbps.

Table 2 lists the industrial and commercial speed grades for the Stratix V GT devices. **Table 2. Stratix V GT Commercial and Industrial Speed Grade Offering** <sup>(1)</sup>, <sup>(2)</sup>

Transseiver Speed Grade	Core Speed Grade							
Transceiver Speeu draue	C1	C2	12	13				
2 GX channel—12.5 Gbps GT channel—28.05 Gbps	Yes	Yes	_	_				
3 GX channel—12.5 Gbps GT channel—25.78 Gbps	Yes	Yes	Yes	Yes				

#### Notes to Table 2:

(1) C = Commercial temperature grade; I = Industrial temperature grade.

(2) Lower number refers to faster speed grade.

## **Absolute Maximum Ratings**

Absolute maximum ratings define the maximum operating conditions for Stratix V devices. The values are based on experiments conducted with the devices and theoretical modeling of breakdown and damage mechanisms. The functional operation of the device is not implied for these conditions.



Conditions other than those listed in Table 3 may cause permanent damage to the device. Additionally, device operation at the absolute maximum ratings for extended periods of time may have adverse effects on the device.

TANIC J. ANSULULC MAXIMUM NALINYS IVI SUALIX V DEVICES (FAIL I UI Z)	Table 3.	<b>Absolute Maximum</b>	Ratings	for Stratix \	/ Devices	(Part 1 of 2)
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Symbol	Description	Minimum	Maximum	Unit
V <sub>CC</sub>	Power supply for core voltage and periphery circuitry	-0.5	1.35	V
V <sub>CCPT</sub>	Power supply for programmable power technology	-0.5	1.8	V
V <sub>CCPGM</sub>	Power supply for configuration pins	-0.5	3.9	V
V <sub>CC_AUX</sub>	Auxiliary supply for the programmable power technology	-0.5	3.4	V
V <sub>CCBAT</sub>	Battery back-up power supply for design security volatile key register	-0.5	3.9	V
V <sub>CCPD</sub>	I/O pre-driver power supply	-0.5	3.9	V
V <sub>CCIO</sub>	I/O power supply	-0.5	3.9	V

Table 5 lists the maximum allowed input overshoot voltage and the duration of the overshoot voltage as a percentage of device lifetime. The maximum allowed overshoot duration is specified as a percentage of high time over the lifetime of the device. A DC signal is equivalent to 100% of the duty cycle. For example, a signal that overshoots to 3.95 V can be at 3.95 V for only ~21% over the lifetime of the device; for a device lifetime of 10 years, the overshoot duration amounts to ~2 years.

		saring transitions		
Symbol	Description	Condition (V)	Overshoot Duration as % @ T <sub>J</sub> = 100°C	Unit
		3.8	100	%
		3.85	64	%
		3.9	36	%
		3.95	21	%
Vi (AC)	AC input voltage	4	12	%
		4.05	7	%
		4.1	4	%
		4.15	2	%
		4.2	1	%

Table 5. Maximum Allowed Overshoot During Transitions

#### Figure 1. Stratix V Device Overshoot Duration



Symbol	Description	Condition	Min <sup>(4)</sup>	Тур	Max <sup>(4)</sup>	Unit
t <sub>RAMP</sub>	Power supply ramp time	Standard POR	200 µs	_	100 ms	—
	Fower supply ramp time	Fast POR	200 µs		4 ms	

#### Table 6. Recommended Operating Conditions for Stratix V Devices (Part 2 of 2)

#### Notes to Table 6:

(1)  $V_{CCPD}$  must be 2.5 V when  $V_{CCI0}$  is 2.5, 1.8, 1.5, 1.35, 1.25 or 1.2 V.  $V_{CCPD}$  must be 3.0 V when  $V_{CCI0}$  is 3.0 V.

(2) If you do not use the design security feature in Stratix V devices, connect V<sub>CCBAT</sub> to a 1.2- to 3.0-V power supply. Stratix V power-on-reset (POR) circuitry monitors V<sub>CCBAT</sub>. Stratix V devices will not exit POR if V<sub>CCBAT</sub> stays at logic low.

(3) C2L and I2L can also be run at 0.90 V for legacy boards that were designed for the C2 and I2 speed grades.

(4) The power supply value describes the budget for the DC (static) power supply tolerance and does not include the dynamic tolerance requirements. Refer to the PDN tool for the additional budget for the dynamic tolerance requirements.

Table 7 lists the transceiver power supply recommended operating conditions for Stratix V GX, GS, and GT devices.

# Table 7. Recommended Transceiver Power Supply Operating Conditions for Stratix V GX, GS, and GT Devices (Part 1 of 2)

Symbol	Description	Devices	Minimum <sup>(4)</sup>	Typical	Maximum <sup>(4)</sup>	Unit	
V <sub>CCA GXBL</sub>	Transceiver channel PLL power supply (left		2.85	3.0	3.15	V	
(1), (3)	side)	un, us, ui	2.375	2.5	2.625	v	
V <sub>CCA_GXBR</sub>	Transceiver channel PLL power supply (right	CV CS	2.85	3.0	3.15	V	
(1), (3)	side)	ux, us	2.375	2.5	2.625	v	
V <sub>CCA_GTBR</sub>	Transceiver channel PLL power supply (right side)	GT	2.85	3.0	3.15	V	
	Transceiver hard IP power supply (left side; C1, C2, I2, and I3YY speed grades)	GX, GS, GT	0.87	0.9	0.93	V	
V <sub>CCHIP_L</sub>	Transceiver hard IP power supply (left side; C2L, C3, C4, I2L, I3, I3L, and I4 speed grades)	GX, GS, GT	0.82	0.85	0.88	V	
	Transceiver hard IP power supply (right side; C1, C2, I2, and I3YY speed grades)	GX, GS, GT	0.87	0.9	0.93	V	
V <sub>CCHIP_R</sub>	Transceiver hard IP power supply (right side; C2L, C3, C4, I2L, I3, I3L, and I4 speed grades)	GX, GS, GT	0.82	0.85	0.88	V	
	Transceiver PCS power supply (left side; C1, C2, I2, and I3YY speed grades)	GX, GS, GT	0.87	0.9	0.93	V	
V <sub>CCHSSI_L</sub>	Transceiver PCS power supply (left side; C2L, C3, C4, I2L, I3, I3L, and I4 speed grades)	GX, GS, GT	0.82	0.85	0.88	V	
	Transceiver PCS power supply (right side; C1, C2, I2, and I3YY speed grades)	GX, GS, GT	0.87	0.9	0.93	V	
V <sub>CCHSSI_R</sub>	Transceiver PCS power supply (right side; C2L, C3, C4, I2L, I3, I3L, and I4 speed grades)	GX, GS, GT	0.82	0.85	0.88	V	
			0.82	0.85	0.88		
V <sub>CCR_GXBL</sub>	Receiver analog nower supply (left side)		0.87	0.90	0.93	v	
(2) _	Therefore analog power supply (left Slue)	un, uo, ui	0.97	1.0	1.03	v	
			1.03	1.05	1.07		

Table 8 shows the transceiver power supply voltage requirements for various conditions.

**Table 8. Transceiver Power Supply Voltage Requirements** 

Conditions	Core Speed Grade	VCCR_GXB & VCCT_GXB <sup>(2)</sup>	VCCA_GXB	VCCH_GXB	Unit
If BOTH of the following conditions are true:	A11	1.05			
■ Data rate > 10.3 Gbps.	All	1.00			
<ul> <li>DFE is used.</li> </ul>					
If ANY of the following conditions are true <sup>(1)</sup> :			3.0		
<ul> <li>ATX PLL is used.</li> </ul>					
■ Data rate > 6.5Gbps.	All	1.0			
■ DFE (data rate ≤ 10.3 Gbps), AEQ, or EyeQ feature is used.				1.5	V
If ALL of the following	C1, C2, I2, and I3YY	0.90	2.5		
<ul> <li>ATX PLL is not used.</li> </ul>					
■ Data rate $\leq$ 6.5Gbps.	C2L, C3, C4, I2L, I3, I3L, and I4	0.85	2.5		
<ul> <li>DFE, AEQ, and EyeQ are not used.</li> </ul>					

#### Notes to Table 8:

(1) Choose this power supply voltage requirement option if you plan to upgrade your design later with any of the listed conditions.

(2) If the VCCR\_GXB and VCCT\_GXB supplies are set to 1.0 V or 1.05 V, they cannot be shared with the VCC core supply. If the VCCR\_GXB and VCCT\_GXB are set to either 0.90 V or 0.85 V, they can be shared with the VCC core supply.

#### **DC Characteristics**

This section lists the supply current, I/O pin leakage current, input pin capacitance, on-chip termination tolerance, and hot socketing specifications.

#### **Supply Current**

Supply current is the current drawn from the respective power rails used for power budgeting. Use the Excel-based Early Power Estimator (EPE) to get supply current estimates for your design because these currents vary greatly with the resources you use.

For more information about power estimation tools, refer to the *PowerPlay Early Power Estimator User Guide* and the *PowerPlay Power Analysis* chapter in the *Quartus II Handbook*.

#### I/O Pin Leakage Current

Table 9 lists the Stratix V I/O pin leakage current specifications.

Table 9.	I/O Pin	Leakage	<b>Current for</b>	Stratix V	Devices (1)
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Symbol	Description	Conditions	Min	Тур	Max	Unit
I <sub>I</sub>	Input pin	$V_I = 0 V \text{ to } V_{CCIOMAX}$	-30	_	30	μA
I <sub>OZ</sub>	Tri-stated I/O pin	$V_0 = 0 V \text{ to } V_{\text{CCIOMAX}}$	-30		30	μA

#### Note to Table 9:

(1) If  $V_0 = V_{CCI0}$  to  $V_{CCI0Max}$ , 100  $\mu$ A of leakage current per I/O is expected.

#### **Bus Hold Specifications**

Table 10 lists the Stratix V device family bus hold specifications.

Table 10. Bus Hold Parameters for Stratix V Devices

			V <sub>CCIO</sub>										
Parameter	Symbol	Conditions	1.2	2 V	1.	5 V	1.8	B V	2.5	5 V	3.0	V	Unit
			Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Low sustaining current	I <sub>SUSL</sub>	V <sub>IN</sub> > V <sub>IL</sub> (maximum)	22.5	_	25.0	_	30.0	_	50.0	_	70.0	_	μA
High sustaining current	I <sub>SUSH</sub>	V <sub>IN</sub> < V <sub>IH</sub> (minimum)	-22.5		-25.0	_	-30.0	_	-50.0	_	-70.0		μA
Low overdrive current	I <sub>odl</sub>	$0V < V_{IN} < V_{CCIO}$		120		160		200	_	300		500	μA
High overdrive current	I <sub>odh</sub>	$0V < V_{IN} < V_{CCIO}$		-120		-160		-200		-300		-500	μΑ
Bus-hold trip point	V <sub>TRIP</sub>	_	0.45	0.95	0.50	1.00	0.68	1.07	0.70	1.70	0.80	2.00	۷

#### **On-Chip Termination (OCT) Specifications**

If you enable OCT calibration, calibration is automatically performed at power-up for I/Os connected to the calibration block. Table 11 lists the Stratix V OCT termination calibration accuracy specifications.

Table 11. OCT Calibration Accuracy Specifications for Stratix V Devices <sup>(1)</sup> (Part 1 of 2)

			Calibration Accuracy						
Symbol	Description	Conditions	C1	C2,12	C3,I3, I3YY	C4,14	Unit		
25- $Ω$ R <sub>S</sub>	Internal series termination with calibration (25- $\Omega$ setting)	V <sub>CCI0</sub> = 3.0, 2.5, 1.8, 1.5, 1.2 V	±15	±15	±15	±15	%		

				Calibratio	n Accuracy		
Symbol	Description	Conditions	C1	C2,I2	C3,I3, I3YY	C4,14	Unit
50-Ω R <sub>S</sub>	Internal series termination with calibration (50- $\Omega$ setting)	V <sub>CCI0</sub> = 3.0, 2.5, 1.8, 1.5, 1.2 V	±15	±15	±15	±15	%
34- $\Omega$ and 40- $\Omega$ R <sub>S</sub>	Internal series termination with calibration (34- $\Omega$ and 40- $\Omega$ setting)	V <sub>CCI0</sub> = 1.5, 1.35, 1.25, 1.2 V	±15	±15	±15	±15	%
48-Ω, 60-Ω, 80-Ω, and 240-Ω R <sub>S</sub>	Internal series termination with calibration (48- $\Omega$ , 60- $\Omega$ , 80- $\Omega$ , and 240- $\Omega$ setting)	V <sub>CCI0</sub> = 1.2 V	±15	±15	±15	±15	%
50-Ω R <sub>T</sub>	Internal parallel termination with calibration (50-Ω setting)	V <sub>CCI0</sub> = 2.5, 1.8, 1.5, 1.2 V	-10 to +40	-10 to +40	-10 to +40	-10 to +40	%
20-Ω, 30-Ω, 40-Ω,60-Ω, and 120-Ω R <sub>T</sub>	Internal parallel termination with calibration ( $20 - \Omega$ , $30 - \Omega$ , $40 - \Omega$ , $60 - \Omega$ , and $120 - \Omega$ setting)	V <sub>CCI0</sub> = 1.5, 1.35, 1.25 V	-10 to +40	-10 to +40	-10 to +40	-10 to +40	%
60- $Ω$ and 120- $Ω$ R <sub>T</sub>	Internal parallel termination with calibration (60-Ω and 120-Ω setting)	V <sub>CCI0</sub> = 1.2	-10 to +40	-10 to +40	-10 to +40	-10 to +40	%
$25-\Omega \\ R_{S\_left\_shift}$	Internal left shift series termination with calibration ( $25-\Omega$ R <sub>S_left_shift</sub> setting)	V <sub>CCI0</sub> = 3.0, 2.5, 1.8, 1.5, 1.2 V	±15	±15	±15	±15	%

Table II. OUI Valiblation Accuracy specifications for Stratix V Devices' / (Latt 2 OF	Table 11.	<b>OCT Calibration A</b>	ccuracy Specificati	ons for Stratix V D	Devices <sup>(1)</sup> (	Part 2 of
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#### Note to Table 11:

(1) OCT calibration accuracy is valid at the time of calibration only.

Table 12 lists the Stratix V OCT without calibration resistance to PVT changes.

Table 12.	OCT Without Calibration	<b>Resistance</b> 1	<b>Tolerance</b>	<b>Specifications</b>	for Stratix	<b>V</b> Devices	(Part 1	of 2)
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			<b>Resistance Tolerance</b>					
Symbol	Description	Conditions	C1	C2,I2	C3, I3, I3YY	C4, I4	Unit	
25-Ω R, 50-Ω R <sub>S</sub>	Internal series termination without calibration (25-Ω setting)	$V_{CCIO} = 3.0$ and 2.5 V	±30	±30	±40	±40	%	
25-Ω R <sub>S</sub>	Internal series termination without calibration (25-Ω setting)	V <sub>CCI0</sub> = 1.8 and 1.5 V	±30	±30	±40	±40	%	
25-Ω R <sub>S</sub>	Internal series termination without calibration (25-Ω setting)	V <sub>CCI0</sub> = 1.2 V	±35	±35	±50	±50	%	

I/O Standard	V <sub>IL(DI</sub>	<sub>c)</sub> (V)	V <sub>IH(D</sub>	<sub>C)</sub> (V)	V <sub>IL(AC)</sub> (V)	V <sub>IH(AC)</sub> (V)	V <sub>ol</sub> (V)	V <sub>oh</sub> (V)	I (mA)	l <sub>oh</sub>
i/U Stanuaru	Min	Max	Min	Max	Max	Min	Max	Min	i <sub>ol</sub> (IIIA)	(mA)
HSTL-18 Class I	—	V <sub>REF</sub> – 0.1	V <sub>REF</sub> + 0.1	_	$V_{REF} - 0.2$	V <sub>REF</sub> + 0.2	0.4	V <sub>CCI0</sub> – 0.4	8	-8
HSTL-18 Class II	_	V <sub>REF</sub> – 0.1	V <sub>REF</sub> + 0.1	_	V <sub>REF</sub> - 0.2	V <sub>REF</sub> + 0.2	0.4	V <sub>CCI0</sub> – 0.4	16	-16
HSTL-15 Class I	_	V <sub>REF</sub> – 0.1	V <sub>REF</sub> + 0.1	_	V <sub>REF</sub> - 0.2	V <sub>REF</sub> + 0.2	0.4	V <sub>CCI0</sub> – 0.4	8	-8
HSTL-15 Class II	_	V <sub>REF</sub> – 0.1	V <sub>REF</sub> + 0.1	_	V <sub>REF</sub> - 0.2	V <sub>REF</sub> + 0.2	0.4	V <sub>CCI0</sub> – 0.4	16	-16
HSTL-12 Class I	-0.15	V <sub>REF</sub> - 0.08	V <sub>REF</sub> + 0.08	V <sub>CCIO</sub> + 0.15	V <sub>REF</sub> – 0.15	V <sub>REF</sub> + 0.15	0.25* V <sub>CCI0</sub>	0.75* V <sub>CCI0</sub>	8	-8
HSTL-12 Class II	-0.15	V <sub>REF</sub> - 0.08	V <sub>REF</sub> + 0.08	V <sub>CCIO</sub> + 0.15	V <sub>REF</sub> – 0.15	V <sub>REF</sub> + 0.15	0.25* V <sub>CCI0</sub>	0.75* V <sub>CCI0</sub>	16	-16
HSUL-12	—	V <sub>REF</sub> - 0.13	V <sub>REF</sub> + 0.13	_	V <sub>REF</sub> – 0.22	V <sub>REF</sub> + 0.22	0.1* V <sub>CCIO</sub>	0.9* V <sub>CCI0</sub>	_	

#### Table 19. Single-Ended SSTL, HSTL, and HSUL I/O Standards Signal Specifications for Stratix V Devices (Part 2 of 2)

Table 20. Differential SSTL I/O Standards for Stratix V Devices

1/0 Standard		V <sub>ccio</sub> (V)		V <sub>SWIN</sub>	<sub>G(DC)</sub> (V)		V <sub>X(AC)</sub> (V)		V <sub>SWING(AC)</sub> (V)		
ijo Stanuaru	Min	Тур	Max	Min	Max	Min	Тур	Max	Min	Max	
SSTL-2 Class I, II	2.375	2.5	2.625	0.3	V <sub>CCI0</sub> + 0.6	V <sub>CCI0</sub> /2- 0.2	_	V <sub>CCI0</sub> /2 + 0.2	0.62	V <sub>CCI0</sub> + 0.6	
SSTL-18 Class I, II	1.71	1.8	1.89	0.25	V <sub>CCIO</sub> + 0.6	V <sub>CCI0</sub> /2- 0.175	_	V <sub>CCI0</sub> /2 + 0.175	0.5	V <sub>CCI0</sub> + 0.6	
SSTL-15 Class I, II	1.425	1.5	1.575	0.2	(1)	V <sub>CCI0</sub> /2- 0.15	_	V <sub>CCI0</sub> /2 + 0.15	0.35	_	
SSTL-135 Class I, II	1.283	1.35	1.45	0.2	(1)	V <sub>CCI0</sub> /2- 0.15	V <sub>CCI0</sub> /2	V <sub>CCI0</sub> /2 + 0.15	2(V <sub>IH(AC)</sub> - V <sub>REF</sub> )	2(V <sub>IL(AC)</sub> - V <sub>REF</sub> )	
SSTL-125 Class I, II	1.19	1.25	1.31	0.18	(1)	V <sub>CCI0</sub> /2- 0.15	V <sub>CCI0</sub> /2	V <sub>CCI0</sub> /2 + 0.15	2(V <sub>IH(AC)</sub> - V <sub>REF</sub> )	_	
SSTL-12 Class I, II	1.14	1.2	1.26	0.18	_	V <sub>REF</sub> 0.15	V <sub>CCI0</sub> /2	V <sub>REF</sub> + 0.15	-0.30	0.30	

Note to Table 20:

(1) The maximum value for  $V_{SWING(DC)}$  is not defined. However, each single-ended signal needs to be within the respective single-ended limits  $(V_{IH(DC)} \text{ and } V_{IL(DC)})$ .

								•	-				
I/O	V <sub>CCIO</sub> (V) V			V <sub>DIF(DC)</sub> (V)			V <sub>X(AC)</sub> (V)			V <sub>CM(DC)</sub> (V	V <sub>DIF(AC)</sub> (V)		
Standard	Min	Тур	Max	Min	Max	Min	Тур	Max	Min	Тур	Max	Min	Max
HSTL-18 Class I, II	1.71	1.8	1.89	0.2	_	0.78	_	1.12	0.78	_	1.12	0.4	_
HSTL-15 Class I, II	1.425	1.5	1.575	0.2	_	0.68	_	0.9	0.68		0.9	0.4	_

Symbol/	Conditions	Trai	nsceive Grade	r Speed 1	Trai	nsceive Grade	r Speed 2	Trar	er Speed e 3	Unit	
Description		Min	Тур	Max	Min	Тур	Max	Min	Тур	Max	
Reconfiguration clock (mgmt_clk_clk) frequency	_	100		125	100		125	100	_	125	MHz
Receiver											
Supported I/O Standards	_			1.4-V PCMI	L, 1.5-V	PCML,	2.5-V PCM	L, LVPE	CL, and	d LVDS	
Data rate (Standard PCS) (9), (23)	_	600	_	12200	600	_	12200	600	_	8500/ 10312.5 (24)	Mbps
Data rate (10G PCS) <sup>(9),</sup> <sup>(23)</sup>	_	600	_	14100	600	_	12500	600	_	8500/ 10312.5 (24)	Mbps
Absolute V <sub>MAX</sub> for a receiver pin <sup>(5)</sup>	_	_	_	1.2	_	_	1.2	_	_	1.2	V
Absolute V <sub>MIN</sub> for a receiver pin	_	-0.4	_	_	-0.4	_	_	-0.4	_	_	V
Maximum peak- to-peak differential input voltage V <sub>ID</sub> (diff p- p) before device configuration <sup>(22)</sup>	_	_	_	1.6	_	_	1.6	_		1.6	V
Maximum peak- to-peak	V <sub>CCR_GXB</sub> = 1.0 V/1.05 V (V <sub>ICM</sub> = 0.70 V)	_	_	2.0	_	_	2.0		_	2.0	V
voltage $V_{ID}$ (diff p- p) after device configuration <sup>(18)</sup> .	V <sub>CCR_GXB</sub> = 0.90 V (V <sub>ICM</sub> = 0.6 V)			2.4			2.4			2.4	V
(22)	$V_{CCR_GXB} = 0.85 V$ (V <sub>ICM</sub> = 0.6 V)			2.4			2.4		_	2.4	V
Minimum differential eye opening at receiver serial input pins <sup>(6), (22),</sup> (27)	_	85			85			85	_	_	mV

### Table 23. Transceiver Specifications for Stratix V GX and GS Devices <sup>(1)</sup> (Part 3 of 7)

Symbol/	Conditions	Trai	nsceive Grade	r Speed 1	Trai	nsceive Grade	r Speed 2	Trai	nsceive Grade	r Speed 3	Unit
Description		Min	Тур	Max	Min	Тур	Max	Min	Тур	Max	
	DC Gain Setting = 0		0	_	_	0	_	_	0	—	dB
	DC Gain Setting = 1	_	2		_	2	_	_	2	_	dB
Programmable DC gain	DC Gain Setting = 2	_	4	_	_	4	_	_	4	_	dB
	DC Gain Setting = 3	_	6	_	_	6	_	_	6	_	dB
	DC Gain Setting = 4		8			8	_		8	_	dB
Transmitter											
Supported I/O Standards	_				-	1.4-V ar	nd 1.5-V PC	ML			
Data rate (Standard PCS)	_	600	_	12200	600	_	12200	600	_	8500/ 10312.5 (24)	Mbps
Data rate (10G PCS)	_	600	_	14100	600	_	12500	600	_	8500/ 10312.5 (24)	Mbps
	85-Ω setting	_	85 ± 20%	_	_	85 ± 20%	_	_	85 ± 20%	—	Ω
Differential on-	100-Ω setting	_	100 ± 20%	_	_	100 ± 20%	_	_	100 ± 20%	_	Ω
chip termination resistors	120-Ω setting		120 ± 20%	_		120 ± 20%	_		120 ± 20%	_	Ω
	150-Ω setting	_	150 ± 20%			150 ± 20%	_		150 ± 20%	_	Ω
V <sub>OCM</sub> (AC coupled)	0.65-V setting	_	650		_	650	_	_	650	—	mV
V <sub>OCM</sub> (DC coupled)	_	_	650	_	_	650		_	650	_	mV
Rise time <sup>(7)</sup>	20% to 80%	30	—	160	30	—	160	30	—	160	ps
Fall time <sup>(7)</sup>	80% to 20%	30		160	30		160	30	—	160	ps
Intra-differential pair skew	Tx V <sub>CM</sub> = 0.5 V and slew rate of 15 ps	_	_	15			15		_	15	ps
Intra-transceiver block transmitter channel-to- channel skew	x6 PMA bonded mode	_	_	120	_	_	120	_		120	ps

#### Table 23. Transceiver Specifications for Stratix V GX and GS Devices <sup>(1)</sup> (Part 5 of 7)





Figure 3 shows the Stratix V AC gain curves for GX channels.

Figure 3. AC Gain Curves for GX Channels (full bandwidth)

Stratix V GT devices contain both GX and GT channels. All transceiver specifications for the GX channels not listed in Table 28 are the same as those listed in Table 23.

Table 28 lists the Stratix V GT transceiver specifications.

Table 29 shows the  $V_{\text{OD}}$  settings for the GT channel.

Symbol	V <sub>OD</sub> Setting	V <sub>od</sub> Value (mV)
	0	0
	1	200
V., differential neak to neak typical $(1)$	2	400
The american hear to hear thicat to	3	600
	4	800
	5	1000

#### Note:

(1) Refer to Figure 4.

Figure 6 shows the Stratix V DC gain curves for GT channels.

Figure 6. DC Gain Curves for GT Channels

#### **Transceiver Characterization**

This section summarizes the Stratix V transceiver characterization results for compliance with the following protocols:

- Interlaken
- 40G (XLAUI)/100G (CAUI)
- 10GBase-KR
- QSGMII
- XAUI
- SFI
- Gigabit Ethernet (Gbe / GIGE)
- SPAUI
- Serial Rapid IO (SRIO)
- CPRI
- OBSAI
- Hyper Transport (HT)
- SATA
- SAS
- CEI

# **PLL Specifications**

Table 31 lists the Stratix V PLL specifications when operating in both the commercial junction temperature range (0° to  $85^{\circ}$ C) and the industrial junction temperature range (-40° to  $100^{\circ}$ C).

Table 31. PLL Specifications for Stratix V Devices (Part 1 of 3)

Symbol	Parameter	Min	Тур	Max	Unit
	Input clock frequency (C1, C2, C2L, I2, and I2L speed grades)	5		800 (1)	MHz
f <sub>IN</sub>	Input clock frequency (C3, I3, I3L, and I3YY speed grades)	5		800 (1)	MHz
	Input clock frequency (C4, I4 speed grades)	5	—	650 <sup>(1)</sup>	MHz
f <sub>INPFD</sub>	Input frequency to the PFD	5	—	325	MHz
f <sub>FINPFD</sub>	Fractional Input clock frequency to the PFD	50	—	160	MHz
	PLL VCO operating range (C1, C2, C2L, I2, I2L speed grades)	600	_	1600	MHz
f <sub>VCO</sub> (9)	PLL VCO operating range (C3, I3, I3L, I3YY speed grades)	600		1600	MHz
	PLL VCO operating range (C4, I4 speed grades)	600	—	1300	MHz
t <sub>einduty</sub>	Input clock or external feedback clock input duty cycle	40	—	60	%
	Output frequency for an internal global or regional clock (C1, C2, C2L, I2, I2L speed grades)	_	_	717 <sup>(2)</sup>	MHz
f <sub>OUT</sub>	Output frequency for an internal global or regional clock (C3, I3, I3L speed grades)			650 <sup>(2)</sup>	MHz
	Output frequency for an internal global or regional clock (C4, I4 speed grades)			580 <sup>(2)</sup>	MHz
	Output frequency for an external clock output (C1, C2, C2L, I2, I2L speed grades)			800 <sup>(2)</sup>	MHz
f <sub>OUT_EXT</sub>	Output frequency for an external clock output (C3, I3, I3L speed grades)			667 <sup>(2)</sup>	MHz
	Output frequency for an external clock output (C4, I4 speed grades)			553 <sup>(2)</sup>	MHz
t <sub>outduty</sub>	Duty cycle for a dedicated external clock output (when set to <b>50%</b> )	45	50	55	%
t <sub>FCOMP</sub>	External feedback clock compensation time	_		10	ns
f <sub>dyconfigclk</sub>	Dynamic Configuration Clock used for mgmt_clk and scanclk		_	100	MHz
t <sub>LOCK</sub>	Time required to lock from the end-of-device configuration or deassertion of areset			1	ms
t <sub>DLOCK</sub>	Time required to lock dynamically (after switchover or reconfiguring any non-post-scale counters/delays)			1	ms
	PLL closed-loop low bandwidth	—	0.3	—	MHz
f <sub>CLBW</sub>	PLL closed-loop medium bandwidth	—	1.5	—	MHz
	PLL closed-loop high bandwidth (7)	—	4	-	MHz
t <sub>PLL_PSERR</sub>	Accuracy of PLL phase shift	—	—	±50	ps
t <sub>ARESET</sub>	Minimum pulse width on the areset signal	10	—	_	ns

Symbol	Parameter	Min	Тур	Max	Unit
+ (3) (4)	Input clock cycle-to-cycle jitter ( $f_{REF} \ge 100 \text{ MHz}$ )			0.15	UI (p-p)
LINCCJ (0), (1)	Input clock cycle-to-cycle jitter (f <sub>REF</sub> < 100 MHz)	-750		+750	ps (p-p)
+ (5)	Period Jitter for dedicated clock output (f_{OUT} $\geq$ 100 MHz)	_	_	175 <sup>(1)</sup>	ps (p-p)
CUTPJ_DC	Period Jitter for dedicated clock output (f <sub>OUT</sub> < 100 MHz)	_	_	17.5 <sup>(1)</sup>	mUI (p-p)
+ (5)	Period Jitter for dedicated clock output in fractional PLL ( $f_{OUT} \ge 100 \text{ MHz}$ )	_	_	250 <sup>(11)</sup> , 175 <sup>(12)</sup>	ps (p-p)
FOUTPJ_DC	Period Jitter for dedicated clock output in fractional PLL (f <sub>OUT</sub> < 100 MHz)	_	_	25 <sup>(11)</sup> , 17.5 <sup>(12)</sup>	mUI (p-p)
+ (5)	Cycle-to-Cycle Jitter for a dedicated clock output ( $f_{\text{OUT}} \geq 100 \text{ MHz})$		_	175	ps (p-p)
COUTCCJ_DC	Cycle-to-Cycle Jitter for a dedicated clock output $(f_{OUT} < 100 \text{ MHz})$		_	17.5	mUI (p-p)
+ (5)	Cycle-to-cycle Jitter for a dedicated clock output in fractional PLL ( $f_{OUT} \ge 100 \text{ MHz}$ )		_	250 <sup>(11)</sup> , 175 <sup>(12)</sup>	ps (p-p)
FOUTCCJ_DC	Cycle-to-cycle Jitter for a dedicated clock output in fractional PLL ( $f_{OUT} < 100 \text{ MHz}$ )+		_	25 <sup>(11)</sup> , 17.5 <sup>(12)</sup>	mUI (p-p)
t <sub>outpj 10</sub> (5),	Period Jitter for a clock output on a regular I/O in integer PLL ( $f_{OUT} \ge 100 \text{ MHz}$ )		_	600	ps (p-p)
(8)	Period Jitter for a clock output on a regular I/O $(f_{OUT} < 100 \text{ MHz})$		_	60	mUI (p-p)
t <sub>foutpj 10</sub> <sup>(5),</sup>	Period Jitter for a clock output on a regular I/O in fractional PLL ( $f_{OUT} \ge 100 \text{ MHz}$ )	_	_	600 <sup>(10)</sup>	ps (p-p)
(8), (11)	Period Jitter for a clock output on a regular I/O in fractional PLL (f <sub>OUT</sub> < 100 MHz)	_	_	60 <sup>(10)</sup>	mUI (p-p)
t <sub>outccj_io</sub> (5),	Cycle-to-cycle Jitter for a clock output on a regular I/O in integer PLL ( $f_{OUT} \geq 100 \mbox{ MHz})$	_	_	600	ps (p-p)
(8)	Cycle-to-cycle Jitter for a clock output on a regular I/O in integer PLL (f <sub>OUT</sub> < 100 MHz)	_	_	60 <sup>(10)</sup>	mUI (p-p)
t <sub>FOUTCCJ 10</sub> (5),	Cycle-to-cycle Jitter for a clock output on a regular I/O in fractional PLL ( $f_{OUT} \ge 100$ MHz)		_	600 <sup>(10)</sup>	ps (p-p)
(8), (11)	Cycle-to-cycle Jitter for a clock output on a regular I/O in fractional PLL (f <sub>OUT</sub> < 100 MHz)	_	_	60	mUI (p-p)
t <sub>CASC OUTPJ DC</sub>	Period Jitter for a dedicated clock output in cascaded PLLs ( $f_{OUT} \ge 100 \text{ MHz}$ )	_	_	175	ps (p-p)
(5), (6)	Period Jitter for a dedicated clock output in cascaded PLLs ( $f_{OUT}$ < 100 MHz)	_	_	17.5	mUI (p-p)
f <sub>DRIFT</sub>	Frequency drift after PFDENA is disabled for a duration of 100 $\mu s$		_	±10	%
dK <sub>BIT</sub>	Bit number of Delta Sigma Modulator (DSM)	8	24	32	Bits
k <sub>VALUE</sub>	Numerator of Fraction	128	8388608	2147483648	—

Table 31. PLL Specifications for Stratix V Devices (Part 2 of 3)

Mode		Peformance						
	C1	C2, C2L	12, 12L	C3	13, 13L, 13YY	C4	14	Unit
		Modes us	ing Three	DSPs				
One complex 18 x 25	425	425	415	340	340	275	265	MHz
Modes using Four DSPs								
One complex 27 x 27	465	465	465	380	380	300	290	MHz

#### Table 32. Block Performance Specifications for Stratix V DSP Devices (Part 2 of 2)

# **Memory Block Specifications**

Table 33 lists the Stratix V memory block specifications.

### Table 33. Memory Block Performance Specifications for Stratix V Devices <sup>(1), (2)</sup> (Part 1 of 2)

		<b>Resources Used</b>		Performance							
Memory	Mode	ALUTS	Memory	C1	C2, C2L	C3	C4	12, 12L	13, 13L, 13YY	14	Unit
	Single port, all supported widths	0	1	450	450	400	315	450	400	315	MHz
MLAR	Simple dual-port, x32/x64 depth	0	1	450	450	400	315	450	400	315	MHz
MLAB	Simple dual-port, x16 depth <sup>(3)</sup>	0	1	675	675	533	400	675	533	400	MHz
	ROM, all supported widths	0	1	600	600	500	450	600	500	450	MHz

Figure 7 shows the dynamic phase alignment (DPA) lock time specifications with the DPA PLL calibration option enabled.

Figure 7. DPA Lock Time Specification with DPA PLL Calibration Enabled

rx_reset			
rx_dpa_locked			<u> </u>
			-

Table 37 lists the DPA lock time specifications for Stratix V devices.

Table 37. DPA Lock Time Specifications for Stratix V GX Devices Only (1), (2), (3)

Standard	Training Pattern	Number of Data Transitions in One Repetition of the Training Pattern	Number of Repetitions per 256 Data Transitions <sup>(4)</sup>	Maximum
SPI-4	00000000001111111111	2	128	640 data transitions
Parallel Rapid I/O	00001111	2	128	640 data transitions
	10010000	4	64	640 data transitions
Miscellaneous	10101010	8	32	640 data transitions
Wiscenareous	01010101	8	32	640 data transitions

#### Notes to Table 37:

(1) The DPA lock time is for one channel.

(2) One data transition is defined as a 0-to-1 or 1-to-0 transition.

(3) The DPA lock time stated in this table applies to both commercial and industrial grade.

(4) This is the number of repetitions for the stated training pattern to achieve the 256 data transitions.

Figure 8 shows the **LVDS** soft-clock data recovery (CDR)/DPA sinusoidal jitter tolerance specification for a data rate  $\geq$  1.25 Gbps. Table 38 lists the **LVDS** soft-CDR/DPA sinusoidal jitter tolerance specification for a data rate  $\geq$  1.25 Gbps.





Speed Grade	Min	Max	Unit
C4,I4	8	16	ps

#### Table 40. DQS Phase Offset Delay Per Setting for Stratix V Devices <sup>(1), (2)</sup> (Part 2 of 2)

#### Notes to Table 40:

(1) The typical value equals the average of the minimum and maximum values.

(2) The delay settings are linear with a cumulative delay variation of 40 ps for all speed grades. For example, when using a -2 speed grade and applying a 10-phase offset setting to a 90° phase shift at 400 MHz, the expected average cumulative delay is [625 ps + (10 × 10 ps) ± 20 ps] = 725 ps ± 20 ps.

Table 41 lists the DQS phase shift error for Stratix V devices.

Table 41. DQS Phase Shift Error Specification for DLL-Delayed Clock (t<sub>DQS\_PSERR</sub>) for Stratix V Devices <sup>(1)</sup>

Number of DQS Delay Buffers	C1	C2, C2L, I2, I2L	C3, I3, I3L, I3YY	C4,14	Unit
1	28	28	30	32	ps
2	56	56	60	64	ps
3	84	84	90	96	ps
4	112	112	120	128	ps

Notes to Table 41:

(1) This error specification is the absolute maximum and minimum error. For example, skew on three DQS delay buffers in a -2 speed grade is  $\pm 78$  ps or  $\pm 39$  ps.

Table 42 lists the memory output clock jitter specifications for Stratix V devices.

Table 42. Memory Output Clock Jitter Specification for Stratix V Devices (1	<sup>),</sup> (Part 1 of 2) <sup>(2), (3)</sup>
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Clock Network	Parameter	Symbol	C1		C2, C2L, I2, I2L		C3, I3, I3L, I3YY		C4,14		Unit
		-	Min	Max	Min	Max	Min	Max	Min	Max	
	Clock period jitter	$t_{JIT(per)}$	-50	50	-50	50	-55	55	-55	55	ps
Regional	Cycle-to-cycle period jitter	$t_{\text{JIT(cc)}}$	-100	100	-100	100	-110	110	-110	110	ps
	Duty cycle jitter	$t_{JIT(duty)}$	-50	50	-50	50	-82.5	82.5	-82.5	82.5	ps
	Clock period jitter	$t_{JIT(per)}$	-75	75	-75	75	-82.5	82.5	-82.5	82.5	ps
Global	Cycle-to-cycle period jitter	$t_{\text{JIT(cc)}}$	-150	150	-150	150	-165	165	-165	165	ps
	Duty cycle jitter	$t_{JIT(duty)}$	-75	75	-75	75	-90	90	-90	90	ps

Symbol	Parameter	Minimum	Maximum	Units
t <sub>CD2UM</sub>	CONF_DONE high to user mode $(3)$	175	437	μS
t <sub>CD2CU</sub>	CONF_DONE high to CLKUSR enabled	4 × maximum DCLK period	_	—
t <sub>CD2UMC</sub>	CONF_DONE high to user mode with CLKUSR option on	t <sub>cd2cu</sub> + (8576 × clkusr period)	_	—

Table 53. AS Timing Parameters for AS  $\times$ 1 and AS  $\times$ 4 Configurations in Stratix V Devices <sup>(1), (2)</sup> (Part 2 of 2)

#### Notes to Table 53:

(1) The minimum and maximum numbers apply only if you choose the internal oscillator as the clock source for initializing the device.

(2) t<sub>CF2CD</sub>, t<sub>CF2ST0</sub>, t<sub>CF2ST0</sub>, t<sub>CF6</sub>, t<sub>STATUS</sub>, and t<sub>CF2ST1</sub> timing parameters are identical to the timing parameters for PS mode listed in Table 54 on page 63.

(3) To enable the CLKUSR pin as the initialization clock source and to obtain the maximum frequency specification on this pin, refer to the Initialization section of the "Configuration, Design Security, and Remote System Upgrades in Stratix V Devices" chapter.

# **Passive Serial Configuration Timing**

Figure 15 shows the timing waveform for a passive serial (PS) configuration when using a MAX II device, MAX V device, or microprocessor as an external host.

Figure 15. PS Configuration Timing Waveform <sup>(1)</sup>



#### Notes to Figure 15:

- (1) The beginning of this waveform shows the device in user mode. In user mode, nCONFIG, nSTATUS, and CONF\_DONE are at logic high levels. When nCONFIG is pulled low, a reconfiguration cycle begins.
- (2) After power-up, the Stratix V device holds nSTATUS low for the time of the POR delay.
- (3) After power-up, before and during configuration, CONF DONE is low.
- (4) Do not leave DCLK floating after configuration. You can drive it high or low, whichever is more convenient.
- (5) DATAO is available as a user I/O pin after configuration. The state of this pin depends on the dual-purpose pin settings in the **Device and Pins Option**.
- (6) To ensure a successful configuration, send the entire configuration data to the Stratix V device. CONF\_DONE is released high after the Stratix V device receives all the configuration data successfully. After CONF\_DONE goes high, send two additional falling edges on DCLK to begin initialization and enter user mode.
- (7) After the option bit to enable the INIT DONE pin is configured into the device, the INIT DONE goes low.

Table 60.	Glossary	(Part 3 of 4)
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Letter	Subject	Definitions		
	SW (sampling window)	Timing Diagram—the period of time during which the data must be valid in order to capture it correctly. The setup and hold times determine the ideal strobe position within the sampling window, as shown:         Bit Time         0.5 x TCCS       RSKM         Sampling Window       RSKM         0.5 x TCCS       RSKM		
S	Single-ended voltage referenced I/O standard	The JEDEC standard for SSTL and HSTL I/O defines both the AC and DC input signal values.         The AC values indicate the voltage levels at which the receiver must meet its timing specifications. The DC values indicate the voltage levels at which the final logic state of the receiver is unambiguously defined. After the receiver input has crossed the AC value, the receiver changes to the new logic state.         The new logic state is then maintained as long as the input stays beyond the DC threshold. This approach is intended to provide predictable receiver timing in the presence of input waveform ringing:         Single-Ended Voltage Referenced I/O Standard         V_CCID         V_HIGC)         V_REF         VILLAC;         VOL         VOL		
	t <sub>C</sub>	High-speed receiver and transmitter input and output clock period.		
т	TCCS (channel- to-channel-skew)	The timing difference between the fastest and slowest output edges, including $t_{CO}$ variation and clock skew, across channels driven by the same PLL. The clock is included in the TCCS measurement (refer to the <i>Timing Diagram</i> figure under <b>SW</b> in this table).		
	t <sub>duty</sub>	High-speed I/O block—Duty cycle on the high-speed transmitter output clock.		
		<b>Timing Unit Interval (TUI)</b> The timing budget allowed for skew, propagation delays, and the data sampling window.		
		$(TUI = 1/(receiver input clock frequency multiplication factor) = t_C/w)$		
	t <sub>FALL</sub>	Signal high-to-low transition time (80-20%)		
	t <sub>INCCJ</sub>	Cycle-to-cycle jitter tolerance on the PLL clock input.		
	t <sub>outpj_i0</sub>	Period jitter on the general purpose I/O driven by a PLL.		
	t <sub>outpj_dc</sub>	Period jitter on the dedicated clock output driven by a PLL.		
	t <sub>RISE</sub>	Signal low-to-high transition time (20-80%)		
U	—	_		

# **Document Revision History**

Table 61 lists the revision history for this chapter.

 Table 61. Document Revision History (Part 1 of 3)

Date	Version	Changes	
June 2018	3.9	<ul> <li>Added the "Stratix V Device Overshoot Duration" figure.</li> </ul>	
April 2017	3.8	Added a footnote to the "High-Speed I/O Specifications for Stratix V Devices" table.	
		<ul> <li>Changed the minimum value for t<sub>CD2UMC</sub> in the "PS Timing Parameters for Stratix V Devices" table.</li> </ul>	
		<ul> <li>Changed the condition for 100-Ω R<sub>D</sub> in the "OCT Without Calibration Resistance Tolerance Specifications for Stratix V Devices" table.</li> </ul>	
		<ul> <li>Changed the minimum value for t<sub>CD2UMC</sub> in the "AS Timing Parameters for AS '1 and AS '4 Configurations in Stratix V Devices" table</li> </ul>	
		<ul> <li>Changed the minimum value for t<sub>CD2UMC</sub> in the "FPP Timing Parameters for Stratix V Devices When the DCLK-to-DATA[] Ratio is &gt;1" table.</li> </ul>	
		<ul> <li>Changed the minimum value for t<sub>CD2UMC</sub> in the "FPP Timing Parameters for Stratix V Devices When the DCLK-to-DATA[] Ratio is &gt;1" table.</li> </ul>	
		<ul> <li>Changed the minimum number of clock cycles value in the "Initialization Clock Source Option and the Maximum Frequency" table.</li> </ul>	
June 2016	3.7	<ul> <li>Added the V<sub>ID</sub> minimum specification for LVPECL in the "Differential I/O Standard Specifications for Stratix V Devices" table</li> </ul>	
		<ul> <li>Added the I<sub>OUT</sub> specification to the "Absolute Maximum Ratings for Stratix V Devices" table.</li> </ul>	
December 2015	3.6	Added a footnote to the "High-Speed I/O Specifications for Stratix V Devices" table.	
December 2015	3.5	<ul> <li>Changed the transmitter, receiver, and ATX PLL data rate specifications in the "Transceiver Specifications for Stratix V GX and GS Devices" table.</li> </ul>	
		<ul> <li>Changed the configuration .rbf sizes in the "Uncompressed .rbf Sizes for Stratix V Devices" table.</li> </ul>	
	3.4	• Changed the data rate specification for transceiver speed grade 3 in the following tables:	
July 2015		<ul> <li>"Transceiver Specifications for Stratix V GX and GS Devices"</li> </ul>	
		<ul> <li>"Stratix V Standard PCS Approximate Maximum Date Rate"</li> </ul>	
		<ul> <li>"Stratix V 10G PCS Approximate Maximum Data Rate"</li> </ul>	
		<ul> <li>Changed the conditions for reference clock rise and fall time, and added a note to the "Transceiver Specifications for Stratix V GX and GS Devices" table.</li> </ul>	
		<ul> <li>Added a note to the "Minimum differential eye opening at receiver serial input pins" specification in the "Transceiver Specifications for Stratix V GX and GS Devices" table.</li> </ul>	
		<ul> <li>Changed the t<sub>c0</sub> maximum value in the "AS Timing Parameters for AS '1 and AS '4 Configurations in Stratix V Devices" table.</li> </ul>	
		<ul> <li>Removed the CDR ppm tolerance specification from the "Transceiver Specifications for Stratix V GX and GS Devices" table.</li> </ul>	