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### Understanding [Embedded - FPGAs \(Field Programmable Gate Array\)](#)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

### Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

#### Details

Product Status	Obsolete
Number of LABs/CLBs	234720
Number of Logic Elements/Cells	622000
Total RAM Bits	51200000
Number of I/O	600
Number of Gates	-
Voltage - Supply	0.82V ~ 0.88V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	1517-BBGA, FCBGA
Supplier Device Package	1517-FBGA (40x40)
Purchase URL	<a href="https://www.e-xfl.com/product-detail/intel/5sgxea7n3f40c2ln">https://www.e-xfl.com/product-detail/intel/5sgxea7n3f40c2ln</a>

**Table 7. Recommended Transceiver Power Supply Operating Conditions for Stratix V GX, GS, and GT Devices (Part 2 of 2)**

Symbol	Description	Devices	Minimum <sup>(4)</sup>	Typical	Maximum <sup>(4)</sup>	Unit
$V_{CCR\_GXBR}$ (2)	Receiver analog power supply (right side)	GX, GS, GT	0.82	0.85	0.88	V
			0.87	0.90	0.93	
			0.97	1.0	1.03	
			1.03	1.05	1.07	
$V_{CCR\_GTBR}$	Receiver analog power supply for GT channels (right side)	GT	1.02	1.05	1.08	V
$V_{CCT\_GXBL}$ (2)	Transmitter analog power supply (left side)	GX, GS, GT	0.82	0.85	0.88	V
			0.87	0.90	0.93	
			0.97	1.0	1.03	
			1.03	1.05	1.07	
$V_{CCT\_GXBR}$ (2)	Transmitter analog power supply (right side)	GX, GS, GT	0.82	0.85	0.88	V
			0.87	0.90	0.93	
			0.97	1.0	1.03	
			1.03	1.05	1.07	
$V_{CCT\_GTBR}$	Transmitter analog power supply for GT channels (right side)	GT	1.02	1.05	1.08	V
$V_{CCL\_GTBR}$	Transmitter clock network power supply	GT	1.02	1.05	1.08	V
$V_{CCH\_GXBL}$	Transmitter output buffer power supply (left side)	GX, GS, GT	1.425	1.5	1.575	V
$V_{CCH\_GXBR}$	Transmitter output buffer power supply (right side)	GX, GS, GT	1.425	1.5	1.575	V

**Notes to Table 7:**

- (1) This supply must be connected to 3.0 V if the CMU PLL, receiver CDR, or both, are configured at a base data rate > 6.5 Gbps. Up to 6.5 Gbps, you can connect this supply to either 3.0 V or 2.5 V.
- (2) Refer to Table 8 to select the correct power supply level for your design.
- (3) When using ATX PLLs, the supply must be 3.0 V.
- (4) This value describes the budget for the DC (static) power supply tolerance and does not include the dynamic tolerance requirements. Refer to the PDN tool for the additional budget for the dynamic tolerance requirements.

Table 8 shows the transceiver power supply voltage requirements for various conditions.

**Table 8. Transceiver Power Supply Voltage Requirements**

Conditions	Core Speed Grade	VCCR_GXB & VCCT_GXB <sup>(2)</sup>	VCCA_GXB	VCCH_GXB	Unit
If BOTH of the following conditions are true: <ul style="list-style-type: none"> <li>■ Data rate &gt; 10.3 Gbps.</li> <li>■ DFE is used.</li> </ul>	All	1.05	3.0	1.5	V
If ANY of the following conditions are true <sup>(1)</sup> : <ul style="list-style-type: none"> <li>■ ATX PLL is used.</li> <li>■ Data rate &gt; 6.5Gbps.</li> <li>■ DFE (data rate ≤ 10.3 Gbps), AEQ, or EyeQ feature is used.</li> </ul>	All	1.0			
If ALL of the following conditions are true: <ul style="list-style-type: none"> <li>■ ATX PLL is not used.</li> <li>■ Data rate ≤ 6.5Gbps.</li> <li>■ DFE, AEQ, and EyeQ are not used.</li> </ul>	C1, C2, I2, and I3YY	0.90	2.5		
	C2L, C3, C4, I2L, I3, I3L, and I4	0.85	2.5		

**Notes to Table 8:**

- (1) Choose this power supply voltage requirement option if you plan to upgrade your design later with any of the listed conditions.
- (2) If the VCCR\_GXB and VCCT\_GXB supplies are set to 1.0 V or 1.05 V, they cannot be shared with the VCC core supply. If the VCCR\_GXB and VCCT\_GXB are set to either 0.90 V or 0.85 V, they can be shared with the VCC core supply.

## DC Characteristics

This section lists the supply current, I/O pin leakage current, input pin capacitance, on-chip termination tolerance, and hot socketing specifications.

### Supply Current

Supply current is the current drawn from the respective power rails used for power budgeting. Use the Excel-based Early Power Estimator (EPE) to get supply current estimates for your design because these currents vary greatly with the resources you use.



For more information about power estimation tools, refer to the *PowerPlay Early Power Estimator User Guide* and the *PowerPlay Power Analysis* chapter in the *Quartus II Handbook*.

**Table 13. OCT Variation after Power-Up Calibration for Stratix V Devices (Part 2 of 2) <sup>(1)</sup>**

Symbol	Description	V <sub>CCIO</sub> (V)	Typical	Unit
dR/dT	OCT variation with temperature without recalibration	3.0	0.189	%/ <sup>o</sup> C
		2.5	0.208	
		1.8	0.266	
		1.5	0.273	
		1.2	0.317	

**Note to Table 13:**

(1) Valid for a V<sub>CCIO</sub> range of  $\pm 5\%$  and a temperature range of 0° to 85°C.

**Pin Capacitance**

Table 14 lists the Stratix V device family pin capacitance.

**Table 14. Pin Capacitance for Stratix V Devices**

Symbol	Description	Value	Unit
C <sub>IOTB</sub>	Input capacitance on the top and bottom I/O pins	6	pF
C <sub>IOLR</sub>	Input capacitance on the left and right I/O pins	6	pF
C <sub>OUTFB</sub>	Input capacitance on dual-purpose clock output and feedback pins	6	pF

**Hot Socketing**

Table 15 lists the hot socketing specifications for Stratix V devices.

**Table 15. Hot Socketing Specifications for Stratix V Devices**

Symbol	Description	Maximum
I <sub>IOPIN</sub> (DC)	DC current per I/O pin	300 $\mu$ A
I <sub>IOPIN</sub> (AC)	AC current per I/O pin	8 mA <sup>(1)</sup>
I <sub>XCVR-TX</sub> (DC)	DC current per transceiver transmitter pin	100 mA
I <sub>XCVR-RX</sub> (DC)	DC current per transceiver receiver pin	50 mA

**Note to Table 15:**

(1) The I/O ramp rate is 10 ns or more. For ramp rates faster than 10 ns,  $|I_{IOPIN}| = C \, dv/dt$ , in which C is the I/O pin capacitance and dv/dt is the slew rate.

## Internal Weak Pull-Up Resistor

Table 16 lists the weak pull-up resistor values for Stratix V devices.

**Table 16. Internal Weak Pull-Up Resistor for Stratix V Devices <sup>(1), (2)</sup>**

Symbol	Description	V <sub>CCIO</sub> Conditions (V) <sup>(3)</sup>	Value <sup>(4)</sup>	Unit
R <sub>PU</sub>	Value of the I/O pin pull-up resistor before and during configuration, as well as user mode if you enable the programmable pull-up resistor option.	3.0 ±5%	25	kΩ
		2.5 ±5%	25	kΩ
		1.8 ±5%	25	kΩ
		1.5 ±5%	25	kΩ
		1.35 ±5%	25	kΩ
		1.25 ±5%	25	kΩ
		1.2 ±5%	25	kΩ

### Notes to Table 16:

- (1) All I/O pins have an option to enable the weak pull-up resistor except the configuration, test, and JTAG pins.
- (2) The internal weak pull-down feature is only available for the JTAG TCK pin. The typical value for this internal weak pull-down resistor is approximately 25 kΩ.
- (3) The pin pull-up resistance values may be lower if an external source drives the pin higher than V<sub>CCIO</sub>.
- (4) These specifications are valid with a ±10% tolerance to cover changes over PVT.

## I/O Standard Specifications

Table 17 through Table 22 list the input voltage (V<sub>IH</sub> and V<sub>IL</sub>), output voltage (V<sub>OH</sub> and V<sub>OL</sub>), and current drive characteristics (I<sub>OH</sub> and I<sub>OL</sub>) for various I/O standards supported by Stratix V devices. These tables also show the Stratix V device family I/O standard specifications. The V<sub>OL</sub> and V<sub>OH</sub> values are valid at the corresponding I<sub>OH</sub> and I<sub>OL</sub>, respectively.

For an explanation of the terms used in Table 17 through Table 22, refer to “Glossary” on page 65. For tolerance calculations across all SSTL and HSTL I/O standards, refer to Altera knowledge base solution rd07262012\_486.

**Table 17. Single-Ended I/O Standards for Stratix V Devices**

I/O Standard	V <sub>CCIO</sub> (V)			V <sub>IL</sub> (V)		V <sub>IH</sub> (V)		V <sub>OL</sub> (V)	V <sub>OH</sub> (V)	I <sub>OL</sub> (mA)	I <sub>OH</sub> (mA)
	Min	Typ	Max	Min	Max	Min	Max	Max	Min		
LVTTTL	2.85	3	3.15	−0.3	0.8	1.7	3.6	0.4	2.4	2	−2
LVC MOS	2.85	3	3.15	−0.3	0.8	1.7	3.6	0.2	V <sub>CCIO</sub> − 0.2	0.1	−0.1
2.5 V	2.375	2.5	2.625	−0.3	0.7	1.7	3.6	0.4	2	1	−1
1.8 V	1.71	1.8	1.89	−0.3	0.35 * V <sub>CCIO</sub>	0.65 * V <sub>CCIO</sub>	V <sub>CCIO</sub> + 0.3	0.45	V <sub>CCIO</sub> − 0.45	2	−2
1.5 V	1.425	1.5	1.575	−0.3	0.35 * V <sub>CCIO</sub>	0.65 * V <sub>CCIO</sub>	V <sub>CCIO</sub> + 0.3	0.25 * V <sub>CCIO</sub>	0.75 * V <sub>CCIO</sub>	2	−2
1.2 V	1.14	1.2	1.26	−0.3	0.35 * V <sub>CCIO</sub>	0.65 * V <sub>CCIO</sub>	V <sub>CCIO</sub> + 0.3	0.25 * V <sub>CCIO</sub>	0.75 * V <sub>CCIO</sub>	2	−2

**Table 19. Single-Ended SSTL, HSTL, and HSUL I/O Standards Signal Specifications for Stratix V Devices (Part 2 of 2)**

I/O Standard	$V_{IL(DC)}$ (V)		$V_{IH(DC)}$ (V)		$V_{IL(AC)}$ (V)	$V_{IH(AC)}$ (V)	$V_{OL}$ (V)	$V_{OH}$ (V)	$I_{ol}$ (mA)	$I_{oh}$ (mA)
	Min	Max	Min	Max	Max	Min	Max	Min		
HSTL-18 Class I	—	$V_{REF} - 0.1$	$V_{REF} + 0.1$	—	$V_{REF} - 0.2$	$V_{REF} + 0.2$	0.4	$V_{CCIO} - 0.4$	8	-8
HSTL-18 Class II	—	$V_{REF} - 0.1$	$V_{REF} + 0.1$	—	$V_{REF} - 0.2$	$V_{REF} + 0.2$	0.4	$V_{CCIO} - 0.4$	16	-16
HSTL-15 Class I	—	$V_{REF} - 0.1$	$V_{REF} + 0.1$	—	$V_{REF} - 0.2$	$V_{REF} + 0.2$	0.4	$V_{CCIO} - 0.4$	8	-8
HSTL-15 Class II	—	$V_{REF} - 0.1$	$V_{REF} + 0.1$	—	$V_{REF} - 0.2$	$V_{REF} + 0.2$	0.4	$V_{CCIO} - 0.4$	16	-16
HSTL-12 Class I	-0.15	$V_{REF} - 0.08$	$V_{REF} + 0.08$	$V_{CCIO} + 0.15$	$V_{REF} - 0.15$	$V_{REF} + 0.15$	$0.25^* V_{CCIO}$	$0.75^* V_{CCIO}$	8	-8
HSTL-12 Class II	-0.15	$V_{REF} - 0.08$	$V_{REF} + 0.08$	$V_{CCIO} + 0.15$	$V_{REF} - 0.15$	$V_{REF} + 0.15$	$0.25^* V_{CCIO}$	$0.75^* V_{CCIO}$	16	-16
HSUL-12	—	$V_{REF} - 0.13$	$V_{REF} + 0.13$	—	$V_{REF} - 0.22$	$V_{REF} + 0.22$	$0.1^* V_{CCIO}$	$0.9^* V_{CCIO}$	—	—

**Table 20. Differential SSTL I/O Standards for Stratix V Devices**

I/O Standard	$V_{CCIO}$ (V)			$V_{SWING(DC)}$ (V)		$V_{X(AC)}$ (V)			$V_{SWING(AC)}$ (V)	
	Min	Typ	Max	Min	Max	Min	Typ	Max	Min	Max
SSTL-2 Class I, II	2.375	2.5	2.625	0.3	$V_{CCIO} + 0.6$	$V_{CCIO}/2 - 0.2$	—	$V_{CCIO}/2 + 0.2$	0.62	$V_{CCIO} + 0.6$
SSTL-18 Class I, II	1.71	1.8	1.89	0.25	$V_{CCIO} + 0.6$	$V_{CCIO}/2 - 0.175$	—	$V_{CCIO}/2 + 0.175$	0.5	$V_{CCIO} + 0.6$
SSTL-15 Class I, II	1.425	1.5	1.575	0.2	(1)	$V_{CCIO}/2 - 0.15$	—	$V_{CCIO}/2 + 0.15$	0.35	—
SSTL-135 Class I, II	1.283	1.35	1.45	0.2	(1)	$V_{CCIO}/2 - 0.15$	$V_{CCIO}/2$	$V_{CCIO}/2 + 0.15$	$2(V_{IH(AC)} - V_{REF})$	$2(V_{IL(AC)} - V_{REF})$
SSTL-125 Class I, II	1.19	1.25	1.31	0.18	(1)	$V_{CCIO}/2 - 0.15$	$V_{CCIO}/2$	$V_{CCIO}/2 + 0.15$	$2(V_{IH(AC)} - V_{REF})$	—
SSTL-12 Class I, II	1.14	1.2	1.26	0.18	—	$V_{REF} - 0.15$	$V_{CCIO}/2$	$V_{REF} + 0.15$	-0.30	0.30

**Note to Table 20:**

(1) The maximum value for  $V_{SWING(DC)}$  is not defined. However, each single-ended signal needs to be within the respective single-ended limits ( $V_{IH(DC)}$  and  $V_{IL(DC)}$ ).

**Table 21. Differential HSTL and HSUL I/O Standards for Stratix V Devices (Part 1 of 2)**

I/O Standard	$V_{CCIO}$ (V)			$V_{DIF(DC)}$ (V)		$V_{X(AC)}$ (V)			$V_{CM(DC)}$ (V)			$V_{DIF(AC)}$ (V)	
	Min	Typ	Max	Min	Max	Min	Typ	Max	Min	Typ	Max	Min	Max
HSTL-18 Class I, II	1.71	1.8	1.89	0.2	—	0.78	—	1.12	0.78	—	1.12	0.4	—
HSTL-15 Class I, II	1.425	1.5	1.575	0.2	—	0.68	—	0.9	0.68	—	0.9	0.4	—

-  You typically use the interactive Excel-based Early Power Estimator before designing the FPGA to get a magnitude estimate of the device power. The Quartus II PowerPlay Power Analyzer provides better quality estimates based on the specifics of the design after you complete place-and-route. The PowerPlay Power Analyzer can apply a combination of user-entered, simulation-derived, and estimated signal activities that, when combined with detailed circuit models, yields very accurate power estimates.
-  For more information about power estimation tools, refer to the *PowerPlay Early Power Estimator User Guide* and the *PowerPlay Power Analysis* chapter in the *Quartus II Handbook*.

**Table 23. Transceiver Specifications for Stratix V GX and GS Devices <sup>(1)</sup> (Part 3 of 7)**

Symbol/ Description	Conditions	Transceiver Speed Grade 1			Transceiver Speed Grade 2			Transceiver Speed Grade 3			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Reconfiguration clock ( <code>mgmt_clk_clk</code> ) frequency	—	100	—	125	100	—	125	100	—	125	MHz
<b>Receiver</b>											
Supported I/O Standards	—	1.4-V PCML, 1.5-V PCML, 2.5-V PCML, LVPECL, and LVDS									
Data rate (Standard PCS) (9), (23)	—	600	—	12200	600	—	12200	600	—	8500/ 10312.5 (24)	Mbps
Data rate (10G PCS) (9), (23)	—	600	—	14100	600	—	12500	600	—	8500/ 10312.5 (24)	Mbps
Absolute $V_{MAX}$ for a receiver pin <sup>(5)</sup>	—	—	—	1.2	—	—	1.2	—	—	1.2	V
Absolute $V_{MIN}$ for a receiver pin	—	−0.4	—	—	−0.4	—	—	−0.4	—	—	V
Maximum peak- to-peak differential input voltage $V_{ID}$ (diff p- p) before device configuration <sup>(22)</sup>	—	—	—	1.6	—	—	1.6	—	—	1.6	V
Maximum peak- to-peak differential input voltage $V_{ID}$ (diff p- p) after device configuration <sup>(18)</sup> , (22)	$V_{CCR\_GXB} =$ 1.0 V/1.05 V ( $V_{ICM} =$ 0.70 V)	—	—	2.0	—	—	2.0	—	—	2.0	V
	$V_{CCR\_GXB} =$ 0.90 V ( $V_{ICM} = 0.6$ V)	—	—	2.4	—	—	2.4	—	—	2.4	V
	$V_{CCR\_GXB} =$ 0.85 V ( $V_{ICM} = 0.6$ V)	—	—	2.4	—	—	2.4	—	—	2.4	V
Minimum differential eye opening at receiver serial input pins <sup>(6)</sup> , (22), (27)	—	85	—	—	85	—	—	85	—	—	mV



**Table 23. Transceiver Specifications for Stratix V GX and GS Devices <sup>(1)</sup> (Part 5 of 7)**

Symbol/ Description	Conditions	Transceiver Speed Grade 1			Transceiver Speed Grade 2			Transceiver Speed Grade 3			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Programmable DC gain	DC Gain Setting = 0	—	0	—	—	0	—	—	0	—	dB
	DC Gain Setting = 1	—	2	—	—	2	—	—	2	—	dB
	DC Gain Setting = 2	—	4	—	—	4	—	—	4	—	dB
	DC Gain Setting = 3	—	6	—	—	6	—	—	6	—	dB
	DC Gain Setting = 4	—	8	—	—	8	—	—	8	—	dB
<b>Transmitter</b>											
Supported I/O Standards	—	1.4-V and 1.5-V PCML									
Data rate (Standard PCS)	—	600	—	12200	600	—	12200	600	—	8500/ 10312.5 <sup>(24)</sup>	Mbps
Data rate (10G PCS)	—	600	—	14100	600	—	12500	600	—	8500/ 10312.5 <sup>(24)</sup>	Mbps
Differential on- chip termination resistors	85- $\Omega$ setting	—	85 $\pm$ 20%	—	—	85 $\pm$ 20%	—	—	85 $\pm$ 20%	—	$\Omega$
	100- $\Omega$ setting	—	100 $\pm$ 20%	—	—	100 $\pm$ 20%	—	—	100 $\pm$ 20%	—	$\Omega$
	120- $\Omega$ setting	—	120 $\pm$ 20%	—	—	120 $\pm$ 20%	—	—	120 $\pm$ 20%	—	$\Omega$
	150- $\Omega$ setting	—	150 $\pm$ 20%	—	—	150 $\pm$ 20%	—	—	150 $\pm$ 20%	—	$\Omega$
V <sub>OCM</sub> (AC coupled)	0.65-V setting	—	650	—	—	650	—	—	650	—	mV
V <sub>OCM</sub> (DC coupled)	—	—	650	—	—	650	—	—	650	—	mV
Rise time <sup>(7)</sup>	20% to 80%	30	—	160	30	—	160	30	—	160	ps
Fall time <sup>(7)</sup>	80% to 20%	30	—	160	30	—	160	30	—	160	ps
Intra-differential pair skew	Tx V <sub>CM</sub> = 0.5 V and slew rate of 15 ps	—	—	15	—	—	15	—	—	15	ps
Intra-transceiver block transmitter channel-to- channel skew	x6 PMA bonded mode	—	—	120	—	—	120	—	—	120	ps

**Table 23. Transceiver Specifications for Stratix V GX and GS Devices <sup>(1)</sup> (Part 6 of 7)**

Symbol/ Description	Conditions	Transceiver Speed Grade 1			Transceiver Speed Grade 2			Transceiver Speed Grade 3			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Inter-transceiver block transmitter channel-to- channel skew	xN PMA bonded mode	—	—	500	—	—	500	—	—	500	ps
<b>CMU PLL</b>											
Supported Data Range	—	600	—	12500	600	—	12500	600	—	8500/ 10312.5 (24)	Mbps
$t_{\text{pll\_powerdown}}$ <sup>(15)</sup>	—	1	—	—	1	—	—	1	—	—	μs
$t_{\text{pll\_lock}}$ <sup>(16)</sup>	—	—	—	10	—	—	10	—	—	10	μs
<b>ATX PLL</b>											
Supported Data Rate Range	VCO post-divider L=2	8000	—	14100	8000	—	12500	8000	—	8500/ 10312.5 (24)	Mbps
	L=4	4000	—	7050	4000	—	6600	4000	—	6600	Mbps
	L=8	2000	—	3525	2000	—	3300	2000	—	3300	Mbps
	L=8, Local/Central Clock Divider =2	1000	—	1762.5	1000	—	1762.5	1000	—	1762.5	Mbps
$t_{\text{pll\_powerdown}}$ <sup>(15)</sup>	—	1	—	—	1	—	—	1	—	—	μs
$t_{\text{pll\_lock}}$ <sup>(16)</sup>	—	—	—	10	—	—	10	—	—	10	μs
<b>fPLL</b>											
Supported Data Range	—	600	—	3250/ 3125 <sup>(25)</sup>	600	—	3250/ 3125 <sup>(25)</sup>	600	—	3250/ 3125 <sup>(25)</sup>	Mbps
$t_{\text{pll\_powerdown}}$ <sup>(15)</sup>	—	1	—	—	1	—	—	1	—	—	μs

Table 27 shows the  $V_{OD}$  settings for the GX channel.

**Table 27. Typical  $V_{OD}$  Setting for GX Channel, TX Termination = 100  $\Omega$  <sup>(2)</sup>**

Symbol	$V_{OD}$ Setting	$V_{OD}$ Value (mV)	$V_{OD}$ Setting	$V_{OD}$ Value (mV)
<b><math>V_{OD}</math> differential peak to peak typical <sup>(3)</sup></b>	0 <sup>(1)</sup>	0	32	640
	1 <sup>(1)</sup>	20	33	660
	2 <sup>(1)</sup>	40	34	680
	3 <sup>(1)</sup>	60	35	700
	4 <sup>(1)</sup>	80	36	720
	5 <sup>(1)</sup>	100	37	740
	6	120	38	760
	7	140	39	780
	8	160	40	800
	9	180	41	820
	10	200	42	840
	11	220	43	860
	12	240	44	880
	13	260	45	900
	14	280	46	920
	15	300	47	940
	16	320	48	960
	17	340	49	980
	18	360	50	1000
	19	380	51	1020
	20	400	52	1040
	21	420	53	1060
	22	440	54	1080
	23	460	55	1100
	24	480	56	1120
	25	500	57	1140
	26	520	58	1160
	27	540	59	1180
	28	560	60	1200
	29	580	61	1220
	30	600	62	1240
	31	620	63	1260

**Note to Table 27:**

- (1) If TX termination resistance = 100 $\Omega$ , this VOD setting is illegal.
- (2) The tolerance is +/-20% for all VOD settings except for settings 2 and below.
- (3) Refer to Figure 2.

**Table 28. Transceiver Specifications for Stratix V GT Devices (Part 2 of 5) <sup>(1)</sup>**

Symbol/ Description	Conditions	Transceiver Speed Grade 2			Transceiver Speed Grade 3			Unit
		Min	Typ	Max	Min	Typ	Max	
Transmitter REFCLK Phase Noise (622 MHz) <sup>(18)</sup>	100 Hz	—	—	-70	—	—	-70	dBc/Hz
	1 kHz	—	—	-90	—	—	-90	
	10 kHz	—	—	-100	—	—	-100	
	100 kHz	—	—	-110	—	—	-110	
	≥ 1 MHz	—	—	-120	—	—	-120	
Transmitter REFCLK Phase Jitter (100 MHz) <sup>(15)</sup>	10 kHz to 1.5 MHz (PCIe)	—	—	3	—	—	3	ps (rms)
RREF <sup>(17)</sup>	—	—	1800 ± 1%	—	—	1800 ± 1%	—	Ω
<b>Transceiver Clocks</b>								
fixedclk clock frequency	PCIe Receiver Detect	—	100 or 125	—	—	100 or 125	—	MHz
Reconfiguration clock (mgmt_clk_clk) frequency	—	100	—	125	100	—	125	MHz
<b>Receiver</b>								
Supported I/O Standards	—	1.4-V PCML, 1.5-V PCML, 2.5-V PCML, LVPECL, and LVDS						
Data rate (Standard PCS) <sup>(21)</sup>	GX channels	600	—	8500	600	—	8500	Mbps
Data rate (10G PCS) <sup>(21)</sup>	GX channels	600	—	12,500	600	—	12,500	Mbps
Data rate	GT channels	19,600	—	28,050	19,600	—	25,780	Mbps
Absolute V <sub>MAX</sub> for a receiver pin <sup>(3)</sup>	GT channels	—	—	1.2	—	—	1.2	V
Absolute V <sub>MIN</sub> for a receiver pin	GT channels	-0.4	—	—	-0.4	—	—	V
Maximum peak-to-peak differential input voltage V <sub>ID</sub> (diff p-p) before device configuration <sup>(20)</sup>	GT channels	—	—	1.6	—	—	1.6	V
	GX channels	<sup>(8)</sup>						
Maximum peak-to-peak differential input voltage V <sub>ID</sub> (diff p-p) after device configuration <sup>(16)</sup> , <sup>(20)</sup>	GT channels V <sub>CCR_GTB</sub> = 1.05 V (V <sub>ICM</sub> = 0.65 V)	—	—	2.2	—	—	2.2	V
	GX channels	<sup>(8)</sup>						
Minimum differential eye opening at receiver serial input pins <sup>(4)</sup> , <sup>(20)</sup>	GT channels	200	—	—	200	—	—	mV
	GX channels	<sup>(8)</sup>						

**Table 28. Transceiver Specifications for Stratix V GT Devices (Part 4 of 5) <sup>(1)</sup>**

Symbol/ Description	Conditions	Transceiver Speed Grade 2			Transceiver Speed Grade 3			Unit
		Min	Typ	Max	Min	Typ	Max	
Data rate	GT channels	19,600	—	28,050	19,600	—	25,780	Mbps
Differential on-chip termination resistors	GT channels	—	100	—	—	100	—	Ω
	GX channels	(8)						
V <sub>OCM</sub> (AC coupled)	GT channels	—	500	—	—	500	—	mV
	GX channels	(8)						
Rise/Fall time	GT channels	—	15	—	—	15	—	ps
	GX channels	(8)						
Intra-differential pair skew	GX channels	(8)						
Intra-transceiver block transmitter channel-to- channel skew	GX channels	(8)						
Inter-transceiver block transmitter channel-to- channel skew	GX channels	(8)						
CMU PLL								
Supported Data Range	—	600	—	12500	600	—	8500	Mbps
t <sub>pll_powerdown</sub> <sup>(13)</sup>	—	1	—	—	1	—	—	μs
t <sub>pll_lock</sub> <sup>(14)</sup>	—	—	—	10	—	—	10	μs
ATX PLL								
Supported Data Rate Range for GX Channels	VCO post- divider L=2	8000	—	12500	8000	—	8500	Mbps
	L=4	4000	—	6600	4000	—	6600	Mbps
	L=8	2000	—	3300	2000	—	3300	Mbps
	L=8, Local/Central Clock Divider =2	1000	—	1762.5	1000	—	1762.5	Mbps
Supported Data Rate Range for GT Channels	VCO post- divider L=2	9800	—	14025	9800	—	12890	Mbps
t <sub>pll_powerdown</sub> <sup>(13)</sup>	—	1	—	—	1	—	—	μs
t <sub>pll_lock</sub> <sup>(14)</sup>	—	—	—	10	—	—	10	μs
fPLL								
Supported Data Range	—	600	—	3250/ 3.125 <sup>(23)</sup>	600	—	3250/ 3.125 <sup>(23)</sup>	Mbps
t <sub>pll_powerdown</sub> <sup>(13)</sup>	—	1	—	—	1	—	—	μs

Table 29 shows the  $V_{OD}$  settings for the GT channel.

**Table 29. Typical  $V_{OD}$  Setting for GT Channel, TX Termination = 100  $\Omega$**

Symbol	$V_{OD}$ Setting	$V_{OD}$ Value (mV)
<b><math>V_{OD}</math> differential peak to peak typical <sup>(1)</sup></b>	0	0
	1	200
	2	400
	3	600
	4	800
	5	1000

**Note:**

(1) Refer to Figure 4.

Figure 4 shows the differential transmitter output waveform.

**Figure 4. Differential Transmitter/Receiver Output/Input Waveform**

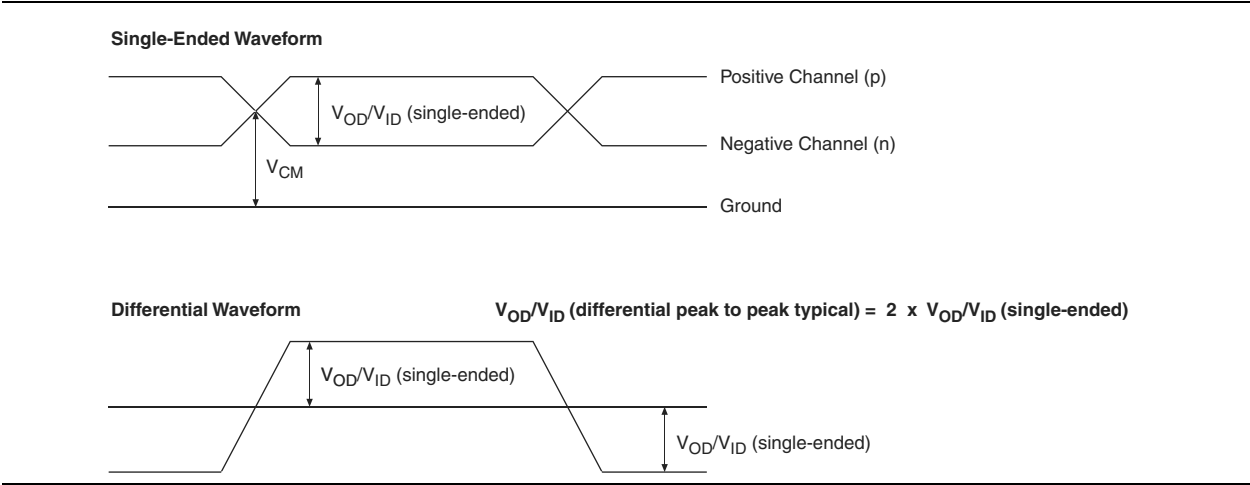


Figure 5 shows the Stratix V AC gain curves for GT channels.

**Figure 5. AC Gain Curves for GT Channels**

## PLL Specifications

Table 31 lists the Stratix V PLL specifications when operating in both the commercial junction temperature range (0° to 85°C) and the industrial junction temperature range (–40° to 100°C).

**Table 31. PLL Specifications for Stratix V Devices (Part 1 of 3)**

Symbol	Parameter	Min	Typ	Max	Unit
$f_{IN}$	Input clock frequency (C1, C2, C2L, I2, and I2L speed grades)	5	—	800 <sup>(1)</sup>	MHz
	Input clock frequency (C3, I3, I3L, and I3YY speed grades)	5	—	800 <sup>(1)</sup>	MHz
	Input clock frequency (C4, I4 speed grades)	5	—	650 <sup>(1)</sup>	MHz
$f_{INPFD}$	Input frequency to the PFD	5	—	325	MHz
$f_{FINPFD}$	Fractional Input clock frequency to the PFD	50	—	160	MHz
$f_{VCO}$ <sup>(9)</sup>	PLL VCO operating range (C1, C2, C2L, I2, I2L speed grades)	600	—	1600	MHz
	PLL VCO operating range (C3, I3, I3L, I3YY speed grades)	600	—	1600	MHz
	PLL VCO operating range (C4, I4 speed grades)	600	—	1300	MHz
$t_{EINDUTY}$	Input clock or external feedback clock input duty cycle	40	—	60	%
$f_{OUT}$	Output frequency for an internal global or regional clock (C1, C2, C2L, I2, I2L speed grades)	—	—	717 <sup>(2)</sup>	MHz
	Output frequency for an internal global or regional clock (C3, I3, I3L speed grades)	—	—	650 <sup>(2)</sup>	MHz
	Output frequency for an internal global or regional clock (C4, I4 speed grades)	—	—	580 <sup>(2)</sup>	MHz
$f_{OUT\_EXT}$	Output frequency for an external clock output (C1, C2, C2L, I2, I2L speed grades)	—	—	800 <sup>(2)</sup>	MHz
	Output frequency for an external clock output (C3, I3, I3L speed grades)	—	—	667 <sup>(2)</sup>	MHz
	Output frequency for an external clock output (C4, I4 speed grades)	—	—	553 <sup>(2)</sup>	MHz
$t_{OUTDUTY}$	Duty cycle for a dedicated external clock output (when set to 50%)	45	50	55	%
$t_{FCOMP}$	External feedback clock compensation time	—	—	10	ns
$f_{DYCONFIGCLK}$	Dynamic Configuration Clock used for <code>mgmt_clk</code> and <code>scanclk</code>	—	—	100	MHz
$t_{LOCK}$	Time required to lock from the end-of-device configuration or deassertion of <code>areset</code>	—	—	1	ms
$t_{DLOCK}$	Time required to lock dynamically (after switchover or reconfiguring any non-post-scale counters/delays)	—	—	1	ms
$f_{CLBW}$	PLL closed-loop low bandwidth	—	0.3	—	MHz
	PLL closed-loop medium bandwidth	—	1.5	—	MHz
	PLL closed-loop high bandwidth <sup>(7)</sup>	—	4	—	MHz
$t_{PLL\_PSERR}$	Accuracy of PLL phase shift	—	—	±50	ps
$t_{ARESET}$	Minimum pulse width on the <code>areset</code> signal	10	—	—	ns



**Table 31. PLL Specifications for Stratix V Devices (Part 3 of 3)**

Symbol	Parameter	Min	Typ	Max	Unit
$f_{RES}$	Resolution of VCO frequency ( $f_{INPFD} = 100$ MHz)	390625	5.96	0.023	Hz

**Notes to Table 31:**

- (1) This specification is limited in the Quartus II software by the I/O maximum frequency. The maximum I/O frequency is different for each I/O standard.
- (2) This specification is limited by the lower of the two: I/O  $f_{MAX}$  or  $f_{OUT}$  of the PLL.
- (3) A high input jitter directly affects the PLL output jitter. To have low PLL output clock jitter, you must provide a clean clock source < 120 ps.
- (4)  $f_{REF}$  is  $f_{IN}/N$  when  $N = 1$ .
- (5) Peak-to-peak jitter with a probability level of  $10^{-12}$  (14 sigma, 99.9999999974404% confidence level). The output jitter specification applies to the intrinsic jitter of the PLL, when an input jitter of 30 ps is applied. The external memory interface clock output jitter specifications use a different measurement method and are available in Table 44 on page 52.
- (6) The cascaded PLL specification is only applicable with the following condition:
  - a. Upstream PLL:  $0.59\text{MHz} \leq \text{Upstream PLL BW} < 1$  MHz
  - b. Downstream PLL: Downstream PLL BW > 2 MHz
- (7) High bandwidth PLL settings are not supported in external feedback mode.
- (8) The external memory interface clock output jitter specifications use a different measurement method, which is available in Table 42 on page 50.
- (9) The VCO frequency reported by the Quartus II software in the PLL Usage Summary section of the compilation report takes into consideration the VCO post-scale counter K value. Therefore, if the counter K has a value of 2, the frequency reported can be lower than the  $f_{VCO}$  specification.
- (10) This specification only covers fractional PLL for low bandwidth. The  $f_{VCO}$  for fractional value range 0.05 - 0.95 must be  $\geq 1000$  MHz, while  $f_{VCO}$  for fractional value range 0.20 - 0.80 must be  $\geq 1200$  MHz.
- (11) This specification only covered fractional PLL for low bandwidth. The  $f_{VCO}$  for fractional value range 0.05-0.95 must be  $\geq 1000$  MHz.
- (12) This specification only covered fractional PLL for low bandwidth. The  $f_{VCO}$  for fractional value range 0.20-0.80 must be  $\geq 1200$  MHz.

## DSP Block Specifications

Table 32 lists the Stratix V DSP block performance specifications.

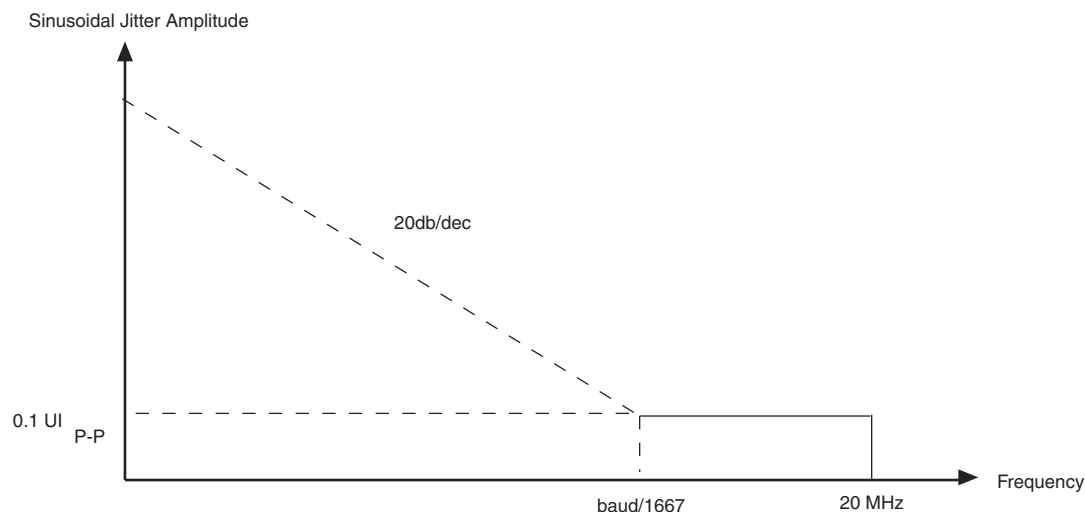
**Table 32. Block Performance Specifications for Stratix V DSP Devices (Part 1 of 2)**

Mode	Peformance							Unit
	C1	C2, C2L	I2, I2L	C3	I3, I3L, I3YY	C4	I4	
Modes using one DSP								
Three 9 x 9	600	600	600	480	480	420	420	MHz
One 18 x 18	600	600	600	480	480	420	400	MHz
Two partial 18 x 18 (or 16 x 16)	600	600	600	480	480	420	400	MHz
One 27 x 27	500	500	500	400	400	350	350	MHz
One 36 x 18	500	500	500	400	400	350	350	MHz
One sum of two 18 x 18(One sum of 2 16 x 16)	500	500	500	400	400	350	350	MHz
One sum of square	500	500	500	400	400	350	350	MHz
One 18 x 18 plus 36 (a x b) + c	500	500	500	400	400	350	350	MHz
Modes using two DSPs								
Three 18 x 18	500	500	500	400	400	350	350	MHz
One sum of four 18 x 18	475	475	475	380	380	300	300	MHz
One sum of two 27 x 27	465	465	450	380	380	300	290	MHz
One sum of two 36 x 18	475	475	475	380	380	300	300	MHz
One complex 18 x 18	500	500	500	400	400	350	350	MHz
One 36 x 36	475	475	475	380	380	300	300	MHz

**Table 38. LVDS Soft-CDR/DPA Sinusoidal Jitter Mask Values for a Data Rate  $\geq 1.25$  Gbps**

Jitter Frequency (Hz)		Sinusoidal Jitter (UI)
F1	10,000	25.000
F2	17,565	25.000
F3	1,493,000	0.350
F4	50,000,000	0.350

Figure 9 shows the LVDS soft-CDR/DPA sinusoidal jitter tolerance specification for a data rate  $< 1.25$  Gbps.

**Figure 9. LVDS Soft-CDR/DPA Sinusoidal Jitter Tolerance Specification for a Data Rate  $< 1.25$  Gbps**

### DLL Range, DQS Logic Block, and Memory Output Clock Jitter Specifications

Table 39 lists the DLL range specification for Stratix V devices. The DLL is always in 8-tap mode in Stratix V devices.

**Table 39. DLL Range Specifications for Stratix V Devices <sup>(1)</sup>**

C1	C2, C2L, I2, I2L	C3, I3, I3L, I3YY	C4,I4	Unit
300-933	300-933	300-890	300-890	MHz

**Note to Table 39:**

- (1) Stratix V devices support memory interface frequencies lower than 300 MHz, although the reference clock that feeds the DLL must be at least 300 MHz. To support interfaces below 300 MHz, multiply the reference clock feeding the DLL to ensure the frequency is within the supported range of the DLL.

Table 40 lists the DQS phase offset delay per stage for Stratix V devices.

**Table 40. DQS Phase Offset Delay Per Setting for Stratix V Devices <sup>(1), (2)</sup> (Part 1 of 2)**

Speed Grade	Min	Max	Unit
C1	8	14	ps
C2, C2L, I2, I2L	8	14	ps
C3,I3, I3L, I3YY	8	15	ps

## Remote System Upgrades

Table 56 lists the timing parameter specifications for the remote system upgrade circuitry.

**Table 56. Remote System Upgrade Circuitry Timing Specifications**

Parameter	Minimum	Maximum	Unit
$t_{RU\_nCONFIG}^{(1)}$	250	—	ns
$t_{RU\_nRSTIMER}^{(2)}$	250	—	ns

**Notes to Table 56:**

- (1) This is equivalent to strobing the reconfiguration input of the ALTREMOTE\_UPDATE megafunction high for the minimum timing specification. For more information, refer to the Remote System Upgrade State Machine section of the “Configuration, Design Security, and Remote System Upgrades in Stratix V Devices” chapter.
- (2) This is equivalent to strobing the reset\_timer input of the ALTREMOTE\_UPDATE megafunction high for the minimum timing specification. For more information, refer to the User Watchdog Timer section of the “Configuration, Design Security, and Remote System Upgrades in Stratix V Devices” chapter.

## User Watchdog Internal Circuitry Timing Specification

Table 57 lists the operating range of the 12.5-MHz internal oscillator.

**Table 57. 12.5-MHz Internal Oscillator Specifications**

Minimum	Typical	Maximum	Units
5.3	7.9	12.5	MHz

## I/O Timing

Altera offers two ways to determine I/O timing—the Excel-based I/O Timing and the Quartus II Timing Analyzer.

Excel-based I/O timing provides pin timing performance for each device density and speed grade. The data is typically used prior to designing the FPGA to get an estimate of the timing budget as part of the link timing analysis. The Quartus II Timing Analyzer provides a more accurate and precise I/O timing data based on the specifics of the design after you complete place-and-route.



You can download the Excel-based I/O Timing spreadsheet from the Stratix V Devices Documentation web page.

## Programmable IOE Delay

Table 58 lists the Stratix V IOE programmable delay settings.

**Table 58. IOE Programmable Delay for Stratix V Devices (Part 1 of 2)**

Parameter (1)	Available Settings	Min Offset (2)	Fast Model		Slow Model							
			Industrial	Commercial	C1	C2	C3	C4	I2	I3, I3YY	I4	Unit
D1	64	0	0.464	0.493	0.838	0.838	0.924	1.011	0.844	0.921	1.006	ns
D2	32	0	0.230	0.244	0.415	0.415	0.459	0.503	0.417	0.456	0.500	ns

**Table 58. IOE Programmable Delay for Stratix V Devices (Part 2 of 2)**

Parameter (1)	Available Settings	Min Offset (2)	Fast Model		Slow Model							
			Industrial	Commercial	C1	C2	C3	C4	I2	I3, I3YY	I4	Unit
D3	8	0	1.587	1.699	2.793	2.793	2.992	3.192	2.811	3.047	3.257	ns
D4	64	0	0.464	0.492	0.838	0.838	0.924	1.011	0.843	0.920	1.006	ns
D5	64	0	0.464	0.493	0.838	0.838	0.924	1.011	0.844	0.921	1.006	ns
D6	32	0	0.229	0.244	0.415	0.415	0.458	0.503	0.418	0.456	0.499	ns

**Notes to Table 58:**

- (1) You can set this value in the Quartus II software by selecting **D1, D2, D3, D5, and D6** in the **Assignment Name** column of **Assignment Editor**.
- (2) Minimum offset does not include the intrinsic delay.

## Programmable Output Buffer Delay

Table 59 lists the delay chain settings that control the rising and falling edge delays of the output buffer. The default delay is 0 ps.

**Table 59. Programmable Output Buffer Delay for Stratix V Devices (1)**

Symbol	Parameter	Typical	Unit
D <sub>OUTBUF</sub>	Rising and/or falling edge delay	0 (default)	ps
		25	ps
		50	ps
		75	ps

**Note to Table 59:**

- (1) You can set the programmable output buffer delay in the Quartus II software by setting the **Output Buffer Delay Control** assignment to either positive, negative, or both edges, with the specific values stated here (in ps) for the **Output Buffer Delay** assignment.

## Glossary

Table 60 lists the glossary for this chapter.

**Table 60. Glossary (Part 1 of 4)**

Letter	Subject	Definitions
A	—	—
B		
C		
D	—	—
E	—	—
F	f <sub>HCLK</sub>	Left and right PLL input clock frequency.
	f <sub>HSDR</sub>	High-speed I/O block—Maximum and minimum <b>LVDS</b> data transfer rate (f <sub>HSDR</sub> = 1/TUI), non-DPA.
	f <sub>HSDRDPA</sub>	High-speed I/O block—Maximum and minimum <b>LVDS</b> data transfer rate (f <sub>HSDRDPA</sub> = 1/TUI), DPA.

**Table 60. Glossary (Part 4 of 4)**

Letter	Subject	Definitions
<b>V</b>	<b>V<sub>CM(DC)</sub></b>	DC common mode input voltage.
	<b>V<sub>ICM</sub></b>	Input common mode voltage—The common mode of the differential signal at the receiver.
	<b>V<sub>ID</sub></b>	Input differential voltage swing—The difference in voltage between the positive and complementary conductors of a differential transmission at the receiver.
	<b>V<sub>DIF(AC)</sub></b>	AC differential input voltage—Minimum AC input differential voltage required for switching.
	<b>V<sub>DIF(DC)</sub></b>	DC differential input voltage— Minimum DC input differential voltage required for switching.
	<b>V<sub>IH</sub></b>	Voltage input high—The minimum positive voltage applied to the input which is accepted by the device as a logic high.
	<b>V<sub>IH(AC)</sub></b>	High-level AC input voltage
	<b>V<sub>IH(DC)</sub></b>	High-level DC input voltage
	<b>V<sub>IL</sub></b>	Voltage input low—The maximum positive voltage applied to the input which is accepted by the device as a logic low.
	<b>V<sub>IL(AC)</sub></b>	Low-level AC input voltage
	<b>V<sub>IL(DC)</sub></b>	Low-level DC input voltage
	<b>V<sub>OCM</sub></b>	Output common mode voltage—The common mode of the differential signal at the transmitter.
	<b>V<sub>OD</sub></b>	Output differential voltage swing—The difference in voltage between the positive and complementary conductors of a differential transmission at the transmitter.
	<b>V<sub>SWING</sub></b>	Differential input voltage
	<b>V<sub>X</sub></b>	Input differential cross point voltage
	<b>V<sub>OX</sub></b>	Output differential cross point voltage
<b>W</b>	<b>W</b>	High-speed I/O block—clock boost factor
<b>X</b>	—	—
<b>Y</b>		
<b>Z</b>		