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Intel - 5SGXEA7N3F40C4 Datasheet



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Details

Product Status	Obsolete
Number of LABs/CLBs	234720
Number of Logic Elements/Cells	622000
Total RAM Bits	51200000
Number of I/O	600
Number of Gates	-
Voltage - Supply	0.82V ~ 0.88V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	1517-BBGA, FCBGA
Supplier Device Package	1517-FBGA (40x40)
Purchase URL	https://www.e-xfl.com/product-detail/intel/5sgxea7n3f40c4

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Table 5 lists the maximum allowed input overshoot voltage and the duration of the overshoot voltage as a percentage of device lifetime. The maximum allowed overshoot duration is specified as a percentage of high time over the lifetime of the device. A DC signal is equivalent to 100% of the duty cycle. For example, a signal that overshoots to 3.95 V can be at 3.95 V for only ~21% over the lifetime of the device; for a device lifetime of 10 years, the overshoot duration amounts to ~2 years.

Symbol	Description	Condition (V)	Overshoot Duration as % @ T _J = 100°C	Unit					
		3.8	100	%					
		3.85	64	%					
		3.9	36	%					
		3.95	21	%					
Vi (AC)	AC input voltage	4	12	%					
		4.05	7	%					
		4.1	4	%					
		4.15	2	%					
		4.2	1	%					

Table 5. Maximum Allowed Overshoot During Transitions

Figure 1. Stratix V Device Overshoot Duration



Symbol	Description	Devices	Minimum ⁽⁴⁾	Typical	Maximum ⁽⁴⁾	Unit
			0.82	0.85	0.88	
V _{CCR_GXBR}	Receiver analog power supply (right side)		0.87	0.90	0.93	v
(2)	neceiver analog power supply (right side)	ux, us, ui	0.97	1.0	1.03	v
			1.03	1.05	1.07	
V _{CCR_GTBR}	Receiver analog power supply for GT channels (right side)	GT	1.02	1.05	1.08	V
			0.82	0.85	0.88	
V _{CCT GXBL}	Transmitter analog newer supply (left side)	GX, GS, GT	0.87	0.90	0.93	V
(2)	Transmitter analog power supply (left side)		0.97	1.0	1.03	
			1.03	1.05	1.07	
			0.82	0.85	0.88	V
V _{CCT GXBR}	Transmitter analog newer supply (right side)	GX, GS, GT	0.87	0.90	0.93	
(2) _	Transmitter analog power supply (light side)		0.97	1.0	1.03	
			1.03	1.05	1.07	
V_{CCT_GTBR}	Transmitter analog power supply for GT channels (right side)	GT	1.02	1.05	1.08	V
V_{CCL_GTBR}	Transmitter clock network power supply	GT	1.02	1.05	1.08	V
V _{CCH_GXBL}	Transmitter output buffer power supply (left side)	GX, GS, GT	1.425	1.5	1.575	V
V _{CCH_GXBR}	Transmitter output buffer power supply (right side)	GX, GS, GT	1.425	1.5	1.575	V

Table 7.	Recommended Transceiver Power Supply Operating Conditions for Stratix V GX ,	GS , and GT Devices
(Part 2	of 2)	

Notes to Table 7:

(1) This supply must be connected to 3.0 V if the CMU PLL, receiver CDR, or both, are configured at a base data rate > 6.5 Gbps. Up to 6.5 Gbps, you can connect this supply to either 3.0 V or 2.5 V.

(2) Refer to Table 8 to select the correct power supply level for your design.

(3) When using ATX PLLs, the supply must be 3.0 V.

(4) This value describes the budget for the DC (static) power supply tolerance and does not include the dynamic tolerance requirements. Refer to the PDN tool for the additional budget for the dynamic tolerance requirements.

I/O Pin Leakage Current

Table 9 lists the Stratix V I/O pin leakage current specifications.

Table 9.	I/O Pin	Leakage	Current for	Stratix V	Devices (1)
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Symbol	Description	Conditions	Min	Тур	Max	Unit
I _I	Input pin	$V_I = 0 V \text{ to } V_{CCIOMAX}$	-30	_	30	μA
I _{OZ}	Tri-stated I/O pin	$V_0 = 0 V \text{ to } V_{\text{CCIOMAX}}$	-30		30	μA

Note to Table 9:

(1) If $V_0 = V_{CCI0}$ to $V_{CCI0Max}$, 100 μ A of leakage current per I/O is expected.

Bus Hold Specifications

Table 10 lists the Stratix V device family bus hold specifications.

Table 10. Bus Hold Parameters for Stratix V Devices

		I Conditions	V _{CCIO}										
Parameter	Symbol		1.2 V		1.5 V		1.8 V		2.5 V		3.0 V		Unit
			Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Low sustaining current	I _{SUSL}	V _{IN} > V _{IL} (maximum)	22.5	_	25.0	_	30.0	_	50.0	_	70.0	_	μA
High sustaining current	I _{SUSH}	V _{IN} < V _{IH} (minimum)	-22.5		-25.0	_	-30.0	_	-50.0	_	-70.0		μA
Low overdrive current	I _{odl}	$0V < V_{IN} < V_{CCIO}$		120		160		200	_	300		500	μA
High overdrive current	I _{odh}	$0V < V_{IN} < V_{CCIO}$		-120		-160		-200		-300		-500	μΑ
Bus-hold trip point	V _{TRIP}	_	0.45	0.95	0.50	1.00	0.68	1.07	0.70	1.70	0.80	2.00	۷

On-Chip Termination (OCT) Specifications

If you enable OCT calibration, calibration is automatically performed at power-up for I/Os connected to the calibration block. Table 11 lists the Stratix V OCT termination calibration accuracy specifications.

Table 11. OCT Calibration Accuracy Specifications for Stratix V Devices ⁽¹⁾ (Part 1 of 2)

			Calibration Accuracy				
Symbol	Description	Conditions	C1	C2,12	C3,I3, I3YY	C4,14	Unit
25- $Ω$ R _S	Internal series termination with calibration (25- Ω setting)	V _{CCI0} = 3.0, 2.5, 1.8, 1.5, 1.2 V	±15	±15	±15	±15	%

1/0 Standard		V _{ccio} (V)		V _{REF} (V)			ν _π (ν)		
i/O Stanuaru	Min	Тур	Max	Min	Тур	Max	Min	Тур	Max
SSTL-2 Class I, II	2.375	2.5	2.625	0.49 * V _{CCIO}	0.5 * V _{CCIO}	0.51 * V _{CCIO}	V _{REF} – 0.04	V _{REF}	V _{REF} + 0.04
SSTL-18 Class I, II	1.71	1.8	1.89	0.833	0.9	0.969	V _{REF} – 0.04	V _{REF}	V _{REF} + 0.04
SSTL-15 Class I, II	1.425	1.5	1.575	0.49 * V _{CCIO}	0.5 * V _{CCIO}	0.51 * V _{CCIO}	0.49 * V _{CCIO}	0.5 * VCCIO	0.51 * V _{CCIO}
SSTL-135 Class I, II	1.283	1.35	1.418	0.49 * V _{CCIO}	0.5 * V _{CCIO}	0.51 * V _{CCIO}	0.49 * V _{CCIO}	0.5 * V _{CCIO}	0.51 * V _{CCIO}
SSTL-125 Class I, II	1.19	1.25	1.26	0.49 * V _{CCIO}	0.5 * V _{CCIO}	0.51 * V _{CCIO}	0.49 * V _{CCIO}	0.5 * VCCIO	0.51 * V _{CCIO}
SSTL-12 Class I, II	1.14	1.20	1.26	0.49 * V _{CCIO}	0.5 * V _{CCIO}	0.51 * V _{CCIO}	0.49 * V _{CCIO}	0.5 * VCCIO	0.51 * V _{CCIO}
HSTL-18 Class I, II	1.71	1.8	1.89	0.85	0.9	0.95	_	V _{CCI0} /2	_
HSTL-15 Class I, II	1.425	1.5	1.575	0.68	0.75	0.9	_	V _{CCI0} /2	_
HSTL-12 Class I, II	1.14	1.2	1.26	0.47 * V _{CCIO}	0.5 * V _{CCIO}	0.53 * V _{CCIO}	_	V _{CCI0} /2	_
HSUL-12	1.14	1.2	1.3	0.49 * V _{CCIO}	0.5 * V _{CCIO}	0.51 * V _{CCIO}	_		

Table 18. Single-Ended SSTL, HSTL, and HSUL I/O Reference Voltage Specifications for Stratix V Devi	ces
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Table 19.	Single-Ended SSTL	, HSTL, and HSUL I/	/O Standards Signal S	Specifications for	Stratix V Devices	(Part 1 of 2)
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1/0 Standard	V _{IL(DC)} (V)		V _{IH(DC)} (V)		V _{IL(AC)} (V)	V _{IH(AC)} (V)	V _{ol} (V)	V _{oh} (V)	I (mA)	I _{oh}
i/o Stanuaru	Min	Max	Min	Max	Max	Min	Max	Min	I _{ol} (IIIA)	(mÄ)
SSTL-2 Class I	-0.3	V _{REF} – 0.15	V _{REF} + 0.15	V _{CCI0} + 0.3	V _{REF} – 0.31	V _{REF} + 0.31	V _{TT} – 0.608	V _{TT} + 0.608	8.1	-8.1
SSTL-2 Class II	-0.3	V _{REF} – 0.15	V _{REF} + 0.15	V _{CCI0} + 0.3	V _{REF} – 0.31	V _{REF} + 0.31	V _{TT} – 0.81	V _{TT} + 0.81	16.2	-16.2
SSTL-18 Class I	-0.3	V _{REF} – 0.125	V _{REF} + 0.125	V _{CCI0} + 0.3	V _{REF} – 0.25	V _{REF} + 0.25	V _{TT} – 0.603	V _{TT} + 0.603	6.7	-6.7
SSTL-18 Class II	-0.3	V _{REF} – 0.125	V _{REF} + 0.125	V _{CCI0} + 0.3	V _{REF} – 0.25	V _{REF} + 0.25	0.28	V _{CCI0} – 0.28	13.4	-13.4
SSTL-15 Class I	_	V _{REF} – 0.1	V _{REF} + 0.1	_	V _{REF} – 0.175	V _{REF} + 0.175	0.2 * V _{CCI0}	0.8 * V _{CCI0}	8	-8
SSTL-15 Class II	_	V _{REF} – 0.1	V _{REF} + 0.1	_	V _{REF} – 0.175	V _{REF} + 0.175	0.2 * V _{CCI0}	0.8 * V _{CCI0}	16	-16
SSTL-135 Class I, II	_	V _{REF} – 0.09	V _{REF} + 0.09	—	V _{REF} – 0.16	V _{REF} + 0.16	0.2 * V _{CCI0}	0.8 * V _{CCI0}	—	_
SSTL-125 Class I, II		V _{REF} – 0.85	V _{REF} + 0.85	_	V _{REF} – 0.15	V _{REF} + 0.15	0.2 * V _{CCI0}	0.8 * V _{CCI0}		
SSTL-12 Class I, II	_	V _{REF} – 0.1	V _{REF} + 0.1	_	V _{REF} – 0.15	V _{REF} + 0.15	0.2 * V _{CCI0}	0.8 * V _{CCI0}	_	

I/O Standard	V _{IL(DI}	_{c)} (V)	V _{IH(D}	_{C)} (V)	V _{IL(AC)} (V)	V _{IH(AC)} (V)	V _{ol} (V)	V _{oh} (V)	I (mA)	l _{oh}
i/U Stanuaru	Min	Max	Min	Max	Max	Min	Max	Min	1 ₀₁ (11174)	(mA)
HSTL-18 Class I	—	V _{REF} – 0.1	V _{REF} + 0.1	_	$V_{REF} - 0.2$	V _{REF} + 0.2	0.4	V _{CCI0} – 0.4	8	-8
HSTL-18 Class II	_	V _{REF} – 0.1	V _{REF} + 0.1	_	V _{REF} - 0.2	V _{REF} + 0.2	0.4	V _{CCI0} – 0.4	16	-16
HSTL-15 Class I	_	V _{REF} – 0.1	V _{REF} + 0.1	_	V _{REF} - 0.2	V _{REF} + 0.2	0.4	V _{CCI0} – 0.4	8	-8
HSTL-15 Class II	_	V _{REF} – 0.1	V _{REF} + 0.1	_	V _{REF} - 0.2	V _{REF} + 0.2	0.4	V _{CCI0} – 0.4	16	-16
HSTL-12 Class I	-0.15	V _{REF} - 0.08	V _{REF} + 0.08	V _{CCIO} + 0.15	V _{REF} – 0.15	V _{REF} + 0.15	0.25* V _{CCI0}	0.75* V _{CCI0}	8	-8
HSTL-12 Class II	-0.15	V _{REF} - 0.08	V _{REF} + 0.08	V _{CCIO} + 0.15	V _{REF} – 0.15	V _{REF} + 0.15	0.25* V _{CCI0}	0.75* V _{CCI0}	16	-16
HSUL-12	—	V _{REF} - 0.13	V _{REF} + 0.13	_	V _{REF} – 0.22	V _{REF} + 0.22	0.1* V _{CCIO}	0.9* V _{CCI0}	_	

Table 19. Single-Ended SSTL, HSTL, and HSUL I/O Standards Signal Specifications for Stratix V Devices (Part 2 of 2)

Table 20. Differential SSTL I/O Standards for Stratix V Devices

1/0 Standard		V _{ccio} (V)		V _{SWIN}	_{G(DC)} (V)		V _{X(AC)} (V)		V _{SWING(AC)} (V)		
ijo Stanuaru	Min	Тур	Max	Min	Max	Min	Тур	Max	Min	Max	
SSTL-2 Class I, II	2.375	2.5	2.625	0.3	V _{CCI0} + 0.6	V _{CCI0} /2- 0.2	_	V _{CCI0} /2 + 0.2	0.62	V _{CCI0} + 0.6	
SSTL-18 Class I, II	1.71	1.8	1.89	0.25	V _{CCIO} + 0.6	V _{CCI0} /2- 0.175	y/2 - V _{CCI0} /2 + 75 - V _{CCI0} /2 + 0.175		0.5	V _{CCI0} + 0.6	
SSTL-15 Class I, II	1.425	1.5	1.575	0.2	(1)	V _{CCI0} /2- 0.15	_	V _{CCI0} /2 + 0.15		_	
SSTL-135 Class I, II	1.283	1.35	1.45	0.2	(1)	V _{CCI0} /2- 0.15	V _{CCIO} /2	V _{CCI0} /2 + 0.15	2(V _{IH(AC)} - V _{REF})	2(V _{IL(AC)} - V _{REF})	
SSTL-125 Class I, II	1.19	1.25	1.31	0.18	(1)	V _{CCI0} /2- 0.15	V _{CCIO} /2	V _{CCI0} /2 + 0.15	2(V _{IH(AC)} - V _{REF})	_	
SSTL-12 Class I, II	1.14	1.2	1.26	0.18	_	V _{REF} 0.15	V _{CCI0} /2	V _{REF} + 0.15	-0.30	0.30	

Note to Table 20:

(1) The maximum value for $V_{SWING(DC)}$ is not defined. However, each single-ended signal needs to be within the respective single-ended limits $(V_{IH(DC)} \text{ and } V_{IL(DC)})$.

						. ,							
I/O		V _{ccio} (V)		V _{DIF(}	_{DC)} (V)	V _{X(AC)} (V)				V _{CM(DC)} (V)	V _{DIF(/}	_{AC)} (V)
Standard	Min	Тур	Max	Min	Max	Min	Тур	Max	Min	Тур	Max	Min	Max
HSTL-18 Class I, II	1.71	1.8	1.89	0.2	_	0.78	_	1.12	0.78	_	1.12	0.4	_
HSTL-15 Class I, II	1.425	1.5	1.575	0.2	_	0.68	_	0.9	0.68		0.9	0.4	_

Symbol/ Description	Conditions	Trai	nsceive Grade	r Speed 1	Trai	nsceive Grade	r Speed 2	Trar	isceive Grade	r Speed 3	Unit
		Min	Тур	Max	Min	Тур	Max	Min	Тур	Max	
t _{pll_lock} (16)	_			10			10		_	10	μs

Table 23. Transceiver Specifications for Stratix V GX and GS Devices ⁽¹⁾ (Part 7 of 7)

Notes to Table 23:

(2) The reference clock common mode voltage is equal to the V_{CCR_GXB} power supply level.

(3) This supply must be connected to 1.0 V if the transceiver is configured at a data rate > 6.5 Gbps, and to 1.05 V if configured at a data rate > 10.3 Gbps when DFE is used. For data rates up to 6.5 Gbps, you can connect this supply to 0.85 V.

- (4) This supply follows VCCR_GXB.
- (5) The device cannot tolerate prolonged operation at this absolute maximum.
- (6) The differential eye opening specification at the receiver input pins assumes that **Receiver Equalization** is disabled. If you enable **Receiver Equalization**, the receiver circuitry can tolerate a lower minimum eye opening, depending on the equalization level.
- (7) The Quartus II software automatically selects the appropriate slew rate depending on the configured data rate or functional mode.
- (8) The input reference clock frequency options depend on the data rate and the device speed grade.
- (9) The line data rate may be limited by PCS-FPGA interface speed grade.
- (10) Refer to Figure 1 for the GX channel AC gain curves. The total effective AC gain is the AC gain minus the DC gain.
- (11) t_{LTR} is the time required for the receive CDR to lock to the input reference clock frequency after coming out of reset.
- (12) t_{LTD} is time required for the receiver CDR to start recovering valid data after the rx_is_lockedtodata signal goes high.
- (13) t_{LTD_manual} is the time required for the receiver CDR to start recovering valid data after the rx_is_lockedtodata signal goes high when the CDR is functioning in the manual mode.
- (14) $t_{LTR_LTD_manual}$ is the time the receiver CDR must be kept in lock to reference (LTR) mode after the rx_is_lockedtoref signal goes high when the CDR is functioning in the manual mode.
- (15) $t_{pll_powerdown}$ is the PLL powerdown minimum pulse width.
- (16) t_{pll lock} is the time required for the transmitter CMU/ATX PLL to lock to the input reference clock frequency after coming out of reset.
- (17) To calculate the REFCLK rms phase jitter requirement for PCIe at reference clock frequencies other than 100 MHz, use the following formula: REFCLK rms phase jitter at f(MHz) = REFCLK rms phase jitter at 100 MHz × 100/f.
- (18) The maximum peak to peak differential input voltage V_{ID} after device configuration is equal to 4 × (absolute V_{MAX} for receiver pin V_{ICM}).
- (19) For ES devices, R_{BEF} is 2000 $\Omega \pm 1\%$.
- (20) To calculate the REFCLK phase noise requirement at frequencies other than 622 MHz, use the following formula: REFCLK phase noise at f(MHz) = REFCLK phase noise at 622 MHz + 20*log(f/622).
- (21) SFP/+ optical modules require the host interface to have RD+/- differentially terminated with 100 Ω. The internal OCT feature is available after the Stratix V FPGA configuration is completed. Altera recommends that FPGA configuration is completed before inserting the optical module. Otherwise, minimize unnecessary removal and insertion with unconfigured devices.
- (22) Refer to Figure 2.
- (23) For oversampling designs to support data rates less than the minimum specification, the CDR needs to be in LTR mode only.
- (24) I3YY devices can achieve data rates up to 10.3125 Gbps.
- (25) When you use fPLL as a TXPLL of the transceiver.
- (26) REFCLK performance requires to meet transmitter REFCLK phase noise specification.
- (27) Minimum eye opening of 85 mV is only for the unstressed input eye condition.

⁽¹⁾ Speed grades shown in Table 23 refer to the PMA Speed Grade in the device ordering code. The maximum data rate could be restricted by the Core/PCS speed grade. Contact your Altera Sales Representative for the maximum data rate specifications in each speed grade combination offered. For more information about device ordering codes, refer to the Stratix V Device Overview.

Table 28. Transceiver Specifications for Stratix V GT Devices (Part 2 of 5)⁽¹⁾

Symbol/	Conditions	S	Transceive peed Grade	r 2	SI	Fransceive Deed Grade	r 3	Unit	
Description		Min	Тур	Max	Min	Тур	Max		
	100 Hz	—	—	-70			-70		
Transmitter REFCLK	1 kHz		_	-90	_	_	-90		
Phase Noise (622	10 kHz		—	-100	_		-100	dBc/Hz	
MHz) ⁽¹⁸⁾	100 kHz			-110			-110		
	\geq 1 MHz	—	—	-120		_	-120		
Transmitter REFCLK Phase Jitter (100 MHz) ⁽¹⁵⁾	10 kHz to 1.5 MHz (PCle)	_	_	3		_	3	ps (rms)	
RREF ⁽¹⁷⁾	_	_	1800 ± 1%	—	_	1800 ± 1%	_	Ω	
Transceiver Clocks									
fixedclk clock frequency	PCIe Receiver Detect	_	100 or 125	_	_	100 or 125	_	MHz	
Reconfiguration clock (mgmt_clk_clk) frequency	_	100	_	125	100	_	125	MHz	
Receiver	•								
Supported I/O Standards	_	1.4-V PCML, 1.5-V PCML, 2.5-V PCML, LVPECL, and LVDS							
Data rate (Standard PCS) ⁽²¹⁾	GX channels	600	_	8500	600	_	8500	Mbps	
Data rate (10G PCS) ⁽²¹⁾	GX channels	600	_	12,500	600	_	12,500	Mbps	
Data rate	GT channels	19,600	—	28,050	19,600		25,780	Mbps	
Absolute V _{MAX} for a receiver pin ⁽³⁾	GT channels	_	_	1.2	_	_	1.2	V	
Absolute V _{MIN} for a receiver pin	GT channels	-0.4	_	—	-0.4	_	_	V	
Maximum peak-to-peak	GT channels	_		1.6	—	_	1.6	V	
differential input voltage V _{ID} (diff p-p) before device configuration ⁽²⁰⁾	GX channels				(8)				
	GT channels								
Maximum peak-to-peak differential input voltage V_{ID} (diff p-p) after device	V _{CCR_GTB} = 1.05 V (V _{ICM} = 0.65 V)	_	_	2.2	_	_	2.2	V	
	GX channels		1	1 1	(8)			1	
Minimum differential	GT channels	200	_	—	200		_	mV	
eye opening at receiver serial input pins ⁽⁴⁾ , ⁽²⁰⁾	GX channels			·	(8)				

	Table 28.	Transceiver S	pecifications	for Stratix V	GT Devices	(Part 4 of 5) (1)
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Symbol/	Conditions	s	Transceive peed Grade	r 2	ר Sp	Fransceive Deed Grade	r 3	Unit		
Description		Min	Transceiver leed Grade 2 Transceiver Speed Grade 3 Typ Max Min Typ Max - 28,050 19,600 25,780 100 100 (8) 500 (8) 15 (8) 15 (8) 100 (8) 10 12500 600 8500 10 10 10 10 12500 8000 8500 12500 8000 1762.5 1250 9800 12890 10 - <td< th=""><th></th></td<>							
Data rate	GT channels	19,600	_	28,050	19,600		25,780	Mbps		
Differential on-chip	GT channels	_	100	—		100	_	Ω		
termination resistors	GX channels				(8)					
	GT channels	_	500	_		500	_	mV		
V _{OCM} (AC Coupled)	GX channels		•	•	(8)					
Dice/Fell time	GT channels	_	15	—	—	15	—	ps		
Rise/Fail lime	GX channels				(8)					
Intra-differential pair skew	GX channels				(8)					
Intra-transceiver block transmitter channel-to- channel skew	GX channels									
Inter-transceiver block transmitter channel-to- channel skew	GX channels	(8)								
CMU PLL										
Supported Data Range	—	600		12500	600		8500	Mbps		
t _{pll_powerdown} ⁽¹³⁾	—	1	—	—	1	_	—	μs		
t _{pll_lock} ⁽¹⁴⁾	—	_	—	10	_	_	10	μs		
ATX PLL										
	VCO post- divider L=2	8000	_	12500	8000	_	8500	Mbps		
	L=4	4000	—	6600	4000	_	6600	Mbps		
Supported Data Rate	L=8	2000	—	3300	2000	_	3300	Mbps		
Range for GX Channels	L=8, Local/Central Clock Divider =2	1000	_	1762.5	1000	_	1762.5	Mbps		
Supported Data Rate Range for GT Channels	VCO post- divider L=2	9800	_	14025	9800	_	12890	Mbps		
t _{pll_powerdown} ⁽¹³⁾	—	1	—	—	1	_	—	μs		
t _{pll_lock} ⁽¹⁴⁾	—	_	—	10	_	_	10	μs		
fPLL										
Supported Data Range		600		3250/ 3.125 ⁽²³⁾	600		3250/ 3.125 ⁽²³⁾	Mbps		
t _{pll_powerdown} ⁽¹³⁾	—	1	—	—	1	—	—	μs		

Table 28. Tra	nsceiver Specifi	cations for Stra	tix V GT Devices	(Part 5 of 5) ⁽¹⁾
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Symbol/ Description	Conditions	TransceiverTransceiverSpeed Grade 2Speed Grade 3					r 3	Unit
		Min	Тур	Max	Min	Тур	Max	
t _{pll_lock} ⁽¹⁴⁾	—	—	_	10	—	—	10	μs

Notes to Table 28:

- (1) Speed grades shown refer to the PMA Speed Grade in the device ordering code. The maximum data rate could be restricted by the Core/PCS speed grade. Contact your Altera Sales Representative for the maximum data rate specifications in each speed grade combination offered. For more information about device ordering codes, refer to the Stratix V Device Overview.
- (2) The reference clock common mode voltage is equal to the VCCR_GXB power supply level.
- (3) The device cannot tolerate prolonged operation at this absolute maximum.
- (4) The differential eye opening specification at the receiver input pins assumes that receiver equalization is disabled. If you enable receiver equalization, the receiver circuitry can tolerate a lower minimum eye opening, depending on the equalization level.
- (5) Refer to Figure 5 for the GT channel AC gain curves. The total effective AC gain is the AC gain minus the DC gain.
- (6) Refer to Figure 6 for the GT channel DC gain curves.
- (7) CFP2 optical modules require the host interface to have the receiver data pins differentially terminated with 100 Ω. The internal OCT feature is available after the Stratix V FPGA configuration is completed. Altera recommends that FPGA configuration is completed before inserting the optical module. Otherwise, minimize unnecessary removal and insertion with unconfigured devices.
- (8) Specifications for this parameter are the same as for Stratix V GX and GS devices. See Table 23 for specifications.
- (9) t_{1 TR} is the time required for the receive CDR to lock to the input reference clock frequency after coming out of reset.
- (10) t_{LTD} is time required for the receiver CDR to start recovering valid data after the rx is lockedtodata signal goes high.
- (11) t_{LTD_manual} is the time required for the receiver CDR to start recovering valid data after the rx_is_lockedtodata signal goes high when the CDR is functioning in the manual mode.
- (12) t_{LTR_LTD_manual} is the time the receiver CDR must be kept in lock to reference (LTR) mode after the rx_is_lockedtoref signal goes high when the CDR is functioning in the manual mode.
- (13) tpll_powerdown is the PLL powerdown minimum pulse width.
- (14) tpll lock is the time required for the transmitter CMU/ATX PLL to lock to the input reference clock frequency after coming out of reset.
- (15) To calculate the REFCLK rms phase jitter requirement for PCle at reference clock frequencies other than 100 MHz, use the following formula: REFCLK rms phase jitter at f(MHz) = REFCLK rms phase jitter at 100 MHz × 100/f.
- (16) The maximum peak to peak differential input voltage V_{ID} after device configuration is equal to 4 × (absolute V_{MAX} for receiver pin V_{ICM}).
- (17) For ES devices, RREF is 2000 $\Omega \pm 1\%$.
- (18) To calculate the REFCLK phase noise requirement at frequencies other than 622 MHz, use the following formula: REFCLK phase noise at f(MHz) = REFCLK phase noise at 622 MHz + 20*log(f/622).
- (19) SFP/+ optical modules require the host interface to have RD+/- differentially terminated with 100 Ω. The internal OCT feature is available after the Stratix V FPGA configuration is completed. Altera recommends that FPGA configuration is completed before inserting the optical module. Otherwise, minimize unnecessary removal and insertion with unconfigured devices.
- (20) Refer to Figure 4.
- (21) For oversampling design to support data rates less than the minimum specification, the CDR needs to be in LTR mode only.
- (22) This supply follows VCCR_GXB for both GX and GT channels.
- (23) When you use fPLL as a TXPLL of the transceiver.

Figure 6 shows the Stratix V DC gain curves for GT channels.

Figure 6. DC Gain Curves for GT Channels

Transceiver Characterization

This section summarizes the Stratix V transceiver characterization results for compliance with the following protocols:

- Interlaken
- 40G (XLAUI)/100G (CAUI)
- 10GBase-KR
- QSGMII
- XAUI
- SFI
- Gigabit Ethernet (Gbe / GIGE)
- SPAUI
- Serial Rapid IO (SRIO)
- CPRI
- OBSAI
- Hyper Transport (HT)
- SATA
- SAS
- CEI

Symbol	Parameter	Min	Тур	Max	Unit
+ (3) (4)	Input clock cycle-to-cycle jitter ($f_{REF} \ge 100 \text{ MHz}$)			0.15	UI (p-p)
LINCCJ (0), (1)	Input clock cycle-to-cycle jitter (f _{REF} < 100 MHz)	-750		+750	ps (p-p)
+ (5)	Period Jitter for dedicated clock output (f_{OUT} \geq 100 MHz)	_	_	175 ⁽¹⁾	ps (p-p)
CUTPJ_DC	Period Jitter for dedicated clock output (f _{OUT} < 100 MHz)	_	_	17.5 ⁽¹⁾	mUI (p-p)
+ (5)	Period Jitter for dedicated clock output in fractional PLL ($f_{OUT} \ge 100 \text{ MHz}$)	_	_	250 ⁽¹¹⁾ , 175 ⁽¹²⁾	ps (p-p)
^L FOUTPJ_DC	Period Jitter for dedicated clock output in fractional PLL (f _{OUT} < 100 MHz)	_	_	25 ⁽¹¹⁾ , 17.5 ⁽¹²⁾	mUI (p-p)
+ (5)	Cycle-to-Cycle Jitter for a dedicated clock output ($f_{\text{OUT}} \geq 100 \text{ MHz})$		_	175	ps (p-p)
COUTCCJ_DC	Cycle-to-Cycle Jitter for a dedicated clock output $(f_{OUT} < 100 \text{ MHz})$		_	17.5	mUI (p-p)
+ (5)	Cycle-to-cycle Jitter for a dedicated clock output in fractional PLL ($f_{OUT} \ge 100 \text{ MHz}$)		_	250 ⁽¹¹⁾ , 175 ⁽¹²⁾	ps (p-p)
FOUTCCJ_DC	Cycle-to-cycle Jitter for a dedicated clock output in fractional PLL ($f_{OUT} < 100 \text{ MHz}$)+		_	25 ⁽¹¹⁾ , 17.5 ⁽¹²⁾	mUI (p-p)
t _{outpj 10} (5),	Period Jitter for a clock output on a regular I/O in integer PLL ($f_{OUT} \ge 100 \text{ MHz}$)		_	600	ps (p-p)
(8)	Period Jitter for a clock output on a regular I/O $(f_{OUT} < 100 \text{ MHz})$		_	60	mUI (p-p)
t _{foutpj 10} ^{(5),}	Period Jitter for a clock output on a regular I/O in fractional PLL ($f_{OUT} \ge 100 \text{ MHz}$)	_	_	600 ⁽¹⁰⁾	ps (p-p)
(8), (11)	Period Jitter for a clock output on a regular I/O in fractional PLL (f _{OUT} < 100 MHz)	_	_	60 ⁽¹⁰⁾	mUI (p-p)
t _{outccj_io} (5),	Cycle-to-cycle Jitter for a clock output on a regular I/O in integer PLL ($f_{OUT} \geq 100 \mbox{ MHz})$	_	_	600	ps (p-p)
(8)	Cycle-to-cycle Jitter for a clock output on a regular I/O in integer PLL (f _{OUT} < 100 MHz)	_	_	60 ⁽¹⁰⁾	mUI (p-p)
t _{FOUTCCJ 10} (5),	Cycle-to-cycle Jitter for a clock output on a regular I/O in fractional PLL ($f_{OUT} \ge 100$ MHz)		_	600 ⁽¹⁰⁾	ps (p-p)
(8), (11)	Cycle-to-cycle Jitter for a clock output on a regular I/O in fractional PLL (f _{OUT} < 100 MHz)	_	_	60	mUI (p-p)
t _{CASC OUTPJ DC}	Period Jitter for a dedicated clock output in cascaded PLLs ($f_{OUT} \ge 100 \text{ MHz}$)	_	_	175	ps (p-p)
(5), (6)	Period Jitter for a dedicated clock output in cascaded PLLs (f_{OUT} < 100 MHz)	_	_	17.5	mUI (p-p)
f _{DRIFT}	Frequency drift after PFDENA is disabled for a duration of 100 μs		_	±10	%
dK _{BIT}	Bit number of Delta Sigma Modulator (DSM)	8	24	32	Bits
k _{VALUE}	Numerator of Fraction	128	8388608	2147483648	—

Table 31. PLL Specifications for Stratix V Devices (Part 2 of 3)

Symbol	Conditiono		C1		C2,	C2L, I	2, I2L	C3,	13, 131	., I 3 YY		C4,14	4	Unit
Symbol	Conditions	Min	Тур	Max	Min	Тур	Max	Min	Тур	Max	Min	Тур	Max	UIIIL
Transmitter														
	SERDES factor J = 3 to 10 ⁽⁹⁾ , ⁽¹¹⁾ , ⁽¹²⁾ , ⁽¹³⁾ , ⁽¹⁴⁾ , ⁽¹⁵⁾ , ⁽¹⁶⁾	(6)	_	1600	(6)	_	1434	(6)	_	1250	(6)	_	1050	Mbps
True Differential I/O Standards	SERDES factor J ≥ 4 LVDS TX with DPA (12), (14), (15), (16)	(6)		1600	(6)		1600	(6)		1600	(6)	_	1250	Mbps
- f _{HSDR} (data rate) Emulated Differential I/O Standards	SERDES factor J = 2, uses DDR Registers	(6)	_	(7)	(6)	_	(7)	(6)	_	(7)	(6)		(7)	Mbps
	SERDES factor J = 1, uses SDR Register	(6)	_	(7)	(6)	_	(7)	(6)	_	(7)	(6)	_	(7)	Mbps
Emulated Differential I/O Standards with Three External Output Resistor Networks - f _{HSDR} (data rate) ⁽¹⁰⁾	SERDES factor J = 4 to 10 $(^{17})$	(6)		1100	(6)		1100	(6)		840	(6)		840	Mbps
t _{x Jitter} - True Differential	Total Jitter for Data Rate 600 Mbps - 1.25 Gbps		_	160		_	160		_	160			160	ps
I/O Standards	Total Jitter for Data Rate < 600 Mbps	_	_	0.1			0.1			0.1		_	0.1	UI
t _{x Jitter} - Emulated Differential I/O Standards	Total Jitter for Data Rate 600 Mbps - 1.25 Gbps	_	_	300	_		300	_	_	300	_		325	ps
with Three External Output Resistor Network	Total Jitter for Data Rate < 600 Mbps	_	_	0.2	_	_	0.2	_	_	0.2	_	_	0.25	UI

Table 36. High-Speed I/O Specifications for Stratix V Devices (1), (2) (Part 2 of 4)

Figure 7 shows the dynamic phase alignment (DPA) lock time specifications with the DPA PLL calibration option enabled.

Figure 7. DPA Lock Time Specification with DPA PLL Calibration Enabled

rx_reset			
rx_dpa_locked			<u> </u>
			-

Table 37 lists the DPA lock time specifications for Stratix V devices.

Table 37. DPA Lock Time Specifications for Stratix V GX Devices Only (1), (2), (3)

Standard	Training Pattern	Number of Data Transitions in One Repetition of the Training Pattern	Number of Repetitions per 256 Data Transitions ⁽⁴⁾	Maximum
SPI-4	00000000001111111111	2	128	640 data transitions
Parallel Rapid I/O	00001111	2	128	640 data transitions
	10010000	4	64	640 data transitions
Miscellaneous	10101010	8	32	640 data transitions
Wiscenareous	01010101	8	32	640 data transitions

Notes to Table 37:

(1) The DPA lock time is for one channel.

(2) One data transition is defined as a 0-to-1 or 1-to-0 transition.

(3) The DPA lock time stated in this table applies to both commercial and industrial grade.

(4) This is the number of repetitions for the stated training pattern to achieve the 256 data transitions.

Figure 8 shows the **LVDS** soft-clock data recovery (CDR)/DPA sinusoidal jitter tolerance specification for a data rate \geq 1.25 Gbps. Table 38 lists the **LVDS** soft-CDR/DPA sinusoidal jitter tolerance specification for a data rate \geq 1.25 Gbps.





Jitter Free	quency (Hz)	Sinusoidal Jitter (UI)
F1	10,000	25.000
F2	17,565	25.000
F3	1,493,000	0.350
F4	50,000,000	0.350

iadie 38. lvus sott-luk/upa sinusoidai jitter mask vaiues tor a uata kate > 1.2	25 G	.2	1.	1	>	>		Ì	e	F	Ł	đ	a	2	1	R	P							Ľ	I.		I.	Ì	1	3	a	3	a	2	2	2	ŀ	t	t	t	ſ	ľ	3	2	2	2	2	2	1)	D		I		Ľ	1	2	2	ź	â	i		۴	۴	r	r		I	I	Ì	1	Π	٥	٢	i	F	f	f	1	1		5	S	S	S	2	2	e	E	I	U	h	I	۱	a	ŀ	I	V	۱			ľ	٢	k	k	s	S	S	1	a	2	2		И	V	N			•	۴	r	r	1	1	1	2	2	2	2	e	e	e	E	t	t	i	ŀ	t	ľ	i	i	f	f	ŀ	ŀ	li
---	------	----	----	---	---	---	--	---	---	---	---	---	---	---	---	---	---	--	--	--	--	--	--	---	----	--	----	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---	--	---	--	---	---	---	---	---	---	---	--	---	---	---	---	--	---	---	---	---	---	---	---	---	---	---	---	---	---	--	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---	--	--	---	---	---	---	---	---	---	---	---	---	---	--	---	---	---	--	--	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---	----

Figure 9 shows the **LVDS** soft-CDR/DPA sinusoidal jitter tolerance specification for a data rate < 1.25 Gbps.





DLL Range, DQS Logic Block, and Memory Output Clock Jitter Specifications

Table 39 lists the DLL range specification for Stratix V devices. The DLL is always in 8-tap mode in Stratix V devices.

Table 39. DLL Range Specifications for Stratix V Devices (1)

C1	C2, C2L, I2, I2L	C3, I3, I3L, I3YY	C4,I4	Unit
300-933	300-933	300-890	300-890	MHz

Note to Table 39:

(1) Stratix V devices support memory interface frequencies lower than 300 MHz, although the reference clock that feeds the DLL must be at least 300 MHz. To support interfaces below 300 MHz, multiply the reference clock feeding the DLL to ensure the frequency is within the supported range of the DLL.

Table 40 lists the DQS phase offset delay per stage for Stratix V devices.

Table 40. DQS Phase Offset Delay Per Setting for Stratix V Devices ^{(1), (2)} (Part 1 of 2)

Speed Grade	Min	Max	Unit
C1	8	14	ps
C2, C2L, I2, I2L	8	14	ps
C3,I3, I3L, I3YY	8	15	ps

Speed Grade	Min	Max	Unit
C4,I4	8	16	ps

Table 40. DQS Phase Offset Delay Per Setting for Stratix V Devices ^{(1), (2)} (Part 2 of 2)

Notes to Table 40:

(1) The typical value equals the average of the minimum and maximum values.

(2) The delay settings are linear with a cumulative delay variation of 40 ps for all speed grades. For example, when using a -2 speed grade and applying a 10-phase offset setting to a 90° phase shift at 400 MHz, the expected average cumulative delay is [625 ps + (10 × 10 ps) ± 20 ps] = 725 ps ± 20 ps.

Table 41 lists the DQS phase shift error for Stratix V devices.

Table 41. DQS Phase Shift Error Specification for DLL-Delayed Clock (t_{DQS_PSERR}) for Stratix V Devices ⁽¹⁾

Number of DQS Delay Buffers	C1	C2, C2L, I2, I2L	C3, I3, I3L, I3YY	C4,14	Unit
1	28	28	30	32	ps
2	56	56	60	64	ps
3	84	84	90	96	ps
4	112	112	120	128	ps

Notes to Table 41:

(1) This error specification is the absolute maximum and minimum error. For example, skew on three DQS delay buffers in a -2 speed grade is ± 78 ps or ± 39 ps.

Table 42 lists the memory output clock jitter specifications for Stratix V devices.

Table 42. Memory Output Clock Jitter Specification for Stratix V Devices (1	^{),} (Part 1 of 2) ^{(2), (3)}
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Clock	Parameter	Symbol	C	1	C2, C2L	, 12, 12L	C3, I3 I3	8, 13L, YY	C4	,14	Unit
NELWURK		-	Min	Max	Min	Max	Min	Max	Min	Max	
	Clock period jitter	$t_{JIT(per)}$	-50	50	-50	50	-55	55	-55	55	ps
Regional	Cycle-to-cycle period jitter	$t_{\text{JIT(cc)}}$	-100	100	-100	100	-110	110	-110	110	ps
	Duty cycle jitter	$t_{JIT(duty)}$	-50	50	-50	50	-82.5	82.5	-82.5	82.5	ps
	Clock period jitter	$t_{JIT(per)}$	-75	75	-75	75	-82.5	82.5	-82.5	82.5	ps
Global	Cycle-to-cycle period jitter	$t_{\text{JIT(cc)}}$	-150	150	-150	150	-165	165	-165	165	ps
	Duty cycle jitter	$t_{JIT(duty)}$	-75	75	-75	75	-90	90	-90	90	ps

Family	Device	Package	Configuration .rbf Size (bits)	IOCSR .rbf Size (bits) ^{(4), (5)}
Stratix $V \in (1)$	5SEE9	—	342,742,976	700,888
	5SEEB	—	342,742,976	700,888

Table 47. Uncompressed .rbf Sizes for Stratix V Devices

Notes to Table 47:

(1) Stratix V E devices do not have PCI Express® (PCIe®) hard IP. Stratix V E devices do not support the CvP configuration scheme.

(2) 36-transceiver devices.

(3) 24-transceiver devices.

(4) File size for the periphery image.

(5) The IOCSR .rbf size is specifically for the CvP feature.

Use the data in Table 47 to estimate the file size before design compilation. Different configuration file formats, such as a hexadecimal (.hex) or tabular text file (.ttf) format, have different file sizes. For the different types of configuration file and file sizes, refer to the Quartus II software. However, for a specific version of the Quartus II software, any design targeted for the same device has the same uncompressed configuration file size. If you are using compression, the file size can vary after each compilation because the compression ratio depends on your design.

• For more information about setting device configuration options, refer to *Configuration, Design Security, and Remote System Upgrades in Stratix V Devices.* For creating configuration files, refer to the *Quartus II Help.*

Table 48 lists the minimum configuration time estimates for Stratix V devices.

Table 48. Minimum Configuration Time Estimation for Stratix V Devi
--

	Member Code	Active Serial ⁽¹⁾			Fast Passive Parallel ⁽²⁾			
Variant		Width	DCLK (MHz)	Min Config Time (s)	Width	DCLK (MHz)	Min Config Time (s)	
	٨٥	4	100	0.534	32	100	0.067	
	AJ	4	100	0.344	32	100	0.043	
	A4	4	100	0.534	32	100	0.067	
	A5	4	100	0.675	32	100	0.084	
	A7	4	100	0.675	32	100	0.084	
GX	A9	4	100	0.857	32	100	0.107	
	AB	4	100	0.857	32	100	0.107	
	B5	4	100	0.676	32	100	0.085	
	B6	4	100	0.676	32	100	0.085	
	B9	4	100	0.857	32	100	0.107	
	BB	4	100	0.857	32	100	0.107	
ст	C5	4	100	0.675	32	100	0.084	
GT	C7	4	100	0.675	32	100	0.084	

Active Serial Configuration Timing

Table 52 lists the DCLK frequency specification in the AS configuration scheme.

Fable 52.	DCLK Frequency	Specification in th	e AS Configuration	Scheme ^{(1),}	(2)
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Minimum	Typical	Maximum	Unit
5.3	7.9	12.5	MHz
10.6	15.7	25.0	MHz
21.3	31.4	50.0	MHz
42.6	62.9	100.0	MHz

Notes to Table 52:

(1) This applies to the DCLK frequency specification when using the internal oscillator as the configuration clock source.

(2) The AS multi-device configuration scheme does not support DCLK frequency of 100 MHz.

Figure 14 shows the single-device configuration setup for an AS ×1 mode.





Notes to Figure 14:

- (1) If you are using AS $\times 4$ mode, this signal represents the AS_DATA[3..0] and EPCQ sends in 4-bits of data for each DCLK cycle.
- (2) The initialization clock can be from internal oscillator or CLKUSR pin.
- (3) After the option bit to enable the INIT_DONE pin is configured into the device, the INIT_DONE goes low.

Table 53 lists the timing parameters for AS $\times 1$ and AS $\times 4$ configurations in Stratix V devices.

Table JS. As fining falancees for as $\times 1$ and as $\times 4$ configurations in straits V devices $(2, 2, 2, 3, 3, 3, 3, 3, 3, 3, 3, 3, 3, 3, 3, 3,$	Table 53.	AS Timing	Parameters for AS	\times 1 and AS \times 4 Confi	gurations in Stratix V	/ Devices ^{(1), (2)}	(Part 1 of 2)
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Symbol	Parameter	Minimum	Maximum	Units
t _{CO}	DCLK falling edge to AS_DATA0/ASDO output	—	2	ns
t _{SU}	Data setup time before falling edge on DCLK	1.5	_	ns
t _H	Data hold time after falling edge on DCLK	0	_	ns

Symbol	Parameter	Minimum	Maximum	Units
t _{CD2UM}	CONF_DONE high to user mode (3)	175	437	μS
t _{CD2CU}	CONF_DONE high to CLKUSR enabled	4 × maximum DCLK period	_	—
t _{CD2UMC}	CONF_DONE high to user mode with CLKUSR option on	t _{cd2cu} + (8576 × clkusr period)	_	—

Table 53. AS Timing Parameters for AS \times 1 and AS \times 4 Configurations in Stratix V Devices ^{(1), (2)} (Part 2 of 2)

Notes to Table 53:

(1) The minimum and maximum numbers apply only if you choose the internal oscillator as the clock source for initializing the device.

(2) t_{CF2CD}, t_{CF2ST0}, t_{CF2ST0}, t_{CF6}, t_{STATUS}, and t_{CF2ST1} timing parameters are identical to the timing parameters for PS mode listed in Table 54 on page 63.

(3) To enable the CLKUSR pin as the initialization clock source and to obtain the maximum frequency specification on this pin, refer to the Initialization section of the "Configuration, Design Security, and Remote System Upgrades in Stratix V Devices" chapter.

Passive Serial Configuration Timing

Figure 15 shows the timing waveform for a passive serial (PS) configuration when using a MAX II device, MAX V device, or microprocessor as an external host.

Figure 15. PS Configuration Timing Waveform ⁽¹⁾



Notes to Figure 15:

- (1) The beginning of this waveform shows the device in user mode. In user mode, nCONFIG, nSTATUS, and CONF_DONE are at logic high levels. When nCONFIG is pulled low, a reconfiguration cycle begins.
- (2) After power-up, the Stratix V device holds nSTATUS low for the time of the POR delay.
- (3) After power-up, before and during configuration, CONF DONE is low.
- (4) Do not leave DCLK floating after configuration. You can drive it high or low, whichever is more convenient.
- (5) DATAO is available as a user I/O pin after configuration. The state of this pin depends on the dual-purpose pin settings in the **Device and Pins Option**.
- (6) To ensure a successful configuration, send the entire configuration data to the Stratix V device. CONF_DONE is released high after the Stratix V device receives all the configuration data successfully. After CONF_DONE goes high, send two additional falling edges on DCLK to begin initialization and enter user mode.
- (7) After the option bit to enable the INIT DONE pin is configured into the device, the INIT DONE goes low.

Paramotor	Availabla	Min	Fast	Model				Slow N	lodel			
(1)	Settings	Offset (2)	Industrial	Commercial	C1	C2	C3	C4	12	13, 13YY	14	Unit
D3	8	0	1.587	1.699	2.793	2.793	2.992	3.192	2.811	3.047	3.257	ns
D4	64	0	0.464	0.492	0.838	0.838	0.924	1.011	0.843	0.920	1.006	ns
D5	64	0	0.464	0.493	0.838	0.838	0.924	1.011	0.844	0.921	1.006	ns
D6	32	0	0.229	0.244	0.415	0.415	0.458	0.503	0.418	0.456	0.499	ns

Table 58.	IOE Pro	grammable De	lay for	Stratix V	V Devices	(Part 2 of 2)
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Notes to Table 58:

(1) You can set this value in the Quartus II software by selecting D1, D2, D3, D5, and D6 in the Assignment Name column of Assignment Editor.

(2) Minimum offset does not include the intrinsic delay.

Programmable Output Buffer Delay

Table 59 lists the delay chain settings that control the rising and falling edge delays of the output buffer. The default delay is 0 ps.

Symbol	Parameter	Typical	Unit
		0 (default)	ps
Dauman	Rising and/or falling edge	25	ps
DOUTBUF	delay	50	ps
		75	ps

Note to Table 59:

(1) You can set the programmable output buffer delay in the Quartus II software by setting the Output Buffer Delay Control assignment to either positive, negative, or both edges, with the specific values stated here (in ps) for the Output Buffer Delay assignment.

Glossary

Table 60 lists the glossary for this chapter.

Table 60. Glossary (Part 1 of 4)

Letter	Subject Definitions		
Α			
В	—	—	
С			
D	—	_	
E	—	_	
	f _{HSCLK}	Left and right PLL input clock frequency.	
F	f _{HSDR}	High-speed I/O block—Maximum and minimum LVDS data transfer rate (f _{HSDR} = 1/TUI), non-DPA.	
	f _{hsdrdpa}	High-speed I/O block—Maximum and minimum LVDS data transfer rate (f _{HSDRDPA} = 1/TUI), DPA.	

Letter	Subject	Definitions
	V _{CM(DC)}	DC common mode input voltage.
	V _{ICM}	Input common mode voltage—The common mode of the differential signal at the receiver.
	V _{ID}	Input differential voltage swing—The difference in voltage between the positive and complementary conductors of a differential transmission at the receiver.
	V _{DIF(AC)}	AC differential input voltage—Minimum AC input differential voltage required for switching.
	V _{DIF(DC)}	DC differential input voltage— Minimum DC input differential voltage required for switching.
	V _{IH}	Voltage input high—The minimum positive voltage applied to the input which is accepted by the device as a logic high.
	V _{IH(AC)}	High-level AC input voltage
	V _{IH(DC)}	High-level DC input voltage
V	V _{IL}	Voltage input low—The maximum positive voltage applied to the input which is accepted by the device as a logic low.
	V _{IL(AC)}	Low-level AC input voltage
	V _{IL(DC)}	Low-level DC input voltage
	V _{OCM}	Output common mode voltage—The common mode of the differential signal at the transmitter.
	V _{OD}	Output differential voltage swing—The difference in voltage between the positive and complementary conductors of a differential transmission at the transmitter.
	V _{SWING}	Differential input voltage
	V _X	Input differential cross point voltage
	V _{OX}	Output differential cross point voltage
W	W	High-speed I/O block—clock boost factor
X		
Y	—	—
Z		

Table 60. Glossary (Part 4 of 4)