# E·XFL

### Intel - 5SGXEA7N3F40I3LN Datasheet



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#### Understanding <u>Embedded - FPGAs (Field</u> <u>Programmable Gate Array)</u>

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

### **Applications of Embedded - FPGAs**

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

#### Details

Product Status	Obsolete
Number of LABs/CLBs	234720
Number of Logic Elements/Cells	622000
Total RAM Bits	51200000
Number of I/O	600
Number of Gates	
Voltage - Supply	0.82V ~ 0.88V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	1517-BBGA, FCBGA
Supplier Device Package	1517-FBGA (40x40)
Purchase URL	https://www.e-xfl.com/product-detail/intel/5sgxea7n3f40i3ln

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

								·
Transceiver Speed				Core Spe	ed Grade			
Grade	C1	C2, C2L	C3	C4	12, 12L	13, 13L	<b>I</b> 3YY	14
3 GX channel—8.5 Gbps	_	Yes	Yes	Yes	_	Yes	Yes <sup>(4)</sup>	Yes

### Table 1. Stratix V GX and GS Commercial and Industrial Speed Grade Offering <sup>(1), (2), (3)</sup> (Part 2 of 2)

Notes to Table 1:

(1) C = Commercial temperature grade; I = Industrial temperature grade.

(2) Lower number refers to faster speed grade.

(3) C2L, I2L, and I3L speed grades are for low-power devices.

(4) I3YY speed grades can achieve up to 10.3125 Gbps.

Table 2 lists the industrial and commercial speed grades for the Stratix V GT devices. **Table 2. Stratix V GT Commercial and Industrial Speed Grade Offering** <sup>(1)</sup>, <sup>(2)</sup>

Transseiver Speed Grade		Core Spe	ed Grade	
Transceiver Speeu draue	C1	C2	12	13
2 GX channel—12.5 Gbps GT channel—28.05 Gbps	Yes	Yes	_	_
3 GX channel—12.5 Gbps GT channel—25.78 Gbps	Yes	Yes	Yes	Yes

#### Notes to Table 2:

(1) C = Commercial temperature grade; I = Industrial temperature grade.

(2) Lower number refers to faster speed grade.

### **Absolute Maximum Ratings**

Absolute maximum ratings define the maximum operating conditions for Stratix V devices. The values are based on experiments conducted with the devices and theoretical modeling of breakdown and damage mechanisms. The functional operation of the device is not implied for these conditions.



Conditions other than those listed in Table 3 may cause permanent damage to the device. Additionally, device operation at the absolute maximum ratings for extended periods of time may have adverse effects on the device.

TANIC J. ANSULULC MAXIMUM NALINYS IVI SUALIX V DEVICES (FAIL I UI Z)	Table 3.	<b>Absolute Maximum</b>	Ratings	for Stratix \	/ Devices	(Part 1 of 2)
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Symbol	Description	Minimum	Maximum	Unit
V <sub>CC</sub>	Power supply for core voltage and periphery circuitry	-0.5	1.35	V
V <sub>CCPT</sub>	Power supply for programmable power technology	-0.5	1.8	V
V <sub>CCPGM</sub>	Power supply for configuration pins	-0.5	3.9	V
V <sub>CC_AUX</sub>	Auxiliary supply for the programmable power technology	-0.5	3.4	V
V <sub>CCBAT</sub>	Battery back-up power supply for design security volatile key register	-0.5	3.9	V
V <sub>CCPD</sub>	I/O pre-driver power supply	-0.5	3.9	V
V <sub>CCIO</sub>	I/O power supply	-0.5	3.9	V

Symbol	Description	Minimum	Maximum	Unit
V <sub>CCD_FPLL</sub>	PLL digital power supply	-0.5	1.8	V
V <sub>CCA_FPLL</sub>	PLL analog power supply	-0.5	3.4	V
VI	DC input voltage	-0.5	3.8	V
TJ	Operating junction temperature	-55	125	°C
T <sub>STG</sub>	Storage temperature (No bias)	-65	150	°C
I <sub>OUT</sub>	DC output current per pin	-25	40	mA

Table 3. Absolute Maximum Ratings for Stratix V Devices (Part 2 of 2)

Table 4 lists the absolute conditions for the transceiver power supply for Stratix V GX, GS, and GT devices.

Table 4. Transceiver Power Supply Absolute Conditions for Stratix V GX, GS, and GT Devices

Symbol	Description	Devices	Minimum	Maximum	Unit
V <sub>CCA_GXBL</sub>	Transceiver channel PLL power supply (left side)	GX, GS, GT	-0.5	3.75	V
V <sub>CCA_GXBR</sub>	Transceiver channel PLL power supply (right side)	GX, GS	-0.5	3.75	V
V <sub>CCA_GTBR</sub>	Transceiver channel PLL power supply (right side)	GT	-0.5	3.75	V
V <sub>CCHIP_L</sub>	Transceiver hard IP power supply (left side)	GX, GS, GT	-0.5	1.35	V
V <sub>CCHIP_R</sub>	Transceiver hard IP power supply (right side)	GX, GS, GT	-0.5	1.35	V
V <sub>CCHSSI_L</sub>	Transceiver PCS power supply (left side)	GX, GS, GT	-0.5	1.35	V
V <sub>CCHSSI_R</sub>	Transceiver PCS power supply (right side)	GX, GS, GT	-0.5	1.35	V
V <sub>CCR_GXBL</sub>	Receiver analog power supply (left side)	GX, GS, GT	-0.5	1.35	V
V <sub>CCR_GXBR</sub>	Receiver analog power supply (right side)	GX, GS, GT	-0.5	1.35	V
V <sub>CCR_GTBR</sub>	Receiver analog power supply for GT channels (right side)	GT	-0.5	1.35	V
V <sub>CCT_GXBL</sub>	Transmitter analog power supply (left side)	GX, GS, GT	-0.5	1.35	V
V <sub>CCT_GXBR</sub>	Transmitter analog power supply (right side)	GX, GS, GT	-0.5	1.35	V
V <sub>CCT_GTBR</sub>	Transmitter analog power supply for GT channels (right side)	GT	-0.5	1.35	V
V <sub>CCL_GTBR</sub>	Transmitter clock network power supply (right side)	GT	-0.5	1.35	V
V <sub>CCH_GXBL</sub>	Transmitter output buffer power supply (left side)	GX, GS, GT	-0.5	1.8	V
V <sub>CCH_GXBR</sub>	Transmitter output buffer power supply (right side)	GX, GS, GT	-0.5	1.8	V

### **Maximum Allowed Overshoot and Undershoot Voltage**

During transitions, input signals may overshoot to the voltage shown in Table 5 and undershoot to -2.0 V for input currents less than 100 mA and periods shorter than 20 ns.

I/O		V <sub>ccio</sub> (V)		V <sub>DIF(</sub>	<sub>DC)</sub> (V)	V <sub>X(AC)</sub> (V)			V <sub>CM(DC)</sub> (V	)	V <sub>DIF(AC)</sub> (V)		
Standard	Min	Тур	Max	Min	Max	Min	Тур	Max	Min	Тур	Max	Min	Max
HSTL-12 Class I, II	1.14	1.2	1.26	0.16	V <sub>CCI0</sub> + 0.3	_	0.5* V <sub>CCI0</sub>	_	0.4* V <sub>CCIO</sub>	0.5* V <sub>CCIO</sub>	0.6* V <sub>CCI0</sub>	0.3	V <sub>CCI0</sub> + 0.48
HSUL-12	1.14	1.2	1.3	0.26	0.26	0.5*V <sub>CCI0</sub> - 0.12	0.5* V <sub>CCI0</sub>	0.5*V <sub>CCI0</sub> + 0.12	0.4* V <sub>CCIO</sub>	0.5* V <sub>CCIO</sub>	0.6* V <sub>CCIO</sub>	0.44	0.44

### Table 21. Differential HSTL and HSUL I/O Standards for Stratix V Devices (Part 2 of 2)

### Table 22. Differential I/O Standard Specifications for Stratix V Devices (7)

I/O	Vc	<sub>cio</sub> (V)	(10)		V <sub>ID</sub> (mV) <sup>(8)</sup>			V <sub>ICM(DC)</sub> (V)		Vo	<sub>D</sub> (V) (	6)	v	<sub>осм</sub> (V)	(6)
Standard	Min	Тур	Max	Min	Condition	Max	Min	Condition	Max	Min	Тур	Max	Min	Тур	Max
PCML	Trar	nsmitte	er, receiv transmi	ver, and itter, rec	input referer ceiver, and re	nce cloo eference	ck pins e clock	of the high-s I/O pin speci	peed tra fications	nsceiver , refer to	rs use o Table	the PC e 23 on	ML I/O s page 18	standard 3.	. For
2.5 V	2 375	25	2 625	100	V <sub>CM</sub> =	_	0.05	D <sub>MAX</sub> ≤ 700 Mbps	1.8	0.247	_	0.6	1.125	1.25	1.375
LVDS <sup>(1)</sup>	2.575	2.0	2.025	100	1.25 V	_	1.05	D <sub>MAX</sub> > 700 Mbps	1.55	0.247	_	0.6	1.125	1.25	1.375
BLVDS (5)	2.375	2.5	2.625	100	_	_	_	_	_	_	_	—	_	—	
RSDS (HIO) <sup>(2)</sup>	2.375	2.5	2.625	100	V <sub>CM</sub> = 1.25 V	_	0.3	_	1.4	0.1	0.2	0.6	0.5	1.2	1.4
Mini- LVDS (HIO) <sup>(3)</sup>	2.375	2.5	2.625	200	_	600	0.4	_	1.325	0.25	_	0.6	1	1.2	1.4
LVPECL (4	_	_	_	300	_		0.6	D <sub>MAX</sub> ≤ 700 Mbps	1.8		_	_	_	_	_
), (9)				300			1	D <sub>MAX</sub> > 700 Mbps	1.6						

Notes to Table 22:

(1) For optimized LVDS receiver performance, the receiver voltage input range must be between 1.0 V to 1.6 V for data rates above 700 Mbps, and 0 V to 1.85 V for data rates below 700 Mbps.

(2) For optimized RSDS receiver performance, the receiver voltage input range must be between 0.25 V to 1.45 V.

(3) For optimized Mini-LVDS receiver performance, the receiver voltage input range must be between 0.3 V to 1.425 V.

- (4) For optimized LVPECL receiver performance, the receiver voltage input range must be between 0.85 V to 1.75 V for data rate above 700 Mbps and 0.45 V to 1.95 V for data rate below 700 Mbps.
- (5) There are no fixed  $V_{ICM}$ ,  $V_{OD}$ , and  $V_{OCM}$  specifications for BLVDS. They depend on the system topology.
- (6) RL range:  $90 \le RL \le 110 \Omega$ .
- (7) The 1.4-V and 1.5-V PCML transceiver I/O standard specifications are described in "Transceiver Performance Specifications" on page 18.
- (8) The minimum VID value is applicable over the entire common mode range, VCM.
- (9) LVPECL is only supported on dedicated clock input pins.
- (10) Differential inputs are powered by VCCPD which requires 2.5 V.

### **Power Consumption**

Altera offers two ways to estimate power consumption for a design—the Excel-based Early Power Estimator and the Quartus<sup>®</sup> II PowerPlay Power Analyzer feature.

## **Switching Characteristics**

This section provides performance characteristics of the Stratix V core and periphery blocks.

These characteristics can be designated as Preliminary or Final.

- Preliminary characteristics are created using simulation results, process data, and other known parameters. The title of these tables show the designation as "Preliminary."
- Final numbers are based on actual silicon characterization and testing. The numbers reflect the actual performance of the device under worst-case silicon process, voltage, and junction temperature conditions. There are no designations on finalized tables.

### **Transceiver Performance Specifications**

This section describes transceiver performance specifications.

Table 23 lists the Stratix V GX and GS transceiver specifications.

Table 23.	Transceiver 3	Specifications	for Stratix	V GX	and GS	Devices	(1)	(Part 1	nf 7	۱
Table 20.	TIANSUCIACI	opeonitionationa	IUI UIIAIIA	I UA	anu uu	DEVICES	• •	(1 61 6 1		

Symbol/	Conditions	Tra	nsceive Grade	r Speed 1	Transceiver Speed Grade 2			Trai	er Speed e 3	Unit	
Description		Min	Тур	Max	Min	Тур	Max	Min	Тур	Max	
Reference Clock											
Supported I/O	Dedicated reference clock pin	1.2-V	PCML,	1.4-V PCM	IL, 1.5-∖	/ PCML	, 2.5-V PCN HCSL	1L, Diffe	rential	LVPECL, L\	/DS, and
Standards	RX reference clock pin			1.4-V PCMI	L, 1.5-V	PCML,	2.5-V PCM	l, lvpe	CL, and	d LVDS	
Input Reference Clock Frequency (CMU PLL) <sup>(8)</sup>	_	40	_	710	40	_	710	40	_	710	MHz
Input Reference Clock Frequency (ATX PLL) <sup>(8)</sup>		100		710	100		710	100	_	710	MHz
Rise time	Measure at ±60 mV of differential signal <sup>(26)</sup>			400	_		400			400	ns
Fall time	Measure at ±60 mV of differential signal <sup>(26)</sup>		_	400	_		400			400	μs
Duty cycle		45		55	45		55	45	—	55	%
Spread-spectrum modulating clock frequency	PCI Express® (PCIe <sup>®</sup> )	30		33	30		33	30	_	33	kHz

### Table 28. Transceiver Specifications for Stratix V GT Devices (Part 2 of 5)<sup>(1)</sup>

Symbol/	Conditions	S	Transceive peed Grade	r 2	SI	Fransceive Deed Grade	r 3	Unit
Description		Min	Тур	Max	Min	Тур	Max	
	100 Hz	—	—	-70			-70	
Transmitter REFCLK	1 kHz		_	-90	_	_	-90	
Phase Noise (622	10 kHz		—	-100	_		-100	dBc/Hz
MHz) <sup>(18)</sup>	100 kHz			-110			-110	
	$\geq$ 1 MHz	—	—	-120		_	-120	
Transmitter REFCLK Phase Jitter (100 MHz) <sup>(15)</sup>	10 kHz to 1.5 MHz (PCle)	_	_	3		_	3	ps (rms)
RREF <sup>(17)</sup>	_	_	1800 ± 1%	—	_	1800 ± 1%	_	Ω
Transceiver Clocks								
fixedclk clock frequency	PCIe Receiver Detect	_	100 or 125	_	_	100 or 125	_	MHz
Reconfiguration clock (mgmt_clk_clk) frequency	_	100	_	125	100	_	125	MHz
Receiver	•							
Supported I/O Standards	_		1.4-V PCML	., 1.5-V PCMI	L, 2.5-V PCI	VIL, LVPEC	L, and LVDS	6
Data rate (Standard PCS) <sup>(21)</sup>	GX channels	600	_	8500	600	_	8500	Mbps
Data rate (10G PCS) <sup>(21)</sup>	GX channels	600	_	12,500	600	_	12,500	Mbps
Data rate	GT channels	19,600	—	28,050	19,600		25,780	Mbps
Absolute V <sub>MAX</sub> for a receiver pin <sup>(3)</sup>	GT channels	_	_	1.2	_	_	1.2	V
Absolute V <sub>MIN</sub> for a receiver pin	GT channels	-0.4	_	—	-0.4	_	_	V
Maximum peak-to-peak	GT channels	_		1.6	—	_	1.6	V
differential input voltage V <sub>ID</sub> (diff p-p) before device configuration <sup>(20)</sup>	GX channels				(8)			
	GT channels							
Maximum peak-to-peak differential input voltage $V_{ID}$ (diff p-p) after device	V <sub>CCR_GTB</sub> = 1.05 V (V <sub>ICM</sub> = 0.65 V)	_	_	2.2	_	_	2.2	V
	GX channels		1	1 1	(8)			1
Minimum differential	GT channels	200	_	—	200		_	mV
eye opening at receiver serial input pins <sup>(4)</sup> , <sup>(20)</sup>	GX channels			·	(8)			

Table 29 shows the  $V_{\text{OD}}$  settings for the GT channel.

Symbol	V <sub>OD</sub> Setting	V <sub>od</sub> Value (mV)
	0	0
	1	200
V., differential neak to neak typical $(1)$	2	400
The second s	3	600
	4	800
	5	1000

### Note:

(1) Refer to Figure 4.

Figure 6 shows the Stratix V DC gain curves for GT channels.

Figure 6. DC Gain Curves for GT Channels

### **Transceiver Characterization**

This section summarizes the Stratix V transceiver characterization results for compliance with the following protocols:

- Interlaken
- 40G (XLAUI)/100G (CAUI)
- 10GBase-KR
- QSGMII
- XAUI
- SFI
- Gigabit Ethernet (Gbe / GIGE)
- SPAUI
- Serial Rapid IO (SRIO)
- CPRI
- OBSAI
- Hyper Transport (HT)
- SATA
- SAS
- CEI

### Table 31. PLL Specifications for Stratix V Devices (Part 3 of 3)

Symbol	Parameter		Тур	Max	Unit
f <sub>RES</sub>	Resolution of VCO frequency ( $f_{INPFD} = 100 \text{ MHz}$ )	390625	5.96	0.023	Hz

#### Notes to Table 31:

(1) This specification is limited in the Quartus II software by the I/O maximum frequency. The maximum I/O frequency is different for each I/O standard.

(2) This specification is limited by the lower of the two: I/O  $f_{MAX}$  or  $f_{OUT}$  of the PLL.

- (3) A high input jitter directly affects the PLL output jitter. To have low PLL output clock jitter, you must provide a clean clock source < 120 ps.
- (4)  $f_{REF}$  is fIN/N when N = 1.
- (5) Peak-to-peak jitter with a probability level of 10<sup>-12</sup> (14 sigma, 99.9999999974404% confidence level). The output jitter specification applies to the intrinsic jitter of the PLL, when an input jitter of 30 ps is applied. The external memory interface clock output jitter specifications use a different measurement method and are available in Table 44 on page 52.
- (6) The cascaded PLL specification is only applicable with the following condition: a. Upstream PLL: 0.59Mhz ≤ Upstream PLL BW < 1 MHz b. Downstream PLL: Downstream PLL BW > 2 MHz
- (7) High bandwidth PLL settings are not supported in external feedback mode.
- (8) The external memory interface clock output jitter specifications use a different measurement method, which is available in Table 42 on page 50.
- (9) The VCO frequency reported by the Quartus II software in the PLL Usage Summary section of the compilation report takes into consideration the VCO post-scale counter K value. Therefore, if the counter K has a value of 2, the frequency reported can be lower than the f<sub>VCO</sub> specification.
- (10) This specification only covers fractional PLL for low bandwidth. The  $f_{VCO}$  for fractional value range 0.05 0.95 must be  $\geq$  1000 MHz, while  $f_{VCO}$  for fractional value range 0.20 0.80 must be  $\geq$  1200 MHz.
- (11) This specification only covered fractional PLL for low bandwidth. The  $f_{VC0}$  for fractional value range 0.05-0.95 must be  $\geq$  1000 MHz.
- (12) This specification only covered fractional PLL for low bandwidth. The  $f_{VC0}$  for fractional value range 0.20-0.80 must be  $\geq$  1200 MHz.

### **DSP Block Specifications**

Table 32 lists the Stratix V DSP block performance specifications.

Peformance									
Mode	C1	C2, C2L	12, 12L	C3	13, 13L, 13YY	C4	14	Unit	
Modes using one DSP									
Three 9 x 9	600	600	600	480	480	420	420	MHz	
One 18 x 18	600	600	600	480	480	420	400	MHz	
Two partial 18 x 18 (or 16 x 16)	600	600	600	480	480	420	400	MHz	
One 27 x 27	500	500	500	400	400	350	350	MHz	
One 36 x 18	500	500	500	400	400	350	350	MHz	
One sum of two 18 x 18(One sum of 2 16 x 16)	500	500	500	400	400	350	350	MHz	
One sum of square	500	500	500	400	400	350	350	MHz	
One 18 x 18 plus 36 (a x b) + c	500	500	500	400	400	350	350	MHz	
		Modes u	sing two l	DSPs				·	
Three 18 x 18	500	500	500	400	400	350	350	MHz	
One sum of four 18 x 18	475	475	475	380	380	300	300	MHz	
One sum of two 27 x 27	465	465	450	380	380	300	290	MHz	
One sum of two 36 x 18	475	475	475	380	380	300	300	MHz	
One complex 18 x 18	500	500	500	400	400	350	350	MHz	
One 36 x 36	475	475	475	380	380	300	300	MHz	

### Table 32. Block Performance Specifications for Stratix V DSP Devices (Part 1 of 2)

### **Periphery Performance**

This section describes periphery performance, including high-speed I/O and external memory interface.

I/O performance supports several system interfaces, such as the **LVDS** high-speed I/O interface, external memory interface, and the **PCI/PCI-X** bus interface. General-purpose I/O standards such as 3.3-, 2.5-, 1.8-, and 1.5-**LVTTL/LVCMOS** are capable of a typical 167 MHz and 1.2-**LVCMOS** at 100 MHz interfacing frequency with a 10 pF load.

The actual achievable frequency depends on design- and system-specific factors. Ensure proper timing closure in your design and perform HSPICE/IBIS simulations based on your specific design and system setup to determine the maximum achievable frequency in your system.

### **High-Speed I/O Specification**

Table 36 lists high-speed I/O timing for Stratix V devices.

Table 36. High-Speed I/O Specifications for Stratix V Devices (1), (2) (Part 1 of 4)

Sumbol	Conditions		C1 C2, C2L, I2, I2L		C3, I3, I3L, I3YY		C4,14			11				
Symbol	Conditions	Min	Тур	Max	Min	Тур	Max	Min	Тур	Max	Min	Тур	Max	UNIT
f <sub>HSCLK_in</sub> (input clock frequency) True Differential I/O Standards	Clock boost factor W = 1 to 40 $^{(4)}$	5	_	800	5		800	5		625	5		525	MHz
f <sub>HSCLK_in</sub> (input clock frequency) Single Ended I/O Standards <sup>(3)</sup>	Clock boost factor W = 1 to 40 $^{(4)}$	5		800	5		800	5		625	5		525	MHz
f <sub>HSCLK_in</sub> (input clock frequency) Single Ended I/O Standards	Clock boost factor W = 1 to 40 $^{(4)}$	5	_	520	5		520	5	_	420	5	_	420	MHz
f <sub>HSCLK_OUT</sub> (output clock frequency)	_	5	_	800	5	_	800	5	_	625 (5)	5	_	525 (5)	MHz

Figure 7 shows the dynamic phase alignment (DPA) lock time specifications with the DPA PLL calibration option enabled.

Figure 7. DPA Lock Time Specification with DPA PLL Calibration Enabled

rx_reset			
rx_dpa_locked			<u> </u>
			-

Table 37 lists the DPA lock time specifications for Stratix V devices.

Table 37. DPA Lock Time Specifications for Stratix V GX Devices Only (1), (2), (3)

Standard	Training Pattern	Number of Data Transitions in One Repetition of the Training Pattern	Number of Repetitions per 256 Data Transitions <sup>(4)</sup>	Maximum
SPI-4	00000000001111111111	2	128	640 data transitions
Parallel Rapid I/O	00001111	2	128	640 data transitions
Parallel Rapid I/O	10010000	4	64	640 data transitions
Miscollanoous	10101010	8	32	640 data transitions
Wiscenareous	01010101	8	32	640 data transitions

### Notes to Table 37:

(1) The DPA lock time is for one channel.

(2) One data transition is defined as a 0-to-1 or 1-to-0 transition.

(3) The DPA lock time stated in this table applies to both commercial and industrial grade.

(4) This is the number of repetitions for the stated training pattern to achieve the 256 data transitions.

Figure 8 shows the **LVDS** soft-clock data recovery (CDR)/DPA sinusoidal jitter tolerance specification for a data rate  $\geq$  1.25 Gbps. Table 38 lists the **LVDS** soft-CDR/DPA sinusoidal jitter tolerance specification for a data rate  $\geq$  1.25 Gbps.





Jitter Free	Sinusoidal Jitter (UI)	
F1	10,000	25.000
F2	17,565	25.000
F3	1,493,000	0.350
F4	50,000,000	0.350

I AULE 30. LVUJ JUIL"GUN/UFA JIIIUSUIUAI JIILEI IVIASK VAIUES IULA VALA NALE / 1.23 UL	able 38.	. LVDS Soft-CDR/DPA	Sinusoidal Jitter N	lask Values for a	Data Rate > 1.2	5 Gbps
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Figure 9 shows the **LVDS** soft-CDR/DPA sinusoidal jitter tolerance specification for a data rate < 1.25 Gbps.





### **DLL Range, DQS Logic Block, and Memory Output Clock Jitter Specifications**

Table 39 lists the DLL range specification for Stratix V devices. The DLL is always in 8-tap mode in Stratix V devices.

Table 39. DLL Range Specifications for Stratix V Devices (1)

C1	C2, C2L, I2, I2L	C3, I3, I3L, I3YY	C4,I4	Unit
300-933	300-933	300-890	300-890	MHz

#### Note to Table 39:

(1) Stratix V devices support memory interface frequencies lower than 300 MHz, although the reference clock that feeds the DLL must be at least 300 MHz. To support interfaces below 300 MHz, multiply the reference clock feeding the DLL to ensure the frequency is within the supported range of the DLL.

Table 40 lists the DQS phase offset delay per stage for Stratix V devices.

Table 40. DQS Phase Offset Delay Per Setting for Stratix V Devices <sup>(1), (2)</sup> (Part 1 of 2)

Speed Grade	Min	Max	Unit
C1	8	14	ps
C2, C2L, I2, I2L	8	14	ps
C3,I3, I3L, I3YY	8	15	ps

Speed Grade	Min	Max	Unit
C4,I4	8	16	ps

### Table 40. DQS Phase Offset Delay Per Setting for Stratix V Devices <sup>(1), (2)</sup> (Part 2 of 2)

#### Notes to Table 40:

(1) The typical value equals the average of the minimum and maximum values.

(2) The delay settings are linear with a cumulative delay variation of 40 ps for all speed grades. For example, when using a -2 speed grade and applying a 10-phase offset setting to a 90° phase shift at 400 MHz, the expected average cumulative delay is [625 ps + (10 × 10 ps) ± 20 ps] = 725 ps ± 20 ps.

Table 41 lists the DQS phase shift error for Stratix V devices.

Table 41. DQS Phase Shift Error Specification for DLL-Delayed Clock (t<sub>DQS\_PSERR</sub>) for Stratix V Devices <sup>(1)</sup>

Number of DQS Delay Buffers	C1	C2, C2L, I2, I2L	C3, I3, I3L, I3YY	C4,14	Unit
1	28	28	30	32	ps
2	56	56	60	64	ps
3	84	84	90	96	ps
4	112	112	120	128	ps

Notes to Table 41:

(1) This error specification is the absolute maximum and minimum error. For example, skew on three DQS delay buffers in a -2 speed grade is  $\pm 78$  ps or  $\pm 39$  ps.

Table 42 lists the memory output clock jitter specifications for Stratix V devices.

Table 42. Memory Output Clock Jitter Specification for Stratix V Devices (1	<sup>),</sup> (Part 1 of 2) <sup>(2), (3)</sup>
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Clock Network	Parameter	Symbol	C	1	C2, C2L	, 12, 12L	C3, I3 I3	8, 13L, YY	C4	,14	Unit
		-	Min	Max	Min	Max	Min	Max	Min	Max	
	Clock period jitter	$t_{JIT(per)}$	-50	50	-50	50	-55	55	-55	55	ps
Regional	Cycle-to-cycle period jitter	$t_{\text{JIT(cc)}}$	-100	100	-100	100	-110	110	-110	110	ps
	Duty cycle jitter	$t_{JIT(duty)}$	-50	50	-50	50	-82.5	82.5	-82.5	82.5	ps
	Clock period jitter	$t_{JIT(per)}$	-75	75	-75	75	-82.5	82.5	-82.5	82.5	ps
Global	Cycle-to-cycle period jitter	$t_{\text{JIT(cc)}}$	-150	150	-150	150	-165	165	-165	165	ps
	Duty cycle jitter	$t_{JIT(duty)}$	-75	75	-75	75	-90	90	-90	90	ps



### Figure 13. FPP Configuration Timing Waveform When the DCLK-to-DATA[] Ratio is >1 (1), (2)

#### Notes to Figure 13:

- (1) Use this timing waveform and parameters when the DCLK-to-DATA [] ratio is >1. To find out the DCLK-to-DATA [] ratio for your system, refer to Table 49 on page 55.
- (2) The beginning of this waveform shows the device in user mode. In user mode, nCONFIG, nSTATUS, and CONF\_DONE are at logic high levels. When nCONFIG is pulled low, a reconfiguration cycle begins.
- (3) After power-up, the Stratix V device holds nSTATUS low for the time as specified by the POR delay.
- (4) After power-up, before and during configuration, CONF\_DONE is low.
- (5) Do not leave DCLK floating after configuration. You can drive it high or low, whichever is more convenient.
- (6) "r" denotes the DCLK-to-DATA [] ratio. For the DCLK-to-DATA [] ratio based on the decompression and the design security feature enable settings, refer to Table 49 on page 55.
- (7) If needed, pause DCLK by holding it low. When DCLK restarts, the external host must provide data on the DATA [31..0] pins prior to sending the first DCLK rising edge.
- (8) To ensure a successful configuration, send the entire configuration data to the Stratix V device. CONF\_DONE is released high after the Stratix V device receives all the configuration data successfully. After CONF\_DONE goes high, send two additional falling edges on DCLK to begin initialization and enter user mode.
- (9) After the option bit to enable the INIT DONE pin is configured into the device, the INIT DONE goes low.

Table 51 lists the timing parameters for Stratix V devices for FPP configuration when the DCLK-to-DATA [] ratio is more than 1.

Table 51.	<b>FPP</b> Timing	Parameters f	or Stratix V	<b>Devices When</b>	the DCLK-te	o-DATA[] Ratio	is >1 (	1)
			•••••••••••••••••••••••••••••••••••••••			• • • • • • • • • • • • • • • • • • •		

Symbol	Parameter	Minimum	Maximum	Units
t <sub>CF2CD</sub>	nCONFIG low to CONF_DONE low	—	600	ns
t <sub>CF2ST0</sub>	nCONFIG low to nSTATUS low	—	600	ns
t <sub>CFG</sub>	nCONFIG low pulse width	2		μS
t <sub>STATUS</sub>	nSTATUS low pulse width	268	1,506 <sup>(2)</sup>	μS
t <sub>CF2ST1</sub>	nCONFIG high to nSTATUS high	—	1,506 <sup>(2)</sup>	μS
t <sub>CF2CK</sub> (5)	nCONFIG high to first rising edge on DCLK	1,506		μS
t <sub>ST2CK</sub> (5)	nSTATUS high to first rising edge of DCLK	2		μS
t <sub>DSU</sub>	DATA [] setup time before rising edge on DCLK	5.5		ns
t <sub>DH</sub>	DATA [] hold time after rising edge on DCLK	N-1/f <sub>DCLK</sub> (5)		S
t <sub>CH</sub>	DCLK high time	$0.45\times 1/f_{MAX}$		S
t <sub>CL</sub>	DCLK low time	$0.45\times 1/f_{MAX}$		S
t <sub>CLK</sub>	DCLK period	1/f <sub>MAX</sub>		S
f	DCLK frequency (FPP ×8/×16)	—	125	MHz
IMAX	DCLK frequency (FPP ×32)	—	100	MHz
t <sub>R</sub>	Input rise time	—	40	ns
t <sub>F</sub>	Input fall time	—	40	ns
t <sub>CD2UM</sub>	CONF_DONE high to user mode <sup>(3)</sup>	175	437	μS
t <sub>CD2CU</sub>	CONF_DONE high to CLKUSR enabled	4 × maximum DCLK period	_	_
t <sub>CD2UMC</sub>	CONF_DONE high to user mode with CLKUSR option on	t <sub>CD2CU</sub> + (8576 × CLKUSR period) <sup>(4)</sup>	_	_

#### Notes to Table 51:

- (1) Use these timing parameters when you use the decompression and design security features.
- (2) You can obtain this value if you do not delay configuration by extending the nCONFIG or nSTATUS low pulse width.
- (3) The minimum and maximum numbers apply only if you use the internal oscillator as the clock source for initializing the device.
- (4) To enable the CLKUSR pin as the initialization clock source and to obtain the maximum frequency specification on these pins, refer to the Initialization section of the "Configuration, Design Security, and Remote System Upgrades in Stratix V Devices" chapter.
- (5) N is the DCLK-to-DATA ratio and  $f_{\text{DCLK}}$  is the DCLK frequency the system is operating.
- (6) If nSTATUS is monitored, follow the t<sub>ST2CK</sub> specification. If nSTATUS is not monitored, follow the t<sub>CF2CK</sub> specification.

Table 54 lists the PS configuration timing parameters for Stratix V devices.

Table 54. PS Timing Parameters for Stratix V Devices

Symbol	Parameter	Minimum	Maximum	Units
t <sub>CF2CD</sub>	nCONFIG low to CONF_DONE low	—	600	ns
t <sub>CF2ST0</sub>	nCONFIG low to nSTATUS low	—	600	ns
t <sub>CFG</sub>	nCONFIG low pulse width	2	—	μS
t <sub>status</sub>	nSTATUS low pulse width	268	1,506 <sup>(1)</sup>	μS
t <sub>CF2ST1</sub>	nCONFIG high to nSTATUS high	—	1,506 <sup>(2)</sup>	μS
t <sub>CF2CK</sub> (5)	nCONFIG high to first rising edge on DCLK	1,506	—	μS
t <sub>ST2CK</sub> (5)	nSTATUS high to first rising edge of DCLK	2	—	μS
t <sub>DSU</sub>	DATA[] setup time before rising edge on DCLK	5.5	—	ns
t <sub>DH</sub>	DATA [] hold time after rising edge on DCLK	0	—	ns
t <sub>CH</sub>	DCLK high time	$0.45\times 1/f_{MAX}$	—	S
t <sub>CL</sub>	DCLK low time	$0.45\times 1/f_{MAX}$	—	S
t <sub>CLK</sub>	DCLK period	1/f <sub>MAX</sub>	—	S
f <sub>MAX</sub>	DCLK frequency	—	125	MHz
t <sub>CD2UM</sub>	CONF_DONE high to user mode <sup>(3)</sup>	175	437	μS
t <sub>CD2CU</sub>	CONF_DONE high to CLKUSR enabled	4 × maximum DCLK period	_	_
t <sub>cd2UMC</sub>	CONF_DONE high to user mode with CLKUSR option on	$t_{CD2CU}$ + (8576 × CLKUSR period) <sup>(4)</sup>	_	_

### Notes to Table 54:

(1) This value is applicable if you do not delay configuration by extending the nCONFIG or nSTATUS low pulse width.

(2) This value is applicable if you do not delay configuration by externally holding the nSTATUS low.

(3) The minimum and maximum numbers apply only if you choose the internal oscillator as the clock source for initializing the device.

(4) To enable the CLKUSR pin as the initialization clock source and to obtain the maximum frequency specification on these pins, refer to the "Initialization" section.

(5) If nSTATUS is monitored, follow the t<sub>ST2CK</sub> specification. If nSTATUS is not monitored, follow the t<sub>CF2CK</sub> specification.

### Initialization

Table 55 lists the initialization clock source option, the applicable configuration schemes, and the maximum frequency.

Table 55.	Initialization	<b>Clock Source</b>	e Option	and the	Maximum	Frequency

Initialization Clock Source	Configuration Schemes	Maximum Frequency	Minimum Number of Clock Cycles <sup>(1)</sup>
Internal Oscillator	AS, PS, FPP	12.5 MHz	
CLKUSR	AS, PS, FPP <sup>(2)</sup>	125 MHz	8576
DCLK	PS, FPP	125 MHz	

### Notes to Table 55:

(1) The minimum number of clock cycles required for device initialization.

(2) To enable CLKUSR as the initialization clock source, turn on the Enable user-supplied start-up clock (CLKUSR) option in the Quartus II software from the General panel of the Device and Pin Options dialog box.

Paramotor	Availabla	Min	Fast	Model	Slow Model							
(1)	Settings	<b>Offset</b> (2)	Industrial	Commercial	C1	C2	C3	C4	12	13, 13YY	14	Unit
D3	8	0	1.587	1.699	2.793	2.793	2.992	3.192	2.811	3.047	3.257	ns
D4	64	0	0.464	0.492	0.838	0.838	0.924	1.011	0.843	0.920	1.006	ns
D5	64	0	0.464	0.493	0.838	0.838	0.924	1.011	0.844	0.921	1.006	ns
D6	32	0	0.229	0.244	0.415	0.415	0.458	0.503	0.418	0.456	0.499	ns

Table 58.	IOE Pro	grammable De	lay for	Stratix V	V Devices	(Part 2 of 2	)
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#### Notes to Table 58:

(1) You can set this value in the Quartus II software by selecting D1, D2, D3, D5, and D6 in the Assignment Name column of Assignment Editor.

(2) Minimum offset does not include the intrinsic delay.

### **Programmable Output Buffer Delay**

Table 59 lists the delay chain settings that control the rising and falling edge delays of the output buffer. The default delay is 0 ps.

Symbol	Parameter	Typical	Unit
		0 (default)	ps
Dauman	Rising and/or falling edge	25	ps
DOUTBUF	delay	50	ps
		75	ps

Note to Table 59:

(1) You can set the programmable output buffer delay in the Quartus II software by setting the Output Buffer Delay Control assignment to either positive, negative, or both edges, with the specific values stated here (in ps) for the Output Buffer Delay assignment.

# Glossary

Table 60 lists the glossary for this chapter.

Table 60. Glossary (Part 1 of 4)

Letter	Subject	Definitions
Α		
В	—	—
С		
D	—	_
E	—	_
F	f <sub>HSCLK</sub>	Left and right PLL input clock frequency.
	f <sub>HSDR</sub>	High-speed I/O block—Maximum and minimum <b>LVDS</b> data transfer rate (f <sub>HSDR</sub> = 1/TUI), non-DPA.
	f <sub>hsdrdpa</sub>	High-speed I/O block—Maximum and minimum <b>LVDS</b> data transfer rate (f <sub>HSDRDPA</sub> = 1/TUI), DPA.

### Table 60. Glossary (Part 2 of 4)

Letter	Subject	Definitions
G H I	JTAG Timing Specifications	High-speed I/O block—Deserialization factor (width of parallel data bus). JTAG Timing Specifications: TMS
K L M N O		
Ρ	PLL Specifications	Diagram of PLL Specifications (1)
Q	_	—
R	RL	Receiver differential input discrete resistor (external to the Stratix V device).

Table 60.	Glossary	(Part 3 of 4)
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Letter	Subject	Definitions		
S	SW (sampling window)	Timing Diagram—the period of time during which the data must be valid in order to capture it correctly. The setup and hold times determine the ideal strobe position within the sampling window, as shown:         Bit Time         0.5 x TCCS       RSKM         Sampling Window       RSKM         0.5 x TCCS       RSKM		
	Single-ended voltage referenced I/O standard	The JEDEC standard for <b>SSTL</b> and <b>HSTL</b> I/O defines both the AC and DC input signal values. The AC values indicate the voltage levels at which the receiver must meet its timing specifications. The DC values indicate the voltage levels at which the final logic state of the receiver is unambiguously defined. After the receiver input has crossed the AC value, the receiver changes to the new logic state. The new logic state is then maintained as long as the input stays beyond the DC threshold. This approach is intended to provide predictable receiver timing in the presence of input waveform ringing: <i>Single-Ended Voltage Referenced I/O Standard</i> 		
	t <sub>C</sub>	High-speed receiver and transmitter input and output clock period.		
	TCCS (channel- to-channel-skew)	The timing difference between the fastest and slowest output edges, including $t_{CO}$ variation and clock skew, across channels driven by the same PLL. The clock is included in the TCCS measurement (refer to the <i>Timing Diagram</i> figure under <b>SW</b> in this table).		
	t <sub>DUTY</sub>	High-speed I/O block—Duty cycle on the high-speed transmitter output clock.		
т		<b>Timing Unit Interval (TUI)</b> The timing budget allowed for skew, propagation delays, and the data sampling window.		
		$(TUI = 1/(receiver input clock frequency multiplication factor) = t_C/W)$		
	t <sub>FALL</sub>	Signal high-to-low transition time (80-20%)		
	t <sub>INCCJ</sub>	Cycle-to-cycle jitter tolerance on the PLL clock input.		
	t <sub>outpj_i0</sub>	Period jitter on the general purpose I/O driven by a PLL.		
	t <sub>outpj_dc</sub>	Period jitter on the dedicated clock output driven by a PLL.		
	t <sub>RISE</sub>	Signal low-to-high transition time (20-80%)		
U	—	_		

Letter	Subject	Definitions
	V <sub>CM(DC)</sub>	DC common mode input voltage.
	V <sub>ICM</sub>	Input common mode voltage—The common mode of the differential signal at the receiver.
	V <sub>ID</sub>	Input differential voltage swing—The difference in voltage between the positive and complementary conductors of a differential transmission at the receiver.
	V <sub>DIF(AC)</sub>	AC differential input voltage—Minimum AC input differential voltage required for switching.
	V <sub>DIF(DC)</sub>	DC differential input voltage— Minimum DC input differential voltage required for switching.
	V <sub>IH</sub>	Voltage input high—The minimum positive voltage applied to the input which is accepted by the device as a logic high.
	V <sub>IH(AC)</sub>	High-level AC input voltage
	V <sub>IH(DC)</sub>	High-level DC input voltage
V	V <sub>IL</sub>	Voltage input low—The maximum positive voltage applied to the input which is accepted by the device as a logic low.
	V <sub>IL(AC)</sub>	Low-level AC input voltage
	V <sub>IL(DC)</sub>	Low-level DC input voltage
	V <sub>OCM</sub>	Output common mode voltage—The common mode of the differential signal at the transmitter.
	V <sub>OD</sub>	Output differential voltage swing—The difference in voltage between the positive and complementary conductors of a differential transmission at the transmitter.
	V <sub>SWING</sub>	Differential input voltage
	V <sub>X</sub>	Input differential cross point voltage
	V <sub>OX</sub>	Output differential cross point voltage
W	W	High-speed I/O block—clock boost factor
X		
Y	—	—
Z		

### Table 60. Glossary (Part 4 of 4)