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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

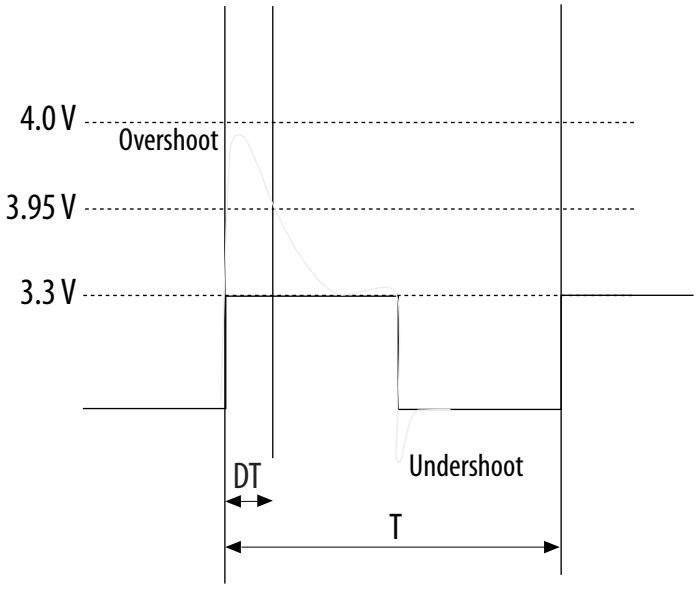
Details	
Product Status	Obsolete
Number of LABs/CLBs	234720
Number of Logic Elements/Cells	622000
Total RAM Bits	51200000
Number of I/O	840
Number of Gates	-
Voltage - Supply	0.82V ~ 0.88V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	1932-BBGA, FCBGA
Supplier Device Package	1932-FBGA, FC (45x45)
Purchase URL	https://www.e-xfl.com/product-detail/intel/5sgxea7n3f45i4n

Table 5 lists the maximum allowed input overshoot voltage and the duration of the overshoot voltage as a percentage of device lifetime. The maximum allowed overshoot duration is specified as a percentage of high time over the lifetime of the device. A DC signal is equivalent to 100% of the duty cycle. For example, a signal that overshoots to 3.95 V can be at 3.95 V for only ~21% over the lifetime of the device; for a device lifetime of 10 years, the overshoot duration amounts to ~2 years.

Table 5. Maximum Allowed Overshoot During Transitions

Symbol	Description	Condition (V)	Overshoot Duration as % @ T_J = 100°C	Unit
V (AC)	AC ·	3.8	100	%
		3.85	64	%
		3.9	36	%
		3.95	21	%
		4	12	%
		4.05	7	%
		4.1	4	%
		4.15	2	%
		4.2	1	%

Figure 1. Stratix V Device Overshoot Duration



I/O Pin Leakage Current

Table 9 lists the Stratix V I/O pin leakage current specifications.

Table 9. I/O Pin Leakage Current for Stratix V Devices (1)

Symbol	Description	Conditions	Min	Typ	Max	Unit
I_I	I · ·	V_I = 0 V V_{CCIOMA}	30		30	A
I_O	T - I/O ·	V_O = 0 V V_{CCIOMA}	30		30	A

Note toTable 9

(1) I $V_O = V_{CCIO}$ V_{CCIOM} , 100 A · I/O · .

Bus Hold Specifications

Table 10 lists the Stratix V device family bus hold specifications.

Table 10. Bus Hold Parameters for Stratix V Devices

Parameter	Symbol	Conditions	V_{CCIO}										Unit
			1.2 V		1.5 V		1.8 V		2.5 V		3.0 V		
			Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
L	I_{SUSL}	$V_{IN} > V_{IL}$ ( )	22.5		25.0		30.0		50.0		70.0		A
H	I_{SUSH}	$V_{IN} < V_{IH}$ ( )	22.5		25.0		30.0		50.0		70.0		A
L	I_{ODL}	0V < V_{IN} < V_{CCIO}		120		160		200		300		500	A
H	I_{ODH}	0V < V_{IN} < V_{CCIO}		120		160		200		300		500	A
B - · ·	V_{TRIP}		0.45	0.95	0.50	1.00	0.68	1.07	0.70	1.70	0.80	2.00	V

On-Chip Termination (OCT) Specifications

If you enable OCT calibration, calibration is automatically performed at power-up for I/Os connected to the calibration block. Table 11 lists the Stratix V OCT termination calibration accuracy specifications.

Table 11. OCT Calibration Accuracy Specifications for Stratix V Devices (1) (Part 1 of 2)

Symbol	Description	Conditions	Calibration Accuracy				Unit
			C1	C2,I2	C3,I3, I3YY	C4,I4	
25-Ω R_S	I (25-Ω)	V_{CCIO} = 3.0, 2.5, 1.8, 1.5, 1.2 V	15	15	15	15	%

Table 11. OCT Calibration Accuracy Specifications for Stratix V Devices (1) (Part 2 of 2)

Symbol	Description	Conditions	Calibration Accuracy				Unit
			C1	C2,I2	C3,I3, I3YY	C4,I4	
50-Ω R_S	I (50-Ω)	V_{CCIO} = 3.0, 2.5, 1.8, 1.5, 1.2 V	15	15	15	15	%
34-Ω 40-Ω R_S	I (34-Ω 40-Ω)	V_{CCIO} = 1.5, 1.35, 1.25, 1.2 V	15	15	15	15	%
48-Ω, 60-Ω, 80-Ω, 240-Ω R_S	I (48-Ω, 60-Ω, 80-Ω, 240-Ω)	V_{CCIO} = 1.2 V	15	15	15	15	%
50-Ω R_T	I . (50-Ω)	V_{CCIO} = 2.5, 1.8, 1.5, 1.2 V	10 +40	10 +40	10 +40	10 +40	%
20-Ω, 30-Ω, 40-Ω,60-Ω, 120-Ω R_T	I . (20-Ω, 30-Ω, 40-Ω, 60-Ω, 120-Ω)	V_{CCIO} = 1.5, 1.35, 1.25 V	10 +40	10 +40	10 +40	10 +40	%
60-Ω 120-Ω R_T	I . (60-Ω 120-Ω)	V_{CCIO} = 1.2	10 +40	10 +40	10 +40	10 +40	%
25-Ω R_S	I (25-Ω R_S)	V_{CCIO} = 3.0, 2.5, 1.8, 1.5, 1.2 V	15	15	15	15	%

Note toTable 11

(1) OCT .

Table 12 lists the Stratix V OCT without calibration resistance tolerance to PVT changes.

Table 12. OCT Without Calibration Resistance Tolerance Specifications for Stratix V Devices (Part 1 of 2)

Symbol	Description	Conditions	Resistance Tolerance				Unit
			C1	C2,I2	C3, I3, I3YY	C4, I4	
25-Ω R, 50-Ω R_S	I (25-Ω)	V_{CCIO} = 3.0 2.5 V	30	30	40	40	%
25-Ω R_S	I (25-Ω)	V_{CCIO} = 1.8 1.5 V	30	30	40	40	%
25-Ω R_S	I (25-Ω)	V_{CCIO} = 1.2 V	35	35	50	50	%

Table 23. Transceiver Specifications for Stratix V GX and GS Devices(1) (Part 4 of 7)

Symbol/ Description	Conditions	Transceiver Speed Grade 1			Transceiver Speed Grade 2			Transceiver Speed Grade 3			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
(21)	85 :		85 30			85 30			85 30		:
	100 :		100 30			100 30			100 30		:
	120 :		120 30			120 30			120 30		:
	150 :		150 30			150 30			150 30		:
( )	085 0		600		600		600				
	085 0		600		600		600				
	10 105		700		700		700				
	10		750		750		750				
(11)			10			10		10			
(12)		4		4			4				
(13)		4		4			4				
(14)		15		15			15				
		200		200			200				
( ) (10)	(625) (3125)		16			16		16			

Table 25 shows the approximate maximum data rate using the standard PCS.

Table 25. Stratix V Standard PCS Approximate Maximum Date Rate (1), (3)

Mode (2)	Transceiver Speed Grade	PMA Width	20	20	16	16	10	10	8	8
		PCS/Core Width	40	20	32	16	20	10	16	8
	1	1, 2, 2, 2, 2	122	114	76	12 65	58	52	472	
	2	1, 2, 2, 2, 2	122	114	76	12 65	58	52	472	
		3, 3, 3	8	0	784	72 53	47	424	376	
	3	1, 2, 2, 2, 2	85	85	85	85	65	58 52	472	
		3	103125	103125	784	72	53	47 424	376	
		3, 3, 3	85	85	784	72	53	47 424	376	
		4, 4	85	82	704	656	48	42 384	344	
	1	1, 2, 2, 2, 2	122	114	76	12 61	57	488	456	
	2	1, 2, 2, 2, 2	122	114	76	12 61	57	488	456	
		3, 3, 3	8	0	72	72 4	45	36 36		
	3	1, 2, 2, 2, 2	103125	103125	103125	103125	61	57	488	456
		3	103125	103125	72	72 4	45	36	36	
		3, 3, 3	85	85	72	72 4	45	36	36	
		4, 4	85	82	704	656	44	41 352	328	

otes to Tale 25

(1)

(2) , ,

(3) 1

Table 28. Transceiver Specifications for Stratix V GT Devices (Part 1 of 5) (1)

Symbol/ Description	Conditions	Transceiver Speed Grade 2			Transceiver Speed Grade 3			Unit
		Min	Typ	Max	Min	Typ	Max	
Reference Clock								
S · · I/O S	D .	1.2-V PCML, 1.4-V PCML, 1.5-V PCML, 2.5-V PCML, D LVPECL, LVDS, HCSL						
	R .	1.4-V PCML, 1.5-V PCML, 2.5-V PCML, LVPECL, LVDS						
I · R C F (CMU PLL) (6)		40		710	40		710	MH
I · R C F (AT PLL) (6)		100		710	100		710	MH
R	20% 80%			400			400	.
F	80% 20%			400			400	
D		45		55	45		55	%
S - ·	PCI E · (PCI)	30		33	30		33	H
S - · .	PCI		0 0.5			0 0.5		%
O - · (19)			100			100		Ω
A V_{MA} (3)	D .			1.6			1.6	V
	R .			1.2			1.2	
A V_{MIN}		-0.4			-0.4			V
P - - .		200		1600	200		1600	V
V_{ICM} (AC ·)	D .	1050/1000 (2)			1050/1000 (2)			V
	R .	1.0/0.9/0.85 (22)			1.0/0.9/0.85 (22)			V
V_{ICM} (DC ·)	HCSL I/O PCI	250		550	250		550	V

Duty Cycle Distortion (DCD) Specifications

Table 44 lists the worst-case DCD for Stratix V devices.

Table 44. Worst-Case DCD on Stratix V I/O Pins *(1)*

Symbol	C1		C2, C2L, I2, I2L		C3, I3, I3L, I3YY		C4,I4		Unit
	Min	Max	Min	Max	Min	Max	Min	Max	
O · D C	45	55	45	55	45	55	45	55	%

Note toTable 44

(1) T DCD .

Configuration Specification

POR Delay Specification

Power-on reset (POR) delay is defined as the delay between the time when all the power supplies monitored by the POR circuitry reach the minimum recommended operating voltage to the time when the nSTATUS is released high and your device is ready to begin configuration.

f For more information about the POR delay, refer to the *Hot Socketing and Power-On Reset in Stratix V Devices* chapter.

Table 45 lists the fast and standard POR delay specification.

Table 45. Fast and Standard POR Delay Specification *(1)*

POR Delay	Minimum	Maximum
F	4	12
S	100	300

Note toTable 45

(1) POR MSEL MSEL P S
C , D S , R S U S V D · .

JTAG Configuration Specifications

Table 46 lists the JTAG timing parameters and values for Stratix V devices.

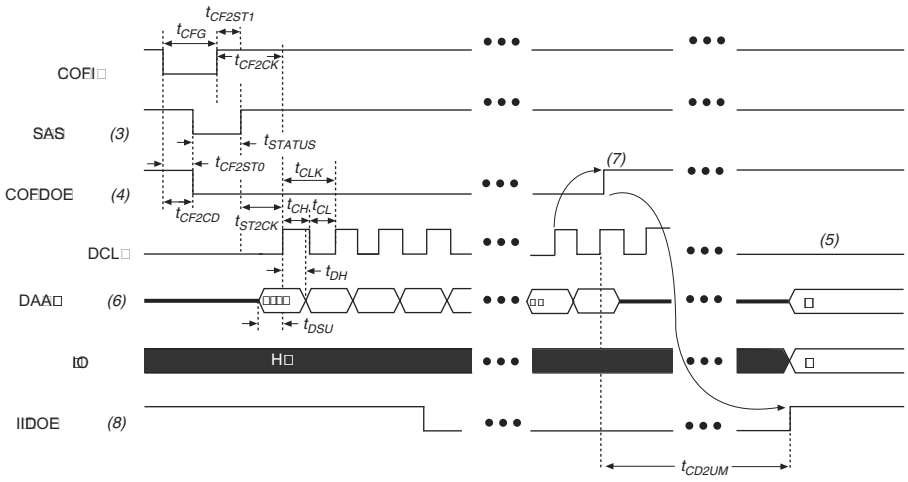
Table 46. JTAG Timing Parameters and Values for Stratix V Devices

Symbol	Description	Min	Max	Unit
JCP	TCK · *(2)*	30		
JCP	TCK · *(2)*	167		
JCH	TCK *(2)*	14		
JCL	TCK *(2)*	14		
JPSU (TDI)	TDI JTAG · ·	2		
JPSU (TMS)	TMS JTAG · ·	3		

FPP Configuration Timing when DCLK-to-DATA [] = 1

Figure 12 shows the timing waveform for FPP configuration when using a MAX II or MAX V device as an external host. This waveform shows timing when the DCLK-to-DATA[] ratio is 1.

Figure 12. FPP Configuration Timing Waveform When the DCLK-to-DATA[] Ratio is 1 *(1), (2)*



Notes toFigure 12

(1) U DCLK- -DATA[] 1.

(2) T .I , nCONFIG, nSTATUS, CONF_DONE - . nCONFIG · , .

(3) A · - · , S V nSTATUS POR .

(4) A · - · , , CONF_DONE .

(5) D DCLK . DCLK · .I .

(6) F FPP 16, DATA[15..0]. F FPP 8, DATA[7..0]. DATA[31..0] I/O· .T .

(7) T , S V . CONF_DONE S V .A CONF_DONE , DCLK .

(8) A · INIT_DONE· , INIT_DONE .

Document Revision History

Table 61 lists the revision history for this chapter.

Table 61. Document Revision History (Part 1 of 3)

Date	Version	Changes
J 2018	3.9	A S V D O D .
A 2017	3.8	A H -S I/O S S V D . C CD2UMC PS T P S V D . C 100-Ω R_D OCT C R T S S V D . C CD2UMC AS T P AS 1 AS 4 C S V D C CD2UMC FPP T P S V D DCLK- -DATA R >1 . C CD2UMC FPP T P S V D DCLK- -DATA R >1 . C I C S O M F .
J 2016	3.7	A V_{ID} · LVPECL D I/O S S S V D A I_{OUT} · A M R S V D .
D 2015	3.6	A H -S I/O S S V D .
D 2015	3.5	C , , AT PLL · T S S V G GS D . C . U · . S S V D .
J 2015	3.4	C · · 3 : T S S V G GS D S V S PCS A · M D R S V 10G PCS A · M D R C , T S S V G GS D . A M · · · T S S V G GS D . C CO AS T P AS 1 AS 4 C S V D . R CDR · · · T S S V G GS D .

Table 61. Document Revision History (Part 2 of 3)

Date	Version	Changes
N 2014	3.3	A I3 · G T 1. A I3 · V_{CC} · T 6. A I3 · $V_{CCHIP\ L}$, $V_{CCHIP\ R}$, $V_{CCHSSI\ L}$, $V_{CCHSSI\ R}$ · T 7. A 240-Ω T 11. C CDR PPM T 23. A PLL T 23. A I3 · · 3 T 25. A I3 · · 3 T 26. C CDR PPM T 28. A PLL T 28. C · MLAB M20K T 33. C M HSCLK OUT C2, C2L, I2, I2L · T 36. C C1 C2 T 39. C .rbf 5SGSD6 5SGSD8 T 47. A nSTATUS T 50, T 51, T 54. C T 58. C P · P . U I/O S S . U R B F S . U · T 22. U LVDS T 36. U DCLK F 11. U T 23 VO_{CM} (DC C ·) . U T 6 T 7. A DCLK · T 55. U T 47. U · T 56.
N 2013	3.2	U T 28
N 2013	3.1	U T 33
N 2013	3.0	U T 23 T 28
O 2013	2.9	U T C
O 2013	2.8	U T 3, T 12, T 14, T 19, T 20, T 23, T 24, T 28, T 30, T 31, T 32, T 33, T 36, T 39, T 40, T 41, T 42, T 47, T 53, T 58, T 59 A F 1 F 3 A T C R P .