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Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Obsolete
Number of LABs/CLBs	359200
Number of Logic Elements/Cells	952000
Total RAM Bits	53248000
Number of I/O	696
Number of Gates	-
Voltage - Supply	0.87V ~ 0.93V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	1517-BBGA, FCBGA
Supplier Device Package	1517-HBGA (45x45)
Purchase URL	https://www.e-xfl.com/product-detail/intel/5sgxeabk2h40i2n

Recommended Operating Conditions

This section lists the functional operating limits for the AC and DC parameters for Stratix V devices. Table 6 lists the steady-state voltage and current values expected from Stratix V devices. Power supply ramps must all be strictly monotonic, without plateaus.

Table 6. Recommended Operating Conditions for Stratix V Devices (Part 1 of 2)

Symbol	Description	Condition	Min ⁽⁴⁾	Typ	Max ⁽⁴⁾	Unit
V _{CC}	Core voltage and periphery circuitry power supply (C1, C2, I2, and I3YY speed grades)	—	0.87	0.9	0.93	V
	Core voltage and periphery circuitry power supply (C2L, C3, C4, I2L, I3, I3L, and I4 speed grades) ⁽³⁾	—	0.82	0.85	0.88	V
V _{CCPT}	Power supply for programmable power technology	—	1.45	1.50	1.55	V
V _{CC_AUX}	Auxiliary supply for the programmable power technology	—	2.375	2.5	2.625	V
V _{CCPD} ⁽¹⁾	I/O pre-driver (3.0 V) power supply	—	2.85	3.0	3.15	V
	I/O pre-driver (2.5 V) power supply	—	2.375	2.5	2.625	V
V _{CCIO}	I/O buffers (3.0 V) power supply	—	2.85	3.0	3.15	V
	I/O buffers (2.5 V) power supply	—	2.375	2.5	2.625	V
	I/O buffers (1.8 V) power supply	—	1.71	1.8	1.89	V
	I/O buffers (1.5 V) power supply	—	1.425	1.5	1.575	V
	I/O buffers (1.35 V) power supply	—	1.283	1.35	1.45	V
	I/O buffers (1.25 V) power supply	—	1.19	1.25	1.31	V
	I/O buffers (1.2 V) power supply	—	1.14	1.2	1.26	V
V _{CCPGM}	Configuration pins (3.0 V) power supply	—	2.85	3.0	3.15	V
	Configuration pins (2.5 V) power supply	—	2.375	2.5	2.625	V
	Configuration pins (1.8 V) power supply	—	1.71	1.8	1.89	V
V _{CCA_FPLL}	PLL analog voltage regulator power supply	—	2.375	2.5	2.625	V
V _{CCD_FPLL}	PLL digital voltage regulator power supply	—	1.45	1.5	1.55	V
V _{CCBAT} ⁽²⁾	Battery back-up power supply (For design security volatile key register)	—	1.2	—	3.0	V
V _I	DC input voltage	—	−0.5	—	3.6	V
V _O	Output voltage	—	0	—	V _{CCIO}	V
T _J	Operating junction temperature	Commercial	0	—	85	°C
		Industrial	−40	—	100	°C

Table 11. OCT Calibration Accuracy Specifications for Stratix V Devices ⁽¹⁾ (Part 2 of 2)

Symbol	Description	Conditions	Calibration Accuracy				Unit
			C1	C2,I2	C3,I3,I3YY	C4,I4	
50-Ω R _S	Internal series termination with calibration (50-Ω setting)	V _{CCIO} = 3.0, 2.5, 1.8, 1.5, 1.2 V	±15	±15	±15	±15	%
34-Ω and 40-Ω R _S	Internal series termination with calibration (34-Ω and 40-Ω setting)	V _{CCIO} = 1.5, 1.35, 1.25, 1.2 V	±15	±15	±15	±15	%
48-Ω, 60-Ω, 80-Ω, and 240-Ω R _S	Internal series termination with calibration (48-Ω, 60-Ω, 80-Ω, and 240-Ω setting)	V _{CCIO} = 1.2 V	±15	±15	±15	±15	%
50-Ω R _T	Internal parallel termination with calibration (50-Ω setting)	V _{CCIO} = 2.5, 1.8, 1.5, 1.2 V	-10 to +40	-10 to +40	-10 to +40	-10 to +40	%
20-Ω, 30-Ω, 40-Ω, 60-Ω, and 120-Ω R _T	Internal parallel termination with calibration (20-Ω, 30-Ω, 40-Ω, 60-Ω, and 120-Ω setting)	V _{CCIO} = 1.5, 1.35, 1.25 V	-10 to +40	-10 to +40	-10 to +40	-10 to +40	%
60-Ω and 120-Ω R _T	Internal parallel termination with calibration (60-Ω and 120-Ω setting)	V _{CCIO} = 1.2	-10 to +40	-10 to +40	-10 to +40	-10 to +40	%
25-Ω R _{S_left_shift}	Internal left shift series termination with calibration (25-Ω R _{S_left_shift} setting)	V _{CCIO} = 3.0, 2.5, 1.8, 1.5, 1.2 V	±15	±15	±15	±15	%

Note to Table 11:

(1) OCT calibration accuracy is valid at the time of calibration only.

Table 12 lists the Stratix V OCT without calibration resistance tolerance to PVT changes.

Table 12. OCT Without Calibration Resistance Tolerance Specifications for Stratix V Devices (Part 1 of 2)

Symbol	Description	Conditions	Resistance Tolerance				Unit
			C1	C2,I2	C3, I3, I3YY	C4, I4	
25-Ω R, 50-Ω R _S	Internal series termination without calibration (25-Ω setting)	V _{CCIO} = 3.0 and 2.5 V	±30	±30	±40	±40	%
25-Ω R _S	Internal series termination without calibration (25-Ω setting)	V _{CCIO} = 1.8 and 1.5 V	±30	±30	±40	±40	%
25-Ω R _S	Internal series termination without calibration (25-Ω setting)	V _{CCIO} = 1.2 V	±35	±35	±50	±50	%

Table 12. OCT Without Calibration Resistance Tolerance Specifications for Stratix V Devices (Part 2 of 2)

Symbol	Description	Conditions	Resistance Tolerance				Unit
			C1	C2, I2	C3, I3, I3YY	C4, I4	
50-Ω R _S	Internal series termination without calibration (50-Ω setting)	V _{CCIO} = 1.8 and 1.5 V	±30	±30	±40	±40	%
50-Ω R _S	Internal series termination without calibration (50-Ω setting)	V _{CCIO} = 1.2 V	±35	±35	±50	±50	%
100-Ω R _D	Internal differential termination (100-Ω setting)	V _{CCPD} = 2.5 V	±25	±25	±25	±25	%

Calibration accuracy for the calibrated series and parallel OCTs are applicable at the moment of calibration. When voltage and temperature conditions change after calibration, the tolerance may change.

OCT calibration is automatically performed at power-up for OCT-enabled I/Os. Table 13 lists the OCT variation with temperature and voltage after power-up calibration. Use Table 13 to determine the OCT variation after power-up calibration and Equation 1 to determine the OCT variation without recalibration.

Equation 1. OCT Variation Without Recalibration for Stratix V Devices ^{(1), (2), (3), (4), (5), (6)}

$$R_{OCT} = R_{SCAL} \left(1 + \left\langle \frac{dR}{dT} \times \Delta T \right\rangle \pm \left\langle \frac{dR}{dV} \times \Delta V \right\rangle \right)$$

Notes to Equation 1:

- (1) The R_{OCT} value shows the range of OCT resistance with the variation of temperature and V_{CCIO}.
- (2) R_{SCAL} is the OCT resistance value at power-up.
- (3) ΔT is the variation of temperature with respect to the temperature at power-up.
- (4) ΔV is the variation of voltage with respect to the V_{CCIO} at power-up.
- (5) dR/dT is the percentage change of R_{SCAL} with temperature.
- (6) dR/dV is the percentage change of R_{SCAL} with voltage.

Table 13 lists the on-chip termination variation after power-up calibration.

Table 13. OCT Variation after Power-Up Calibration for Stratix V Devices (Part 1 of 2) ⁽¹⁾

Symbol	Description	V _{CCIO} (V)	Typical	Unit
dR/dV	OCT variation with voltage without recalibration	3.0	0.0297	% / mV
		2.5	0.0344	
		1.8	0.0499	
		1.5	0.0744	
		1.2	0.1241	

Table 19. Single-Ended SSTL, HSTL, and HSUL I/O Standards Signal Specifications for Stratix V Devices (Part 2 of 2)

I/O Standard	$V_{IL(DC)}$ (V)		$V_{IH(DC)}$ (V)		$V_{IL(AC)}$ (V)	$V_{IH(AC)}$ (V)	V_{OL} (V)	V_{OH} (V)	I_{ol} (mA)	I_{oh} (mA)
	Min	Max	Min	Max	Max	Min	Max	Min		
HSTL-18 Class I	—	$V_{REF} - 0.1$	$V_{REF} + 0.1$	—	$V_{REF} - 0.2$	$V_{REF} + 0.2$	0.4	$V_{CCIO} - 0.4$	8	-8
HSTL-18 Class II	—	$V_{REF} - 0.1$	$V_{REF} + 0.1$	—	$V_{REF} - 0.2$	$V_{REF} + 0.2$	0.4	$V_{CCIO} - 0.4$	16	-16
HSTL-15 Class I	—	$V_{REF} - 0.1$	$V_{REF} + 0.1$	—	$V_{REF} - 0.2$	$V_{REF} + 0.2$	0.4	$V_{CCIO} - 0.4$	8	-8
HSTL-15 Class II	—	$V_{REF} - 0.1$	$V_{REF} + 0.1$	—	$V_{REF} - 0.2$	$V_{REF} + 0.2$	0.4	$V_{CCIO} - 0.4$	16	-16
HSTL-12 Class I	-0.15	$V_{REF} - 0.08$	$V_{REF} + 0.08$	$V_{CCIO} + 0.15$	$V_{REF} - 0.15$	$V_{REF} + 0.15$	$0.25^* V_{CCIO}$	$0.75^* V_{CCIO}$	8	-8
HSTL-12 Class II	-0.15	$V_{REF} - 0.08$	$V_{REF} + 0.08$	$V_{CCIO} + 0.15$	$V_{REF} - 0.15$	$V_{REF} + 0.15$	$0.25^* V_{CCIO}$	$0.75^* V_{CCIO}$	16	-16
HSUL-12	—	$V_{REF} - 0.13$	$V_{REF} + 0.13$	—	$V_{REF} - 0.22$	$V_{REF} + 0.22$	$0.1^* V_{CCIO}$	$0.9^* V_{CCIO}$	—	—

Table 20. Differential SSTL I/O Standards for Stratix V Devices

I/O Standard	V_{CCIO} (V)			$V_{SWING(DC)}$ (V)		$V_{X(AC)}$ (V)			$V_{SWING(AC)}$ (V)	
	Min	Typ	Max	Min	Max	Min	Typ	Max	Min	Max
SSTL-2 Class I, II	2.375	2.5	2.625	0.3	$V_{CCIO} + 0.6$	$V_{CCIO}/2 - 0.2$	—	$V_{CCIO}/2 + 0.2$	0.62	$V_{CCIO} + 0.6$
SSTL-18 Class I, II	1.71	1.8	1.89	0.25	$V_{CCIO} + 0.6$	$V_{CCIO}/2 - 0.175$	—	$V_{CCIO}/2 + 0.175$	0.5	$V_{CCIO} + 0.6$
SSTL-15 Class I, II	1.425	1.5	1.575	0.2	(1)	$V_{CCIO}/2 - 0.15$	—	$V_{CCIO}/2 + 0.15$	0.35	—
SSTL-135 Class I, II	1.283	1.35	1.45	0.2	(1)	$V_{CCIO}/2 - 0.15$	$V_{CCIO}/2$	$V_{CCIO}/2 + 0.15$	$2(V_{IH(AC)} - V_{REF})$	$2(V_{IL(AC)} - V_{REF})$
SSTL-125 Class I, II	1.19	1.25	1.31	0.18	(1)	$V_{CCIO}/2 - 0.15$	$V_{CCIO}/2$	$V_{CCIO}/2 + 0.15$	$2(V_{IH(AC)} - V_{REF})$	—
SSTL-12 Class I, II	1.14	1.2	1.26	0.18	—	$V_{REF} - 0.15$	$V_{CCIO}/2$	$V_{REF} + 0.15$	-0.30	0.30

Note to Table 20:

(1) The maximum value for $V_{SWING(DC)}$ is not defined. However, each single-ended signal needs to be within the respective single-ended limits ($V_{IH(DC)}$ and $V_{IL(DC)}$).

Table 21. Differential HSTL and HSUL I/O Standards for Stratix V Devices (Part 1 of 2)

I/O Standard	V_{CCIO} (V)			$V_{DIF(DC)}$ (V)		$V_{X(AC)}$ (V)			$V_{CM(DC)}$ (V)			$V_{DIF(AC)}$ (V)	
	Min	Typ	Max	Min	Max	Min	Typ	Max	Min	Typ	Max	Min	Max
HSTL-18 Class I, II	1.71	1.8	1.89	0.2	—	0.78	—	1.12	0.78	—	1.12	0.4	—
HSTL-15 Class I, II	1.425	1.5	1.575	0.2	—	0.68	—	0.9	0.68	—	0.9	0.4	—

Table 21. Differential HSTL and HSUL I/O Standards for Stratix V Devices (Part 2 of 2)

I/O Standard	V_{CCIO} (V)			$V_{DIF(DC)}$ (V)		$V_{X(AC)}$ (V)			$V_{CM(DC)}$ (V)			$V_{DIF(AC)}$ (V)	
	Min	Typ	Max	Min	Max	Min	Typ	Max	Min	Typ	Max	Min	Max
HSTL-12 Class I, II	1.14	1.2	1.26	0.16	$V_{CCIO} + 0.3$	—	$0.5^* V_{CCIO}$	—	$0.4^* V_{CCIO}$	$0.5^* V_{CCIO}$	$0.6^* V_{CCIO}$	0.3	$V_{CCIO} + 0.48$
HSUL-12	1.14	1.2	1.3	0.26	0.26	$0.5^* V_{CCIO} - 0.12$	$0.5^* V_{CCIO}$	$0.5^* V_{CCIO} + 0.12$	$0.4^* V_{CCIO}$	$0.5^* V_{CCIO}$	$0.6^* V_{CCIO}$	0.44	0.44

Table 22. Differential I/O Standard Specifications for Stratix V Devices ⁽⁷⁾

I/O Standard	V_{CCIO} (V) ⁽¹⁰⁾			V_{ID} (mV) ⁽⁸⁾			$V_{ICM(DC)}$ (V)			V_{OD} (V) ⁽⁶⁾			V_{OCM} (V) ⁽⁶⁾		
	Min	Typ	Max	Min	Condition	Max	Min	Condition	Max	Min	Typ	Max	Min	Typ	Max
PCML	Transmitter, receiver, and input reference clock pins of the high-speed transceivers use the PCML I/O standard. For transmitter, receiver, and reference clock I/O pin specifications, refer to Table 23 on page 18.														
2.5 V LVDS ⁽¹⁾	2.375	2.5	2.625	100	$V_{CM} = 1.25$ V	—	0.05	$D_{MAX} \leq 700$ Mbps	1.8	0.247	—	0.6	1.125	1.25	1.375
						—	1.05	$D_{MAX} > 700$ Mbps	1.55	0.247	—	0.6	1.125	1.25	1.375
BLVDS ⁽⁵⁾	2.375	2.5	2.625	100	—	—	—	—	—	—	—	—	—	—	—
RSDS (HIO) ⁽²⁾	2.375	2.5	2.625	100	$V_{CM} = 1.25$ V	—	0.3	—	1.4	0.1	0.2	0.6	0.5	1.2	1.4
Mini-LVDS (HIO) ⁽³⁾	2.375	2.5	2.625	200	—	600	0.4	—	1.325	0.25	—	0.6	1	1.2	1.4
LVPECL ^{(4), (9)}	—	—	—	300	—	—	0.6	$D_{MAX} \leq 700$ Mbps	1.8	—	—	—	—	—	—
	—	—	—	300	—	—	1	$D_{MAX} > 700$ Mbps	1.6	—	—	—	—	—	—

Notes to Table 22:

- (1) For optimized LVDS receiver performance, the receiver voltage input range must be between 1.0 V to 1.6 V for data rates above 700 Mbps, and 0 V to 1.85 V for data rates below 700 Mbps.
- (2) For optimized RSDS receiver performance, the receiver voltage input range must be between 0.25 V to 1.45 V.
- (3) For optimized Mini-LVDS receiver performance, the receiver voltage input range must be between 0.3 V to 1.425 V.
- (4) For optimized LVPECL receiver performance, the receiver voltage input range must be between 0.85 V to 1.75 V for data rate above 700 Mbps and 0.45 V to 1.95 V for data rate below 700 Mbps.
- (5) There are no fixed V_{ICM} , V_{OD} , and V_{OCM} specifications for BLVDS. They depend on the system topology.
- (6) RL range: $90 \leq RL \leq 110 \Omega$.
- (7) The 1.4-V and 1.5-V PCML transceiver I/O standard specifications are described in "Transceiver Performance Specifications" on page 18.
- (8) The minimum VID value is applicable over the entire common mode range, VCM.
- (9) LVPECL is only supported on dedicated clock input pins.
- (10) Differential inputs are powered by VCCPD which requires 2.5 V.

Power Consumption

Altera offers two ways to estimate power consumption for a design—the Excel-based Early Power Estimator and the Quartus® II PowerPlay Power Analyzer feature.

Table 23. Transceiver Specifications for Stratix V GX and GS Devices ⁽¹⁾ (Part 3 of 7)

Symbol/ Description	Conditions	Transceiver Speed Grade 1			Transceiver Speed Grade 2			Transceiver Speed Grade 3			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Reconfiguration clock (<code>mgmt_clk_clk</code>) frequency	—	100	—	125	100	—	125	100	—	125	MHz
Receiver											
Supported I/O Standards	—	1.4-V PCML, 1.5-V PCML, 2.5-V PCML, LVPECL, and LVDS									
Data rate (Standard PCS) (9), (23)	—	600	—	12200	600	—	12200	600	—	8500/ 10312.5 (24)	Mbps
Data rate (10G PCS) (9), (23)	—	600	—	14100	600	—	12500	600	—	8500/ 10312.5 (24)	Mbps
Absolute V_{MAX} for a receiver pin ⁽⁵⁾	—	—	—	1.2	—	—	1.2	—	—	1.2	V
Absolute V_{MIN} for a receiver pin	—	−0.4	—	—	−0.4	—	—	−0.4	—	—	V
Maximum peak- to-peak differential input voltage V_{ID} (diff p- p) before device configuration ⁽²²⁾	—	—	—	1.6	—	—	1.6	—	—	1.6	V
Maximum peak- to-peak differential input voltage V_{ID} (diff p- p) after device configuration ⁽¹⁸⁾ , (22)	$V_{CCR_GXB} =$ 1.0 V/1.05 V ($V_{ICM} =$ 0.70 V)	—	—	2.0	—	—	2.0	—	—	2.0	V
	$V_{CCR_GXB} =$ 0.90 V ($V_{ICM} = 0.6$ V)	—	—	2.4	—	—	2.4	—	—	2.4	V
	$V_{CCR_GXB} =$ 0.85 V ($V_{ICM} = 0.6$ V)	—	—	2.4	—	—	2.4	—	—	2.4	V
Minimum differential eye opening at receiver serial input pins ⁽⁶⁾ , (22), (27)	—	85	—	—	85	—	—	85	—	—	mV

Table 23. Transceiver Specifications for Stratix V GX and GS Devices ⁽¹⁾ (Part 7 of 7)

Symbol/ Description	Conditions	Transceiver Speed Grade 1			Transceiver Speed Grade 2			Transceiver Speed Grade 3			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
$t_{pll_lock}^{(16)}$	—	—	—	10	—	—	10	—	—	10	μs

Notes to Table 23:

- (1) Speed grades shown in Table 23 refer to the PMA Speed Grade in the device ordering code. The maximum data rate could be restricted by the Core/PCS speed grade. Contact your Altera Sales Representative for the maximum data rate specifications in each speed grade combination offered. For more information about device ordering codes, refer to the *Stratix V Device Overview*.
- (2) The reference clock common mode voltage is equal to the V_{CCR_GXB} power supply level.
- (3) This supply must be connected to 1.0 V if the transceiver is configured at a data rate > 6.5 Gbps, and to 1.05 V if configured at a data rate > 10.3 Gbps when DFE is used. For data rates up to 6.5 Gbps, you can connect this supply to 0.85 V.
- (4) This supply follows $VCCR_GXB$.
- (5) The device cannot tolerate prolonged operation at this absolute maximum.
- (6) The differential eye opening specification at the receiver input pins assumes that **Receiver Equalization** is disabled. If you enable **Receiver Equalization**, the receiver circuitry can tolerate a lower minimum eye opening, depending on the equalization level.
- (7) The Quartus II software automatically selects the appropriate slew rate depending on the configured data rate or functional mode.
- (8) The input reference clock frequency options depend on the data rate and the device speed grade.
- (9) The line data rate may be limited by PCS-FPGA interface speed grade.
- (10) Refer to Figure 1 for the GX channel AC gain curves. The total effective AC gain is the AC gain minus the DC gain.
- (11) t_{LTR} is the time required for the receive CDR to lock to the input reference clock frequency after coming out of reset.
- (12) t_{LTD} is time required for the receiver CDR to start recovering valid data after the rx_is_lockedtodata signal goes high.
- (13) t_{LTD_manual} is the time required for the receiver CDR to start recovering valid data after the rx_is_lockedtodata signal goes high when the CDR is functioning in the manual mode.
- (14) $t_{LTR_LTD_manual}$ is the time the receiver CDR must be kept in lock to reference (LTR) mode after the rx_is_lockedtoref signal goes high when the CDR is functioning in the manual mode.
- (15) $t_{pll_powerdown}$ is the PLL powerdown minimum pulse width.
- (16) t_{pll_lock} is the time required for the transmitter CMU/ATX PLL to lock to the input reference clock frequency after coming out of reset.
- (17) To calculate the REFCLK rms phase jitter requirement for PCIe at reference clock frequencies other than 100 MHz, use the following formula: REFCLK rms phase jitter at f(MHz) = REFCLK rms phase jitter at 100 MHz \times 100/f.
- (18) The maximum peak to peak differential input voltage V_{ID} after device configuration is equal to $4 \times (\text{absolute } V_{MAX} \text{ for receiver pin} - V_{ICM})$.
- (19) For ES devices, R_{REF} is $2000 \Omega \pm 1\%$.
- (20) To calculate the REFCLK phase noise requirement at frequencies other than 622 MHz, use the following formula: REFCLK phase noise at f(MHz) = REFCLK phase noise at 622 MHz + $20 \times \log(f/622)$.
- (21) SFP/+ optical modules require the host interface to have RD+/- differentially terminated with 100Ω . The internal OCT feature is available after the Stratix V FPGA configuration is completed. Altera recommends that FPGA configuration is completed before inserting the optical module. Otherwise, minimize unnecessary removal and insertion with unconfigured devices.
- (22) Refer to Figure 2.
- (23) For oversampling designs to support data rates less than the minimum specification, the CDR needs to be in LTR mode only.
- (24) I3YY devices can achieve data rates up to 10.3125 Gbps.
- (25) When you use fPLL as a TXPLL of the transceiver.
- (26) REFCLK performance requires to meet transmitter REFCLK phase noise specification.
- (27) Minimum eye opening of 85 mV is only for the unstressed input eye condition.

Table 26 shows the approximate maximum data rate using the 10G PCS.

Table 26. Stratix V 10G PCS Approximate Maximum Data Rate ⁽¹⁾

Mode ⁽²⁾	Transceiver Speed Grade	PMA Width	64	40	40	40	32	32
		PCS Width	64	66/67	50	40	64/66/67	32
FIFO or Register	1	C1, C2, C2L, I2, I2L core speed grade	14.1	14.1	10.69	14.1	13.6	13.6
	2	C1, C2, C2L, I2, I2L core speed grade	12.5	12.5	10.69	12.5	12.5	12.5
		C3, I3, I3L core speed grade	12.5	12.5	10.69	12.5	10.88	10.88
	3	C1, C2, C2L, I2, I2L core speed grade	8.5 Gbps					
		C3, I3, I3L core speed grade						
		C4, I4 core speed grade						
		I3YY core speed grade	10.3125 Gbps					

Notes to Table 26:

- (1) The maximum data rate is in Gbps.
- (2) The Phase Compensation FIFO can be configured in FIFO mode or register mode. In the FIFO mode, the pointers are not fixed, and the latency can vary. In the register mode the pointers are fixed for low latency.

Table 28. Transceiver Specifications for Stratix V GT Devices (Part 2 of 5) ⁽¹⁾

Symbol/ Description	Conditions	Transceiver Speed Grade 2			Transceiver Speed Grade 3			Unit
		Min	Typ	Max	Min	Typ	Max	
Transmitter REFCLK Phase Noise (622 MHz) ⁽¹⁸⁾	100 Hz	—	—	-70	—	—	-70	dBc/Hz
	1 kHz	—	—	-90	—	—	-90	
	10 kHz	—	—	-100	—	—	-100	
	100 kHz	—	—	-110	—	—	-110	
	≥ 1 MHz	—	—	-120	—	—	-120	
Transmitter REFCLK Phase Jitter (100 MHz) ⁽¹⁵⁾	10 kHz to 1.5 MHz (PCIe)	—	—	3	—	—	3	ps (rms)
RREF ⁽¹⁷⁾	—	—	1800 ± 1%	—	—	1800 ± 1%	—	Ω
Transceiver Clocks								
fixedclk clock frequency	PCIe Receiver Detect	—	100 or 125	—	—	100 or 125	—	MHz
Reconfiguration clock (mgmt_clk_clk) frequency	—	100	—	125	100	—	125	MHz
Receiver								
Supported I/O Standards	—	1.4-V PCML, 1.5-V PCML, 2.5-V PCML, LVPECL, and LVDS						
Data rate (Standard PCS) ⁽²¹⁾	GX channels	600	—	8500	600	—	8500	Mbps
Data rate (10G PCS) ⁽²¹⁾	GX channels	600	—	12,500	600	—	12,500	Mbps
Data rate	GT channels	19,600	—	28,050	19,600	—	25,780	Mbps
Absolute V _{MAX} for a receiver pin ⁽³⁾	GT channels	—	—	1.2	—	—	1.2	V
Absolute V _{MIN} for a receiver pin	GT channels	-0.4	—	—	-0.4	—	—	V
Maximum peak-to-peak differential input voltage V _{ID} (diff p-p) before device configuration ⁽²⁰⁾	GT channels	—	—	1.6	—	—	1.6	V
	GX channels	⁽⁸⁾						
Maximum peak-to-peak differential input voltage V _{ID} (diff p-p) after device configuration ⁽¹⁶⁾ , ⁽²⁰⁾	GT channels V _{CCR_GTB} = 1.05 V (V _{ICM} = 0.65 V)	—	—	2.2	—	—	2.2	V
	GX channels	⁽⁸⁾						
Minimum differential eye opening at receiver serial input pins ⁽⁴⁾ , ⁽²⁰⁾	GT channels	200	—	—	200	—	—	mV
	GX channels	⁽⁸⁾						

PLL Specifications

Table 31 lists the Stratix V PLL specifications when operating in both the commercial junction temperature range (0° to 85°C) and the industrial junction temperature range (–40° to 100°C).

Table 31. PLL Specifications for Stratix V Devices (Part 1 of 3)

Symbol	Parameter	Min	Typ	Max	Unit
f_{IN}	Input clock frequency (C1, C2, C2L, I2, and I2L speed grades)	5	—	800 ⁽¹⁾	MHz
	Input clock frequency (C3, I3, I3L, and I3YY speed grades)	5	—	800 ⁽¹⁾	MHz
	Input clock frequency (C4, I4 speed grades)	5	—	650 ⁽¹⁾	MHz
f_{INPFD}	Input frequency to the PFD	5	—	325	MHz
f_{FINPFD}	Fractional Input clock frequency to the PFD	50	—	160	MHz
f_{VCO} ⁽⁹⁾	PLL VCO operating range (C1, C2, C2L, I2, I2L speed grades)	600	—	1600	MHz
	PLL VCO operating range (C3, I3, I3L, I3YY speed grades)	600	—	1600	MHz
	PLL VCO operating range (C4, I4 speed grades)	600	—	1300	MHz
$t_{EINDUTY}$	Input clock or external feedback clock input duty cycle	40	—	60	%
f_{OUT}	Output frequency for an internal global or regional clock (C1, C2, C2L, I2, I2L speed grades)	—	—	717 ⁽²⁾	MHz
	Output frequency for an internal global or regional clock (C3, I3, I3L speed grades)	—	—	650 ⁽²⁾	MHz
	Output frequency for an internal global or regional clock (C4, I4 speed grades)	—	—	580 ⁽²⁾	MHz
f_{OUT_EXT}	Output frequency for an external clock output (C1, C2, C2L, I2, I2L speed grades)	—	—	800 ⁽²⁾	MHz
	Output frequency for an external clock output (C3, I3, I3L speed grades)	—	—	667 ⁽²⁾	MHz
	Output frequency for an external clock output (C4, I4 speed grades)	—	—	553 ⁽²⁾	MHz
$t_{OUTDUTY}$	Duty cycle for a dedicated external clock output (when set to 50%)	45	50	55	%
t_{FCOMP}	External feedback clock compensation time	—	—	10	ns
$f_{DYCONFIGCLK}$	Dynamic Configuration Clock used for <code>mgmt_clk</code> and <code>scanclk</code>	—	—	100	MHz
t_{LOCK}	Time required to lock from the end-of-device configuration or deassertion of <code>areset</code>	—	—	1	ms
t_{DLOCK}	Time required to lock dynamically (after switchover or reconfiguring any non-post-scale counters/delays)	—	—	1	ms
f_{CLBW}	PLL closed-loop low bandwidth	—	0.3	—	MHz
	PLL closed-loop medium bandwidth	—	1.5	—	MHz
	PLL closed-loop high bandwidth ⁽⁷⁾	—	4	—	MHz
t_{PLL_PSERR}	Accuracy of PLL phase shift	—	—	±50	ps
t_{ARESET}	Minimum pulse width on the <code>areset</code> signal	10	—	—	ns

Table 31. PLL Specifications for Stratix V Devices (Part 2 of 3)

Symbol	Parameter	Min	Typ	Max	Unit
t_{INCCJ} ^{(3), (4)}	Input clock cycle-to-cycle jitter ($f_{\text{REF}} \geq 100$ MHz)	—	—	0.15	UI (p-p)
	Input clock cycle-to-cycle jitter ($f_{\text{REF}} < 100$ MHz)	−750	—	+750	ps (p-p)
$t_{\text{OUTPJ_DC}}$ ⁽⁵⁾	Period Jitter for dedicated clock output ($f_{\text{OUT}} \geq 100$ MHz)	—	—	175 ⁽¹⁾	ps (p-p)
	Period Jitter for dedicated clock output ($f_{\text{OUT}} < 100$ MHz)	—	—	17.5 ⁽¹⁾	mUI (p-p)
$t_{\text{FOUTPJ_DC}}$ ⁽⁵⁾	Period Jitter for dedicated clock output in fractional PLL ($f_{\text{OUT}} \geq 100$ MHz)	—	—	250 ⁽¹¹⁾ , 175 ⁽¹²⁾	ps (p-p)
	Period Jitter for dedicated clock output in fractional PLL ($f_{\text{OUT}} < 100$ MHz)	—	—	25 ⁽¹¹⁾ , 17.5 ⁽¹²⁾	mUI (p-p)
$t_{\text{OUTCCJ_DC}}$ ⁽⁵⁾	Cycle-to-Cycle Jitter for a dedicated clock output ($f_{\text{OUT}} \geq 100$ MHz)	—	—	175	ps (p-p)
	Cycle-to-Cycle Jitter for a dedicated clock output ($f_{\text{OUT}} < 100$ MHz)	—	—	17.5	mUI (p-p)
$t_{\text{FOUTCCJ_DC}}$ ⁽⁵⁾	Cycle-to-cycle Jitter for a dedicated clock output in fractional PLL ($f_{\text{OUT}} \geq 100$ MHz)	—	—	250 ⁽¹¹⁾ , 175 ⁽¹²⁾	ps (p-p)
	Cycle-to-cycle Jitter for a dedicated clock output in fractional PLL ($f_{\text{OUT}} < 100$ MHz)+	—	—	25 ⁽¹¹⁾ , 17.5 ⁽¹²⁾	mUI (p-p)
$t_{\text{OUTPJ_IO}}$ ^{(5), (8)}	Period Jitter for a clock output on a regular I/O in integer PLL ($f_{\text{OUT}} \geq 100$ MHz)	—	—	600	ps (p-p)
	Period Jitter for a clock output on a regular I/O ($f_{\text{OUT}} < 100$ MHz)	—	—	60	mUI (p-p)
$t_{\text{FOUTPJ_IO}}$ ^{(5), (8), (11)}	Period Jitter for a clock output on a regular I/O in fractional PLL ($f_{\text{OUT}} \geq 100$ MHz)	—	—	600 ⁽¹⁰⁾	ps (p-p)
	Period Jitter for a clock output on a regular I/O in fractional PLL ($f_{\text{OUT}} < 100$ MHz)	—	—	60 ⁽¹⁰⁾	mUI (p-p)
$t_{\text{OUTCCJ_IO}}$ ^{(5), (8)}	Cycle-to-cycle Jitter for a clock output on a regular I/O in integer PLL ($f_{\text{OUT}} \geq 100$ MHz)	—	—	600	ps (p-p)
	Cycle-to-cycle Jitter for a clock output on a regular I/O in integer PLL ($f_{\text{OUT}} < 100$ MHz)	—	—	60 ⁽¹⁰⁾	mUI (p-p)
$t_{\text{FOUTCCJ_IO}}$ ^{(5), (8), (11)}	Cycle-to-cycle Jitter for a clock output on a regular I/O in fractional PLL ($f_{\text{OUT}} \geq 100$ MHz)	—	—	600 ⁽¹⁰⁾	ps (p-p)
	Cycle-to-cycle Jitter for a clock output on a regular I/O in fractional PLL ($f_{\text{OUT}} < 100$ MHz)	—	—	60	mUI (p-p)
$t_{\text{CASC_OUTPJ_DC}}$ ^{(5), (6)}	Period Jitter for a dedicated clock output in cascaded PLLs ($f_{\text{OUT}} \geq 100$ MHz)	—	—	175	ps (p-p)
	Period Jitter for a dedicated clock output in cascaded PLLs ($f_{\text{OUT}} < 100$ MHz)	—	—	17.5	mUI (p-p)
f_{DRIFT}	Frequency drift after PFDENA is disabled for a duration of 100 μ s	—	—	± 10	%
dK_{BIT}	Bit number of Delta Sigma Modulator (DSM)	8	24	32	Bits
k_{VALUE}	Numerator of Fraction	128	8388608	2147483648	—

Table 32. Block Performance Specifications for Stratix V DSP Devices (Part 2 of 2)

Mode	Peformance							Unit
	C1	C2, C2L	I2, I2L	C3	I3, I3L, I3YY	C4	I4	
Modes using Three DSPs								
One complex 18 x 25	425	425	415	340	340	275	265	MHz
Modes using Four DSPs								
One complex 27 x 27	465	465	465	380	380	300	290	MHz

Memory Block Specifications

Table 33 lists the Stratix V memory block specifications.

Table 33. Memory Block Performance Specifications for Stratix V Devices ⁽¹⁾, ⁽²⁾ (Part 1 of 2)

Memory	Mode	Resources Used		Performance							Unit
		ALUTs	Memory	C1	C2, C2L	C3	C4	I2, I2L	I3, I3L, I3YY	I4	
MLAB	Single port, all supported widths	0	1	450	450	400	315	450	400	315	MHz
	Simple dual-port, x32/x64 depth	0	1	450	450	400	315	450	400	315	MHz
	Simple dual-port, x16 depth ⁽³⁾	0	1	675	675	533	400	675	533	400	MHz
	ROM, all supported widths	0	1	600	600	500	450	600	500	450	MHz

Table 33. Memory Block Performance Specifications for Stratix V Devices ^{(1), (2)} (Part 2 of 2)

Memory	Mode	Resources Used		Performance							Unit
		ALUTs	Memory	C1	C2, C2L	C3	C4	I2, I2L	I3, I3L, I3YY	I4	
M20K Block	Single-port, all supported widths	0	1	700	700	650	550	700	500	450	MHz
	Simple dual-port, all supported widths	0	1	700	700	650	550	700	500	450	MHz
	Simple dual-port with the read-during-write option set to Old Data , all supported widths	0	1	525	525	455	400	525	455	400	MHz
	Simple dual-port with ECC enabled, 512 × 32	0	1	450	450	400	350	450	400	350	MHz
	Simple dual-port with ECC and optional pipeline registers enabled, 512 × 32	0	1	600	600	500	450	600	500	450	MHz
	True dual port, all supported widths	0	1	700	700	650	550	700	500	450	MHz
	ROM, all supported widths	0	1	700	700	650	550	700	500	450	MHz

Notes to Table 33:

- (1) To achieve the maximum memory block performance, use a memory block clock that comes through global clock routing from an on-chip PLL set to **50%** output duty cycle. Use the Quartus II software to report timing for this and other memory block clocking schemes.
- (2) When you use the error detection cyclical redundancy check (CRC) feature, there is no degradation in F_{MAX}.
- (3) The F_{MAX} specification is only achievable with Fitter options, **MLAB Implementation In 16-Bit Deep Mode** enabled.

Temperature Sensing Diode Specifications

Table 34 lists the internal TSD specification.

Table 34. Internal Temperature Sensing Diode Specification

Temperature Range	Accuracy	Offset Calibrated Option	Sampling Rate	Conversion Time	Resolution	Minimum Resolution with no Missing Codes
–40°C to 100°C	±8°C	No	1 MHz, 500 KHz	< 100 ms	8 bits	8 bits

Table 35 lists the specifications for the Stratix V external temperature sensing diode.

Table 35. External Temperature Sensing Diode Specifications for Stratix V Devices

Description	Min	Typ	Max	Unit
I _{bias} , diode source current	8	—	200	μA
V _{bias} , voltage across diode	0.3	—	0.9	V
Series resistance	—	—	< 1	Ω
Diode ideality factor	1.006	1.008	1.010	—

Table 46. JTAG Timing Parameters and Values for Stratix V Devices

Symbol	Description	Min	Max	Unit
t_{JPH}	JTAG port hold time	5	—	ns
t_{JPCO}	JTAG port clock to output	—	11 ⁽¹⁾	ns
t_{JPZX}	JTAG port high impedance to valid output	—	14 ⁽¹⁾	ns
t_{JPXZ}	JTAG port valid output to high impedance	—	14 ⁽¹⁾	ns

Notes to Table 46:

- (1) A 1 ns adder is required for each V_{CCIO} voltage step down from 3.0 V. For example, t_{JPCO} = 12 ns if V_{CCIO} of the TDO I/O bank = 2.5 V, or 13 ns if it equals 1.8 V.
- (2) The minimum TCK clock period is 167 ns if VCCBAT is within the range 1.2V-1.5V when you perform the volatile key programming.

Raw Binary File Size

For the POR delay specification, refer to the “POR Delay Specification” section of the “Configuration, Design Security, and Remote System Upgrades in Stratix V Devices”.

Table 47 lists the uncompressed raw binary file (.rbf) sizes for Stratix V devices.

Table 47. Uncompressed .rbf Sizes for Stratix V Devices

Family	Device	Package	Configuration .rbf Size (bits)	IOCSR .rbf Size (bits) ^{(4), (5)}
Stratix V GX	5SGXA3	H35, F40, F35 ⁽²⁾	213,798,880	562,392
		H29, F35 ⁽³⁾	137,598,880	564,504
	5SGXA4	—	213,798,880	563,672
	5SGXA5	—	269,979,008	562,392
	5SGXA7	—	269,979,008	562,392
	5SGXA9	—	342,742,976	700,888
	5SGXAB	—	342,742,976	700,888
	5SGXB5	—	270,528,640	584,344
	5SGXB6	—	270,528,640	584,344
	5SGXB9	—	342,742,976	700,888
	5SGXBB	—	342,742,976	700,888
Stratix V GT	5SGTC5	—	269,979,008	562,392
	5SGTC7	—	269,979,008	562,392
Stratix V GS	5SGSD3	—	137,598,880	564,504
	5SGSD4	F1517	213,798,880	563,672
		—	137,598,880	564,504
	5SGSD5	—	213,798,880	563,672
	5SGSD6	—	293,441,888	565,528
	5SGSD8	—	293,441,888	565,528

Table 47. Uncompressed .rbf Sizes for Stratix V Devices

Family	Device	Package	Configuration .rbf Size (bits)	IOCSR .rbf Size (bits) ^{(4), (5)}
Stratix V E ⁽¹⁾	5SEE9	—	342,742,976	700,888
	5SEEB	—	342,742,976	700,888

Notes to Table 47:

- (1) Stratix V E devices do not have PCI Express® (PCIe®) hard IP. Stratix V E devices do not support the CvP configuration scheme.
- (2) 36-transceiver devices.
- (3) 24-transceiver devices.
- (4) File size for the periphery image.
- (5) The IOCSR .rbf size is specifically for the CvP feature.

Use the data in Table 47 to estimate the file size before design compilation. Different configuration file formats, such as a hexadecimal (.hex) or tabular text file (.tff) format, have different file sizes. For the different types of configuration file and file sizes, refer to the Quartus II software. However, for a specific version of the Quartus II software, any design targeted for the same device has the same uncompressed configuration file size. If you are using compression, the file size can vary after each compilation because the compression ratio depends on your design.



For more information about setting device configuration options, refer to *Configuration, Design Security, and Remote System Upgrades in Stratix V Devices*. For creating configuration files, refer to the *Quartus II Help*.

Table 48 lists the minimum configuration time estimates for Stratix V devices.

Table 48. Minimum Configuration Time Estimation for Stratix V Devices

Variant	Member Code	Active Serial ⁽¹⁾			Fast Passive Parallel ⁽²⁾		
		Width	DCLK (MHz)	Min Config Time (s)	Width	DCLK (MHz)	Min Config Time (s)
GX	A3	4	100	0.534	32	100	0.067
		4	100	0.344	32	100	0.043
	A4	4	100	0.534	32	100	0.067
	A5	4	100	0.675	32	100	0.084
	A7	4	100	0.675	32	100	0.084
	A9	4	100	0.857	32	100	0.107
	AB	4	100	0.857	32	100	0.107
	B5	4	100	0.676	32	100	0.085
	B6	4	100	0.676	32	100	0.085
	B9	4	100	0.857	32	100	0.107
	BB	4	100	0.857	32	100	0.107
GT	C5	4	100	0.675	32	100	0.084
	C7	4	100	0.675	32	100	0.084

FPP Configuration Timing when DCLK-to-DATA [] = 1

Figure 12 shows the timing waveform for FPP configuration when using a MAX II or MAX V device as an external host. This waveform shows timing when the DCLK-to-DATA [] ratio is 1.

Figure 12. FPP Configuration Timing Waveform When the DCLK-to-DATA[] Ratio is 1 ^{(1), (2)}



Notes to Figure 12:

- (1) Use this timing waveform when the DCLK-to-DATA [] ratio is 1.
- (2) The beginning of this waveform shows the device in user mode. In user mode, nCONFIG, nSTATUS, and CONF_DONE are at logic-high levels. When nCONFIG is pulled low, a reconfiguration cycle begins.
- (3) After power-up, the Stratix V device holds nSTATUS low for the time of the POR delay.
- (4) After power-up, before and during configuration, CONF_DONE is low.
- (5) Do not leave DCLK floating after configuration. DCLK is ignored after configuration is complete. It can toggle high or low if required.
- (6) For FPP x16, use DATA [15..0]. For FPP x8, use DATA [7..0]. DATA [31..0] are available as a user I/O pin after configuration. The state of this pin depends on the dual-purpose pin settings.
- (7) To ensure a successful configuration, send the entire configuration data to the Stratix V device. CONF_DONE is released high when the Stratix V device receives all the configuration data successfully. After CONF_DONE goes high, send two additional falling edges on DCLK to begin initialization and enter user mode.
- (8) After the option bit to enable the INIT_DONE pin is configured into the device, the INIT_DONE goes low.

Table 50 lists the timing parameters for Stratix V devices for FPP configuration when the DCLK-to-DATA [] ratio is 1.

Table 50. FPP Timing Parameters for Stratix V Devices ⁽¹⁾

Symbol	Parameter	Minimum	Maximum	Units
t _{CF2CD}	nCONFIG low to CONF_DONE low	—	600	ns
t _{CF2ST0}	nCONFIG low to nSTATUS low	—	600	ns
t _{CFG}	nCONFIG low pulse width	2	—	μs
t _{STATUS}	nSTATUS low pulse width	268	1,506 ⁽²⁾	μs
t _{CF2ST1}	nCONFIG high to nSTATUS high	—	1,506 ⁽³⁾	μs
t _{CF2CK} ⁽⁶⁾	nCONFIG high to first rising edge on DCLK	1,506	—	μs
t _{ST2CK} ⁽⁶⁾	nSTATUS high to first rising edge of DCLK	2	—	μs
t _{DSU}	DATA [] setup time before rising edge on DCLK	5.5	—	ns
t _{DH}	DATA [] hold time after rising edge on DCLK	0	—	ns
t _{CH}	DCLK high time	$0.45 \times 1/f_{\text{MAX}}$	—	s
t _{CL}	DCLK low time	$0.45 \times 1/f_{\text{MAX}}$	—	s
t _{CLK}	DCLK period	$1/f_{\text{MAX}}$	—	s
f _{MAX}	DCLK frequency (FPP ×8/×16)	—	125	MHz
	DCLK frequency (FPP ×32)	—	100	MHz
t _{CD2UM}	CONF_DONE high to user mode ⁽⁴⁾	175	437	μs
t _{CD2CU}	CONF_DONE high to CLKUSR enabled	4 × maximum DCLK period	—	—
t _{CD2UMC}	CONF_DONE high to user mode with CLKUSR option on	t _{CD2CU} + (8576 × CLKUSR period) ⁽⁵⁾	—	—

Notes to Table 50:

- (1) Use these timing parameters when the decompression and design security features are disabled.
- (2) This value is applicable if you do not delay configuration by extending the nCONFIG or nSTATUS low pulse width.
- (3) This value is applicable if you do not delay configuration by externally holding the nSTATUS low.
- (4) The minimum and maximum numbers apply only if you chose the internal oscillator as the clock source for initializing the device.
- (5) To enable the CLKUSR pin as the initialization clock source and to obtain the maximum frequency specification on these pins, refer to the Initialization section of the “Configuration, Design Security, and Remote System Upgrades in Stratix V Devices” chapter.
- (6) If nSTATUS is monitored, follow the t_{ST2CK} specification. If nSTATUS is not monitored, follow the t_{CF2CK} specification.

FPP Configuration Timing when DCLK-to-DATA [] > 1

Figure 13 shows the timing waveform for FPP configuration when using a MAX II device, MAX V device, or microprocessor as an external host. This waveform shows timing when the DCLK-to-DATA [] ratio is more than 1.

Table 51 lists the timing parameters for Stratix V devices for FPP configuration when the DCLK-to-DATA [] ratio is more than 1.

Table 51. FPP Timing Parameters for Stratix V Devices When the DCLK-to-DATA[] Ratio is >1 ⁽¹⁾

Symbol	Parameter	Minimum	Maximum	Units
t_{CF2CD}	nCONFIG low to CONF_DONE low	—	600	ns
t_{CF2ST0}	nCONFIG low to nSTATUS low	—	600	ns
t_{CFG}	nCONFIG low pulse width	2	—	μ s
t_{STATUS}	nSTATUS low pulse width	268	1,506 ⁽²⁾	μ s
t_{CF2ST1}	nCONFIG high to nSTATUS high	—	1,506 ⁽²⁾	μ s
t_{CF2CK} ⁽⁵⁾	nCONFIG high to first rising edge on DCLK	1,506	—	μ s
t_{ST2CK} ⁽⁵⁾	nSTATUS high to first rising edge of DCLK	2	—	μ s
t_{DSU}	DATA [] setup time before rising edge on DCLK	5.5	—	ns
t_{DH}	DATA [] hold time after rising edge on DCLK	$N-1/f_{DCLK}$ ⁽⁵⁾	—	s
t_{CH}	DCLK high time	$0.45 \times 1/f_{MAX}$	—	s
t_{CL}	DCLK low time	$0.45 \times 1/f_{MAX}$	—	s
t_{CLK}	DCLK period	$1/f_{MAX}$	—	s
f_{MAX}	DCLK frequency (FPP $\times 8/\times 16$)	—	125	MHz
	DCLK frequency (FPP $\times 32$)	—	100	MHz
t_R	Input rise time	—	40	ns
t_F	Input fall time	—	40	ns
t_{CD2UM}	CONF_DONE high to user mode ⁽³⁾	175	437	μ s
t_{CD2CU}	CONF_DONE high to CLKUSR enabled	$4 \times$ maximum DCLK period	—	—
t_{CD2UMC}	CONF_DONE high to user mode with CLKUSR option on	$t_{CD2CU} + (8576 \times \text{CLKUSR period})$ ⁽⁴⁾	—	—

Notes to Table 51:

- (1) Use these timing parameters when you use the decompression and design security features.
- (2) You can obtain this value if you do not delay configuration by extending the nCONFIG or nSTATUS low pulse width.
- (3) The minimum and maximum numbers apply only if you use the internal oscillator as the clock source for initializing the device.
- (4) To enable the CLKUSR pin as the initialization clock source and to obtain the maximum frequency specification on these pins, refer to the Initialization section of the “Configuration, Design Security, and Remote System Upgrades in Stratix V Devices” chapter.
- (5) N is the DCLK-to-DATA ratio and f_{DCLK} is the DCLK frequency the system is operating.
- (6) If nSTATUS is monitored, follow the t_{ST2CK} specification. If nSTATUS is not monitored, follow the t_{CF2CK} specification.

Table 53. AS Timing Parameters for AS ×1 and AS ×4 Configurations in Stratix V Devices ^{(1), (2)} (Part 2 of 2)

Symbol	Parameter	Minimum	Maximum	Units
t_{CD2UM}	CONF_DONE high to user mode ⁽³⁾	175	437	μs
t_{CD2CU}	CONF_DONE high to CLKUSR enabled	4 × maximum DCLK period	—	—
t_{CD2UMC}	CONF_DONE high to user mode with CLKUSR option on	$t_{CD2CU} + (8576 \times \text{CLKUSR period})$	—	—

Notes to Table 53:

- (1) The minimum and maximum numbers apply only if you choose the internal oscillator as the clock source for initializing the device.
- (2) t_{CF2CD} , t_{CF2ST0} , t_{CFG} , t_{STATUS} , and t_{CF2ST1} timing parameters are identical to the timing parameters for PS mode listed in Table 54 on page 63.
- (3) To enable the CLKUSR pin as the initialization clock source and to obtain the maximum frequency specification on this pin, refer to the Initialization section of the “Configuration, Design Security, and Remote System Upgrades in Stratix V Devices” chapter.

Passive Serial Configuration Timing

Figure 15 shows the timing waveform for a passive serial (PS) configuration when using a MAX II device, MAX V device, or microprocessor as an external host.

Figure 15. PS Configuration Timing Waveform ⁽¹⁾**Notes to Figure 15:**

- (1) The beginning of this waveform shows the device in user mode. In user mode, nCONFIG, nSTATUS, and CONF_DONE are at logic high levels. When nCONFIG is pulled low, a reconfiguration cycle begins.
- (2) After power-up, the Stratix V device holds nSTATUS low for the time of the POR delay.
- (3) After power-up, before and during configuration, CONF_DONE is low.
- (4) Do not leave DCLK floating after configuration. You can drive it high or low, whichever is more convenient.
- (5) DATA0 is available as a user I/O pin after configuration. The state of this pin depends on the dual-purpose pin settings in the **Device and Pins Option**.
- (6) To ensure a successful configuration, send the entire configuration data to the Stratix V device. CONF_DONE is released high after the Stratix V device receives all the configuration data successfully. After CONF_DONE goes high, send two additional falling edges on DCLK to begin initialization and enter user mode.
- (7) After the option bit to enable the INIT_DONE pin is configured into the device, the INIT_DONE goes low.

Table 60. Glossary (Part 3 of 4)

Letter	Subject	Definitions
S	SW (sampling window)	<p>Timing Diagram—the period of time during which the data must be valid in order to capture it correctly. The setup and hold times determine the ideal strobe position within the sampling window, as shown:</p> 
	Single-ended voltage referenced I/O standard	<p>The JEDEC standard for SSTL and HSTL I/O defines both the AC and DC input signal values. The AC values indicate the voltage levels at which the receiver must meet its timing specifications. The DC values indicate the voltage levels at which the final logic state of the receiver is unambiguously defined. After the receiver input has crossed the AC value, the receiver changes to the new logic state.</p> <p>The new logic state is then maintained as long as the input stays beyond the DC threshold. This approach is intended to provide predictable receiver timing in the presence of input waveform ringing:</p> <p><i>Single-Ended Voltage Referenced I/O Standard</i></p> 
T	t_c	High-speed receiver and transmitter input and output clock period.
	TCCS (channel-to-channel-skew)	The timing difference between the fastest and slowest output edges, including t_{CO} variation and clock skew, across channels driven by the same PLL. The clock is included in the TCCS measurement (refer to the <i>Timing Diagram</i> figure under SW in this table).
	t_{DUTY}	<p>High-speed I/O block—Duty cycle on the high-speed transmitter output clock.</p> <p>Timing Unit Interval (TUI)</p> <p>The timing budget allowed for skew, propagation delays, and the data sampling window. (TUI = $1/(\text{receiver input clock frequency multiplication factor}) = t_c/w$)</p>
	t_{FALL}	Signal high-to-low transition time (80-20%)
	t_{INCCJ}	Cycle-to-cycle jitter tolerance on the PLL clock input.
	t_{OUTPJ_IO}	Period jitter on the general purpose I/O driven by a PLL.
	t_{OUTPJ_DC}	Period jitter on the dedicated clock output driven by a PLL.
	t_{RISE}	Signal low-to-high transition time (20-80%)
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