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## Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

## Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

| Details | |
|---|---|
| Product Status | Obsolete |
| Number of LABs/CLBs | 359200 |
| Number of Logic Elements/Cells | 952000 |
| Total RAM Bits | 53248000 |
| Number of I/O | 840 |
| Number of Gates | - |
| Voltage - Supply | 0.87V ~ 0.93V |
| Mounting Type | Surface Mount |
| Operating Temperature | 0°C ~ 85°C (TJ) |
| Package / Case | 1932-BBGA, FCBGA |
| Supplier Device Package | 1932-FBGA, FC (45x45) |
| Purchase URL | https://www.e-xfl.com/product-detail/intel/5sgxeabn2f45c2n |

## Recommended Operating Conditions

This section lists the functional operating limits for the AC and DC parameters for Stratix V devices. Table 6 lists the steady-state voltage and current values expected from Stratix V devices. Power supply ramps must all be strictly monotonic, without plateaus.

**Table 6. Recommended Operating Conditions for Stratix V Devices (Part 1 of 2)**

| Symbol | Description | Condition | Min (4) | Typ | Max (4) | Unit |
|---|---|---|---|---|---|---|
| $V_{CC}$ | Core voltage and periphery circuitry power supply (C1, C2, I2, and I3YY speed grades) | — | 0.87 | 0.9 | 0.93 | V |
| | Core voltage and periphery circuitry power supply (C2L, C3, C4, I2L, I3, I3L, and I4 speed grades) (3) | — | 0.82 | 0.85 | 0.88 | V |
| $V_{CCPT}$ | Power supply for programmable power technology | — | 1.45 | 1.50 | 1.55 | V |
| $V_{CC\_AUX}$ | Auxiliary supply for the programmable power technology | — | 2.375 | 2.5 | 2.625 | V |
| $V_{CCPD}$ (1) | I/O pre-driver (3.0 V) power supply | — | 2.85 | 3.0 | 3.15 | V |
| | I/O pre-driver (2.5 V) power supply | — | 2.375 | 2.5 | 2.625 | V |
| $V_{CCIO}$ | I/O buffers (3.0 V) power supply | — | 2.85 | 3.0 | 3.15 | V |
| | I/O buffers (2.5 V) power supply | — | 2.375 | 2.5 | 2.625 | V |
| | I/O buffers (1.8 V) power supply | — | 1.71 | 1.8 | 1.89 | V |
| | I/O buffers (1.5 V) power supply | — | 1.425 | 1.5 | 1.575 | V |
| | I/O buffers (1.35 V) power supply | — | 1.283 | 1.35 | 1.45 | V |
| | I/O buffers (1.25 V) power supply | — | 1.19 | 1.25 | 1.31 | V |
| | I/O buffers (1.2 V) power supply | — | 1.14 | 1.2 | 1.26 | V |
| $V_{CCPGM}$ | Configuration pins (3.0 V) power supply | — | 2.85 | 3.0 | 3.15 | V |
| | Configuration pins (2.5 V) power supply | — | 2.375 | 2.5 | 2.625 | V |
| | Configuration pins (1.8 V) power supply | — | 1.71 | 1.8 | 1.89 | V |
| $V_{CCA\_FPLL}$ | PLL analog voltage regulator power supply | — | 2.375 | 2.5 | 2.625 | V |
| $V_{CCD\_FPLL}$ | PLL digital voltage regulator power supply | — | 1.45 | 1.5 | 1.55 | V |
| $V_{CCBAT}$ (2) | Battery back-up power supply (For design security volatile key register) | — | 1.2 | — | 3.0 | V |
| $V_I$ | DC input voltage | — | –0.5 | — | 3.6 | V |
| $V_O$ | Output voltage | — | 0 | — | $V_{CCIO}$ | V |
| $T_J$ | Operating junction temperature | Commercial | 0 | — | 85 | °C |
| | | Industrial | –40 | — | 100 | °C |

**Table 6. Recommended Operating Conditions for Stratix V Devices (Part 2 of 2)**

| Symbol | Description | Condition | Min (4) | Typ | Max (4) | Unit |
|---|---|---|---|---|---|---|
| $t_{RAMP}$ | Power supply ramp time | Standard POR | 200 µs | — | 100 ms | — |
| | | Fast POR | 200 µs | — | 4 ms | — |

**Notes to Table 6:**

(1) $V_{CCPD}$ must be 2.5 V when $V_{CCIO}$ is 2.5, 1.8, 1.5, 1.35, 1.25 or 1.2 V. $V_{CCPD}$ must be 3.0 V when $V_{CCIO}$ is 3.0 V.

(2) If you do not use the design security feature in Stratix V devices, connect $V_{CCBAT}$ to a 1.2- to 3.0-V power supply. Stratix V power-on-reset (POR) circuitry monitors $V_{CCBAT}$. Stratix V devices will not exit POR if $V_{CCBAT}$ stays at logic low.

(3) C2L and I2L can also be run at 0.90 V for legacy boards that were designed for the C2 and I2 speed grades.

(4) The power supply value describes the budget for the DC (static) power supply tolerance and does not include the dynamic tolerance requirements. Refer to the PDN tool for the additional budget for the dynamic tolerance requirements.

Table 7 lists the transceiver power supply recommended operating conditions for Stratix V GX, GS, and GT devices.

**Table 7. Recommended Transceiver Power Supply Operating Conditions for Stratix V GX, GS, and GT Devices (Part 1 of 2)**

| Symbol | Description | Devices | Minimum (4) | Typical | Maximum (4) | Unit |
|---|---|---|---|---|---|---|
| $V_{CCA\_GXBL}$ (1), (3) | Transceiver channel PLL power supply (left side) | GX, GS, GT | 2.85 | 3.0 | 3.15 | V |
| | | | 2.375 | 2.5 | 2.625 | |
| $V_{CCA\_GXBR}$ (1), (3) | Transceiver channel PLL power supply (right side) | GX, GS | 2.85 | 3.0 | 3.15 | V |
| | | | 2.375 | 2.5 | 2.625 | |
| $V_{CCA\_GTBR}$ | Transceiver channel PLL power supply (right side) | GT | 2.85 | 3.0 | 3.15 | V |
| $V_{CCHIP\_L}$ | Transceiver hard IP power supply (left side; C1, C2, I2, and I3YY speed grades) | GX, GS, GT | 0.87 | 0.9 | 0.93 | V |
| | Transceiver hard IP power supply (left side; C2L, C3, C4, I2L, I3, I3L, and I4 speed grades) | GX, GS, GT | 0.82 | 0.85 | 0.88 | V |
| $V_{CCHIP\_R}$ | Transceiver hard IP power supply (right side; C1, C2, I2, and I3YY speed grades) | GX, GS, GT | 0.87 | 0.9 | 0.93 | V |
| | Transceiver hard IP power supply (right side; C2L, C3, C4, I2L, I3, I3L, and I4 speed grades) | GX, GS, GT | 0.82 | 0.85 | 0.88 | V |
| $V_{CCHSSI\_L}$ | Transceiver PCS power supply (left side; C1, C2, I2, and I3YY speed grades) | GX, GS, GT | 0.87 | 0.9 | 0.93 | V |
| | Transceiver PCS power supply (left side; C2L, C3, C4, I2L, I3, I3L, and I4 speed grades) | GX, GS, GT | 0.82 | 0.85 | 0.88 | V |
| $V_{CCHSSI\_R}$ | Transceiver PCS power supply (right side; C1, C2, I2, and I3YY speed grades) | GX, GS, GT | 0.87 | 0.9 | 0.93 | V |
| | Transceiver PCS power supply (right side; C2L, C3, C4, I2L, I3, I3L, and I4 speed grades) | GX, GS, GT | 0.82 | 0.85 | 0.88 | V |
| $V_{CCR\_GXBL}$ (2) | Receiver analog power supply (left side) | GX, GS, GT | 0.82 | 0.85 | 0.88 | V |
| | | | 0.87 | 0.90 | 0.93 | |
| | | | 0.97 | 1.0 | 1.03 | |
| | | | 1.03 | 1.05 | 1.07 | |

### I/O Pin Leakage Current

Table 9 lists the Stratix V I/O pin leakage current specifications.

**Table 9. I/O Pin Leakage Current for Stratix V Devices (1)**

| Symbol | Description | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $I_I$ | Input pin | $V_I$ = 0 V to $V_{CCIOMAX}$ | –30 | — | 30 | µA |
| $I_{OZ}$ | Tri-stated I/O pin | $V_O$ = 0 V to $V_{CCIOMAX}$ | –30 | — | 30 | µA |

**Note to Table 9:**

(1) If $V_O = V_{CCIO}$ to $V_{CCIOMax}$, 100 µA of leakage current per I/O is expected.

### Bus Hold Specifications

Table 10 lists the Stratix V device family bus hold specifications.

**Table 10. Bus Hold Parameters for Stratix V Devices**

| Parameter | Symbol | Conditions | $V_{CCIO}$ | | | | | | | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | 1.2 V | | 1.5 V | | 1.8 V | | 2.5 V | | 3.0 V | | |
| | | | Min | Max | Min | Max | Min | Max | Min | Max | Min | Max | |
| Low sustaining current | $I_{SUSL}$ | $V_{IN} > V_{IL}$ (maximum) | 22.5 | — | 25.0 | — | 30.0 | — | 50.0 | — | 70.0 | — | µA |
| High sustaining current | $I_{SUSH}$ | $V_{IN} < V_{IH}$ (minimum) | –22.5 | — | –25.0 | — | –30.0 | — | –50.0 | — | –70.0 | — | µA |
| Low overdrive current | $I_{ODL}$ | $0V < V_{IN} < V_{CCIO}$ | — | 120 | — | 160 | — | 200 | — | 300 | — | 500 | µA |
| High overdrive current | $I_{ODH}$ | $0V < V_{IN} < V_{CCIO}$ | — | –120 | — | –160 | — | –200 | — | –300 | — | –500 | µA |
| Bus-hold trip point | $V_{TRIP}$ | — | 0.45 | 0.95 | 0.50 | 1.00 | 0.68 | 1.07 | 0.70 | 1.70 | 0.80 | 2.00 | V |

### On-Chip Termination (OCT) Specifications

If you enable OCT calibration, calibration is automatically performed at power-up for I/Os connected to the calibration block. Table 11 lists the Stratix V OCT termination calibration accuracy specifications.

**Table 11. OCT Calibration Accuracy Specifications for Stratix V Devices (1) (Part 1 of 2)**

| Symbol | Description | Conditions | Calibration Accuracy | | | | Unit |
|---|---|---|---|---|---|---|---|
| | | | C1 | C2,I2 | C3,I3, I3YY | C4,I4 | |
| 25-Ω $R_S$ | Internal series termination with calibration (25-Ω setting) | $V_{CCIO}$ = 3.0, 2.5, 1.8, 1.5, 1.2 V | ±15 | ±15 | ±15 | ±15 | % |

**Table 13. OCT Variation after Power-Up Calibration for Stratix V Devices (Part 2 of 2) (1)**

| Symbol | Description | $V_{CCIO}$ (V) | Typical | Unit |
|---|---|---|---|---|
| dR/dT | OCT variation with temperature without recalibration | 3.0 | 0.189 | %/°C |
| | | 2.5 | 0.208 | |
| | | 1.8 | 0.266 | |
| | | 1.5 | 0.273 | |
| | | 1.2 | 0.317 | |

**Note to Table 13:**

(1) Valid for a $V_{CCIO}$ range of ±5% and a temperature range of 0° to 85°C.

### Pin Capacitance

Table 14 lists the Stratix V device family pin capacitance.

**Table 14. Pin Capacitance for Stratix V Devices**

| Symbol | Description | Value | Unit |
|---|---|---|---|
| $C_{IOTB}$ | Input capacitance on the top and bottom I/O pins | 6 | pF |
| $C_{IOLR}$ | Input capacitance on the left and right I/O pins | 6 | pF |
| $C_{OUTFB}$ | Input capacitance on dual-purpose clock output and feedback pins | 6 | pF |

### Hot Socketing

Table 15 lists the hot socketing specifications for Stratix V devices.

**Table 15. Hot Socketing Specifications for Stratix V Devices**

| Symbol | Description | Maximum |
|---|---|---|
| $I_{IOPIN\ (DC)}$ | DC current per I/O pin | 300 µA |
| $I_{IOPIN\ (AC)}$ | AC current per I/O pin | 8 mA (1) |
| $I_{XCVR\text{-}TX\ (DC)}$ | DC current per transceiver transmitter pin | 100 mA |
| $I_{XCVR\text{-}RX\ (DC)}$ | DC current per transceiver receiver pin | 50 mA |

**Note to Table 15:**

(1) The I/O ramp rate is 10 ns or more. For ramp rates faster than 10 ns, $|I_{IOPIN}| = C\ dv/dt$, in which C is the I/O pin capacitance and dv/dt is the slew rate.

**Table 23. Transceiver Specifications for Stratix V GX and GS Devices (1) (Part 3 of 7)**

| Symbol/ Description | Conditions | Transceiver Speed Grade 1 | | | Transceiver Speed Grade 2 | | | Transceiver Speed Grade 3 | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| Reconfiguration clock (mgmt_clk_clk) frequency | — | 100 | — | 125 | 100 | — | 125 | 100 | — | 125 | MHz |
| **Receiver** | | | | | | | | | | | |
| Supported I/O Standards | — | 1.4-V PCML, 1.5-V PCML, 2.5-V PCML, LVPECL, and LVDS | | | | | | | | | |
| Data rate (Standard PCS) (9), (23) | — | 600 | — | 12200 | 600 | — | 12200 | 600 | — | 8500/ 10312.5 (24) | Mbps |
| Data rate (10G PCS) (9), (23) | — | 600 | — | 14100 | 600 | — | 12500 | 600 | — | 8500/ 10312.5 (24) | Mbps |
| Absolute $V_{MAX}$ for a receiver pin (5) | — | — | — | 1.2 | — | — | 1.2 | — | — | 1.2 | V |
| Absolute $V_{MIN}$ for a receiver pin | — | –0.4 | — | — | –0.4 | — | — | –0.4 | — | — | V |
| Maximum peak-to-peak differential input voltage $V_{ID}$ (diff p-p) before device configuration (22) | — | — | — | 1.6 | — | — | 1.6 | — | — | 1.6 | V |
| Maximum peak-to-peak differential input voltage $V_{ID}$ (diff p-p) after device configuration (18), (22) | $V_{CCR\_GXB}$ = 1.0 V/1.05 V ($V_{ICM}$ = 0.70 V) | — | — | 2.0 | — | — | 2.0 | — | — | 2.0 | V |
| | $V_{CCR\_GXB}$ = 0.90 V ($V_{ICM}$ = 0.6 V) | — | — | 2.4 | — | — | 2.4 | — | — | 2.4 | V |
| | $V_{CCR\_GXB}$ = 0.85 V ($V_{ICM}$ = 0.6 V) | — | — | 2.4 | — | — | 2.4 | — | — | 2.4 | V |
| Minimum differential eye opening at receiver serial input pins (6), (22), (27) | — | 85 | — | — | 85 | — | — | 85 | — | — | mV |

**Table 23. Transceiver Specifications for Stratix V GX and GS Devices (1) (Part 5 of 7)**

| Symbol/ Description | Conditions | Transceiver Speed Grade 1 | | | Transceiver Speed Grade 2 | | | Transceiver Speed Grade 3 | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| Programmable DC gain | DC Gain Setting = 0 | — | 0 | — | — | 0 | — | — | 0 | — | dB |
| | DC Gain Setting = 1 | — | 2 | — | — | 2 | — | — | 2 | — | dB |
| | DC Gain Setting = 2 | — | 4 | — | — | 4 | — | — | 4 | — | dB |
| | DC Gain Setting = 3 | — | 6 | — | — | 6 | — | — | 6 | — | dB |
| | DC Gain Setting = 4 | — | 8 | — | — | 8 | — | — | 8 | — | dB |
| **Transmitter** | | | | | | | | | | | |
| Supported I/O Standards | — | 1.4-V and 1.5-V PCML | | | | | | | | | |
| Data rate (Standard PCS) | — | 600 | — | 12200 | 600 | — | 12200 | 600 | — | 8500/ 10312.5 (24) | Mbps |
| Data rate (10G PCS) | — | 600 | — | 14100 | 600 | — | 12500 | 600 | — | 8500/ 10312.5 (24) | Mbps |
| Differential on-chip termination resistors | 85-Ω setting | — | 85 ± 20% | — | — | 85 ± 20% | — | — | 85 ± 20% | — | Ω |
| | 100-Ω setting | — | 100 ± 20% | — | — | 100 ± 20% | — | — | 100 ± 20% | — | Ω |
| | 120-Ω setting | — | 120 ± 20% | — | — | 120 ± 20% | — | — | 120 ± 20% | — | Ω |
| | 150-Ω setting | — | 150 ± 20% | — | — | 150 ± 20% | — | — | 150 ± 20% | — | Ω |
| $V_{OCM}$ (AC coupled) | 0.65-V setting | — | 650 | — | — | 650 | — | — | 650 | — | mV |
| $V_{OCM}$ (DC coupled) | — | — | 650 | — | — | 650 | — | — | 650 | — | mV |
| Rise time (7) | 20% to 80% | 30 | — | 160 | 30 | — | 160 | 30 | — | 160 | ps |
| Fall time (7) | 80% to 20% | 30 | — | 160 | 30 | — | 160 | 30 | — | 160 | ps |
| Intra-differential pair skew | Tx $V_{CM}$ = 0.5 V and slew rate of 15 ps | — | — | 15 | — | — | 15 | — | — | 15 | ps |
| Intra-transceiver block transmitter channel-to-channel skew | x6 PMA bonded mode | — | — | 120 | — | — | 120 | — | — | 120 | ps |

**Table 23. Transceiver Specifications for Stratix V GX and GS Devices (1) (Part 6 of 7)**

| Symbol/ Description | Conditions | Transceiver Speed Grade 1 | | | Transceiver Speed Grade 2 | | | Transceiver Speed Grade 3 | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| Inter-transceiver block transmitter channel-to-channel skew | xN PMA bonded mode | — | — | 500 | — | — | 500 | — | — | 500 | ps |
| **CMU PLL** | | | | | | | | | | | |
| Supported Data Range | — | 600 | — | 12500 | 600 | — | 12500 | 600 | — | 8500/ 10312.5 (24) | Mbps |
| $t_{pll\_powerdown}$ (15) | — | 1 | — | — | 1 | — | — | 1 | — | — | µs |
| $t_{pll\_lock}$ (16) | — | — | — | 10 | — | — | 10 | — | — | 10 | µs |
| **ATX PLL** | | | | | | | | | | | |
| Supported Data Rate Range | VCO post-divider L=2 | 8000 | — | 14100 | 8000 | — | 12500 | 8000 | — | 8500/ 10312.5 (24) | Mbps |
| | L=4 | 4000 | — | 7050 | 4000 | — | 6600 | 4000 | — | 6600 | Mbps |
| | L=8 | 2000 | — | 3525 | 2000 | — | 3300 | 2000 | — | 3300 | Mbps |
| | L=8, Local/Central Clock Divider =2 | 1000 | — | 1762.5 | 1000 | — | 1762.5 | 1000 | — | 1762.5 | Mbps |
| $t_{pll\_powerdown}$ (15) | — | 1 | — | — | 1 | — | — | 1 | — | — | µs |
| $t_{pll\_lock}$ (16) | — | — | — | 10 | — | — | 10 | — | — | 10 | µs |
| **fPLL** | | | | | | | | | | | |
| Supported Data Range | — | 600 | — | 3250/ 3125 (25) | 600 | — | 3250/ 3125 (25) | 600 | — | 3250/ 3125 (25) | Mbps |
| $t_{pll\_powerdown}$ (15) | — | 1 | — | — | 1 | — | — | 1 | — | — | µs |

Table 26 shows the approximate maximum data rate using the 10G PCS.

**Table 26. Stratix V 10G PCS Approximate Maximum Data Rate** *(1)*

| Mode *(2)* | Transceiver Speed Grade | PMA Width | 64 | 40 | 40 | 40 | 32 | 32 |
|---|---|---|---|---|---|---|---|---|
| | | **PCS Width** | **64** | **66/67** | **50** | **40** | **64/66/67** | **32** |
| FIFO or Register | 1 | C1, C2, C2L, I2, I2L core speed grade | 14.1 | 14.1 | 10.69 | 14.1 | 13.6 | 13.6 |
| | 2 | C1, C2, C2L, I2, I2L core speed grade | 12.5 | 12.5 | 10.69 | 12.5 | 12.5 | 12.5 |
| | | C3, I3, I3L core speed grade | 12.5 | 12.5 | 10.69 | 12.5 | 10.88 | 10.88 |
| | 3 | C1, C2, C2L, I2, I2L core speed grade | 8.5 Gbps | | | | | |
| | | C3, I3, I3L core speed grade | | | | | | |
| | | C4, I4 core speed grade | | | | | | |
| | | I3YY core speed grade | 10.3125 Gbps | | | | | |

**Notes to Table 26**:

(1) The maximum data rate is in Gbps.

(2) The Phase Compensation FIFO can be configured in FIFO mode or register mode. In the FIFO mode, the pointers are not fixed, and the latency can vary. In the register mode the pointers are fixed for low latency.

Figure 2 shows the differential transmitter output waveform.

**Figure 2. Differential Transmitter Output Waveform**

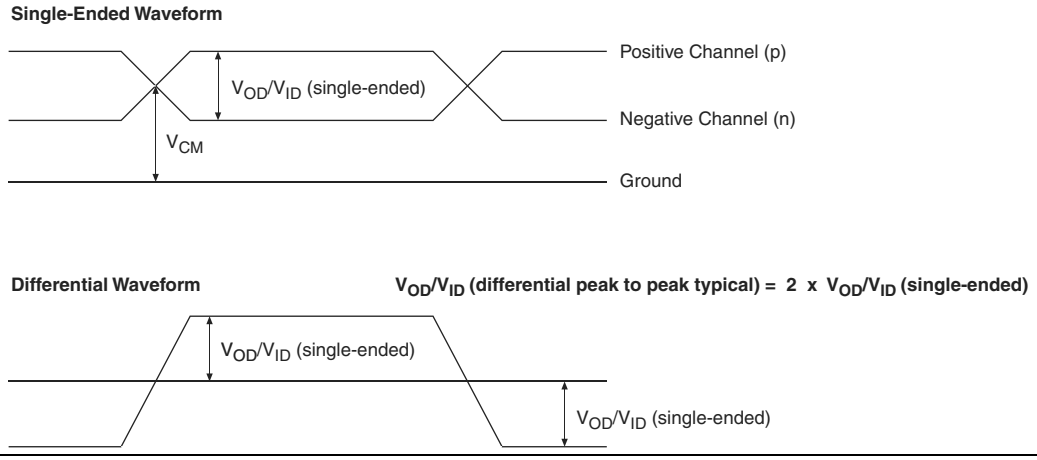



Figure 3 shows the Stratix V AC gain curves for GX channels.

**Figure 3. AC Gain Curves for GX Channels (full bandwidth)**

Stratix V GT devices contain both GX and GT channels. All transceiver specifications for the GX channels not listed in Table 28 are the same as those listed in Table 23.

Table 28 lists the Stratix V GT transceiver specifications.

Table 29 shows the $V_{OD}$ settings for the GT channel.

**Table 29. Typical $V_{OD}$ Setting for GT Channel, TX Termination = 100 Ω**

| Symbol | $V_{OD}$ Setting | $V_{OD}$ Value (mV) |
|---|---|---|
| $V_{OD}$ differential peak to peak typical (1) | 0 | 0 |
| | 1 | 200 |
| | 2 | 400 |
| | 3 | 600 |
| | 4 | 800 |
| | 5 | 1000 |

**Note:**

(1) Refer to Figure 4.

Figure 4 shows the differential transmitter output waveform.

**Figure 4. Differential Transmitter/Receiver Output/Input Waveform**

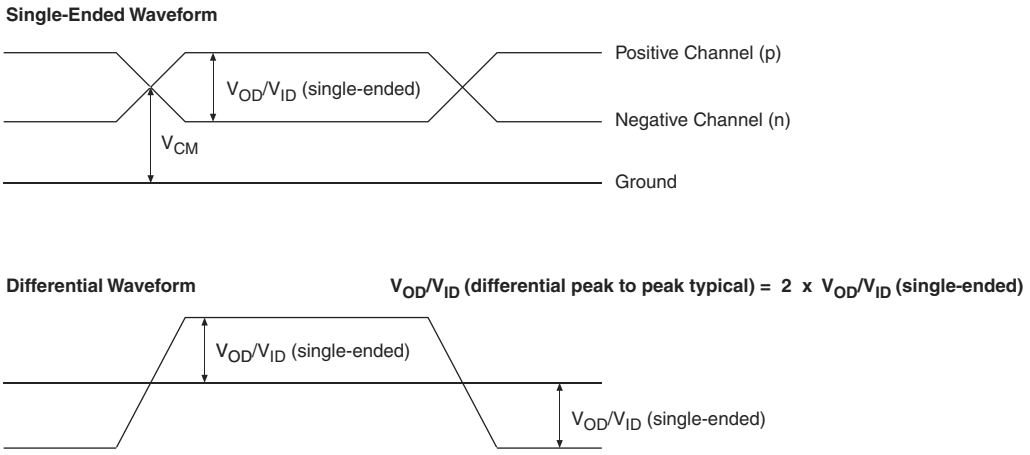



Figure 5 shows the Stratix V AC gain curves for GT channels.

**Figure 5. AC Gain Curves for GT Channels**

Figure 6 shows the Stratix V DC gain curves for GT channels.

**Figure 6. DC Gain Curves for GT Channels**

## Transceiver Characterization

This section summarizes the Stratix V transceiver characterization results for compliance with the following protocols:

- Interlaken
- 40G (XLAUI)/100G (CAUI)
- 10GBase-KR
- QSGMII
- XAUI
- SFI
- Gigabit Ethernet (Gbe / GIGE)
- SPAUI
- Serial Rapid IO (SRIO)
- CPRI
- OBSAI
- Hyper Transport (HT)
- SATA
- SAS
- CEI

- XFI
- ASI
- HiGig/HiGig+
- HiGig2/HiGig2+
- Serial Data Converter (SDC)
- GPON
- SDI
- SONET
- Fibre Channel (FC)
- PCIe
- QPI
- SFF-8431

Download the Stratix V Characterization Report Tool to view the characterization report summary for these protocols.

# Core Performance Specifications

This section describes the clock tree, phase-locked loop (PLL), digital signal processing (DSP), memory blocks, configuration, and JTAG specifications.

## Clock Tree Specifications

Table 30 lists the clock tree specifications for Stratix V devices.

**Table 30. Clock Tree Performance for Stratix V Devices** *(1)*

| Symbol | Performance | | | Unit |
|---|---|---|---|---|
| | C1, C2, C2L, I2, and I2L | C3, I3, I3L, and I3YY | C4, I4 | |
| Global and Regional Clock | 717 | 650 | 580 | MHz |
| Periphery Clock | 550 | 500 | 500 | MHz |

**Note to Table 30:**

(1) The Stratix V ES devices are limited to 600 MHz core clock tree performance.

**Table 36. High-Speed I/O Specifications for Stratix V Devices (1), (2) (Part 4 of 4)**

| Symbol | Conditions | C1 | | | C2, C2L, I2, I2L | | | C3, I3, I3L, I3YY | | | C4,I4 | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| $f_{HSDR}$ (data rate) | SERDES factor J = 3 to 10 | (6) | — | (8) | (6) | — | (8) | (6) | — | (8) | (6) | — | (8) | Mbps |
| | SERDES factor J = 2, uses DDR Registers | (6) | — | (7) | (6) | — | (7) | (6) | — | (7) | (6) | — | (7) | Mbps |
| | SERDES factor J = 1, uses SDR Register | (6) | — | (7) | (6) | — | (7) | (6) | — | (7) | (6) | — | (7) | Mbps |
| **DPA Mode** | | | | | | | | | | | | | | |
| DPA run length | — | — | — | 10000 | — | — | 10000 | — | — | 10000 | — | — | 10000 | UI |
| **Soft CDR mode** | | | | | | | | | | | | | | |
| Soft-CDR PPM tolerance | — | — | — | 300 | — | — | 300 | — | — | 300 | — | — | 300 | ± PPM |
| **Non DPA Mode** | | | | | | | | | | | | | | |
| Sampling Window | — | — | — | 300 | — | — | 300 | — | — | 300 | — | — | 300 | ps |

**Notes to Table 36:**

(1) When J = 3 to 10, use the serializer/deserializer (SERDES) block.

(2) When J = 1 or 2, bypass the SERDES block.

(3) This only applies to DPA and soft-CDR modes.

(4) Clock Boost Factor (W) is the ratio between the input data rate to the input clock rate.

(5) This is achieved by using the **LVDS** clock network.

(6) The minimum specification depends on the clock source (for example, the PLL and clock pin) and the clock routing resource (global, regional, or local) that you use. The I/O differential buffer and input register do not have a minimum toggle rate.

(7) The maximum ideal frequency is the SERDES factor (J) x the PLL maximum output frequency (fOUT) provided you can close the design timing and the signal integrity simulation is clean.

(8) You can estimate the achievable maximum data rate for non-DPA mode by performing link timing closure analysis. You must consider the board skew margin, transmitter delay margin, and receiver sampling margin to determine the maximum data rate supported.

(9) If the receiver with DPA enabled and transmitter are using shared PLLs, the minimum data rate is 150 Mbps.

(10) You must calculate the leftover timing margin in the receiver by performing link timing closure analysis. You must consider the board skew margin, transmitter channel-to-channel skew, and receiver sampling margin to determine leftover timing margin.

(11) The $F_{MAX}$ specification is based on the fast clock used for serial data. The interface $F_{MAX}$ is also dependent on the parallel clock domain which is design-dependent and requires timing analysis.

(12) Stratix V RX LVDS will need DPA. For Stratix V TX LVDS, the receiver side component must have DPA.

(13) Stratix V LVDS serialization and de-serialization factor needs to be x4 and above.

(14) Requires package skew compensation with PCB trace length.

(15) Do not mix single-ended I/O buffer within LVDS I/O bank.

(16) Chip-to-chip communication only with a maximum load of 5 pF.

(17) When using True LVDS RX channels for emulated LVDS TX channel, only serialization factors 1 and 2 are supported.

**Table 40. DQS Phase Offset Delay Per Setting for Stratix V Devices (1), (2) (Part 2 of 2)**

| Speed Grade | Min | Max | Unit |
|---|---|---|---|
| C4,I4 | 8 | 16 | ps |

**Notes to Table 40:**

(1) The typical value equals the average of the minimum and maximum values.

(2) The delay settings are linear with a cumulative delay variation of 40 ps for all speed grades. For example, when using a –2 speed grade and applying a 10-phase offset setting to a 90° phase shift at 400 MHz, the expected average cumulative delay is [625 ps + (10 × 10 ps) ± 20 ps] = 725 ps ± 20 ps.

Table 41 lists the DQS phase shift error for Stratix V devices.

**Table 41. DQS Phase Shift Error Specification for DLL-Delayed Clock ($t_{DQS\_PSERR}$) for Stratix V Devices (1)**

| Number of DQS Delay Buffers | C1 | C2, C2L, I2, I2L | C3, I3, I3L, I3YY | C4,I4 | Unit |
|---|---|---|---|---|---|
| 1 | 28 | 28 | 30 | 32 | ps |
| 2 | 56 | 56 | 60 | 64 | ps |
| 3 | 84 | 84 | 90 | 96 | ps |
| 4 | 112 | 112 | 120 | 128 | ps |

**Notes to Table 41:**

(1) This error specification is the absolute maximum and minimum error. For example, skew on three DQS delay buffers in a –2 speed grade is ±78 ps or ±39 ps.

Table 42 lists the memory output clock jitter specifications for Stratix V devices.

**Table 42. Memory Output Clock Jitter Specification for Stratix V Devices (1), (2), (3) (Part 1 of 2)**

| Clock Network | Parameter | Symbol | C1 | | C2, C2L, I2, I2L | | C3, I3, I3L, I3YY | | C4,I4 | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | Min | Max | Min | Max | Min | Max | Min | Max | |
| Regional | Clock period jitter | $t_{JIT(per)}$ | –50 | 50 | –50 | 50 | –55 | 55 | –55 | 55 | ps |
| | Cycle-to-cycle period jitter | $t_{JIT(cc)}$ | –100 | 100 | –100 | 100 | –110 | 110 | –110 | 110 | ps |
| | Duty cycle jitter | $t_{JIT(duty)}$ | –50 | 50 | –50 | 50 | –82.5 | 82.5 | –82.5 | 82.5 | ps |
| Global | Clock period jitter | $t_{JIT(per)}$ | –75 | 75 | –75 | 75 | –82.5 | 82.5 | –82.5 | 82.5 | ps |
| | Cycle-to-cycle period jitter | $t_{JIT(cc)}$ | –150 | 150 | –150 | 150 | –165 | 165 | –165 | 165 | ps |
| | Duty cycle jitter | $t_{JIT(duty)}$ | –75 | 75 | –75 | 75 | –90 | 90 | –90 | 90 | ps |

**Table 42. Memory Output Clock Jitter Specification for Stratix V Devices (1), (Part 2 of 2) (2), (3)**

| Clock Network | Parameter | Symbol | C1 | | C2, C2L, I2, I2L | | C3, I3, I3L, I3YY | | C4,I4 | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | Min | Max | Min | Max | Min | Max | Min | Max | |
| PHY Clock | Clock period jitter | $t_{JIT(per)}$ | –25 | 25 | –25 | 25 | –30 | 30 | –35 | 35 | ps |
| | Cycle-to-cycle period jitter | $t_{JIT(cc)}$ | –50 | 50 | –50 | 50 | –60 | 60 | –70 | 70 | ps |
| | Duty cycle jitter | $t_{JIT(duty)}$ | –37.5 | 37.5 | –37.5 | 37.5 | –45 | 45 | –56 | 56 | ps |

**Notes to Table 42:**

(1) The clock jitter specification applies to the memory output clock pins generated using differential signal-splitter and DDIO circuits clocked by a PLL output routed on a PHY, regional, or global clock network as specified. Altera recommends using PHY clock networks whenever possible.

(2) The clock jitter specification applies to the memory output clock pins clocked by an integer PLL.

(3) The memory output clock jitter is applicable when an input jitter of 30 ps peak-to-peak is applied with bit error rate (BER) -12, equivalent to 14 sigma.

## OCT Calibration Block Specifications

Table 43 lists the OCT calibration block specifications for Stratix V devices.

**Table 43. OCT Calibration Block Specifications for Stratix V Devices**

| Symbol | Description | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| OCTUSRCLK | Clock required by the OCT calibration blocks | — | — | 20 | MHz |
| $T_{OCTCAL}$ | Number of OCTUSRCLK clock cycles required for OCT $R_S/R_T$ calibration | — | 1000 | — | Cycles |
| $T_{OCTSHIFT}$ | Number of OCTUSRCLK clock cycles required for the OCT code to shift out | — | 32 | — | Cycles |
| $T_{RS\_RT}$ | Time required between the `dyn_term_ctrl` and `oe` signal transitions in a bidirectional I/O buffer to dynamically switch between OCT $R_S$ and $R_T$ (Figure 10) | — | 2.5 | — | ns |

Figure 10 shows the timing diagram for the `oe` and `dyn_term_ctrl` signals.

**Figure 10. Timing Diagram for oe and dyn_term_ctrl Signals**

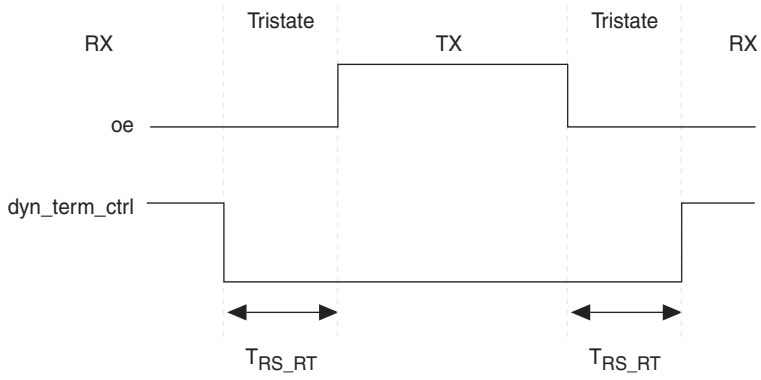


**Table 48. Minimum Configuration Time Estimation for Stratix V Devices**

| Variant | Member Code | Active Serial (1) | | | Fast Passive Parallel (2) | | |
|---|---|---|---|---|---|---|---|
| | | Width | DCLK (MHz) | Min Config Time (s) | Width | DCLK (MHz) | Min Config Time (s) |
| GS | D3 | 4 | 100 | 0.344 | 32 | 100 | 0.043 |
| | D4 | 4 | 100 | 0.534 | 32 | 100 | 0.067 |
| | | 4 | 100 | 0.344 | 32 | 100 | 0.043 |
| | D5 | 4 | 100 | 0.534 | 32 | 100 | 0.067 |
| | D6 | 4 | 100 | 0.741 | 32 | 100 | 0.093 |
| | D8 | 4 | 100 | 0.741 | 32 | 100 | 0.093 |
| E | E9 | 4 | 100 | 0.857 | 32 | 100 | 0.107 |
| | EB | 4 | 100 | 0.857 | 32 | 100 | 0.107 |

**Notes to Table 48:**

(1) DCLK frequency of 100 MHz using external CLKUSR.

(2) Max FPGA FPP bandwidth may exceed bandwidth available from some external storage or control logic.

# Fast Passive Parallel Configuration Timing

This section describes the fast passive parallel (FPP) configuration timing parameters for Stratix V devices.

## DCLK-to-DATA[] Ratio for FPP Configuration

FPP configuration requires a different DCLK-to-DATA[] ratio when you enable the design security, decompression, or both features. Table 49 lists the DCLK-to-DATA[] ratio for each combination.

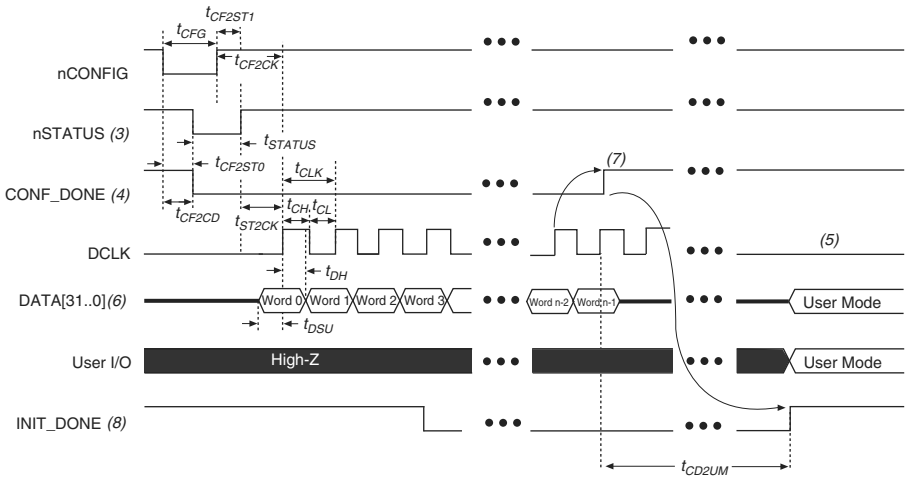
**Table 49. DCLK-to-DATA[] Ratio (1) (Part 1 of 2)**

| Configuration Scheme | Decompression | Design Security | DCLK-to-DATA[] Ratio |
|---|---|---|---|
| FPP ×8 | Disabled | Disabled | 1 |
| | Disabled | Enabled | 1 |
| | Enabled | Disabled | 2 |
| | Enabled | Enabled | 2 |
| FPP ×16 | Disabled | Disabled | 1 |
| | Disabled | Enabled | 2 |
| | Enabled | Disabled | 4 |
| | Enabled | Enabled | 4 |

## FPP Configuration Timing when DCLK-to-DATA [] = 1

Figure 12 shows the timing waveform for FPP configuration when using a MAX II or MAX V device as an external host. This waveform shows timing when the DCLK-to-DATA[] ratio is 1.

**Figure 12. FPP Configuration Timing Waveform When the DCLK-to-DATA[] Ratio is 1** *(1), (2)*




**Notes to Figure 12:**

(1) Use this timing waveform when the DCLK-to-DATA[] ratio is 1.

(2) The beginning of this waveform shows the device in user mode. In user mode, nCONFIG, nSTATUS, and CONF_DONE are at logic-high levels. When nCONFIG is pulled low, a reconfiguration cycle begins.

(3) After power-up, the Stratix V device holds nSTATUS low for the time of the POR delay.

(4) After power-up, before and during configuration, CONF_DONE is low.

(5) Do not leave DCLK floating after configuration. DCLK is ignored after configuration is complete. It can toggle high or low if required.

(6) For FPP ×16, use DATA[15..0]. For FPP ×8, use DATA[7..0]. DATA[31..0] are available as a user I/O pin after configuration. The state of this pin depends on the dual-purpose pin settings.

(7) To ensure a successful configuration, send the entire configuration data to the Stratix V device. CONF_DONE is released high when the Stratix V device receives all the configuration data successfully. After CONF_DONE goes high, send two additional falling edges on DCLK to begin initialization and enter user mode.

(8) After the option bit to enable the INIT_DONE pin is configured into the device, the INIT_DONE goes low.

Table 51 lists the timing parameters for Stratix V devices for FPP configuration when the DCLK-to-DATA[] ratio is more than 1.

**Table 51. FPP Timing Parameters for Stratix V Devices When the DCLK-to-DATA[] Ratio is >1 (1)**

| Symbol | Parameter | Minimum | Maximum | Units |
|---|---|---|---|---|
| $t_{CF2CD}$ | nCONFIG low to CONF_DONE low | — | 600 | ns |
| $t_{CF2ST0}$ | nCONFIG low to nSTATUS low | — | 600 | ns |
| $t_{CFG}$ | nCONFIG low pulse width | 2 | — | µs |
| $t_{STATUS}$ | nSTATUS low pulse width | 268 | 1,506 (2) | µs |
| $t_{CF2ST1}$ | nCONFIG high to nSTATUS high | — | 1,506 (2) | µs |
| $t_{CF2CK}$ (5) | nCONFIG high to first rising edge on DCLK | 1,506 | — | µs |
| $t_{ST2CK}$ (5) | nSTATUS high to first rising edge of DCLK | 2 | — | µs |
| $t_{DSU}$ | DATA[] setup time before rising edge on DCLK | 5.5 | — | ns |
| $t_{DH}$ | DATA[] hold time after rising edge on DCLK | N–1/$f_{DCLK}$ (5) | — | s |
| $t_{CH}$ | DCLK high time | 0.45 × 1/$f_{MAX}$ | — | s |
| $t_{CL}$ | DCLK low time | 0.45 × 1/$f_{MAX}$ | — | s |
| $t_{CLK}$ | DCLK period | 1/$f_{MAX}$ | — | s |
| $f_{MAX}$ | DCLK frequency (FPP ×8/×16) | — | 125 | MHz |
| | DCLK frequency (FPP ×32) | — | 100 | MHz |
| $t_R$ | Input rise time | — | 40 | ns |
| $t_F$ | Input fall time | — | 40 | ns |
| $t_{CD2UM}$ | CONF_DONE high to user mode (3) | 175 | 437 | µs |
| $t_{CD2CU}$ | CONF_DONE high to CLKUSR enabled | 4 × maximum DCLK period | — | — |
| $t_{CD2UMC}$ | CONF_DONE high to user mode with CLKUSR option on | $t_{CD2CU}$ + (8576 × CLKUSR period) (4) | — | — |

**Notes to Table 51:**

(1) Use these timing parameters when you use the decompression and design security features.

(2) You can obtain this value if you do not delay configuration by extending the nCONFIG or nSTATUS low pulse width.

(3) The minimum and maximum numbers apply only if you use the internal oscillator as the clock source for initializing the device.

(4) To enable the CLKUSR pin as the initialization clock source and to obtain the maximum frequency specification on these pins, refer to the Initialization section of the "Configuration, Design Security, and Remote System Upgrades in Stratix V Devices" chapter.

(5) N is the DCLK-to-DATA ratio and $f_{DCLK}$ is the DCLK frequency the system is operating.

(6) If nSTATUS is monitored, follow the $t_{ST2CK}$ specification. If nSTATUS is not monitored, follow the $t_{CF2CK}$ specification.

**Table 61. Document Revision History (Part 2 of 3)**

| Date | Version | Changes |
|---|---|---|
| November 2014 | 3.3 | ■ Added the I3YY speed grade and changed the data rates for the GX channel in Table 1.<br>■ Added the I3YY speed grade to the $V_{CC}$ description in Table 6.<br>■ Added the I3YY speed grade to $V_{CCHIP\_L}$, $V_{CCHIP\_R}$, $V_{CCHSSI\_L}$, and $V_{CCHSSI\_R}$ descriptions in Table 7.<br>■ Added 240-Ω to Table 11.<br>■ Changed CDR PPM tolerance in Table 23.<br>■ Added additional max data rate for fPLL in Table 23.<br>■ Added the I3YY speed grade and changed the data rates for transceiver speed grade 3 in Table 25.<br>■ Added the I3YY speed grade and changed the data rates for transceiver speed grade 3 in Table 26.<br>■ Changed CDR PPM tolerance in Table 28.<br>■ Added additional max data rate for fPLL in Table 28.<br>■ Changed the mode descriptions for MLAB and M20K in Table 33.<br>■ Changed the Max value of $f_{HSCLK\_OUT}$ for the C2, C2L, I2, I2L speed grades in Table 36.<br>■ Changed the frequency ranges for C1 and C2 in Table 39.<br>■ Changed the **.rbf** file sizes for 5SGSD6 and 5SGSD8 in Table 47.<br>■ Added note about `nSTATUS` to Table 50, Table 51, Table 54.<br>■ Changed the available settings in Table 58.<br>■ Changed the note in “Periphery Performance”.<br>■ Updated the “I/O Standard Specifications” section.<br>■ Updated the “Raw Binary File Size” section.<br>■ Updated the receiver voltage input range in Table 22.<br>■ Updated the max frequency for the LVDS clock network in Table 36.<br>■ Updated the `DCLK` note to Figure 11.<br>■ Updated Table 23 $VO_{CM}$ (DC Coupled) condition.<br>■ Updated Table 6 and Table 7.<br>■ Added the `DCLK` specification to Table 55.<br>■ Updated the notes for Table 47.<br>■ Updated the list of parameters for Table 56. |
| November 2013 | 3.2 | ■ Updated Table 28 |
| November 2013 | 3.1 | ■ Updated Table 33 |
| November 2013 | 3.0 | ■ Updated Table 23 and Table 28 |
| October 2013 | 2.9 | ■ Updated the “Transceiver Characterization” section |
| October 2013 | 2.8 | ■ Updated Table 3, Table 12, Table 14, Table 19, Table 20, Table 23, Table 24, Table 28, Table 30, Table 31, Table 32, Table 33, Table 36, Table 39, Table 40, Table 41, Table 42, Table 47, Table 53, Table 58, and Table 59<br>■ Added Figure 1 and Figure 3<br>■ Added the “Transceiver Characterization” section<br>■ Removed all “Preliminary” designations. |