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## Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

## Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

| Details | |
|---|---|
| Product Status | Obsolete |
| Number of LABs/CLBs | 359200 |
| Number of Logic Elements/Cells | 952000 |
| Total RAM Bits | 53248000 |
| Number of I/O | 840 |
| Number of Gates | - |
| Voltage - Supply | 0.82V ~ 0.88V |
| Mounting Type | Surface Mount |
| Operating Temperature | 0°C ~ 85°C (TJ) |
| Package / Case | 1932-BBGA, FCBGA |
| Supplier Device Package | 1932-FBGA, FC (45x45) |
| Purchase URL | https://www.e-xfl.com/product-detail/intel/5sgxeabn2f45c3n |

**Table 7. Recommended Transceiver Power Supply Operating Conditions for Stratix V GX, GS, and GT Devices (Part 2 of 2)**

| Symbol | Description | Devices | Minimum (4) | Typical | Maximum (4) | Unit |
|---|---|---|---|---|---|---|
| $V_{CCR\_GXBR}$ (2) | Receiver analog power supply (right side) | GX, GS, GT | 0.82 | 0.85 | 0.88 | V |
| | | | 0.87 | 0.90 | 0.93 | |
| | | | 0.97 | 1.0 | 1.03 | |
| | | | 1.03 | 1.05 | 1.07 | |
| $V_{CCR\_GTBR}$ | Receiver analog power supply for GT channels (right side) | GT | 1.02 | 1.05 | 1.08 | V |
| $V_{CCT\_GXBL}$ (2) | Transmitter analog power supply (left side) | GX, GS, GT | 0.82 | 0.85 | 0.88 | V |
| | | | 0.87 | 0.90 | 0.93 | |
| | | | 0.97 | 1.0 | 1.03 | |
| | | | 1.03 | 1.05 | 1.07 | |
| $V_{CCT\_GXBR}$ (2) | Transmitter analog power supply (right side) | GX, GS, GT | 0.82 | 0.85 | 0.88 | V |
| | | | 0.87 | 0.90 | 0.93 | |
| | | | 0.97 | 1.0 | 1.03 | |
| | | | 1.03 | 1.05 | 1.07 | |
| $V_{CCT\_GTBR}$ | Transmitter analog power supply for GT channels (right side) | GT | 1.02 | 1.05 | 1.08 | V |
| $V_{CCL\_GTBR}$ | Transmitter clock network power supply | GT | 1.02 | 1.05 | 1.08 | V |
| $V_{CCH\_GXBL}$ | Transmitter output buffer power supply (left side) | GX, GS, GT | 1.425 | 1.5 | 1.575 | V |
| $V_{CCH\_GXBR}$ | Transmitter output buffer power supply (right side) | GX, GS, GT | 1.425 | 1.5 | 1.575 | V |

**Notes to Table 7:**

(1) This supply must be connected to 3.0 V if the CMU PLL, receiver CDR, or both, are configured at a base data rate > 6.5 Gbps. Up to 6.5 Gbps, you can connect this supply to either 3.0 V or 2.5 V.

(2) Refer to Table 8 to select the correct power supply level for your design.

(3) When using ATX PLLs, the supply must be 3.0 V.

(4) This value describes the budget for the DC (static) power supply tolerance and does not include the dynamic tolerance requirements. Refer to the PDN tool for the additional budget for the dynamic tolerance requirements.

**Table 12. OCT Without Calibration Resistance Tolerance Specifications for Stratix V Devices (Part 2 of 2)**

| Symbol | Description | Conditions | Resistance Tolerance | | | | Unit |
|---|---|---|---|---|---|---|---|
| | | | C1 | C2,I2 | C3, I3, I3YY | C4, I4 | |
| 50-Ω $R_S$ | Internal series termination without calibration (50-Ω setting) | $V_{CCIO}$ = 1.8 and 1.5 V | ±30 | ±30 | ±40 | ±40 | % |
| 50-Ω $R_S$ | Internal series termination without calibration (50-Ω setting) | $V_{CCIO}$ = 1.2 V | ±35 | ±35 | ±50 | ±50 | % |
| 100-Ω $R_D$ | Internal differential termination (100-Ω setting) | $V_{CCPD}$ = 2.5 V | ±25 | ±25 | ±25 | ±25 | % |

Calibration accuracy for the calibrated series and parallel OCTs are applicable at the moment of calibration. When voltage and temperature conditions change after calibration, the tolerance may change.

OCT calibration is automatically performed at power-up for OCT-enabled I/Os. Table 13 lists the OCT variation with temperature and voltage after power-up calibration. Use Table 13 to determine the OCT variation after power-up calibration and Equation 1 to determine the OCT variation without recalibration.

**Equation 1. OCT Variation Without Recalibration for Stratix V Devices** *(1), (2), (3), (4), (5), (6)*

$$R_{OCT} = R_{SCAL}\left(1 + \langle\frac{dR}{dT} \times \Delta T\rangle \pm \langle\frac{dR}{dV} \times \Delta V\rangle\right)$$

**Notes to Equation 1:**

(1) The $R_{OCT}$ value shows the range of OCT resistance with the variation of temperature and $V_{CCIO}$.
(2) $R_{SCAL}$ is the OCT resistance value at power-up.
(3) $\Delta T$ is the variation of temperature with respect to the temperature at power-up.
(4) $\Delta V$ is the variation of voltage with respect to the $V_{CCIO}$ at power-up.
(5) dR/dT is the percentage change of $R_{SCAL}$ with temperature.
(6) dR/dV is the percentage change of $R_{SCAL}$ with voltage.

Table 13 lists the on-chip termination variation after power-up calibration.

**Table 13. OCT Variation after Power-Up Calibration for Stratix V Devices (Part 1 of 2)** *(1)*

| Symbol | Description | $V_{CCIO}$ (V) | Typical | Unit |
|---|---|---|---|---|
| dR/dV | OCT variation with voltage without recalibration | 3.0 | 0.0297 | %/mV |
| | | 2.5 | 0.0344 | |
| | | 1.8 | 0.0499 | |
| | | 1.5 | 0.0744 | |
| | | 1.2 | 0.1241 | |

**Table 13. OCT Variation after Power-Up Calibration for Stratix V Devices (Part 2 of 2) (1)**

| Symbol | Description | $V_{CCIO}$ (V) | Typical | Unit |
|---|---|---|---|---|
| dR/dT | OCT variation with temperature without recalibration | 3.0 | 0.189 | %/°C |
| | | 2.5 | 0.208 | |
| | | 1.8 | 0.266 | |
| | | 1.5 | 0.273 | |
| | | 1.2 | 0.317 | |

**Note to Table 13:**

(1) Valid for a $V_{CCIO}$ range of ±5% and a temperature range of 0° to 85°C.

### Pin Capacitance

Table 14 lists the Stratix V device family pin capacitance.

**Table 14. Pin Capacitance for Stratix V Devices**

| Symbol | Description | Value | Unit |
|---|---|---|---|
| $C_{IOTB}$ | Input capacitance on the top and bottom I/O pins | 6 | pF |
| $C_{IOLR}$ | Input capacitance on the left and right I/O pins | 6 | pF |
| $C_{OUTFB}$ | Input capacitance on dual-purpose clock output and feedback pins | 6 | pF |

### Hot Socketing

Table 15 lists the hot socketing specifications for Stratix V devices.

**Table 15. Hot Socketing Specifications for Stratix V Devices**

| Symbol | Description | Maximum |
|---|---|---|
| $I_{IOPIN\ (DC)}$ | DC current per I/O pin | 300 µA |
| $I_{IOPIN\ (AC)}$ | AC current per I/O pin | 8 mA (1) |
| $I_{XCVR\text{-}TX\ (DC)}$ | DC current per transceiver transmitter pin | 100 mA |
| $I_{XCVR\text{-}RX\ (DC)}$ | DC current per transceiver receiver pin | 50 mA |

**Note to Table 15:**

(1) The I/O ramp rate is 10 ns or more. For ramp rates faster than 10 ns, $|I_{IOPIN}| = C\ dv/dt$, in which C is the I/O pin capacitance and dv/dt is the slew rate.

**Table 18. Single-Ended SSTL, HSTL, and HSUL I/O Reference Voltage Specifications for Stratix V Devices**

| I/O Standard | $V_{CCIO}$ (V) | | | $V_{REF}$ (V) | | | $V_{TT}$ (V) | | |
|---|---|---|---|---|---|---|---|---|---|
| | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max |
| SSTL-2 Class I, II | 2.375 | 2.5 | 2.625 | 0.49 * $V_{CCIO}$ | 0.5 * $V_{CCIO}$ | 0.51 * $V_{CCIO}$ | $V_{REF}$ – 0.04 | $V_{REF}$ | $V_{REF}$ + 0.04 |
| SSTL-18 Class I, II | 1.71 | 1.8 | 1.89 | 0.833 | 0.9 | 0.969 | $V_{REF}$ – 0.04 | $V_{REF}$ | $V_{REF}$ + 0.04 |
| SSTL-15 Class I, II | 1.425 | 1.5 | 1.575 | 0.49 * $V_{CCIO}$ | 0.5 * $V_{CCIO}$ | 0.51 * $V_{CCIO}$ | 0.49 * $V_{CCIO}$ | 0.5 * VCCIO | 0.51 * $V_{CCIO}$ |
| SSTL-135 Class I, II | 1.283 | 1.35 | 1.418 | 0.49 * $V_{CCIO}$ | 0.5 * $V_{CCIO}$ | 0.51 * $V_{CCIO}$ | 0.49 * $V_{CCIO}$ | 0.5 * $V_{CCIO}$ | 0.51 * $V_{CCIO}$ |
| SSTL-125 Class I, II | 1.19 | 1.25 | 1.26 | 0.49 * $V_{CCIO}$ | 0.5 * $V_{CCIO}$ | 0.51 * $V_{CCIO}$ | 0.49 * $V_{CCIO}$ | 0.5 * VCCIO | 0.51 * $V_{CCIO}$ |
| SSTL-12 Class I, II | 1.14 | 1.20 | 1.26 | 0.49 * $V_{CCIO}$ | 0.5 * $V_{CCIO}$ | 0.51 * $V_{CCIO}$ | 0.49 * $V_{CCIO}$ | 0.5 * VCCIO | 0.51 * $V_{CCIO}$ |
| HSTL-18 Class I, II | 1.71 | 1.8 | 1.89 | 0.85 | 0.9 | 0.95 | — | $V_{CCIO}$/2 | — |
| HSTL-15 Class I, II | 1.425 | 1.5 | 1.575 | 0.68 | 0.75 | 0.9 | — | $V_{CCIO}$/2 | — |
| HSTL-12 Class I, II | 1.14 | 1.2 | 1.26 | 0.47 * $V_{CCIO}$ | 0.5 * $V_{CCIO}$ | 0.53 * $V_{CCIO}$ | — | $V_{CCIO}$/2 | — |
| HSUL-12 | 1.14 | 1.2 | 1.3 | 0.49 * $V_{CCIO}$ | 0.5 * $V_{CCIO}$ | 0.51 * $V_{CCIO}$ | — | — | — |

**Table 19. Single-Ended SSTL, HSTL, and HSUL I/O Standards Signal Specifications for Stratix V Devices (Part 1 of 2)**

| I/O Standard | $V_{IL(DC)}$ (V) | | $V_{IH(DC)}$ (V) | | $V_{IL(AC)}$ (V) | $V_{IH(AC)}$ (V) | $V_{OL}$ (V) | $V_{OH}$ (V) | $I_{ol}$ (mA) | $I_{oh}$ (mA) |
|---|---|---|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Max | Min | Max | Min | | |
| SSTL-2 Class I | –0.3 | $V_{REF}$ – 0.15 | $V_{REF}$ + 0.15 | $V_{CCIO}$ + 0.3 | $V_{REF}$ – 0.31 | $V_{REF}$ + 0.31 | $V_{TT}$ – 0.608 | $V_{TT}$ + 0.608 | 8.1 | –8.1 |
| SSTL-2 Class II | –0.3 | $V_{REF}$ – 0.15 | $V_{REF}$ + 0.15 | $V_{CCIO}$ + 0.3 | $V_{REF}$ – 0.31 | $V_{REF}$ + 0.31 | $V_{TT}$ – 0.81 | $V_{TT}$ + 0.81 | 16.2 | –16.2 |
| SSTL-18 Class I | –0.3 | $V_{REF}$ – 0.125 | $V_{REF}$ + 0.125 | $V_{CCIO}$ + 0.3 | $V_{REF}$ – 0.25 | $V_{REF}$ + 0.25 | $V_{TT}$ – 0.603 | $V_{TT}$ + 0.603 | 6.7 | –6.7 |
| SSTL-18 Class II | –0.3 | $V_{REF}$ – 0.125 | $V_{REF}$ + 0.125 | $V_{CCIO}$ + 0.3 | $V_{REF}$ – 0.25 | $V_{REF}$ + 0.25 | 0.28 | $V_{CCIO}$ – 0.28 | 13.4 | –13.4 |
| SSTL-15 Class I | — | $V_{REF}$ – 0.1 | $V_{REF}$ + 0.1 | — | $V_{REF}$ – 0.175 | $V_{REF}$ + 0.175 | 0.2 * $V_{CCIO}$ | 0.8 * $V_{CCIO}$ | 8 | –8 |
| SSTL-15 Class II | — | $V_{REF}$ – 0.1 | $V_{REF}$ + 0.1 | — | $V_{REF}$ – 0.175 | $V_{REF}$ + 0.175 | 0.2 * $V_{CCIO}$ | 0.8 * $V_{CCIO}$ | 16 | –16 |
| SSTL-135 Class I, II | — | $V_{REF}$ – 0.09 | $V_{REF}$ + 0.09 | — | $V_{REF}$ – 0.16 | $V_{REF}$ + 0.16 | 0.2 * $V_{CCIO}$ | 0.8 * $V_{CCIO}$ | — | — |
| SSTL-125 Class I, II | — | $V_{REF}$ – 0.85 | $V_{REF}$ + 0.85 | — | $V_{REF}$ – 0.15 | $V_{REF}$ + 0.15 | 0.2 * $V_{CCIO}$ | 0.8 * $V_{CCIO}$ | — | — |
| SSTL-12 Class I, II | — | $V_{REF}$ – 0.1 | $V_{REF}$ + 0.1 | — | $V_{REF}$ – 0.15 | $V_{REF}$ + 0.15 | 0.2 * $V_{CCIO}$ | 0.8 * $V_{CCIO}$ | — | — |

**Table 19. Single-Ended SSTL, HSTL, and HSUL I/O Standards Signal Specifications for Stratix V Devices (Part 2 of 2)**

| I/O Standard | $V_{IL(DC)}$ (V) | | $V_{IH(DC)}$ (V) | | $V_{IL(AC)}$ (V) | $V_{IH(AC)}$ (V) | $V_{OL}$ (V) | $V_{OH}$ (V) | $I_{ol}$ (mA) | $I_{oh}$ (mA) |
|---|---|---|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Max | Min | Max | Min | | |
| HSTL-18 Class I | — | $V_{REF}$ – 0.1 | $V_{REF}$ + 0.1 | — | $V_{REF}$ – 0.2 | $V_{REF}$ + 0.2 | 0.4 | $V_{CCIO}$ – 0.4 | 8 | –8 |
| HSTL-18 Class II | — | $V_{REF}$ – 0.1 | $V_{REF}$ + 0.1 | — | $V_{REF}$ – 0.2 | $V_{REF}$ + 0.2 | 0.4 | $V_{CCIO}$ – 0.4 | 16 | –16 |
| HSTL-15 Class I | — | $V_{REF}$ – 0.1 | $V_{REF}$ + 0.1 | — | $V_{REF}$ – 0.2 | $V_{REF}$ + 0.2 | 0.4 | $V_{CCIO}$ – 0.4 | 8 | –8 |
| HSTL-15 Class II | — | $V_{REF}$ – 0.1 | $V_{REF}$ + 0.1 | — | $V_{REF}$ – 0.2 | $V_{REF}$ + 0.2 | 0.4 | $V_{CCIO}$ – 0.4 | 16 | –16 |
| HSTL-12 Class I | –0.15 | $V_{REF}$ – 0.08 | $V_{REF}$ + 0.08 | $V_{CCIO}$ + 0.15 | $V_{REF}$ – 0.15 | $V_{REF}$ + 0.15 | 0.25* $V_{CCIO}$ | 0.75* $V_{CCIO}$ | 8 | –8 |
| HSTL-12 Class II | –0.15 | $V_{REF}$ – 0.08 | $V_{REF}$ + 0.08 | $V_{CCIO}$ + 0.15 | $V_{REF}$ – 0.15 | $V_{REF}$ + 0.15 | 0.25* $V_{CCIO}$ | 0.75* $V_{CCIO}$ | 16 | –16 |
| HSUL-12 | — | $V_{REF}$ – 0.13 | $V_{REF}$ + 0.13 | — | $V_{REF}$ – 0.22 | $V_{REF}$ + 0.22 | 0.1* $V_{CCIO}$ | 0.9* $V_{CCIO}$ | — | — |

**Table 20. Differential SSTL I/O Standards for Stratix V Devices**

| I/O Standard | $V_{CCIO}$ (V) | | | $V_{SWING(DC)}$ (V) | | $V_{X(AC)}$ (V) | | | $V_{SWING(AC)}$ (V) | |
|---|---|---|---|---|---|---|---|---|---|---|
| | Min | Typ | Max | Min | Max | Min | Typ | Max | Min | Max |
| SSTL-2 Class I, II | 2.375 | 2.5 | 2.625 | 0.3 | $V_{CCIO}$ + 0.6 | $V_{CCIO}/2$ – 0.2 | — | $V_{CCIO}/2$ + 0.2 | 0.62 | $V_{CCIO}$ + 0.6 |
| SSTL-18 Class I, II | 1.71 | 1.8 | 1.89 | 0.25 | $V_{CCIO}$ + 0.6 | $V_{CCIO}/2$ – 0.175 | — | $V_{CCIO}/2$ + 0.175 | 0.5 | $V_{CCIO}$ + 0.6 |
| SSTL-15 Class I, II | 1.425 | 1.5 | 1.575 | 0.2 | *(1)* | $V_{CCIO}/2$ – 0.15 | — | $V_{CCIO}/2$ + 0.15 | 0.35 | — |
| SSTL-135 Class I, II | 1.283 | 1.35 | 1.45 | 0.2 | *(1)* | $V_{CCIO}/2$ – 0.15 | $V_{CCIO}/2$ | $V_{CCIO}/2$ + 0.15 | $2(V_{IH(AC)} - V_{REF})$ | $2(V_{IL(AC)} - V_{REF})$ |
| SSTL-125 Class I, II | 1.19 | 1.25 | 1.31 | 0.18 | *(1)* | $V_{CCIO}/2$ – 0.15 | $V_{CCIO}/2$ | $V_{CCIO}/2$ + 0.15 | $2(V_{IH(AC)} - V_{REF})$ | — |
| SSTL-12 Class I, II | 1.14 | 1.2 | 1.26 | 0.18 | — | $V_{REF}$ –0.15 | $V_{CCIO}/2$ | $V_{REF}$ + 0.15 | –0.30 | 0.30 |

**Note to Table 20:**

(1) The maximum value for $V_{SWING(DC)}$ is not defined. However, each single-ended signal needs to be within the respective single-ended limits ($V_{IH(DC)}$ and $V_{IL(DC)}$).

**Table 21. Differential HSTL and HSUL I/O Standards for Stratix V Devices (Part 1 of 2)**

| I/O Standard | $V_{CCIO}$ (V) | | | $V_{DIF(DC)}$ (V) | | $V_{X(AC)}$ (V) | | | $V_{CM(DC)}$ (V) | | | $V_{DIF(AC)}$ (V) | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | Min | Typ | Max | Min | Max | Min | Typ | Max | Min | Typ | Max | Min | Max |
| HSTL-18 Class I, II | 1.71 | 1.8 | 1.89 | 0.2 | — | 0.78 | — | 1.12 | 0.78 | — | 1.12 | 0.4 | — |
| HSTL-15 Class I, II | 1.425 | 1.5 | 1.575 | 0.2 | — | 0.68 | — | 0.9 | 0.68 | — | 0.9 | 0.4 | — |

**Table 21. Differential HSTL and HSUL I/O Standards for Stratix V Devices (Part 2 of 2)**

| I/O Standard | $V_{CCIO}$ (V) | | | $V_{DIF(DC)}$ (V) | | $V_{X(AC)}$ (V) | | | $V_{CM(DC)}$ (V) | | | $V_{DIF(AC)}$ (V) | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | Min | Typ | Max | Min | Max | Min | Typ | Max | Min | Typ | Max | Min | Max |
| HSTL-12 Class I, II | 1.14 | 1.2 | 1.26 | 0.16 | $V_{CCIO}$ + 0.3 | — | 0.5* $V_{CCIO}$ | — | 0.4* $V_{CCIO}$ | 0.5* $V_{CCIO}$ | 0.6* $V_{CCIO}$ | 0.3 | $V_{CCIO}$ + 0.48 |
| HSUL-12 | 1.14 | 1.2 | 1.3 | 0.26 | 0.26 | 0.5*$V_{CCIO}$ – 0.12 | 0.5* $V_{CCIO}$ | 0.5*$V_{CCIO}$ + 0.12 | 0.4* $V_{CCIO}$ | 0.5* $V_{CCIO}$ | 0.6* $V_{CCIO}$ | 0.44 | 0.44 |

**Table 22. Differential I/O Standard Specifications for Stratix V Devices (7)**

| I/O Standard | $V_{CCIO}$ (V) (10) | | | $V_{ID}$ (mV) (8) | | | $V_{ICM(DC)}$ (V) | | | $V_{OD}$ (V) (6) | | | $V_{OCM}$ (V) (6) | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | Min | Typ | Max | Min | Condition | Max | Min | Condition | Max | Min | Typ | Max | Min | Typ | Max |
| PCML | Transmitter, receiver, and input reference clock pins of the high-speed transceivers use the PCML I/O standard. For transmitter, receiver, and reference clock I/O pin specifications, refer to Table 23 on page 18. | | | | | | | | | | | | | | |
| 2.5 V LVDS (1) | 2.375 | 2.5 | 2.625 | 100 | $V_{CM}$ = 1.25 V | — | 0.05 | $D_{MAX} \leq$ 700 Mbps | 1.8 | 0.247 | — | 0.6 | 1.125 | 1.25 | 1.375 |
| | | | | | | — | 1.05 | $D_{MAX} >$ 700 Mbps | 1.55 | 0.247 | — | 0.6 | 1.125 | 1.25 | 1.375 |
| BLVDS (5) | 2.375 | 2.5 | 2.625 | 100 | — | — | — | — | — | — | — | — | — | — | — |
| RSDS (HIO) (2) | 2.375 | 2.5 | 2.625 | 100 | $V_{CM}$ = 1.25 V | — | 0.3 | — | 1.4 | 0.1 | 0.2 | 0.6 | 0.5 | 1.2 | 1.4 |
| Mini-LVDS (HIO) (3) | 2.375 | 2.5 | 2.625 | 200 | — | 600 | 0.4 | — | 1.325 | 0.25 | — | 0.6 | 1 | 1.2 | 1.4 |
| LVPECL (4), (9) | — | — | — | 300 | — | — | 0.6 | $D_{MAX} \leq$ 700 Mbps | 1.8 | — | — | — | — | — | — |
| | — | — | — | 300 | — | — | 1 | $D_{MAX} >$ 700 Mbps | 1.6 | — | — | — | — | — | — |

**Notes to Table 22:**

(1) For optimized LVDS receiver performance, the receiver voltage input range must be between 1.0 V to 1.6 V for data rates above 700 Mbps, and 0 V to 1.85 V for data rates below 700 Mbps.

(2) For optimized RSDS receiver performance, the receiver voltage input range must be between 0.25 V to 1.45 V.

(3) For optimized Mini-LVDS receiver performance, the receiver voltage input range must be between 0.3 V to 1.425 V.

(4) For optimized LVPECL receiver performance, the receiver voltage input range must be between 0.85 V to 1.75 V for data rate above 700 Mbps and 0.45 V to 1.95 V for data rate below 700 Mbps.

(5) There are no fixed $V_{ICM}$, $V_{OD}$, and $V_{OCM}$ specifications for BLVDS. They depend on the system topology.

(6) RL range: $90 \leq RL \leq 110\ \Omega$ .

(7) The 1.4-V and 1.5-V PCML transceiver I/O standard specifications are described in "Transceiver Performance Specifications" on page 18.

(8) The minimum VID value is applicable over the entire common mode range, VCM.

(9) LVPECL is only supported on dedicated clock input pins.

(10) Differential inputs are powered by VCCPD which requires 2.5 V.

## Power Consumption

Altera offers two ways to estimate power consumption for a design—the Excel-based Early Power Estimator and the Quartus® II PowerPlay Power Analyzer feature.

# Switching Characteristics

This section provides performance characteristics of the Stratix V core and periphery blocks.

These characteristics can be designated as Preliminary or Final.

- Preliminary characteristics are created using simulation results, process data, and other known parameters. The title of these tables show the designation as "Preliminary."
- Final numbers are based on actual silicon characterization and testing. The numbers reflect the actual performance of the device under worst-case silicon process, voltage, and junction temperature conditions. There are no designations on finalized tables.

## Transceiver Performance Specifications

This section describes transceiver performance specifications.

Table 23 lists the Stratix V GX and GS transceiver specifications.

**Table 23. Transceiver Specifications for Stratix V GX and GS Devices (1) (Part 1 of 7)**

| Symbol/ Description | Conditions | Transceiver Speed Grade 1 | | | Transceiver Speed Grade 2 | | | Transceiver Speed Grade 3 | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| **Reference Clock** | | | | | | | | | | | |
| Supported I/O Standards | Dedicated reference clock pin | 1.2-V PCML, 1.4-V PCML, 1.5-V PCML, 2.5-V PCML, Differential LVPECL, LVDS, and HCSL | | | | | | | | | |
| | RX reference clock pin | 1.4-V PCML, 1.5-V PCML, 2.5-V PCML, LVPECL, and LVDS | | | | | | | | | |
| Input Reference Clock Frequency (CMU PLL) (8) | — | 40 | — | 710 | 40 | — | 710 | 40 | — | 710 | MHz |
| Input Reference Clock Frequency (ATX PLL) (8) | — | 100 | — | 710 | 100 | — | 710 | 100 | — | 710 | MHz |
| Rise time | Measure at ±60 mV of differential signal (26) | — | — | 400 | — | — | 400 | — | — | 400 | ps |
| Fall time | Measure at ±60 mV of differential signal (26) | — | — | 400 | — | — | 400 | — | — | 400 | |
| Duty cycle | — | 45 | — | 55 | 45 | — | 55 | 45 | — | 55 | % |
| Spread-spectrum modulating clock frequency | PCI Express® (PCIe®) | 30 | — | 33 | 30 | — | 33 | 30 | — | 33 | kHz |

**Table 23. Transceiver Specifications for Stratix V GX and GS Devices (1) (Part 2 of 7)**

| Symbol/ Description | Conditions | Transceiver Speed Grade 1 | | | Transceiver Speed Grade 2 | | | Transceiver Speed Grade 3 | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| Spread-spectrum downspread | PCIe | — | 0 to –0.5 | — | — | 0 to –0.5 | — | — | 0 to –0.5 | — | % |
| On-chip termination resistors (21) | — | — | 100 | — | — | 100 | — | — | 100 | — | Ω |
| Absolute $V_{MAX}$ (5) | Dedicated reference clock pin | — | — | 1.6 | — | — | 1.6 | — | — | 1.6 | V |
| | RX reference clock pin | — | — | 1.2 | — | — | 1.2 | — | — | 1.2 | |
| Absolute $V_{MIN}$ | — | –0.4 | — | — | –0.4 | — | — | –0.4 | — | — | V |
| Peak-to-peak differential input voltage | — | 200 | — | 1600 | 200 | — | 1600 | 200 | — | 1600 | mV |
| $V_{ICM}$ (AC coupled) (3) | Dedicated reference clock pin | 1050/1000/900/850 (2) | | | 1050/1000/900/850 (2) | | | 1050/1000/900/850 (2) | | | mV |
| | RX reference clock pin | 1.0/0.9/0.85 (4) | | | 1.0/0.9/0.85 (4) | | | 1.0/0.9/0.85 (4) | | | V |
| $V_{ICM}$ (DC coupled) | HCSL I/O standard for PCIe reference clock | 250 | — | 550 | 250 | — | 550 | 250 | — | 550 | mV |
| Transmitter REFCLK Phase Noise (622 MHz) (20) | 100 Hz | — | — | -70 | — | — | -70 | — | — | -70 | dBc/Hz |
| | 1 kHz | — | — | -90 | — | — | -90 | — | — | -90 | dBc/Hz |
| | 10 kHz | — | — | -100 | — | — | -100 | — | — | -100 | dBc/Hz |
| | 100 kHz | — | — | -110 | — | — | -110 | — | — | -110 | dBc/Hz |
| | ≥1 MHz | — | — | -120 | — | — | -120 | — | — | -120 | dBc/Hz |
| Transmitter REFCLK Phase Jitter (100 MHz) (17) | 10 kHz to 1.5 MHz (PCIe) | — | — | 3 | — | — | 3 | — | — | 3 | ps (rms) |
| $R_{REF}$ (19) | — | — | 1800 ±1% | — | — | 1800 ±1% | — | — | 1800 ±1% | — | Ω |
| **Transceiver Clocks** | | | | | | | | | | | |
| `fixedclk` clock frequency | PCIe Receiver Detect | — | 100 or 125 | — | — | 100 or 125 | — | — | 100 or 125 | — | MHz |

**Table 23. Transceiver Specifications for Stratix V GX and GS Devices (1) (Part 3 of 7)**

| Symbol/ Description | Conditions | Transceiver Speed Grade 1 | | | Transceiver Speed Grade 2 | | | Transceiver Speed Grade 3 | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| Reconfiguration clock (mgmt_clk_clk) frequency | — | 100 | — | 125 | 100 | — | 125 | 100 | — | 125 | MHz |
| **Receiver** | | | | | | | | | | | |
| Supported I/O Standards | — | 1.4-V PCML, 1.5-V PCML, 2.5-V PCML, LVPECL, and LVDS | | | | | | | | | |
| Data rate (Standard PCS) (9), (23) | — | 600 | — | 12200 | 600 | — | 12200 | 600 | — | 8500/ 10312.5 (24) | Mbps |
| Data rate (10G PCS) (9), (23) | — | 600 | — | 14100 | 600 | — | 12500 | 600 | — | 8500/ 10312.5 (24) | Mbps |
| Absolute $V_{MAX}$ for a receiver pin (5) | — | — | — | 1.2 | — | — | 1.2 | — | — | 1.2 | V |
| Absolute $V_{MIN}$ for a receiver pin | — | –0.4 | — | — | –0.4 | — | — | –0.4 | — | — | V |
| Maximum peak-to-peak differential input voltage $V_{ID}$ (diff p-p) before device configuration (22) | — | — | — | 1.6 | — | — | 1.6 | — | — | 1.6 | V |
| Maximum peak-to-peak differential input voltage $V_{ID}$ (diff p-p) after device configuration (18), (22) | $V_{CCR\_GXB}$ = 1.0 V/1.05 V ($V_{ICM}$ = 0.70 V) | — | — | 2.0 | — | — | 2.0 | — | — | 2.0 | V |
| | $V_{CCR\_GXB}$ = 0.90 V ($V_{ICM}$ = 0.6 V) | — | — | 2.4 | — | — | 2.4 | — | — | 2.4 | V |
| | $V_{CCR\_GXB}$ = 0.85 V ($V_{ICM}$ = 0.6 V) | — | — | 2.4 | — | — | 2.4 | — | — | 2.4 | V |
| Minimum differential eye opening at receiver serial input pins (6), (22), (27) | — | 85 | — | — | 85 | — | — | 85 | — | — | mV |

**Table 28. Transceiver Specifications for Stratix V GT Devices (Part 3 of 5) (1)**

| Symbol/ Description | Conditions | Transceiver Speed Grade 2 | | | Transceiver Speed Grade 3 | | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | Min | Typ | Max | Min | Typ | Max | |
| Differential on-chip termination resistors (7) | GT channels | — | 100 | — | — | 100 | — | Ω |
| Differential on-chip termination resistors for GX channels (19) | 85-Ω setting | — | 85 ± 30% | — | — | 85 ± 30% | — | Ω |
| | 100-Ω setting | — | 100 ± 30% | — | — | 100 ± 30% | — | Ω |
| | 120-Ω setting | — | 120 ± 30% | — | — | 120 ± 30% | — | Ω |
| | 150-Ω setting | — | 150 ± 30% | — | — | 150 ± 30% | — | Ω |
| $V_{ICM}$ (AC coupled) | GT channels | — | 650 | — | — | 650 | — | mV |
| VICM (AC and DC coupled) for GX Channels | VCCR_GXB = 0.85 V or 0.9 V | — | 600 | — | — | 600 | — | mV |
| | VCCR_GXB = 1.0 V full bandwidth | — | 700 | — | — | 700 | — | mV |
| | VCCR_GXB = 1.0 V half bandwidth | — | 750 | — | — | 750 | — | mV |
| $t_{LTR}$ (9) | — | — | — | 10 | — | — | 10 | µs |
| $t_{LTD}$ (10) | — | 4 | — | — | 4 | — | — | µs |
| $t_{LTD\_manual}$ (11) | — | 4 | — | — | 4 | — | — | µs |
| $t_{LTR\_LTD\_manual}$ (12) | — | 15 | — | — | 15 | — | — | µs |
| Run Length | GT channels | — | — | 72 | — | — | 72 | CID |
| | GX channels | (8) | | | | | | |
| CDR PPM | GT channels | — | — | 1000 | — | — | 1000 | ± PPM |
| | GX channels | (8) | | | | | | |
| Programmable equalization (AC Gain) (5) | GT channels | — | — | 14 | — | — | 14 | dB |
| | GX channels | (8) | | | | | | |
| Programmable DC gain (6) | GT channels | — | — | 7.5 | — | — | 7.5 | dB |
| | GX channels | (8) | | | | | | |
| Differential on-chip termination resistors (7) | GT channels | — | 100 | — | — | 100 | — | Ω |
| **Transmitter** | | | | | | | | |
| Supported I/O Standards | — | 1.4-V and 1.5-V PCML | | | | | | |
| Data rate (Standard PCS) | GX channels | 600 | — | 8500 | 600 | — | 8500 | Mbps |
| Data rate (10G PCS) | GX channels | 600 | — | 12,500 | 600 | — | 12,500 | Mbps |

**Table 28. Transceiver Specifications for Stratix V GT Devices (Part 4 of 5) (1)**

| Symbol/ Description | Conditions | Transceiver Speed Grade 2 | | | Transceiver Speed Grade 3 | | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | Min | Typ | Max | Min | Typ | Max | |
| Data rate | GT channels | 19,600 | — | 28,050 | 19,600 | — | 25,780 | Mbps |
| Differential on-chip termination resistors | GT channels | — | 100 | — | — | 100 | — | Ω |
| | GX channels | (8) | | | | | | |
| $V_{OCM}$ (AC coupled) | GT channels | — | 500 | — | — | 500 | — | mV |
| | GX channels | (8) | | | | | | |
| Rise/Fall time | GT channels | — | 15 | — | — | 15 | — | ps |
| | GX channels | (8) | | | | | | |
| Intra-differential pair skew | GX channels | (8) | | | | | | |
| Intra-transceiver block transmitter channel-to-channel skew | GX channels | (8) | | | | | | |
| Inter-transceiver block transmitter channel-to-channel skew | GX channels | (8) | | | | | | |
| **CMU PLL** | | | | | | | | |
| Supported Data Range | — | 600 | — | 12500 | 600 | — | 8500 | Mbps |
| $t_{pll\_powerdown}$ (13) | — | 1 | — | — | 1 | — | — | µs |
| $t_{pll\_lock}$ (14) | — | — | — | 10 | — | — | 10 | µs |
| **ATX PLL** | | | | | | | | |
| Supported Data Rate Range for GX Channels | VCO post-divider L=2 | 8000 | — | 12500 | 8000 | — | 8500 | Mbps |
| | L=4 | 4000 | — | 6600 | 4000 | — | 6600 | Mbps |
| | L=8 | 2000 | — | 3300 | 2000 | — | 3300 | Mbps |
| | L=8, Local/Central Clock Divider =2 | 1000 | — | 1762.5 | 1000 | — | 1762.5 | Mbps |
| Supported Data Rate Range for GT Channels | VCO post-divider L=2 | 9800 | — | 14025 | 9800 | — | 12890 | Mbps |
| $t_{pll\_powerdown}$ (13) | — | 1 | — | — | 1 | — | — | µs |
| $t_{pll\_lock}$ (14) | — | — | — | 10 | — | — | 10 | µs |
| **fPLL** | | | | | | | | |
| Supported Data Range | — | 600 | — | 3250/ 3.125 (23) | 600 | — | 3250/ 3.125 (23) | Mbps |
| $t_{pll\_powerdown}$ (13) | — | 1 | — | — | 1 | — | — | µs |

**Table 28. Transceiver Specifications for Stratix V GT Devices (Part 5 of 5) (1)**

| Symbol/ Description | Conditions | Transceiver Speed Grade 2 | | | Transceiver Speed Grade 3 | | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | Min | Typ | Max | Min | Typ | Max | |
| $t_{pll\_lock}$ (14) | — | — | — | 10 | — | — | 10 | µs |

**Notes to Table 28:**

(1) Speed grades shown refer to the PMA Speed Grade in the device ordering code. The maximum data rate could be restricted by the Core/PCS speed grade. Contact your Altera Sales Representative for the maximum data rate specifications in each speed grade combination offered. For more information about device ordering codes, refer to the *Stratix V Device Overview*.

(2) The reference clock common mode voltage is equal to the VCCR_GXB power supply level.

(3) The device cannot tolerate prolonged operation at this absolute maximum.

(4) The differential eye opening specification at the receiver input pins assumes that receiver equalization is disabled. If you enable receiver equalization, the receiver circuitry can tolerate a lower minimum eye opening, depending on the equalization level.

(5) Refer to Figure 5 for the GT channel AC gain curves. The total effective AC gain is the AC gain minus the DC gain.

(6) Refer to Figure 6 for the GT channel DC gain curves.

(7) CFP2 optical modules require the host interface to have the receiver data pins differentially terminated with 100 Ω. The internal OCT feature is available after the Stratix V FPGA configuration is completed. Altera recommends that FPGA configuration is completed before inserting the optical module. Otherwise, minimize unnecessary removal and insertion with unconfigured devices.

(8) Specifications for this parameter are the same as for Stratix V GX and GS devices. See Table 23 for specifications.

(9) $t_{LTR}$ is the time required for the receive CDR to lock to the input reference clock frequency after coming out of reset.

(10) $t_{LTD}$ is time required for the receiver CDR to start recovering valid data after the `rx_is_lockedtodata` signal goes high.

(11) $t_{LTD\_manual}$ is the time required for the receiver CDR to start recovering valid data after the `rx_is_lockedtodata` signal goes high when the CDR is functioning in the manual mode.

(12) $t_{LTR\_LTD\_manual}$ is the time the receiver CDR must be kept in lock to reference (LTR) mode after the `rx_is_lockedtoref` signal goes high when the CDR is functioning in the manual mode.

(13) `tpll_powerdown` is the PLL powerdown minimum pulse width.

(14) `tpll_lock` is the time required for the transmitter CMU/ATX PLL to lock to the input reference clock frequency after coming out of reset.

(15) To calculate the REFCLK rms phase jitter requirement for PCIe at reference clock frequencies other than 100 MHz, use the following formula: REFCLK rms phase jitter at f(MHz) = REFCLK rms phase jitter at 100 MHz × 100/f.

(16) The maximum peak to peak differential input voltage $V_{ID}$ after device configuration is equal to 4 × (absolute $V_{MAX}$ for receiver pin - $V_{ICM}$).

(17) For ES devices, RREF is 2000 Ω ±1%.

(18) To calculate the REFCLK phase noise requirement at frequencies other than 622 MHz, use the following formula: REFCLK phase noise at f(MHz) = REFCLK phase noise at 622 MHz + 20*log(f/622).

(19) SFP/+ optical modules require the host interface to have RD+/- differentially terminated with 100 Ω. The internal OCT feature is available after the Stratix V FPGA configuration is completed. Altera recommends that FPGA configuration is completed before inserting the optical module. Otherwise, minimize unnecessary removal and insertion with unconfigured devices.

(20) Refer to Figure 4.

(21) For oversampling design to support data rates less than the minimum specification, the CDR needs to be in LTR mode only.

(22) This supply follows VCCR_GXB for both GX and GT channels.

(23) When you use fPLL as a TXPLL of the transceiver.

## PLL Specifications

Table 31 lists the Stratix V PLL specifications when operating in both the commercial junction temperature range (0° to 85°C) and the industrial junction temperature range (–40° to 100°C).

**Table 31. PLL Specifications for Stratix V Devices (Part 1 of 3)**

| Symbol | Parameter | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| $f_{IN}$ | Input clock frequency (C1, C2, C2L, I2, and I2L speed grades) | 5 | — | 800 (1) | MHz |
| | Input clock frequency (C3, I3, I3L, and I3YY speed grades) | 5 | — | 800 (1) | MHz |
| | Input clock frequency (C4, I4 speed grades) | 5 | — | 650 (1) | MHz |
| $f_{INPFD}$ | Input frequency to the PFD | 5 | — | 325 | MHz |
| $f_{FINPFD}$ | Fractional Input clock frequency to the PFD | 50 | — | 160 | MHz |
| $f_{VCO}$ (9) | PLL VCO operating range (C1, C2, C2L, I2, I2L speed grades) | 600 | — | 1600 | MHz |
| | PLL VCO operating range (C3, I3, I3L, I3YY speed grades) | 600 | — | 1600 | MHz |
| | PLL VCO operating range (C4, I4 speed grades) | 600 | — | 1300 | MHz |
| $t_{EINDUTY}$ | Input clock or external feedback clock input duty cycle | 40 | — | 60 | % |
| $f_{OUT}$ | Output frequency for an internal global or regional clock (C1, C2, C2L, I2, I2L speed grades) | — | — | 717 (2) | MHz |
| | Output frequency for an internal global or regional clock (C3, I3, I3L speed grades) | — | — | 650 (2) | MHz |
| | Output frequency for an internal global or regional clock (C4, I4 speed grades) | — | — | 580 (2) | MHz |
| $f_{OUT\_EXT}$ | Output frequency for an external clock output (C1, C2, C2L, I2, I2L speed grades) | — | — | 800 (2) | MHz |
| | Output frequency for an external clock output (C3, I3, I3L speed grades) | — | — | 667 (2) | MHz |
| | Output frequency for an external clock output (C4, I4 speed grades) | — | — | 553 (2) | MHz |
| $t_{OUTDUTY}$ | Duty cycle for a dedicated external clock output (when set to **50%**) | 45 | 50 | 55 | % |
| $t_{FCOMP}$ | External feedback clock compensation time | — | — | 10 | ns |
| $f_{DYCONFIGCLK}$ | Dynamic Configuration Clock used for `mgmt_clk` and `scanclk` | — | — | 100 | MHz |
| $t_{LOCK}$ | Time required to lock from the end-of-device configuration or deassertion of `areset` | — | — | 1 | ms |
| $t_{DLOCK}$ | Time required to lock dynamically (after switchover or reconfiguring any non-post-scale counters/delays) | — | — | 1 | ms |
| $f_{CLBW}$ | PLL closed-loop low bandwidth | — | 0.3 | — | MHz |
| | PLL closed-loop medium bandwidth | — | 1.5 | — | MHz |
| | PLL closed-loop high bandwidth (7) | — | 4 | — | MHz |
| $t_{PLL\_PSERR}$ | Accuracy of PLL phase shift | — | — | ±50 | ps |
| $t_{ARESET}$ | Minimum pulse width on the `areset` signal | 10 | — | — | ns |

**Table 31. PLL Specifications for Stratix V Devices (Part 2 of 3)**

| Symbol | Parameter | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| $t_{INCCJ}$ (3), (4) | Input clock cycle-to-cycle jitter ($f_{REF} \geq 100$ MHz) | — | — | 0.15 | UI (p-p) |
| | Input clock cycle-to-cycle jitter ($f_{REF} < 100$ MHz) | –750 | — | +750 | ps (p-p) |
| $t_{OUTPJ\_DC}$ (5) | Period Jitter for dedicated clock output ($f_{OUT} \geq 100$ MHz) | — | — | 175 (1) | ps (p-p) |
| | Period Jitter for dedicated clock output ($f_{OUT} < 100$ MHz) | — | — | 17.5 (1) | mUI (p-p) |
| $t_{FOUTPJ\_DC}$ (5) | Period Jitter for dedicated clock output in fractional PLL ($f_{OUT} \geq 100$ MHz) | — | — | 250 (11), 175 (12) | ps (p-p) |
| | Period Jitter for dedicated clock output in fractional PLL ($f_{OUT} < 100$ MHz) | — | — | 25 (11), 17.5 (12) | mUI (p-p) |
| $t_{OUTCCJ\_DC}$ (5) | Cycle-to-Cycle Jitter for a dedicated clock output ($f_{OUT} \geq 100$ MHz) | — | — | 175 | ps (p-p) |
| | Cycle-to-Cycle Jitter for a dedicated clock output ($f_{OUT} < 100$ MHz) | — | — | 17.5 | mUI (p-p) |
| $t_{FOUTCCJ\_DC}$ (5) | Cycle-to-cycle Jitter for a dedicated clock output in fractional PLL ($f_{OUT} \geq 100$ MHz) | — | — | 250 (11), 175 (12) | ps (p-p) |
| | Cycle-to-cycle Jitter for a dedicated clock output in fractional PLL ($f_{OUT} < 100$ MHz)+ | — | — | 25 (11), 17.5 (12) | mUI (p-p) |
| $t_{OUTPJ\_IO}$ (5), (8) | Period Jitter for a clock output on a regular I/O in integer PLL ($f_{OUT} \geq 100$ MHz) | — | — | 600 | ps (p-p) |
| | Period Jitter for a clock output on a regular I/O ($f_{OUT} < 100$ MHz) | — | — | 60 | mUI (p-p) |
| $t_{FOUTPJ\_IO}$ (5), (8), (11) | Period Jitter for a clock output on a regular I/O in fractional PLL ($f_{OUT} \geq 100$ MHz) | — | — | 600 (10) | ps (p-p) |
| | Period Jitter for a clock output on a regular I/O in fractional PLL ($f_{OUT} < 100$ MHz) | — | — | 60 (10) | mUI (p-p) |
| $t_{OUTCCJ\_IO}$ (5), (8) | Cycle-to-cycle Jitter for a clock output on a regular I/O in integer PLL ($f_{OUT} \geq 100$ MHz) | — | — | 600 | ps (p-p) |
| | Cycle-to-cycle Jitter for a clock output on a regular I/O in integer PLL ($f_{OUT} < 100$ MHz) | — | — | 60 (10) | mUI (p-p) |
| $t_{FOUTCCJ\_IO}$ (5), (8), (11) | Cycle-to-cycle Jitter for a clock output on a regular I/O in fractional PLL ($f_{OUT} \geq 100$ MHz) | — | — | 600 (10) | ps (p-p) |
| | Cycle-to-cycle Jitter for a clock output on a regular I/O in fractional PLL ($f_{OUT} < 100$ MHz) | — | — | 60 | mUI (p-p) |
| $t_{CASC\_OUTPJ\_DC}$ (5), (6) | Period Jitter for a dedicated clock output in cascaded PLLs ($f_{OUT} \geq 100$ MHz) | — | — | 175 | ps (p-p) |
| | Period Jitter for a dedicated clock output in cascaded PLLs ($f_{OUT} < 100$ MHz) | — | — | 17.5 | mUI (p-p) |
| $f_{DRIFT}$ | Frequency drift after PFDENA is disabled for a duration of 100 µs | — | — | ±10 | % |
| $dK_{BIT}$ | Bit number of Delta Sigma Modulator (DSM) | 8 | 24 | 32 | Bits |
| $k_{VALUE}$ | Numerator of Fraction | 128 | 8388608 | 2147483648 | — |

**Table 36. High-Speed I/O Specifications for Stratix V Devices (1), (2) (Part 2 of 4)**

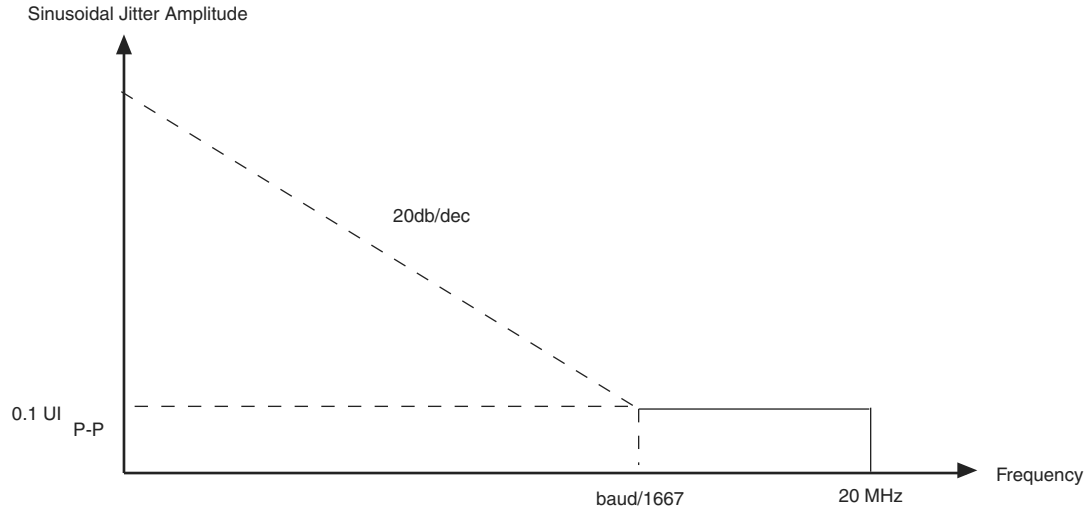
| Symbol | Conditions | C1 | | | C2, C2L, I2, I2L | | | C3, I3, I3L, I3YY | | | C4,I4 | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| **Transmitter** | | | | | | | | | | | | | | |
| True Differential I/O Standards - $f_{HSDR}$ (data rate) | SERDES factor J = 3 to 10 (9), (11), (12), (13), (14), (15), (16) | (6) | — | 1600 | (6) | — | 1434 | (6) | — | 1250 | (6) | — | 1050 | Mbps |
| | SERDES factor J ≥ 4 LVDS TX with DPA (12), (14), (15), (16) | (6) | — | 1600 | (6) | — | 1600 | (6) | — | 1600 | (6) | — | 1250 | Mbps |
| | SERDES factor J = 2, uses DDR Registers | (6) | — | (7) | (6) | — | (7) | (6) | — | (7) | (6) | — | (7) | Mbps |
| | SERDES factor J = 1, uses SDR Register | (6) | — | (7) | (6) | — | (7) | (6) | — | (7) | (6) | — | (7) | Mbps |
| Emulated Differential I/O Standards with Three External Output Resistor Networks - $f_{HSDR}$ (data rate) (10) | SERDES factor J = 4 to 10 (17) | (6) | — | 1100 | (6) | — | 1100 | (6) | — | 840 | (6) | — | 840 | Mbps |
| $t_{x\ Jitter}$ - True Differential I/O Standards | Total Jitter for Data Rate 600 Mbps - 1.25 Gbps | — | — | 160 | — | — | 160 | — | — | 160 | — | — | 160 | ps |
| | Total Jitter for Data Rate < 600 Mbps | — | — | 0.1 | — | — | 0.1 | — | — | 0.1 | — | — | 0.1 | UI |
| $t_{x\ Jitter}$ - Emulated Differential I/O Standards with Three External Output Resistor Network | Total Jitter for Data Rate 600 Mbps - 1.25 Gbps | — | — | 300 | — | — | 300 | — | — | 300 | — | — | 325 | ps |
| | Total Jitter for Data Rate < 600 Mbps | — | — | 0.2 | — | — | 0.2 | — | — | 0.2 | — | — | 0.25 | UI |

**Table 38. LVDS Soft-CDR/DPA Sinusoidal Jitter Mask Values for a Data Rate ≥ 1.25 Gbps**

| Jitter Frequency (Hz) | | Sinusoidal Jitter (UI) |
|---|---|---|
| F1 | 10,000 | 25.000 |
| F2 | 17,565 | 25.000 |
| F3 | 1,493,000 | 0.350 |
| F4 | 50,000,000 | 0.350 |

Figure 9 shows the **LVDS** soft-CDR/DPA sinusoidal jitter tolerance specification for a data rate < 1.25 Gbps.

**Figure 9. LVDS Soft-CDR/DPA Sinusoidal Jitter Tolerance Specification for a Data Rate < 1.25 Gbps**




## DLL Range, DQS Logic Block, and Memory Output Clock Jitter Specifications

Table 39 lists the DLL range specification for Stratix V devices. The DLL is always in 8-tap mode in Stratix V devices.

**Table 39. DLL Range Specifications for Stratix V Devices (1)**

| C1 | C2, C2L, I2, I2L | C3, I3, I3L, I3YY | C4,I4 | Unit |
|---|---|---|---|---|
| 300-933 | 300-933 | 300-890 | 300-890 | MHz |

**Note to Table 39:**

(1) Stratix V devices support memory interface frequencies lower than 300 MHz, although the reference clock that feeds the DLL must be at least 300 MHz. To support interfaces below 300 MHz, multiply the reference clock feeding the DLL to ensure the frequency is within the supported range of the DLL.

Table 40 lists the DQS phase offset delay per stage for Stratix V devices.

**Table 40. DQS Phase Offset Delay Per Setting for Stratix V Devices (1), (2) (Part 1 of 2)**

| Speed Grade | Min | Max | Unit |
|---|---|---|---|
| C1 | 8 | 14 | ps |
| C2, C2L, I2, I2L | 8 | 14 | ps |
| C3,I3, I3L, I3YY | 8 | 15 | ps |

### Duty Cycle Distortion (DCD) Specifications

Table 44 lists the worst-case DCD for Stratix V devices.

**Table 44. Worst-Case DCD on Stratix V I/O Pins** *(1)*

| Symbol | C1 | | C2, C2L, I2, I2L | | C3, I3, I3L, I3YY | | C4,I4 | | Unit |
|---|---|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | Min | Max | |
| Output Duty Cycle | 45 | 55 | 45 | 55 | 45 | 55 | 45 | 55 | % |

**Note to Table 44:**

(1) The DCD numbers do not cover the core clock network.

# Configuration Specification

## POR Delay Specification

Power-on reset (POR) delay is defined as the delay between the time when all the power supplies monitored by the POR circuitry reach the minimum recommended operating voltage to the time when the nSTATUS is released high and your device is ready to begin configuration.

For more information about the POR delay, refer to the *Hot Socketing and Power-On Reset in Stratix V Devices* chapter.

Table 45 lists the fast and standard POR delay specification.

**Table 45. Fast and Standard POR Delay Specification** *(1)*

| POR Delay | Minimum | Maximum |
|---|---|---|
| Fast | 4 ms | 12 ms |
| Standard | 100 ms | 300 ms |

**Note to Table 45:**

(1) You can select the POR delay based on the MSEL settings as described in the MSEL Pin Settings section of the "Configuration, Design Security, and Remote System Upgrades in Stratix V Devices" chapter.

## JTAG Configuration Specifications

Table 46 lists the JTAG timing parameters and values for Stratix V devices.

**Table 46. JTAG Timing Parameters and Values for Stratix V Devices**

| Symbol | Description | Min | Max | Unit |
|---|---|---|---|---|
| $t_{JCP}$ | TCK clock period *(2)* | 30 | — | ns |
| $t_{JCP}$ | TCK clock period *(2)* | 167 | — | ns |
| $t_{JCH}$ | TCK clock high time *(2)* | 14 | — | ns |
| $t_{JCL}$ | TCK clock low time *(2)* | 14 | — | ns |
| $t_{JPSU\ (TDI)}$ | TDI JTAG port setup time | 2 | — | ns |
| $t_{JPSU\ (TMS)}$ | TMS JTAG port setup time | 3 | — | ns |

**Table 46. JTAG Timing Parameters and Values for Stratix V Devices**

| Symbol | Description | Min | Max | Unit |
|---|---|---|---|---|
| $t_{JPH}$ | JTAG port hold time | 5 | — | ns |
| $t_{JPCO}$ | JTAG port clock to output | — | 11 (1) | ns |
| $t_{JPZX}$ | JTAG port high impedance to valid output | — | 14 (1) | ns |
| $t_{JPXZ}$ | JTAG port valid output to high impedance | — | 14 (1) | ns |

**Notes to Table 46:**

(1) A 1 ns adder is required for each $V_{CCIO}$ voltage step down from 3.0 V. For example, $t_{JPCO}$ = 12 ns if $V_{CCIO}$ of the TDO I/O bank = 2.5 V, or 13 ns if it equals 1.8 V.

(2) The minimum TCK clock period is 167 ns if VCCBAT is within the range 1.2V-1.5V when you perform the volatile key programming.

## Raw Binary File Size

For the POR delay specification, refer to the "POR Delay Specification" section of the "Configuration, Design Security, and Remote System Upgrades in Stratix V Devices".

Table 47 lists the uncompressed raw binary file (**.rbf**) sizes for Stratix V devices.

**Table 47. Uncompressed .rbf Sizes for Stratix V Devices**

| Family | Device | Package | Configuration .rbf Size (bits) | IOCSR .rbf Size (bits) (4), (5) |
|---|---|---|---|---|
| Stratix V GX | 5SGXA3 | H35, F40, F35 (2) | 213,798,880 | 562,392 |
| | | H29, F35 (3) | 137,598,880 | 564,504 |
| | 5SGXA4 | — | 213,798,880 | 563,672 |
| | 5SGXA5 | — | 269,979,008 | 562,392 |
| | 5SGXA7 | — | 269,979,008 | 562,392 |
| | 5SGXA9 | — | 342,742,976 | 700,888 |
| | 5SGXAB | — | 342,742,976 | 700,888 |
| | 5SGXB5 | — | 270,528,640 | 584,344 |
| | 5SGXB6 | — | 270,528,640 | 584,344 |
| | 5SGXB9 | — | 342,742,976 | 700,888 |
| | 5SGXBB | — | 342,742,976 | 700,888 |
| Stratix V GT | 5SGTC5 | — | 269,979,008 | 562,392 |
| | 5SGTC7 | — | 269,979,008 | 562,392 |
| Stratix V GS | 5SGSD3 | — | 137,598,880 | 564,504 |
| | 5SGSD4 | F1517 | 213,798,880 | 563,672 |
| | | — | 137,598,880 | 564,504 |
| | 5SGSD5 | — | 213,798,880 | 563,672 |
| | 5SGSD6 | — | 293,441,888 | 565,528 |
| | 5SGSD8 | — | 293,441,888 | 565,528 |

**Table 53. AS Timing Parameters for AS ×1 and AS ×4 Configurations in Stratix V Devices (1), (2) (Part 2 of 2)**

| Symbol | Parameter | Minimum | Maximum | Units |
|---|---|---|---|---|
| $t_{CD2UM}$ | CONF_DONE high to user mode (3) | 175 | 437 | µs |
| $t_{CD2CU}$ | CONF_DONE high to CLKUSR enabled | 4 × maximum DCLK period | — | — |
| $t_{CD2UMC}$ | CONF_DONE high to user mode with CLKUSR option on | $t_{CD2CU}$ + (8576 × CLKUSR period) | — | — |

**Notes to Table 53:**

(1) The minimum and maximum numbers apply only if you choose the internal oscillator as the clock source for initializing the device.

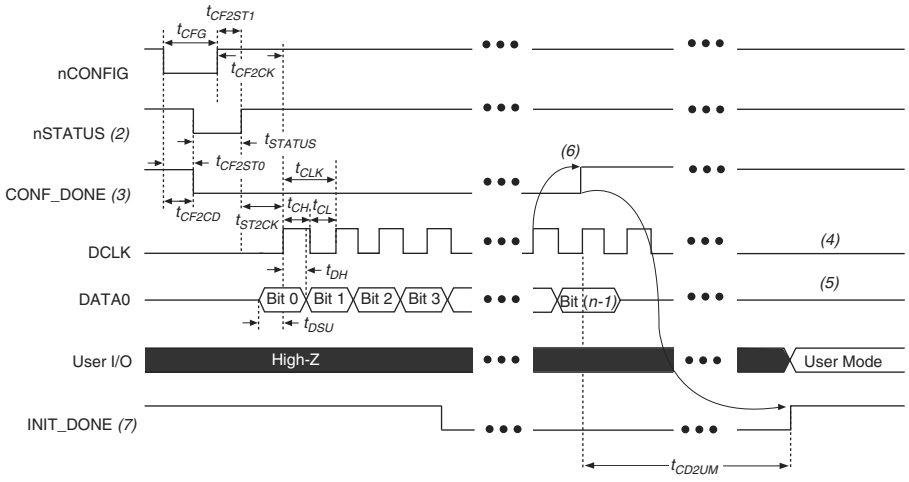
(2) $t_{CF2CD}$, $t_{CF2ST0}$, $t_{CFG}$, $t_{STATUS}$, and $t_{CF2ST1}$ timing parameters are identical to the timing parameters for PS mode listed in Table 54 on page 63.

(3) To enable the CLKUSR pin as the initialization clock source and to obtain the maximum frequency specification on this pin, refer to the Initialization section of the "Configuration, Design Security, and Remote System Upgrades in Stratix V Devices" chapter.

## Passive Serial Configuration Timing

Figure 15 shows the timing waveform for a passive serial (PS) configuration when using a MAX II device, MAX V device, or microprocessor as an external host.

**Figure 15. PS Configuration Timing Waveform (1)**




**Notes to Figure 15:**

(1) The beginning of this waveform shows the device in user mode. In user mode, nCONFIG, nSTATUS, and CONF_DONE are at logic high levels. When nCONFIG is pulled low, a reconfiguration cycle begins.

(2) After power-up, the Stratix V device holds nSTATUS low for the time of the POR delay.

(3) After power-up, before and during configuration, CONF_DONE is low.

(4) Do not leave DCLK floating after configuration. You can drive it high or low, whichever is more convenient.

(5) DATA0 is available as a user I/O pin after configuration. The state of this pin depends on the dual-purpose pin settings in the **Device and Pins Option**.

(6) To ensure a successful configuration, send the entire configuration data to the Stratix V device. CONF_DONE is released high after the Stratix V device receives all the configuration data successfully. After CONF_DONE goes high, send two additional falling edges on DCLK to begin initialization and enter user mode.

(7) After the option bit to enable the INIT_DONE pin is configured into the device, the INIT_DONE goes low.

# Document Revision History

Table 61 lists the revision history for this chapter.

**Table 61. Document Revision History (Part 1 of 3)**

| Date | Version | Changes |
|---|---|---|
| June 2018 | 3.9 | ■ Added the “Stratix V Device Overshoot Duration” figure. |
| April 2017 | 3.8 | ■ Added a footnote to the “High-Speed I/O Specifications for Stratix V Devices” table.<br>■ Changed the minimum value for $t_{CD2UMC}$ in the “PS Timing Parameters for Stratix V Devices” table.<br>■ Changed the condition for 100-Ω $R_D$ in the “OCT Without Calibration Resistance Tolerance Specifications for Stratix V Devices” table.<br>■ Changed the minimum value for $t_{CD2UMC}$ in the “AS Timing Parameters for AS ´1 and AS ´4 Configurations in Stratix V Devices” table<br>■ Changed the minimum value for $t_{CD2UMC}$ in the “FPP Timing Parameters for Stratix V Devices When the DCLK-to-DATA[] Ratio is >1” table.<br>■ Changed the minimum value for $t_{CD2UMC}$ in the “FPP Timing Parameters for Stratix V Devices When the DCLK-to-DATA[] Ratio is >1” table.<br>■ Changed the minimum number of clock cycles value in the “Initialization Clock Source Option and the Maximum Frequency” table. |
| June 2016 | 3.7 | ■ Added the $V_{ID}$ minimum specification for LVPECL in the “Differential I/O Standard Specifications for Stratix V Devices” table<br>■ Added the $I_{OUT}$ specification to the “Absolute Maximum Ratings for Stratix V Devices” table. |
| December 2015 | 3.6 | ■ Added a footnote to the “High-Speed I/O Specifications for Stratix V Devices” table. |
| December 2015 | 3.5 | ■ Changed the transmitter, receiver, and ATX PLL data rate specifications in the “Transceiver Specifications for Stratix V GX and GS Devices” table.<br>■ Changed the configuration .rbf sizes in the “Uncompressed .rbf Sizes for Stratix V Devices” table. |
| July 2015 | 3.4 | ■ Changed the data rate specification for transceiver speed grade 3 in the following tables:<br>  ■ “Transceiver Specifications for Stratix V GX and GS Devices”<br>  ■ “Stratix V Standard PCS Approximate Maximum Date Rate”<br>  ■ “Stratix V 10G PCS Approximate Maximum Data Rate”<br>■ Changed the conditions for reference clock rise and fall time, and added a note to the “Transceiver Specifications for Stratix V GX and GS Devices” table.<br>■ Added a note to the “Minimum differential eye opening at receiver serial input pins” specification in the “Transceiver Specifications for Stratix V GX and GS Devices” table.<br>■ Changed the $t_{CO}$ maximum value in the “AS Timing Parameters for AS ´1 and AS ´4 Configurations in Stratix V Devices” table.<br>■ Removed the CDR ppm tolerance specification from the “Transceiver Specifications for Stratix V GX and GS Devices” table. |