# E·XFL

#### Intel - 5SGXEABN3F45I3N Datasheet



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#### Understanding <u>Embedded - FPGAs (Field</u> <u>Programmable Gate Array)</u>

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

#### **Applications of Embedded - FPGAs**

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

#### Details

Product Status	Obsolete
Number of LABs/CLBs	359200
Number of Logic Elements/Cells	952000
Total RAM Bits	53248000
Number of I/O	840
Number of Gates	-
Voltage - Supply	0.82V ~ 0.88V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	1932-BBGA, FCBGA
Supplier Device Package	1932-FBGA, FC (45x45)
Purchase URL	https://www.e-xfl.com/product-detail/intel/5sgxeabn3f45i3n

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

								·		
Transceiver Speed	Core Speed Grade									
Grade	C1	C2, C2L	C3	C4	<b>12, 12L</b>	13, 13L	<b>I</b> 3YY	14		
3 GX channel—8.5 Gbps	_	Yes	Yes	Yes	_	Yes	Yes <sup>(4)</sup>	Yes		

#### Table 1. Stratix V GX and GS Commercial and Industrial Speed Grade Offering <sup>(1), (2), (3)</sup> (Part 2 of 2)

Notes to Table 1:

(1) C = Commercial temperature grade; I = Industrial temperature grade.

(2) Lower number refers to faster speed grade.

(3) C2L, I2L, and I3L speed grades are for low-power devices.

(4) I3YY speed grades can achieve up to 10.3125 Gbps.

Table 2 lists the industrial and commercial speed grades for the Stratix V GT devices. **Table 2. Stratix V GT Commercial and Industrial Speed Grade Offering** <sup>(1)</sup>, <sup>(2)</sup>

Transseiver Speed Grade	Core Speed Grade							
Transceiver Speeu draue	C1	C2	12	13				
2 GX channel—12.5 Gbps GT channel—28.05 Gbps	Yes	Yes	_	_				
3 GX channel—12.5 Gbps GT channel—25.78 Gbps	Yes	Yes	Yes	Yes				

#### Notes to Table 2:

(1) C = Commercial temperature grade; I = Industrial temperature grade.

(2) Lower number refers to faster speed grade.

### **Absolute Maximum Ratings**

Absolute maximum ratings define the maximum operating conditions for Stratix V devices. The values are based on experiments conducted with the devices and theoretical modeling of breakdown and damage mechanisms. The functional operation of the device is not implied for these conditions.



Conditions other than those listed in Table 3 may cause permanent damage to the device. Additionally, device operation at the absolute maximum ratings for extended periods of time may have adverse effects on the device.

TANIC J. ANSULULC MAXIMUM NALINYS IVI SUALIX V DEVICES (FAIL I UI Z)	Table 3.	<b>Absolute Maximum</b>	Ratings	for Stratix \	/ Devices	(Part 1 of 2)
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Symbol	Description	Minimum	Maximum	Unit
V <sub>CC</sub>	Power supply for core voltage and periphery circuitry	-0.5	1.35	V
V <sub>CCPT</sub>	Power supply for programmable power technology	-0.5	1.8	V
V <sub>CCPGM</sub>	Power supply for configuration pins	-0.5	3.9	V
V <sub>CC_AUX</sub>	Auxiliary supply for the programmable power technology	-0.5	3.4	V
V <sub>CCBAT</sub>	Battery back-up power supply for design security volatile key register	-0.5	3.9	V
V <sub>CCPD</sub>	I/O pre-driver power supply	-0.5	3.9	V
V <sub>CCIO</sub>	I/O power supply	-0.5	3.9	V

Symbol	Description	Devices	Minimum <sup>(4)</sup>	Typical	Maximum <sup>(4)</sup>	Unit
			0.82	0.85	0.88	v
V <sub>CCR_GXBR</sub>	Receiver analog power supply (right side)	CY CS CT	0.87	0.90	0.93	
(2)	neceiver analog power supply (right side)	ux, us, ui	0.97	1.0	1.03	v
			1.03	1.05	1.07	
V <sub>CCR_GTBR</sub>	Receiver analog power supply for GT channels (right side)	GT	1.02	1.05	1.08	V
V <sub>CCT_GXBL</sub>			0.82	0.85	0.88	
	Transmitter analog newer supply (left side)	GX GS GT	0.87	0.90	0.93	V
	Transmitter analog power supply (left side)	un, uo, ui	0.97	1.0	1.03	
			1.03	1.05	1.07	
		GX, GS, GT	0.82	0.85	0.88	V
V <sub>CCT GXBR</sub>	Transmitter analog newer supply (right side)		0.87	0.90	0.93	
(2) _	Transmitter analog power supply (light side)		0.97	1.0	1.03	
			1.03	1.05	1.07	
$V_{CCT_GTBR}$	Transmitter analog power supply for GT channels (right side)	GT	1.02	1.05	1.08	V
$V_{CCL\_GTBR}$	Transmitter clock network power supply	GT	1.02	1.05	1.08	V
V <sub>CCH_GXBL</sub>	Transmitter output buffer power supply (left side)	GX, GS, GT	1.425	1.5	1.575	V
V <sub>CCH_GXBR</sub>	Transmitter output buffer power supply (right side)	GX, GS, GT	1.425	1.5	1.575	V

Table 7.	<b>Recommended Transceiver Power Supply Operating Conditions for Stratix V GX</b> ,	<b>GS</b> , and <b>GT</b> Devices
(Part 2	of 2)	

#### Notes to Table 7:

(1) This supply must be connected to 3.0 V if the CMU PLL, receiver CDR, or both, are configured at a base data rate > 6.5 Gbps. Up to 6.5 Gbps, you can connect this supply to either 3.0 V or 2.5 V.

(2) Refer to Table 8 to select the correct power supply level for your design.

(3) When using ATX PLLs, the supply must be 3.0 V.

(4) This value describes the budget for the DC (static) power supply tolerance and does not include the dynamic tolerance requirements. Refer to the PDN tool for the additional budget for the dynamic tolerance requirements.

#### I/O Pin Leakage Current

Table 9 lists the Stratix V I/O pin leakage current specifications.

Table 9.	I/O Pin	Leakage	<b>Current for</b>	Stratix V	Devices (1)
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Symbol	Description	Conditions	Min	Тур	Max	Unit
I <sub>I</sub>	Input pin	$V_I = 0 V \text{ to } V_{CCIOMAX}$	-30	_	30	μA
I <sub>OZ</sub>	Tri-stated I/O pin	$V_0 = 0 V \text{ to } V_{\text{CCIOMAX}}$	-30		30	μA

#### Note to Table 9:

(1) If  $V_0 = V_{CCI0}$  to  $V_{CCI0Max}$ , 100  $\mu$ A of leakage current per I/O is expected.

#### **Bus Hold Specifications**

Table 10 lists the Stratix V device family bus hold specifications.

Table 10. Bus Hold Parameters for Stratix V Devices

			V <sub>CCIO</sub>										
Parameter	Symbol	Conditions	1.2	2 V	1.	5 V	1.8	B V	2.5	5 V	3.0	V	Unit
			Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Low sustaining current	I <sub>SUSL</sub>	V <sub>IN</sub> > V <sub>IL</sub> (maximum)	22.5	_	25.0	_	30.0	_	50.0	_	70.0	_	μA
High sustaining current	I <sub>SUSH</sub>	V <sub>IN</sub> < V <sub>IH</sub> (minimum)	-22.5		-25.0	_	-30.0	_	-50.0	_	-70.0		μA
Low overdrive current	I <sub>odl</sub>	$0V < V_{IN} < V_{CCIO}$		120		160		200	_	300		500	μA
High overdrive current	I <sub>odh</sub>	$0V < V_{IN} < V_{CCIO}$		-120		-160		-200		-300		-500	μΑ
Bus-hold trip point	V <sub>TRIP</sub>	_	0.45	0.95	0.50	1.00	0.68	1.07	0.70	1.70	0.80	2.00	۷

#### **On-Chip Termination (OCT) Specifications**

If you enable OCT calibration, calibration is automatically performed at power-up for I/Os connected to the calibration block. Table 11 lists the Stratix V OCT termination calibration accuracy specifications.

Table 11. OCT Calibration Accuracy Specifications for Stratix V Devices <sup>(1)</sup> (Part 1 of 2)

			Calibration Accuracy					
Symbol	Description	Conditions	C1	C2,12	C3,I3, I3YY	C4,14	Unit	
25- $Ω$ R <sub>S</sub>	Internal series termination with calibration (25- $\Omega$ setting)	V <sub>CCI0</sub> = 3.0, 2.5, 1.8, 1.5, 1.2 V	±15	±15	±15	±15	%	

I/O Standard	V <sub>IL(DC)</sub> (V)		V <sub>IH(D</sub>	<sub>C)</sub> (V)	V <sub>IL(AC)</sub> (V)	V <sub>IH(AC)</sub> (V)	V <sub>ol</sub> (V)	V <sub>oh</sub> (V)	I (mA)	l <sub>oh</sub>
i/U Stanuaru	Min	Max	Min	Max	Max	Min	Max	Min	i <sub>ol</sub> (IIIA)	(mA)
HSTL-18 Class I	—	V <sub>REF</sub> – 0.1	V <sub>REF</sub> + 0.1	_	$V_{REF} - 0.2$	V <sub>REF</sub> + 0.2	0.4	V <sub>CCI0</sub> – 0.4	8	-8
HSTL-18 Class II	_	V <sub>REF</sub> – 0.1	V <sub>REF</sub> + 0.1	_	V <sub>REF</sub> - 0.2	V <sub>REF</sub> + 0.2	0.4	V <sub>CCI0</sub> – 0.4	16	-16
HSTL-15 Class I	_	V <sub>REF</sub> – 0.1	V <sub>REF</sub> + 0.1	_	V <sub>REF</sub> - 0.2	V <sub>REF</sub> + 0.2	0.4	V <sub>CCIO</sub> – 0.4	8	-8
HSTL-15 Class II	_	V <sub>REF</sub> – 0.1	V <sub>REF</sub> + 0.1	_	V <sub>REF</sub> - 0.2	V <sub>REF</sub> + 0.2	0.4	V <sub>CCI0</sub> – 0.4	16	-16
HSTL-12 Class I	-0.15	V <sub>REF</sub> - 0.08	V <sub>REF</sub> + 0.08	V <sub>CCIO</sub> + 0.15	V <sub>REF</sub> – 0.15	V <sub>REF</sub> + 0.15	0.25* V <sub>CCI0</sub>	0.75* V <sub>CCI0</sub>	8	-8
HSTL-12 Class II	-0.15	V <sub>REF</sub> - 0.08	V <sub>REF</sub> + 0.08	V <sub>CCIO</sub> + 0.15	V <sub>REF</sub> – 0.15	V <sub>REF</sub> + 0.15	0.25* V <sub>CCI0</sub>	0.75* V <sub>CCI0</sub>	16	-16
HSUL-12	—	V <sub>REF</sub> – 0.13	V <sub>REF</sub> + 0.13	_	V <sub>REF</sub> – 0.22	V <sub>REF</sub> + 0.22	0.1* V <sub>CCIO</sub>	0.9* V <sub>CCI0</sub>	_	

#### Table 19. Single-Ended SSTL, HSTL, and HSUL I/O Standards Signal Specifications for Stratix V Devices (Part 2 of 2)

Table 20. Differential SSTL I/O Standards for Stratix V Devices

1/0 Standard		V <sub>ccio</sub> (V)		V <sub>SWING(DC)</sub> (V)			V <sub>X(AC)</sub> (V)		V <sub>SWING(AC)</sub> (V)		
ijo Stanuaru	Min	Тур	Max	Min	Max	Min	Тур	Max	Min	Max	
SSTL-2 Class I, II	2.375	2.5	2.625	0.3	V <sub>CCI0</sub> + 0.6	V <sub>CCI0</sub> /2- 0.2	_	V <sub>CCI0</sub> /2 + 0.2	0.62	V <sub>CCI0</sub> + 0.6	
SSTL-18 Class I, II	1.71	1.8	1.89	0.25	V <sub>CCIO</sub> + 0.6	V <sub>CCI0</sub> /2- 0.175	_	V <sub>CCI0</sub> /2 + 0.175	0.5	V <sub>CCI0</sub> + 0.6	
SSTL-15 Class I, II	1.425	1.5	1.575	0.2	(1)	V <sub>CCI0</sub> /2- 0.15	_	V <sub>CCI0</sub> /2 + 0.15	0.35	_	
SSTL-135 Class I, II	1.283	1.35	1.45	0.2	(1)	V <sub>CCI0</sub> /2- 0.15	V <sub>CCIO</sub> /2	V <sub>CCI0</sub> /2 + 0.15	2(V <sub>IH(AC)</sub> - V <sub>REF</sub> )	2(V <sub>IL(AC)</sub> - V <sub>REF</sub> )	
SSTL-125 Class I, II	1.19	1.25	1.31	0.18	(1)	V <sub>CCI0</sub> /2- 0.15	V <sub>CCIO</sub> /2	V <sub>CCI0</sub> /2 + 0.15	2(V <sub>IH(AC)</sub> - V <sub>REF</sub> )	_	
SSTL-12 Class I, II	1.14	1.2	1.26	0.18	_	V <sub>REF</sub> 0.15	V <sub>CCI0</sub> /2	V <sub>REF</sub> + 0.15	-0.30	0.30	

Note to Table 20:

(1) The maximum value for  $V_{SWING(DC)}$  is not defined. However, each single-ended signal needs to be within the respective single-ended limits  $(V_{IH(DC)} \text{ and } V_{IL(DC)})$ .

l/O Stondard	V <sub>CCIO</sub> (V)			V <sub>DIF(DC)</sub> (V)		V <sub>X(AC)</sub> (V)				V <sub>CM(DC)</sub> (V	V <sub>DIF(AC)</sub> (V)		
Standard	Min	Тур	Max	Min	Max	Min	Тур	Max	Min	Тур	Max	Min	Max
HSTL-18 Class I, II	1.71	1.8	1.89	0.2	_	0.78	_	1.12	0.78	_	1.12	0.4	_
HSTL-15 Class I, II	1.425	1.5	1.575	0.2	_	0.68	_	0.9	0.68		0.9	0.4	_

I/O		V <sub>CCIO</sub> (V)			<sub>DC)</sub> (V)	V <sub>X(AC)</sub> (V)				V <sub>CM(DC)</sub> (V	V <sub>DIF(AC)</sub> (V)		
Standard	Min	Тур	Max	Min	Max	Min	Тур	Max	Min	Тур	Max	Min	Max
HSTL-12 Class I, II	1.14	1.2	1.26	0.16	V <sub>CCI0</sub> + 0.3	_	0.5* V <sub>CCI0</sub>	_	0.4* V <sub>CCIO</sub>	0.5* V <sub>CCIO</sub>	0.6* V <sub>CCI0</sub>	0.3	V <sub>CCI0</sub> + 0.48
HSUL-12	1.14	1.2	1.3	0.26	0.26	0.5*V <sub>CCI0</sub> - 0.12	0.5* V <sub>CCI0</sub>	0.5*V <sub>CCI0</sub> + 0.12	0.4* V <sub>CCIO</sub>	0.5* V <sub>CCIO</sub>	0.6* V <sub>CCIO</sub>	0.44	0.44

#### Table 21. Differential HSTL and HSUL I/O Standards for Stratix V Devices (Part 2 of 2)

#### Table 22. Differential I/O Standard Specifications for Stratix V Devices (7)

I/O V <sub>CCI0</sub> (V) <sup>(10)</sup> V <sub>ID</sub> (mV) <sup>(8)</sup> V <sub>ICM(DC)</sub> (V) V <sub>0D</sub> (V) <sup>(6)</sup>							6)	V <sub>OCM</sub> (V) <i>(6)</i>							
Standard	Min	Тур	Max	Min	Condition	Max	Min	Condition	Max	Min	Тур	Max	Min	Тур	Max
PCML	Trar	nsmitte	er, receiv transmi	ver, and itter, rec	input referer ceiver, and re	nce cloo eference	ck pins e clock	of the high-s I/O pin speci	peed tra fications	nsceiver , refer to	rs use o Table	the PC e 23 on	ML I/O s page 18	standard 3.	. For
2.5 V	2 375	25	2 625	100	V <sub>CM</sub> =	_	0.05	D <sub>MAX</sub> ≤ 700 Mbps	1.8	0.247	_	0.6	1.125	1.25	1.375
LVDS <sup>(1)</sup>	2.575	2.0	2.025	100	1.25 V	_	1.05	D <sub>MAX</sub> > 700 Mbps	1.55	0.247	_	0.6	1.125	1.25	1.375
BLVDS (5)	2.375	2.5	2.625	100	_	—	_	_	_	_	_	—	_	—	
RSDS (HIO) <sup>(2)</sup>	2.375	2.5	2.625	100	V <sub>CM</sub> = 1.25 V	_	0.3	_	1.4	0.1	0.2	0.6	0.5	1.2	1.4
Mini- LVDS (HIO) <sup>(3)</sup>	2.375	2.5	2.625	200	_	600	0.4	_	1.325	0.25	_	0.6	1	1.2	1.4
LVPECL (4	_	_	_	300	_		0.6	D <sub>MAX</sub> ≤ 700 Mbps	1.8	_	_	_	_	_	_
), (9)				300			1	D <sub>MAX</sub> > 700 Mbps	1.6						

Notes to Table 22:

(1) For optimized LVDS receiver performance, the receiver voltage input range must be between 1.0 V to 1.6 V for data rates above 700 Mbps, and 0 V to 1.85 V for data rates below 700 Mbps.

(2) For optimized RSDS receiver performance, the receiver voltage input range must be between 0.25 V to 1.45 V.

(3) For optimized Mini-LVDS receiver performance, the receiver voltage input range must be between 0.3 V to 1.425 V.

- (4) For optimized LVPECL receiver performance, the receiver voltage input range must be between 0.85 V to 1.75 V for data rate above 700 Mbps and 0.45 V to 1.95 V for data rate below 700 Mbps.
- (5) There are no fixed  $V_{ICM}$ ,  $V_{OD}$ , and  $V_{OCM}$  specifications for BLVDS. They depend on the system topology.
- (6) RL range:  $90 \le RL \le 110 \Omega$ .
- (7) The 1.4-V and 1.5-V PCML transceiver I/O standard specifications are described in "Transceiver Performance Specifications" on page 18.
- (8) The minimum VID value is applicable over the entire common mode range, VCM.
- (9) LVPECL is only supported on dedicated clock input pins.
- (10) Differential inputs are powered by VCCPD which requires 2.5 V.

### **Power Consumption**

Altera offers two ways to estimate power consumption for a design—the Excel-based Early Power Estimator and the Quartus<sup>®</sup> II PowerPlay Power Analyzer feature.

- You typically use the interactive Excel-based Early Power Estimator before designing the FPGA to get a magnitude estimate of the device power. The Quartus II PowerPlay Power Analyzer provides better quality estimates based on the specifics of the design after you complete place-and-route. The PowerPlay Power Analyzer can apply a combination of user-entered, simulation-derived, and estimated signal activities that, when combined with detailed circuit models, yields very accurate power estimates.
- **\*** For more information about power estimation tools, refer to the *PowerPlay Early Power Estimator User Guide* and the *PowerPlay Power Analysis* chapter in the *Quartus II Handbook*.

### **Switching Characteristics**

This section provides performance characteristics of the Stratix V core and periphery blocks.

These characteristics can be designated as Preliminary or Final.

- Preliminary characteristics are created using simulation results, process data, and other known parameters. The title of these tables show the designation as "Preliminary."
- Final numbers are based on actual silicon characterization and testing. The numbers reflect the actual performance of the device under worst-case silicon process, voltage, and junction temperature conditions. There are no designations on finalized tables.

### **Transceiver Performance Specifications**

This section describes transceiver performance specifications.

Table 23 lists the Stratix V GX and GS transceiver specifications.

Table 23.	Transceiver 3	Specifications	for Stratix	V GX	and GS	Devices	(1)	(Part 1	nf 7	۱
Table 20.	TIANSUCIACI	opeonitionationa	IUI UIIAIIA	I UA	anu uu	DEVICES	• •	(1 61 6 1		

Symbol/	Conditions	Tra	nsceive Grade	r Speed 1	Trai	nsceive Grade	r Speed 2	Trai	er Speed e 3	Unit			
Description		Min	Тур	Max	Min	Тур	Max	Min	Тур	Max			
Reference Clock													
Supported I/O	Dedicated reference clock pin	1.2-V	PCML,	1.4-V PCM	IL, 1.5-∖	/ PCML	ML, 2.5-V PCML, Differential LVPECL, LVDS, a HCSL						
Standards	RX reference clock pin			1.4-V PCMI	L, 1.5-V	PCML,	2.5-V PCM	/IL, LVPECL, and LVDS					
Input Reference Clock Frequency (CMU PLL) <sup>(8)</sup>	_	40		710	40	_	710	40	_	710	MHz		
Input Reference Clock Frequency (ATX PLL) <sup>(8)</sup>		100		710	100		710	100		710	MHz		
Rise time	Measure at ±60 mV of differential signal <sup>(26)</sup>			400	_		400			400	ns		
Fall time	Measure at ±60 mV of differential signal <sup>(26)</sup>		_	400	_		400			400	μs		
Duty cycle		45		55	45		55	45	—	55	%		
Spread-spectrum modulating clock frequency	PCI Express® (PCIe <sup>®</sup> )	30		33	30		33	30	_	33	kHz		

Symbol/	Conditions	Tra	nsceive Grade	r Speed 1	Trai	nsceive Grade	r Speed 2	Trai	nsceive Grade	er Speed e 3	Unit
Description		Min	Тур	Max	Min	Тур	Max	Min	Тур	Max	
Spread-spectrum downspread	PCIe	_	0 to 0.5	_	_	0 to 0.5	_	_	0 to 0.5	_	%
On-chip termination resistors <sup>(21)</sup>	_	_	100		_	100		_	100		Ω
Absolute V <sub>MAX</sub> <sup>(5)</sup>	Dedicated reference clock pin	_	_	1.6	_	_	1.6	_	_	1.6	V
	RX reference clock pin	_		1.2		_	1.2			1.2	
Absolute V <sub>MIN</sub>	—	-0.4	-	_	-0.4	_		-0.4	—		V
Peak-to-peak differential input voltage	_	200	_	1600	200	_	1600	200		1600	mV
V <sub>ICM</sub> (AC	Dedicated reference clock pin	1050/	(1000/90	00/850 <sup>(2)</sup>	1050/	1000/9	00/850 <sup>(2)</sup>	1050/	1000/9	00/850 <sup>(2)</sup>	mV
coupled) (9	RX reference clock pin	1	.0/0.9/0	.85 (4)	1.	.0/0.9/0	.85 (4)	1.	.0/0.9/0	.85 <sup>(4)</sup>	V
V <sub>ICM</sub> (DC coupled)	HCSL I/O standard for PCIe reference clock	250		550	250		550	250	_	550	mV
	100 Hz	—	—	-70	—	—	-70	—	—	-70	dBc/Hz
Transmitter	1 kHz	—	—	-90	—	—	-90	—	—	-90	dBc/Hz
REFCLK Phase	10 kHz	—	—	-100	—	—	-100	—	—	-100	dBc/Hz
(622 MHz) <sup>(20)</sup>	100 kHz	—	—	-110	—	—	-110	—	—	-110	dBc/Hz
	≥1 MHz	—	—	-120		—	-120	—	—	-120	dBc/Hz
Transmitter REFCLK Phase Jitter (100 MHz) <sup>(17)</sup>	10 kHz to 1.5 MHz (PCIe)	_	_	3	_	_	3	_	_	3	ps (rms)
R <sub>REF</sub> (19)	_	_	1800 ±1%	_	_	1800 ±1%	_	_	180 0 ±1%	_	Ω
Transceiver Clock	s										
fixedclk <b>clock</b> frequency	PCIe Receiver Detect		100 or 125			100 or 125		_	100 or 125		MHz

### Table 23. Transceiver Specifications for Stratix V GX and GS Devices <sup>(1)</sup> (Part 2 of 7)





Figure 3 shows the Stratix V AC gain curves for GX channels.

Figure 3. AC Gain Curves for GX Channels (full bandwidth)

Stratix V GT devices contain both GX and GT channels. All transceiver specifications for the GX channels not listed in Table 28 are the same as those listed in Table 23.

Table 28 lists the Stratix V GT transceiver specifications.

### Table 28. Transceiver Specifications for Stratix V GT Devices (Part 2 of 5)<sup>(1)</sup>

Symbol/	Conditions	S	Transceive peed Grade	r 2	SI	Fransceive Deed Grade	r 3	Unit
Description		Min	Тур	Max	Min	Тур	Max	
	100 Hz	—	—	-70			-70	
Transmitter REFCLK	1 kHz		_	-90	_	_	-90	
Phase Noise (622	10 kHz		—	-100	_		-100	dBc/Hz
MHz) <sup>(18)</sup>	100 kHz			-110			-110	
	$\geq$ 1 MHz	—	—	-120		_	-120	
Transmitter REFCLK Phase Jitter (100 MHz) <sup>(15)</sup>	10 kHz to 1.5 MHz (PCle)	_	_	3		_	3	ps (rms)
RREF <sup>(17)</sup>	_	_	1800 ± 1%	—	_	1800 ± 1%	_	Ω
Transceiver Clocks								
fixedclk clock frequency	PCIe Receiver Detect	_	100 or 125	_	_	100 or 125	_	MHz
Reconfiguration clock (mgmt_clk_clk) frequency	_	100	_	125	100	_	125	MHz
Receiver	•							
Supported I/O Standards	_		1.4-V PCML	., 1.5-V PCMI	L, 2.5-V PCI	VIL, LVPEC	L, and LVDS	6
Data rate (Standard PCS) <sup>(21)</sup>	GX channels	600	_	8500	600	_	8500	Mbps
Data rate (10G PCS) <sup>(21)</sup>	GX channels	600	_	12,500	600	_	12,500	Mbps
Data rate	GT channels	19,600	—	28,050	19,600		25,780	Mbps
Absolute V <sub>MAX</sub> for a receiver pin <sup>(3)</sup>	GT channels	_	_	1.2	_	_	1.2	V
Absolute V <sub>MIN</sub> for a receiver pin	GT channels	-0.4	_	—	-0.4	_	_	V
Maximum peak-to-peak	GT channels	_		1.6	—	_	1.6	V
differential input voltage V <sub>ID</sub> (diff p-p) before device configuration <sup>(20)</sup>	GX channels				(8)			
	GT channels							
Maximum peak-to-peak differential input voltage $V_{ID}$ (diff p-p) after device	V <sub>CCR_GTB</sub> = 1.05 V (V <sub>ICM</sub> = 0.65 V)	_	_	2.2	_	_	2.2	V
	GX channels		1	1 1	(8)			1
Minimum differential	GT channels	200	_	—	200		_	mV
eye opening at receiver serial input pins <sup>(4)</sup> , <sup>(20)</sup>	GX channels			·	(8)			

Figure 4 shows the differential transmitter output waveform.





Figure 5 shows the Stratix V AC gain curves for GT channels.

Figure 5. AC Gain Curves for GT Channels

### **PLL Specifications**

Table 31 lists the Stratix V PLL specifications when operating in both the commercial junction temperature range (0° to  $85^{\circ}$ C) and the industrial junction temperature range (-40° to  $100^{\circ}$ C).

Table 31. PLL Specifications for Stratix V Devices (Part 1 of 3)

Symbol	Parameter	Min	Тур	Max	Unit
	Input clock frequency (C1, C2, C2L, I2, and I2L speed grades)	5		800 (1)	MHz
f <sub>IN</sub>	Input clock frequency (C3, I3, I3L, and I3YY speed grades)	5		800 (1)	MHz
	Input clock frequency (C4, I4 speed grades)	5	—	650 <sup>(1)</sup>	MHz
f <sub>INPFD</sub>	Input frequency to the PFD	5	—	325	MHz
f <sub>FINPFD</sub>	Fractional Input clock frequency to the PFD	50	—	160	MHz
	PLL VCO operating range (C1, C2, C2L, I2, I2L speed grades)	600	_	1600	MHz
f <sub>VCO</sub> (9)	PLL VCO operating range (C3, I3, I3L, I3YY speed grades)	600		1600	MHz
	PLL VCO operating range (C4, I4 speed grades)	600	—	1300	MHz
t <sub>einduty</sub>	Input clock or external feedback clock input duty cycle	40	—	60	%
	Output frequency for an internal global or regional clock (C1, C2, C2L, I2, I2L speed grades)	_	_	717 <sup>(2)</sup>	MHz
f <sub>OUT</sub>	Output frequency for an internal global or regional clock (C3, I3, I3L speed grades)			650 <sup>(2)</sup>	MHz
	Output frequency for an internal global or regional clock (C4, I4 speed grades)			580 <sup>(2)</sup>	MHz
	Output frequency for an external clock output (C1, C2, C2L, I2, I2L speed grades)			800 <sup>(2)</sup>	MHz
f <sub>OUT_EXT</sub>	Output frequency for an external clock output (C3, I3, I3L speed grades)			667 <sup>(2)</sup>	MHz
	Output frequency for an external clock output (C4, I4 speed grades)			553 <sup>(2)</sup>	MHz
t <sub>outduty</sub>	Duty cycle for a dedicated external clock output (when set to <b>50%</b> )	45	50	55	%
t <sub>FCOMP</sub>	External feedback clock compensation time	_		10	ns
f <sub>dyconfigclk</sub>	Dynamic Configuration Clock used for mgmt_clk and scanclk		_	100	MHz
t <sub>LOCK</sub>	Time required to lock from the end-of-device configuration or deassertion of areset			1	ms
t <sub>DLOCK</sub>	Time required to lock dynamically (after switchover or reconfiguring any non-post-scale counters/delays)			1	ms
	PLL closed-loop low bandwidth	—	0.3	—	MHz
f <sub>CLBW</sub>	PLL closed-loop medium bandwidth	—	1.5	—	MHz
	PLL closed-loop high bandwidth (7)	—	4	-	MHz
t <sub>PLL_PSERR</sub>	Accuracy of PLL phase shift	—	—	±50	ps
t <sub>ARESET</sub>	Minimum pulse width on the areset signal	10	—	_	ns

#### Table 31. PLL Specifications for Stratix V Devices (Part 3 of 3)

Symbol	Parameter	Min	Тур	Max	Unit
f <sub>RES</sub>	Resolution of VCO frequency ( $f_{INPFD} = 100 \text{ MHz}$ )	390625	5.96	0.023	Hz

#### Notes to Table 31:

(1) This specification is limited in the Quartus II software by the I/O maximum frequency. The maximum I/O frequency is different for each I/O standard.

(2) This specification is limited by the lower of the two: I/O  $f_{MAX}$  or  $f_{OUT}$  of the PLL.

- (3) A high input jitter directly affects the PLL output jitter. To have low PLL output clock jitter, you must provide a clean clock source < 120 ps.
- (4)  $f_{REF}$  is fIN/N when N = 1.
- (5) Peak-to-peak jitter with a probability level of 10<sup>-12</sup> (14 sigma, 99.9999999974404% confidence level). The output jitter specification applies to the intrinsic jitter of the PLL, when an input jitter of 30 ps is applied. The external memory interface clock output jitter specifications use a different measurement method and are available in Table 44 on page 52.
- (6) The cascaded PLL specification is only applicable with the following condition: a. Upstream PLL: 0.59Mhz ≤ Upstream PLL BW < 1 MHz b. Downstream PLL: Downstream PLL BW > 2 MHz
- (7) High bandwidth PLL settings are not supported in external feedback mode.
- (8) The external memory interface clock output jitter specifications use a different measurement method, which is available in Table 42 on page 50.
- (9) The VCO frequency reported by the Quartus II software in the PLL Usage Summary section of the compilation report takes into consideration the VCO post-scale counter K value. Therefore, if the counter K has a value of 2, the frequency reported can be lower than the f<sub>VCO</sub> specification.
- (10) This specification only covers fractional PLL for low bandwidth. The  $f_{VCO}$  for fractional value range 0.05 0.95 must be  $\geq$  1000 MHz, while  $f_{VCO}$  for fractional value range 0.20 0.80 must be  $\geq$  1200 MHz.
- (11) This specification only covered fractional PLL for low bandwidth. The  $f_{VC0}$  for fractional value range 0.05-0.95 must be  $\geq$  1000 MHz.
- (12) This specification only covered fractional PLL for low bandwidth. The  $f_{VC0}$  for fractional value range 0.20-0.80 must be  $\geq$  1200 MHz.

#### **DSP Block Specifications**

Table 32 lists the Stratix V DSP block performance specifications.

			F	Peformanc	e				
Mode	C1	C2, C2L	12, 12L	C3	13, 13L, 13YY	C4	14	Unit	
		Modes ı	using one	DSP					
Three 9 x 9	600	600	600	480	480	420	420	MHz	
One 18 x 18	600	600	600	480	480	420	400	MHz	
Two partial 18 x 18 (or 16 x 16)	600	600	600	480	480	420	400	MHz	
One 27 x 27	500	500	500	400	400	350	350	MHz	
One 36 x 18	500	500	500	400	400	350	350	MHz	
One sum of two 18 x 18(One sum of 2 16 x 16)	500	500	500	400	400	350	350	MHz	
One sum of square	500	500	500	400	400	350	350	MHz	
One 18 x 18 plus 36 (a x b) + c	500	500	500	400	400	350	350	MHz	
		Modes u	sing two l	DSPs					
Three 18 x 18	500	500	500	400	400	350	350	MHz	
One sum of four 18 x 18	475	475	475	380	380	300	300	MHz	
One sum of two 27 x 27	465	465	450	380	380	300	290	MHz	
One sum of two 36 x 18	475	475	475	380	380	300	300	MHz	
One complex 18 x 18	500	500	500	400	400	350	350	MHz	
One 36 x 36	475	475	475	380	380	300	300	MHz	

#### Table 32. Block Performance Specifications for Stratix V DSP Devices (Part 1 of 2)

Mode										
	C1	C2, C2L	12, 12L	C3	13, 13L, 13YY	C4	14	Unit		
Modes using Three DSPs										
One complex 18 x 25	425	425	415	340	340	275	265	MHz		
Modes using Four DSPs										
One complex 27 x 27	465	465	465	380	380	300	290	MHz		

#### Table 32. Block Performance Specifications for Stratix V DSP Devices (Part 2 of 2)

### **Memory Block Specifications**

Table 33 lists the Stratix V memory block specifications.

### Table 33. Memory Block Performance Specifications for Stratix V Devices <sup>(1), (2)</sup> (Part 1 of 2)

		<b>Resources Used</b>		Performance							
Memory	Mode	ALUTS	Memory	C1	C2, C2L	C3	C4	12, 12L	13, 13L, 13YY	14	Unit
MLAB	Single port, all supported widths	0	1	450	450	400	315	450	400	315	MHz
	Simple dual-port, x32/x64 depth	0	1	450	450	400	315	450	400	315	MHz
	Simple dual-port, x16 depth <sup>(3)</sup>	0	1	675	675	533	400	675	533	400	MHz
	ROM, all supported widths	0	1	600	600	500	450	600	500	450	MHz

		Resour	ces Used			Ρε	erforman	ce			
Memory	Mode	ALUTS	Memory	C1	C2, C2L	C3	C4	12, 12L	13, 13L, 13YY	14	Unit
	Single-port, all supported widths	0	1	700	700	650	550	700	500	450	MHz
	Simple dual-port, all supported widths	0	1	700	700	650	550	700	500	450	MHz
	Simple dual-port with the read-during-write option set to <b>Old Data</b> , all supported widths	0	1	525	525	455	400	525	455	400	MHz
M20K Block	Simple dual-port with ECC enabled, 512 × 32	0	1	450	450	400	350	450	400	350	MHz
	Simple dual-port with ECC and optional pipeline registers enabled, 512 × 32	0	1	600	600	500	450	600	500	450	MHz
	True dual port, all supported widths	0	1	700	700	650	550	700	500	450	MHz
	ROM, all supported widths	0	1	700	700	650	550	700	500	450	MHz

#### Table 33. Memory Block Performance Specifications for Stratix V Devices <sup>(1), (2)</sup> (Part 2 of 2)

#### Notes to Table 33:

(1) To achieve the maximum memory block performance, use a memory block clock that comes through global clock routing from an on-chip PLL set to **50**% output duty cycle. Use the Quartus II software to report timing for this and other memory block clocking schemes.

(2) When you use the error detection cyclical redundancy check (CRC) feature, there is no degradation in F<sub>MAX</sub>.

(3) The F<sub>MAX</sub> specification is only achievable with Fitter options, MLAB Implementation In 16-Bit Deep Mode enabled.

### **Temperature Sensing Diode Specifications**

Table 34 lists the internal TSD specification.

#### **Table 34. Internal Temperature Sensing Diode Specification**

Temperature Range	Accuracy	Offset Calibrated Option	Sampling Rate	Conversion Time	Resolution	Minimum Resolution with no Missing Codes
-40°C to 100°C	±8°C	No	1 MHz, 500 KHz	< 100 ms	8 bits	8 bits

Table 35 lists the specifications for the Stratix V external temperature sensing diode.

Table 35.	External	Temperature	Sensing Dic	de Specifica	ations for Stratix	V Devices
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Description	Min	Тур	Max	Unit
I <sub>bias</sub> , diode source current	8	—	200	μA
V <sub>bias,</sub> voltage across diode	0.3	—	0.9	V
Series resistance	—	_	< 1	Ω
Diode ideality factor	1.006	1.008	1.010	_

Symbol	Parameter	Minimum	Maximum	Units
t <sub>CD2UM</sub>	CONF_DONE high to user mode $(3)$	175	437	μS
t <sub>CD2CU</sub>	CONF_DONE high to CLKUSR enabled	4 × maximum DCLK period	_	—
t <sub>CD2UMC</sub>	CONF_DONE high to user mode with CLKUSR option on	t <sub>cd2cu</sub> + (8576 × clkusr period)	_	—

Table 53. AS Timing Parameters for AS  $\times$ 1 and AS  $\times$ 4 Configurations in Stratix V Devices <sup>(1), (2)</sup> (Part 2 of 2)

#### Notes to Table 53:

(1) The minimum and maximum numbers apply only if you choose the internal oscillator as the clock source for initializing the device.

(2) t<sub>CF2CD</sub>, t<sub>CF2ST0</sub>, t<sub>CF2ST0</sub>, t<sub>CF6</sub>, t<sub>STATUS</sub>, and t<sub>CF2ST1</sub> timing parameters are identical to the timing parameters for PS mode listed in Table 54 on page 63.

(3) To enable the CLKUSR pin as the initialization clock source and to obtain the maximum frequency specification on this pin, refer to the Initialization section of the "Configuration, Design Security, and Remote System Upgrades in Stratix V Devices" chapter.

### **Passive Serial Configuration Timing**

Figure 15 shows the timing waveform for a passive serial (PS) configuration when using a MAX II device, MAX V device, or microprocessor as an external host.

Figure 15. PS Configuration Timing Waveform <sup>(1)</sup>



#### Notes to Figure 15:

- (1) The beginning of this waveform shows the device in user mode. In user mode, nCONFIG, nSTATUS, and CONF\_DONE are at logic high levels. When nCONFIG is pulled low, a reconfiguration cycle begins.
- (2) After power-up, the Stratix V device holds nSTATUS low for the time of the POR delay.
- (3) After power-up, before and during configuration, CONF DONE is low.
- (4) Do not leave DCLK floating after configuration. You can drive it high or low, whichever is more convenient.
- (5) DATAO is available as a user I/O pin after configuration. The state of this pin depends on the dual-purpose pin settings in the **Device and Pins Option**.
- (6) To ensure a successful configuration, send the entire configuration data to the Stratix V device. CONF\_DONE is released high after the Stratix V device receives all the configuration data successfully. After CONF\_DONE goes high, send two additional falling edges on DCLK to begin initialization and enter user mode.
- (7) After the option bit to enable the INIT DONE pin is configured into the device, the INIT DONE goes low.

### **Remote System Upgrades**

Table 56 lists the timing parameter specifications for the remote system upgrade circuitry.

Table 56. Remote System Upgrade Circuitry Timing Specificatio
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Parameter	Minimum	Maximum	Unit
t <sub>RU_nCONFIG</sub> <sup>(1)</sup>	250	—	ns
t <sub>RU_nRSTIMER</sub> <sup>(2)</sup>	250	_	ns

#### Notes to Table 56:

- (1) This is equivalent to strobing the reconfiguration input of the ALTREMOTE\_UPDATE megafunction high for the minimum timing specification. For more information, refer to the Remote System Upgrade State Machine section of the "Configuration, Design Security, and Remote System Upgrades in Stratix V Devices" chapter.
- (2) This is equivalent to strobing the reset\_timer input of the ALTREMOTE\_UPDATE megafunction high for the minimum timing specification. For more information, refer to the User Watchdog Timer section of the "Configuration, Design Security, and Remote System Upgrades in Stratix V Devices" chapter.

### **User Watchdog Internal Circuitry Timing Specification**

Table 57 lists the operating range of the 12.5-MHz internal oscillator.

#### Table 57. 12.5-MHz Internal Oscillator Specifications

Minimum	Typical	Maximum	Units
5.3	7.9	12.5	MHz

# I/O Timing

Altera offers two ways to determine I/O timing—the Excel-based I/O Timing and the Quartus II Timing Analyzer.

Excel-based I/O timing provides pin timing performance for each device density and speed grade. The data is typically used prior to designing the FPGA to get an estimate of the timing budget as part of the link timing analysis. The Quartus II Timing Analyzer provides a more accurate and precise I/O timing data based on the specifics of the design after you complete place-and-route.

 You can download the Excel-based I/O Timing spreadsheet from the Stratix V Devices Documentation web page.

### **Programmable IOE Delay**

Table 58 lists the Stratix V IOE programmable delay settings.

Table 58. IOE Programmable Delay for Stratix V Devices (Part 1 of 2)

Parameter Available (1) Settings	Available	Min	Fast Model		Slow Model								
	Offset (2)	Industrial	Commercial	C1	C2	C3	C4	12	13, 13YY	14	Unit		
D1	64	0	0.464	0.493	0.838	0.838	0.924	1.011	0.844	0.921	1.006	ns	
D2	32	0	0.230	0.244	0.415	0.415	0.459	0.503	0.417	0.456	0.500	ns	

Parameter A	Available Settings	Available M	Min	Fast	Model	Slow Model								
		<b>Offset</b> (2)	Industrial	Commercial	C1	C2	C3	C4	12	13, 13YY	14	Unit		
D3	8	0	1.587	1.699	2.793	2.793	2.992	3.192	2.811	3.047	3.257	ns		
D4	64	0	0.464	0.492	0.838	0.838	0.924	1.011	0.843	0.920	1.006	ns		
D5	64	0	0.464	0.493	0.838	0.838	0.924	1.011	0.844	0.921	1.006	ns		
D6	32	0	0.229	0.244	0.415	0.415	0.458	0.503	0.418	0.456	0.499	ns		

Table 58.	IOE Pro	grammable De	lay for	Stratix V	V Devices	(Part 2 of 2	)
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#### Notes to Table 58:

(1) You can set this value in the Quartus II software by selecting D1, D2, D3, D5, and D6 in the Assignment Name column of Assignment Editor.

(2) Minimum offset does not include the intrinsic delay.

### **Programmable Output Buffer Delay**

Table 59 lists the delay chain settings that control the rising and falling edge delays of the output buffer. The default delay is 0 ps.

Symbol	Parameter	Typical	Unit
		0 (default)	ps
Dauman	Rising and/or falling edge delay	25	ps
DOUTBUF		50	ps
		75	ps

Note to Table 59:

(1) You can set the programmable output buffer delay in the Quartus II software by setting the Output Buffer Delay Control assignment to either positive, negative, or both edges, with the specific values stated here (in ps) for the Output Buffer Delay assignment.

## Glossary

Table 60 lists the glossary for this chapter.

Table 60. Glossary (Part 1 of 4)

Letter	Subject	Definitions
Α		
В	—	—
С		
D	—	_
E	—	_
F	f <sub>HSCLK</sub>	Left and right PLL input clock frequency.
	f <sub>HSDR</sub>	High-speed I/O block—Maximum and minimum <b>LVDS</b> data transfer rate (f <sub>HSDR</sub> = 1/TUI), non-DPA.
	f <sub>hsdrdpa</sub>	High-speed I/O block—Maximum and minimum <b>LVDS</b> data transfer rate (f <sub>HSDRDPA</sub> = 1/TUI), DPA.

# **Document Revision History**

Table 61 lists the revision history for this chapter.

 Table 61. Document Revision History (Part 1 of 3)

Date	Version	Changes	
June 2018	3.9	<ul> <li>Added the "Stratix V Device Overshoot Duration" figure.</li> </ul>	
	3.8	Added a footnote to the "High-Speed I/O Specifications for Stratix V Devices" table.	
		<ul> <li>Changed the minimum value for t<sub>CD2UMC</sub> in the "PS Timing Parameters for Stratix V Devices" table.</li> </ul>	
		<ul> <li>Changed the condition for 100-Ω R<sub>D</sub> in the "OCT Without Calibration Resistance Tolerance Specifications for Stratix V Devices" table.</li> </ul>	
April 2017		<ul> <li>Changed the minimum value for t<sub>CD2UMC</sub> in the "AS Timing Parameters for AS '1 and AS '4 Configurations in Stratix V Devices" table</li> </ul>	
		<ul> <li>Changed the minimum value for t<sub>CD2UMC</sub> in the "FPP Timing Parameters for Stratix V Devices When the DCLK-to-DATA[] Ratio is &gt;1" table.</li> </ul>	
		<ul> <li>Changed the minimum value for t<sub>CD2UMC</sub> in the "FPP Timing Parameters for Stratix V Devices When the DCLK-to-DATA[] Ratio is &gt;1" table.</li> </ul>	
		<ul> <li>Changed the minimum number of clock cycles value in the "Initialization Clock Source Option and the Maximum Frequency" table.</li> </ul>	
June 2016	3.7	<ul> <li>Added the V<sub>ID</sub> minimum specification for LVPECL in the "Differential I/O Standard Specifications for Stratix V Devices" table</li> </ul>	
		<ul> <li>Added the I<sub>OUT</sub> specification to the "Absolute Maximum Ratings for Stratix V Devices" table.</li> </ul>	
December 2015	3.6	Added a footnote to the "High-Speed I/O Specifications for Stratix V Devices" table.	
December 2015	3.5	<ul> <li>Changed the transmitter, receiver, and ATX PLL data rate specifications in the "Transceiver Specifications for Stratix V GX and GS Devices" table.</li> </ul>	
December 2015		<ul> <li>Changed the configuration .rbf sizes in the "Uncompressed .rbf Sizes for Stratix V Devices" table.</li> </ul>	
	3.4	• Changed the data rate specification for transceiver speed grade 3 in the following tables:	
		<ul> <li>"Transceiver Specifications for Stratix V GX and GS Devices"</li> </ul>	
		<ul> <li>"Stratix V Standard PCS Approximate Maximum Date Rate"</li> </ul>	
		<ul> <li>"Stratix V 10G PCS Approximate Maximum Data Rate"</li> </ul>	
July 2015		<ul> <li>Changed the conditions for reference clock rise and fall time, and added a note to the "Transceiver Specifications for Stratix V GX and GS Devices" table.</li> </ul>	
		<ul> <li>Added a note to the "Minimum differential eye opening at receiver serial input pins" specification in the "Transceiver Specifications for Stratix V GX and GS Devices" table.</li> </ul>	
		<ul> <li>Changed the t<sub>c0</sub> maximum value in the "AS Timing Parameters for AS '1 and AS '4 Configurations in Stratix V Devices" table.</li> </ul>	
		<ul> <li>Removed the CDR ppm tolerance specification from the "Transceiver Specifications for Stratix V GX and GS Devices" table.</li> </ul>	