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### Understanding [Embedded - FPGAs \(Field Programmable Gate Array\)](#)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

### Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

#### Details

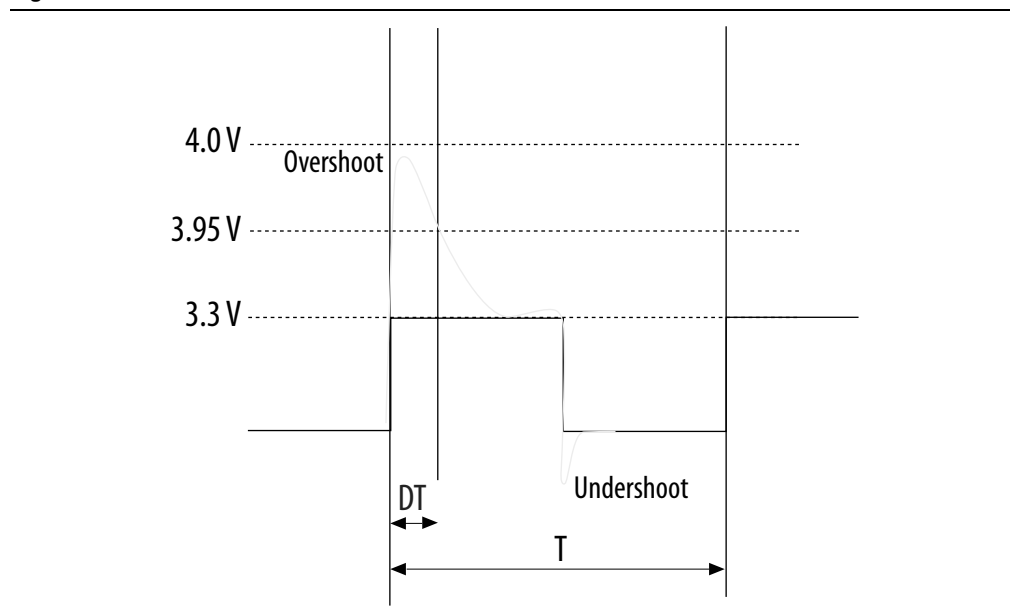
|                                |                                                                                                                                       |
|--------------------------------|---------------------------------------------------------------------------------------------------------------------------------------|
| Product Status                 | Obsolete                                                                                                                              |
| Number of LABs/CLBs            | 185000                                                                                                                                |
| Number of Logic Elements/Cells | 490000                                                                                                                                |
| Total RAM Bits                 | 41984000                                                                                                                              |
| Number of I/O                  | 432                                                                                                                                   |
| Number of Gates                | -                                                                                                                                     |
| Voltage - Supply               | 0.82V ~ 0.88V                                                                                                                         |
| Mounting Type                  | Surface Mount                                                                                                                         |
| Operating Temperature          | -40°C ~ 100°C (TJ)                                                                                                                    |
| Package / Case                 | 1517-FBGA (40x40)                                                                                                                     |
| Supplier Device Package        | 1517-FBGA (40x40)                                                                                                                     |
| Purchase URL                   | <a href="https://www.e-xfl.com/product-detail/intel/5sgxeb5r2f40i2ln">https://www.e-xfl.com/product-detail/intel/5sgxeb5r2f40i2ln</a> |

Table 5 lists the maximum allowed input overshoot voltage and the duration of the overshoot voltage as a percentage of device lifetime. The maximum allowed overshoot duration is specified as a percentage of high time over the lifetime of the device. A DC signal is equivalent to 100% of the duty cycle. For example, a signal that overshoots to 3.95 V can be at 3.95 V for only ~21% over the lifetime of the device; for a device lifetime of 10 years, the overshoot duration amounts to ~2 years.

**Table 5. Maximum Allowed Overshoot During Transitions**

| Symbol     | Description      | Condition (V) | Overshoot Duration as %<br>@ $T_J = 100^{\circ}\text{C}$ | Unit |
|------------|------------------|---------------|----------------------------------------------------------|------|
| $V_i$ (AC) | AC input voltage | 3.8           | 100                                                      | %    |
|            |                  | 3.85          | 64                                                       | %    |
|            |                  | 3.9           | 36                                                       | %    |
|            |                  | 3.95          | 21                                                       | %    |
|            |                  | 4             | 12                                                       | %    |
|            |                  | 4.05          | 7                                                        | %    |
|            |                  | 4.1           | 4                                                        | %    |
|            |                  | 4.15          | 2                                                        | %    |
|            |                  | 4.2           | 1                                                        | %    |

**Figure 1. Stratix V Device Overshoot Duration**



## Recommended Operating Conditions

This section lists the functional operating limits for the AC and DC parameters for Stratix V devices. Table 6 lists the steady-state voltage and current values expected from Stratix V devices. Power supply ramps must all be strictly monotonic, without plateaus.

**Table 6. Recommended Operating Conditions for Stratix V Devices (Part 1 of 2)**

| Symbol                            | Description                                                                                                       | Condition  | Min <sup>(4)</sup> | Typ  | Max <sup>(4)</sup> | Unit |
|-----------------------------------|-------------------------------------------------------------------------------------------------------------------|------------|--------------------|------|--------------------|------|
| V <sub>CC</sub>                   | Core voltage and periphery circuitry power supply (C1, C2, I2, and I3YY speed grades)                             | —          | 0.87               | 0.9  | 0.93               | V    |
|                                   | Core voltage and periphery circuitry power supply (C2L, C3, C4, I2L, I3, I3L, and I4 speed grades) <sup>(3)</sup> | —          | 0.82               | 0.85 | 0.88               | V    |
| V <sub>CCPT</sub>                 | Power supply for programmable power technology                                                                    | —          | 1.45               | 1.50 | 1.55               | V    |
| V <sub>CC_AUX</sub>               | Auxiliary supply for the programmable power technology                                                            | —          | 2.375              | 2.5  | 2.625              | V    |
| V <sub>CCPD</sub> <sup>(1)</sup>  | I/O pre-driver (3.0 V) power supply                                                                               | —          | 2.85               | 3.0  | 3.15               | V    |
|                                   | I/O pre-driver (2.5 V) power supply                                                                               | —          | 2.375              | 2.5  | 2.625              | V    |
| V <sub>CCIO</sub>                 | I/O buffers (3.0 V) power supply                                                                                  | —          | 2.85               | 3.0  | 3.15               | V    |
|                                   | I/O buffers (2.5 V) power supply                                                                                  | —          | 2.375              | 2.5  | 2.625              | V    |
|                                   | I/O buffers (1.8 V) power supply                                                                                  | —          | 1.71               | 1.8  | 1.89               | V    |
|                                   | I/O buffers (1.5 V) power supply                                                                                  | —          | 1.425              | 1.5  | 1.575              | V    |
|                                   | I/O buffers (1.35 V) power supply                                                                                 | —          | 1.283              | 1.35 | 1.45               | V    |
|                                   | I/O buffers (1.25 V) power supply                                                                                 | —          | 1.19               | 1.25 | 1.31               | V    |
|                                   | I/O buffers (1.2 V) power supply                                                                                  | —          | 1.14               | 1.2  | 1.26               | V    |
| V <sub>CCPGM</sub>                | Configuration pins (3.0 V) power supply                                                                           | —          | 2.85               | 3.0  | 3.15               | V    |
|                                   | Configuration pins (2.5 V) power supply                                                                           | —          | 2.375              | 2.5  | 2.625              | V    |
|                                   | Configuration pins (1.8 V) power supply                                                                           | —          | 1.71               | 1.8  | 1.89               | V    |
| V <sub>CCA_FPLL</sub>             | PLL analog voltage regulator power supply                                                                         | —          | 2.375              | 2.5  | 2.625              | V    |
| V <sub>CCD_FPLL</sub>             | PLL digital voltage regulator power supply                                                                        | —          | 1.45               | 1.5  | 1.55               | V    |
| V <sub>CCBAT</sub> <sup>(2)</sup> | Battery back-up power supply (For design security volatile key register)                                          | —          | 1.2                | —    | 3.0                | V    |
| V <sub>I</sub>                    | DC input voltage                                                                                                  | —          | −0.5               | —    | 3.6                | V    |
| V <sub>O</sub>                    | Output voltage                                                                                                    | —          | 0                  | —    | V <sub>CCIO</sub>  | V    |
| T <sub>J</sub>                    | Operating junction temperature                                                                                    | Commercial | 0                  | —    | 85                 | °C   |
|                                   |                                                                                                                   | Industrial | −40                | —    | 100                | °C   |

**Table 18. Single-Ended SSTL, HSTL, and HSUL I/O Reference Voltage Specifications for Stratix V Devices**

| I/O Standard            | $V_{CCIO}$ (V) |      |       | $V_{REF}$ (V)     |                  |                   | $V_{TT}$ (V)      |                  |                   |
|-------------------------|----------------|------|-------|-------------------|------------------|-------------------|-------------------|------------------|-------------------|
|                         | Min            | Typ  | Max   | Min               | Typ              | Max               | Min               | Typ              | Max               |
| SSTL-2<br>Class I, II   | 2.375          | 2.5  | 2.625 | $0.49 * V_{CCIO}$ | $0.5 * V_{CCIO}$ | $0.51 * V_{CCIO}$ | $V_{REF} - 0.04$  | $V_{REF}$        | $V_{REF} + 0.04$  |
| SSTL-18<br>Class I, II  | 1.71           | 1.8  | 1.89  | 0.833             | 0.9              | 0.969             | $V_{REF} - 0.04$  | $V_{REF}$        | $V_{REF} + 0.04$  |
| SSTL-15<br>Class I, II  | 1.425          | 1.5  | 1.575 | $0.49 * V_{CCIO}$ | $0.5 * V_{CCIO}$ | $0.51 * V_{CCIO}$ | $0.49 * V_{CCIO}$ | $0.5 * V_{CCIO}$ | $0.51 * V_{CCIO}$ |
| SSTL-135<br>Class I, II | 1.283          | 1.35 | 1.418 | $0.49 * V_{CCIO}$ | $0.5 * V_{CCIO}$ | $0.51 * V_{CCIO}$ | $0.49 * V_{CCIO}$ | $0.5 * V_{CCIO}$ | $0.51 * V_{CCIO}$ |
| SSTL-125<br>Class I, II | 1.19           | 1.25 | 1.26  | $0.49 * V_{CCIO}$ | $0.5 * V_{CCIO}$ | $0.51 * V_{CCIO}$ | $0.49 * V_{CCIO}$ | $0.5 * V_{CCIO}$ | $0.51 * V_{CCIO}$ |
| SSTL-12<br>Class I, II  | 1.14           | 1.20 | 1.26  | $0.49 * V_{CCIO}$ | $0.5 * V_{CCIO}$ | $0.51 * V_{CCIO}$ | $0.49 * V_{CCIO}$ | $0.5 * V_{CCIO}$ | $0.51 * V_{CCIO}$ |
| HSTL-18<br>Class I, II  | 1.71           | 1.8  | 1.89  | 0.85              | 0.9              | 0.95              | —                 | $V_{CCIO}/2$     | —                 |
| HSTL-15<br>Class I, II  | 1.425          | 1.5  | 1.575 | 0.68              | 0.75             | 0.9               | —                 | $V_{CCIO}/2$     | —                 |
| HSTL-12<br>Class I, II  | 1.14           | 1.2  | 1.26  | $0.47 * V_{CCIO}$ | $0.5 * V_{CCIO}$ | $0.53 * V_{CCIO}$ | —                 | $V_{CCIO}/2$     | —                 |
| HSUL-12                 | 1.14           | 1.2  | 1.3   | $0.49 * V_{CCIO}$ | $0.5 * V_{CCIO}$ | $0.51 * V_{CCIO}$ | —                 | —                | —                 |

**Table 19. Single-Ended SSTL, HSTL, and HSUL I/O Standards Signal Specifications for Stratix V Devices (Part 1 of 2)**

| I/O Standard            | $V_{IL(DC)}$ (V) |                   | $V_{IH(DC)}$ (V)  |                  | $V_{IL(AC)}$ (V)  | $V_{IH(AC)}$ (V)  | $V_{OL}$ (V)     | $V_{OH}$ (V)      | $I_{OI}$ (mA) | $I_{OH}$ (mA) |
|-------------------------|------------------|-------------------|-------------------|------------------|-------------------|-------------------|------------------|-------------------|---------------|---------------|
|                         | Min              | Max               | Min               | Max              | Max               | Min               | Max              | Min               |               |               |
| SSTL-2<br>Class I       | -0.3             | $V_{REF} - 0.15$  | $V_{REF} + 0.15$  | $V_{CCIO} + 0.3$ | $V_{REF} - 0.31$  | $V_{REF} + 0.31$  | $V_{TT} - 0.608$ | $V_{TT} + 0.608$  | 8.1           | -8.1          |
| SSTL-2<br>Class II      | -0.3             | $V_{REF} - 0.15$  | $V_{REF} + 0.15$  | $V_{CCIO} + 0.3$ | $V_{REF} - 0.31$  | $V_{REF} + 0.31$  | $V_{TT} - 0.81$  | $V_{TT} + 0.81$   | 16.2          | -16.2         |
| SSTL-18<br>Class I      | -0.3             | $V_{REF} - 0.125$ | $V_{REF} + 0.125$ | $V_{CCIO} + 0.3$ | $V_{REF} - 0.25$  | $V_{REF} + 0.25$  | $V_{TT} - 0.603$ | $V_{TT} + 0.603$  | 6.7           | -6.7          |
| SSTL-18<br>Class II     | -0.3             | $V_{REF} - 0.125$ | $V_{REF} + 0.125$ | $V_{CCIO} + 0.3$ | $V_{REF} - 0.25$  | $V_{REF} + 0.25$  | 0.28             | $V_{CCIO} - 0.28$ | 13.4          | -13.4         |
| SSTL-15<br>Class I      | —                | $V_{REF} - 0.1$   | $V_{REF} + 0.1$   | —                | $V_{REF} - 0.175$ | $V_{REF} + 0.175$ | $0.2 * V_{CCIO}$ | $0.8 * V_{CCIO}$  | 8             | -8            |
| SSTL-15<br>Class II     | —                | $V_{REF} - 0.1$   | $V_{REF} + 0.1$   | —                | $V_{REF} - 0.175$ | $V_{REF} + 0.175$ | $0.2 * V_{CCIO}$ | $0.8 * V_{CCIO}$  | 16            | -16           |
| SSTL-135<br>Class I, II | —                | $V_{REF} - 0.09$  | $V_{REF} + 0.09$  | —                | $V_{REF} - 0.16$  | $V_{REF} + 0.16$  | $0.2 * V_{CCIO}$ | $0.8 * V_{CCIO}$  | —             | —             |
| SSTL-125<br>Class I, II | —                | $V_{REF} - 0.85$  | $V_{REF} + 0.85$  | —                | $V_{REF} - 0.15$  | $V_{REF} + 0.15$  | $0.2 * V_{CCIO}$ | $0.8 * V_{CCIO}$  | —             | —             |
| SSTL-12<br>Class I, II  | —                | $V_{REF} - 0.1$   | $V_{REF} + 0.1$   | —                | $V_{REF} - 0.15$  | $V_{REF} + 0.15$  | $0.2 * V_{CCIO}$ | $0.8 * V_{CCIO}$  | —             | —             |

**Table 21. Differential HSTL and HSUL I/O Standards for Stratix V Devices (Part 2 of 2)**

| I/O Standard        | V <sub>CCIO</sub> (V) |     |      | V <sub>DIF(DC)</sub> (V) |                         | V <sub>X(AC)</sub> (V)       |                           |                              | V <sub>CM(DC)</sub> (V)   |                           |                           | V <sub>DIF(AC)</sub> (V) |                          |
|---------------------|-----------------------|-----|------|--------------------------|-------------------------|------------------------------|---------------------------|------------------------------|---------------------------|---------------------------|---------------------------|--------------------------|--------------------------|
|                     | Min                   | Typ | Max  | Min                      | Max                     | Min                          | Typ                       | Max                          | Min                       | Typ                       | Max                       | Min                      | Max                      |
| HSTL-12 Class I, II | 1.14                  | 1.2 | 1.26 | 0.16                     | V <sub>CCIO</sub> + 0.3 | —                            | 0.5*<br>V <sub>CCIO</sub> | —                            | 0.4*<br>V <sub>CCIO</sub> | 0.5*<br>V <sub>CCIO</sub> | 0.6*<br>V <sub>CCIO</sub> | 0.3                      | V <sub>CCIO</sub> + 0.48 |
| HSUL-12             | 1.14                  | 1.2 | 1.3  | 0.26                     | 0.26                    | 0.5*V <sub>CCIO</sub> – 0.12 | 0.5*<br>V <sub>CCIO</sub> | 0.5*V <sub>CCIO</sub> + 0.12 | 0.4*<br>V <sub>CCIO</sub> | 0.5*<br>V <sub>CCIO</sub> | 0.6*<br>V <sub>CCIO</sub> | 0.44                     | 0.44                     |

**Table 22. Differential I/O Standard Specifications for Stratix V Devices <sup>(7)</sup>**

| I/O Standard                   | V <sub>CCIO</sub> (V) <sup>(10)</sup>                                                                                                                                                                                |     |       | V <sub>ID</sub> (mV) <sup>(8)</sup> |                          |     | V <sub>ICM(DC)</sub> (V) |                             |       | V <sub>OD</sub> (V) <sup>(6)</sup> |     |     | V <sub>OCM</sub> (V) <sup>(6)</sup> |      |       |
|--------------------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----|-------|-------------------------------------|--------------------------|-----|--------------------------|-----------------------------|-------|------------------------------------|-----|-----|-------------------------------------|------|-------|
|                                | Min                                                                                                                                                                                                                  | Typ | Max   | Min                                 | Condition                | Max | Min                      | Condition                   | Max   | Min                                | Typ | Max | Min                                 | Typ  | Max   |
| PCML                           | Transmitter, receiver, and input reference clock pins of the high-speed transceivers use the PCML I/O standard. For transmitter, receiver, and reference clock I/O pin specifications, refer to Table 23 on page 18. |     |       |                                     |                          |     |                          |                             |       |                                    |     |     |                                     |      |       |
| 2.5 V LVDS <sup>(1)</sup>      | 2.375                                                                                                                                                                                                                | 2.5 | 2.625 | 100                                 | V <sub>CM</sub> = 1.25 V | —   | 0.05                     | D <sub>MAX</sub> ≤ 700 Mbps | 1.8   | 0.247                              | —   | 0.6 | 1.125                               | 1.25 | 1.375 |
|                                |                                                                                                                                                                                                                      |     |       |                                     |                          | —   | 1.05                     | D <sub>MAX</sub> > 700 Mbps | 1.55  | 0.247                              | —   | 0.6 | 1.125                               | 1.25 | 1.375 |
| BLVDS <sup>(5)</sup>           | 2.375                                                                                                                                                                                                                | 2.5 | 2.625 | 100                                 | —                        | —   | —                        | —                           | —     | —                                  | —   | —   | —                                   | —    | —     |
| RSDS (HIO) <sup>(2)</sup>      | 2.375                                                                                                                                                                                                                | 2.5 | 2.625 | 100                                 | V <sub>CM</sub> = 1.25 V | —   | 0.3                      | —                           | 1.4   | 0.1                                | 0.2 | 0.6 | 0.5                                 | 1.2  | 1.4   |
| Mini-LVDS (HIO) <sup>(3)</sup> | 2.375                                                                                                                                                                                                                | 2.5 | 2.625 | 200                                 | —                        | 600 | 0.4                      | —                           | 1.325 | 0.25                               | —   | 0.6 | 1                                   | 1.2  | 1.4   |
| LVPECL <sup>(4), (9)</sup>     | —                                                                                                                                                                                                                    | —   | —     | 300                                 | —                        | —   | 0.6                      | D <sub>MAX</sub> ≤ 700 Mbps | 1.8   | —                                  | —   | —   | —                                   | —    | —     |
|                                | —                                                                                                                                                                                                                    | —   | —     | 300                                 | —                        | —   | 1                        | D <sub>MAX</sub> > 700 Mbps | 1.6   | —                                  | —   | —   | —                                   | —    | —     |

**Notes to Table 22:**

- (1) For optimized LVDS receiver performance, the receiver voltage input range must be between 1.0 V to 1.6 V for data rates above 700 Mbps, and 0 V to 1.85 V for data rates below 700 Mbps.
- (2) For optimized RSDS receiver performance, the receiver voltage input range must be between 0.25 V to 1.45 V.
- (3) For optimized Mini-LVDS receiver performance, the receiver voltage input range must be between 0.3 V to 1.425 V.
- (4) For optimized LVPECL receiver performance, the receiver voltage input range must be between 0.85 V to 1.75 V for data rate above 700 Mbps and 0.45 V to 1.95 V for data rate below 700 Mbps.
- (5) There are no fixed V<sub>ICM</sub>, V<sub>OD</sub>, and V<sub>OCM</sub> specifications for BLVDS. They depend on the system topology.
- (6) RL range: 90 ≤ RL ≤ 110 Ω.
- (7) The 1.4-V and 1.5-V PCML transceiver I/O standard specifications are described in “Transceiver Performance Specifications” on page 18.
- (8) The minimum V<sub>ID</sub> value is applicable over the entire common mode range, V<sub>CM</sub>.
- (9) LVPECL is only supported on dedicated clock input pins.
- (10) Differential inputs are powered by VCCPD which requires 2.5 V.

## Power Consumption

Altera offers two ways to estimate power consumption for a design—the Excel-based Early Power Estimator and the Quartus® II PowerPlay Power Analyzer feature.

**Table 23. Transceiver Specifications for Stratix V GX and GS Devices <sup>(1)</sup> (Part 2 of 7)**

| Symbol/<br>Description                                             | Conditions                                             | Transceiver Speed<br>Grade 1     |                   |      | Transceiver Speed<br>Grade 2     |                   |      | Transceiver Speed<br>Grade 3     |                   |      | Unit        |
|--------------------------------------------------------------------|--------------------------------------------------------|----------------------------------|-------------------|------|----------------------------------|-------------------|------|----------------------------------|-------------------|------|-------------|
|                                                                    |                                                        | Min                              | Typ               | Max  | Min                              | Typ               | Max  | Min                              | Typ               | Max  |             |
| Spread-spectrum<br>downspread                                      | PCIe                                                   | —                                | 0 to<br>-0.5      | —    | —                                | 0 to<br>-0.5      | —    | —                                | 0 to<br>-0.5      | —    | %           |
| On-chip<br>termination<br>resistors <sup>(21)</sup>                | —                                                      | —                                | 100               | —    | —                                | 100               | —    | —                                | 100               | —    | $\Omega$    |
| Absolute $V_{MAX}$ <sup>(5)</sup>                                  | Dedicated<br>reference<br>clock pin                    | —                                | —                 | 1.6  | —                                | —                 | 1.6  | —                                | —                 | 1.6  | V           |
|                                                                    | RX reference<br>clock pin                              | —                                | —                 | 1.2  | —                                | —                 | 1.2  | —                                | —                 | 1.2  |             |
| Absolute $V_{MIN}$                                                 | —                                                      | -0.4                             | —                 | —    | -0.4                             | —                 | —    | -0.4                             | —                 | —    | V           |
| Peak-to-peak<br>differential input<br>voltage                      | —                                                      | 200                              | —                 | 1600 | 200                              | —                 | 1600 | 200                              | —                 | 1600 | mV          |
| $V_{ICM}$ (AC<br>coupled) <sup>(3)</sup>                           | Dedicated<br>reference<br>clock pin                    | 1050/1000/900/850 <sup>(2)</sup> |                   |      | 1050/1000/900/850 <sup>(2)</sup> |                   |      | 1050/1000/900/850 <sup>(2)</sup> |                   |      | mV          |
|                                                                    | RX reference<br>clock pin                              | 1.0/0.9/0.85 <sup>(4)</sup>      |                   |      | 1.0/0.9/0.85 <sup>(4)</sup>      |                   |      | 1.0/0.9/0.85 <sup>(4)</sup>      |                   |      | V           |
| $V_{ICM}$ (DC coupled)                                             | HCSL I/O<br>standard for<br>PCIe<br>reference<br>clock | 250                              | —                 | 550  | 250                              | —                 | 550  | 250                              | —                 | 550  | mV          |
| Transmitter<br>REFCLK Phase<br>Noise<br>(622 MHz) <sup>(20)</sup>  | 100 Hz                                                 | —                                | —                 | -70  | —                                | —                 | -70  | —                                | —                 | -70  | dBc/Hz      |
|                                                                    | 1 kHz                                                  | —                                | —                 | -90  | —                                | —                 | -90  | —                                | —                 | -90  | dBc/Hz      |
|                                                                    | 10 kHz                                                 | —                                | —                 | -100 | —                                | —                 | -100 | —                                | —                 | -100 | dBc/Hz      |
|                                                                    | 100 kHz                                                | —                                | —                 | -110 | —                                | —                 | -110 | —                                | —                 | -110 | dBc/Hz      |
|                                                                    | $\geq 1$ MHz                                           | —                                | —                 | -120 | —                                | —                 | -120 | —                                | —                 | -120 | dBc/Hz      |
| Transmitter<br>REFCLK Phase<br>Jitter<br>(100 MHz) <sup>(17)</sup> | 10 kHz to<br>1.5 MHz<br>(PCIe)                         | —                                | —                 | 3    | —                                | —                 | 3    | —                                | —                 | 3    | ps<br>(rms) |
| $R_{REF}$ <sup>(19)</sup>                                          | —                                                      | —                                | 1800<br>$\pm 1\%$ | —    | —                                | 1800<br>$\pm 1\%$ | —    | —                                | 1800<br>$\pm 1\%$ | —    | $\Omega$    |
| <b>Transceiver Clocks</b>                                          |                                                        |                                  |                   |      |                                  |                   |      |                                  |                   |      |             |
| fixedclk clock<br>frequency                                        | PCIe<br>Receiver<br>Detect                             | —                                | 100<br>or<br>125  | —    | —                                | 100<br>or<br>125  | —    | —                                | 100<br>or<br>125  | —    | MHz         |

**Table 23. Transceiver Specifications for Stratix V GX and GS Devices <sup>(1)</sup> (Part 3 of 7)**

| Symbol/<br>Description                                                                                                                    | Conditions                                                   | Transceiver Speed<br>Grade 1                         |     |       | Transceiver Speed<br>Grade 2 |     |       | Transceiver Speed<br>Grade 3 |     |                          | Unit |
|-------------------------------------------------------------------------------------------------------------------------------------------|--------------------------------------------------------------|------------------------------------------------------|-----|-------|------------------------------|-----|-------|------------------------------|-----|--------------------------|------|
|                                                                                                                                           |                                                              | Min                                                  | Typ | Max   | Min                          | Typ | Max   | Min                          | Typ | Max                      |      |
| Reconfiguration clock<br>( <code>mgmt_clk_clk</code> )<br>frequency                                                                       | —                                                            | 100                                                  | —   | 125   | 100                          | —   | 125   | 100                          | —   | 125                      | MHz  |
| <b>Receiver</b>                                                                                                                           |                                                              |                                                      |     |       |                              |     |       |                              |     |                          |      |
| Supported I/O Standards                                                                                                                   | —                                                            | 1.4-V PCML, 1.5-V PCML, 2.5-V PCML, LVPECL, and LVDS |     |       |                              |     |       |                              |     |                          |      |
| Data rate<br>(Standard PCS)<br>(9), (23)                                                                                                  | —                                                            | 600                                                  | —   | 12200 | 600                          | —   | 12200 | 600                          | —   | 8500/<br>10312.5<br>(24) | Mbps |
| Data rate<br>(10G PCS) (9), (23)                                                                                                          | —                                                            | 600                                                  | —   | 14100 | 600                          | —   | 12500 | 600                          | —   | 8500/<br>10312.5<br>(24) | Mbps |
| Absolute $V_{MAX}$ for<br>a receiver pin <sup>(5)</sup>                                                                                   | —                                                            | —                                                    | —   | 1.2   | —                            | —   | 1.2   | —                            | —   | 1.2                      | V    |
| Absolute $V_{MIN}$ for<br>a receiver pin                                                                                                  | —                                                            | −0.4                                                 | —   | —     | −0.4                         | —   | —     | −0.4                         | —   | —                        | V    |
| Maximum peak-<br>to-peak<br>differential input<br>voltage $V_{ID}$ (diff p-<br>p) before device<br>configuration <sup>(22)</sup>          | —                                                            | —                                                    | —   | 1.6   | —                            | —   | 1.6   | —                            | —   | 1.6                      | V    |
| Maximum peak-<br>to-peak<br>differential input<br>voltage $V_{ID}$ (diff p-<br>p) after device<br>configuration <sup>(18)</sup> ,<br>(22) | $V_{CCR\_GXB} =$<br>1.0 V/1.05 V<br>( $V_{ICM} =$<br>0.70 V) | —                                                    | —   | 2.0   | —                            | —   | 2.0   | —                            | —   | 2.0                      | V    |
|                                                                                                                                           | $V_{CCR\_GXB} =$<br>0.90 V<br>( $V_{ICM} = 0.6$ V)           | —                                                    | —   | 2.4   | —                            | —   | 2.4   | —                            | —   | 2.4                      | V    |
|                                                                                                                                           | $V_{CCR\_GXB} =$<br>0.85 V<br>( $V_{ICM} = 0.6$ V)           | —                                                    | —   | 2.4   | —                            | —   | 2.4   | —                            | —   | 2.4                      | V    |
| Minimum<br>differential eye<br>opening at<br>receiver serial<br>input pins <sup>(6)</sup> , (22),<br>(27)                                 | —                                                            | 85                                                   | —   | —     | 85                           | —   | —     | 85                           | —   | —                        | mV   |

**Table 23. Transceiver Specifications for Stratix V GX and GS Devices <sup>(1)</sup> (Part 4 of 7)**

| Symbol/<br>Description                                     | Conditions                                                 | Transceiver Speed<br>Grade 1 |               |     | Transceiver Speed<br>Grade 2 |               |     | Transceiver Speed<br>Grade 3 |               |     | Unit          |
|------------------------------------------------------------|------------------------------------------------------------|------------------------------|---------------|-----|------------------------------|---------------|-----|------------------------------|---------------|-----|---------------|
|                                                            |                                                            | Min                          | Typ           | Max | Min                          | Typ           | Max | Min                          | Typ           | Max |               |
| Differential on-chip termination resistors <sup>(21)</sup> | 85- $\Omega$ setting                                       | —                            | 85 $\pm$ 30%  | —   | —                            | 85 $\pm$ 30%  | —   | —                            | 85 $\pm$ 30%  | —   | $\Omega$      |
|                                                            | 100- $\Omega$ setting                                      | —                            | 100 $\pm$ 30% | —   | —                            | 100 $\pm$ 30% | —   | —                            | 100 $\pm$ 30% | —   | $\Omega$      |
|                                                            | 120- $\Omega$ setting                                      | —                            | 120 $\pm$ 30% | —   | —                            | 120 $\pm$ 30% | —   | —                            | 120 $\pm$ 30% | —   | $\Omega$      |
|                                                            | 150- $\Omega$ setting                                      | —                            | 150 $\pm$ 30% | —   | —                            | 150 $\pm$ 30% | —   | —                            | 150 $\pm$ 30% | —   | $\Omega$      |
| $V_{ICM}$<br>(AC and DC coupled)                           | $V_{CCR\_GXB} = 0.85\text{ V}$ or 0.9 V full bandwidth     | —                            | 600           | —   | —                            | 600           | —   | —                            | 600           | —   | mV            |
|                                                            | $V_{CCR\_GXB} = 0.85\text{ V}$ or 0.9 V half bandwidth     | —                            | 600           | —   | —                            | 600           | —   | —                            | 600           | —   | mV            |
|                                                            | $V_{CCR\_GXB} = 1.0\text{ V}/1.05\text{ V}$ full bandwidth | —                            | 700           | —   | —                            | 700           | —   | —                            | 700           | —   | mV            |
|                                                            | $V_{CCR\_GXB} = 1.0\text{ V}$ half bandwidth               | —                            | 750           | —   | —                            | 750           | —   | —                            | 750           | —   | mV            |
| $t_{LTR}$ <sup>(11)</sup>                                  | —                                                          | —                            | —             | 10  | —                            | —             | 10  | —                            | —             | 10  | $\mu\text{s}$ |
| $t_{LTD}$ <sup>(12)</sup>                                  | —                                                          | 4                            | —             | —   | 4                            | —             | —   | 4                            | —             | —   | $\mu\text{s}$ |
| $t_{LTD\_manual}$ <sup>(13)</sup>                          | —                                                          | 4                            | —             | —   | 4                            | —             | —   | 4                            | —             | —   | $\mu\text{s}$ |
| $t_{LTR\_LTD\_manual}$ <sup>(14)</sup>                     | —                                                          | 15                           | —             | —   | 15                           | —             | —   | 15                           | —             | —   | $\mu\text{s}$ |
| Run Length                                                 | —                                                          | —                            | —             | 200 | —                            | —             | 200 | —                            | —             | 200 | UI            |
| Programmable equalization (AC Gain) <sup>(10)</sup>        | Full bandwidth (6.25 GHz)<br>Half bandwidth (3.125 GHz)    | —                            | —             | 16  | —                            | —             | 16  | —                            | —             | 16  | dB            |

Table 24 shows the maximum transmitter data rate for the clock network.

**Table 24. Clock Network Maximum Data Rate Transmitter Specifications <sup>(1)</sup>**

| Clock Network                  | ATX PLL                |                    |                                       | CMU PLL <sup>(2)</sup> |                    |                                       | fPLL                   |                    |                                       |
|--------------------------------|------------------------|--------------------|---------------------------------------|------------------------|--------------------|---------------------------------------|------------------------|--------------------|---------------------------------------|
|                                | Non-bonded Mode (Gbps) | Bonded Mode (Gbps) | Channel Span                          | Non-bonded Mode (Gbps) | Bonded Mode (Gbps) | Channel Span                          | Non-bonded Mode (Gbps) | Bonded Mode (Gbps) | Channel Span                          |
| x1 <sup>(3)</sup>              | 14.1                   | —                  | 6                                     | 12.5                   | —                  | 6                                     | 3.125                  | —                  | 3                                     |
| x6 <sup>(3)</sup>              | —                      | 14.1               | 6                                     | —                      | 12.5               | 6                                     | —                      | 3.125              | 6                                     |
| x6 PLL Feedback <sup>(4)</sup> | —                      | 14.1               | Side-wide                             | —                      | 12.5               | Side-wide                             | —                      | —                  | —                                     |
| xN (PCIe)                      | —                      | 8.0                | 8                                     | —                      | 5.0                | 8                                     | —                      | —                  | —                                     |
| xN (Native PHY IP)             | 8.0                    | 8.0                | Up to 13 channels above and below PLL | 7.99                   | 7.99               | Up to 13 channels above and below PLL | 3.125                  | 3.125              | Up to 13 channels above and below PLL |
|                                | —                      | 8.01 to 9.8304     | Up to 7 channels above and below PLL  |                        |                    |                                       |                        |                    |                                       |

**Notes to Table 24:**

- (1) Valid data rates below the maximum specified in this table depend on the reference clock frequency and the PLL counter settings. Check the MegaWizard message during the PHY IP instantiation.
- (2) ATX PLL is recommended at 8 Gbps and above data rates for improved jitter performance.
- (3) Channel span is within a transceiver bank.
- (4) Side-wide channel bonding is allowed up to the maximum supported by the PHY IP.

Table 25 shows the approximate maximum data rate using the standard PCS.

**Table 25. Stratix V Standard PCS Approximate Maximum Date Rate <sup>(1)</sup>, <sup>(3)</sup>**

| Mode <sup>(2)</sup> | Transceiver Speed Grade | PMA Width                             | 20      | 20      | 16      | 16      | 10  | 10  | 8    | 8    |
|---------------------|-------------------------|---------------------------------------|---------|---------|---------|---------|-----|-----|------|------|
|                     |                         | PCS/Core Width                        | 40      | 20      | 32      | 16      | 20  | 10  | 16   | 8    |
| FIFO                | 1                       | C1, C2, C2L, I2, I2L core speed grade | 12.2    | 11.4    | 9.76    | 9.12    | 6.5 | 5.8 | 5.2  | 4.72 |
|                     | 2                       | C1, C2, C2L, I2, I2L core speed grade | 12.2    | 11.4    | 9.76    | 9.12    | 6.5 | 5.8 | 5.2  | 4.72 |
|                     |                         | C3, I3, I3L core speed grade          | 9.8     | 9.0     | 7.84    | 7.2     | 5.3 | 4.7 | 4.24 | 3.76 |
|                     | 3                       | C1, C2, C2L, I2, I2L core speed grade | 8.5     | 8.5     | 8.5     | 8.5     | 6.5 | 5.8 | 5.2  | 4.72 |
|                     |                         | I3YY core speed grade                 | 10.3125 | 10.3125 | 7.84    | 7.2     | 5.3 | 4.7 | 4.24 | 3.76 |
|                     |                         | C3, I3, I3L core speed grade          | 8.5     | 8.5     | 7.84    | 7.2     | 5.3 | 4.7 | 4.24 | 3.76 |
|                     |                         | C4, I4 core speed grade               | 8.5     | 8.2     | 7.04    | 6.56    | 4.8 | 4.2 | 3.84 | 3.44 |
| Register            | 1                       | C1, C2, C2L, I2, I2L core speed grade | 12.2    | 11.4    | 9.76    | 9.12    | 6.1 | 5.7 | 4.88 | 4.56 |
|                     | 2                       | C1, C2, C2L, I2, I2L core speed grade | 12.2    | 11.4    | 9.76    | 9.12    | 6.1 | 5.7 | 4.88 | 4.56 |
|                     |                         | C3, I3, I3L core speed grade          | 9.8     | 9.0     | 7.92    | 7.2     | 4.9 | 4.5 | 3.96 | 3.6  |
|                     | 3                       | C1, C2, C2L, I2, I2L core speed grade | 10.3125 | 10.3125 | 10.3125 | 10.3125 | 6.1 | 5.7 | 4.88 | 4.56 |
|                     |                         | I3YY core speed grade                 | 10.3125 | 10.3125 | 7.92    | 7.2     | 4.9 | 4.5 | 3.96 | 3.6  |
|                     |                         | C3, I3, I3L core speed grade          | 8.5     | 8.5     | 7.92    | 7.2     | 4.9 | 4.5 | 3.96 | 3.6  |
|                     |                         | C4, I4 core speed grade               | 8.5     | 8.2     | 7.04    | 6.56    | 4.4 | 4.1 | 3.52 | 3.28 |

**Notes to Table 25:**

- (1) The maximum data rate is in Gbps.
- (2) The Phase Compensation FIFO can be configured in FIFO mode or register mode. In the FIFO mode, the pointers are not fixed, and the latency can vary. In the register mode the pointers are fixed for low latency.
- (3) The maximum data rate is also constrained by the transceiver speed grade. Refer to Table 1 for the transceiver speed grade.

**Table 28. Transceiver Specifications for Stratix V GT Devices (Part 3 of 5) <sup>(1)</sup>**

| Symbol/<br>Description                                                     | Conditions                      | Transceiver<br>Speed Grade 2 |               |        | Transceiver<br>Speed Grade 3 |               |        | Unit      |
|----------------------------------------------------------------------------|---------------------------------|------------------------------|---------------|--------|------------------------------|---------------|--------|-----------|
|                                                                            |                                 | Min                          | Typ           | Max    | Min                          | Typ           | Max    |           |
| Differential on-chip termination resistors <sup>(7)</sup>                  | GT channels                     | —                            | 100           | —      | —                            | 100           | —      | $\Omega$  |
| Differential on-chip termination resistors for GX channels <sup>(19)</sup> | 85- $\Omega$ setting            | —                            | 85 $\pm$ 30%  | —      | —                            | 85 $\pm$ 30%  | —      | $\Omega$  |
|                                                                            | 100- $\Omega$ setting           | —                            | 100 $\pm$ 30% | —      | —                            | 100 $\pm$ 30% | —      | $\Omega$  |
|                                                                            | 120- $\Omega$ setting           | —                            | 120 $\pm$ 30% | —      | —                            | 120 $\pm$ 30% | —      | $\Omega$  |
|                                                                            | 150- $\Omega$ setting           | —                            | 150 $\pm$ 30% | —      | —                            | 150 $\pm$ 30% | —      | $\Omega$  |
| V <sub>ICM</sub> (AC coupled)                                              | GT channels                     | —                            | 650           | —      | —                            | 650           | —      | mV        |
| VICM (AC and DC coupled) for GX Channels                                   | VCCR_GXB = 0.85 V or 0.9 V      | —                            | 600           | —      | —                            | 600           | —      | mV        |
|                                                                            | VCCR_GXB = 1.0 V full bandwidth | —                            | 700           | —      | —                            | 700           | —      | mV        |
|                                                                            | VCCR_GXB = 1.0 V half bandwidth | —                            | 750           | —      | —                            | 750           | —      | mV        |
| t <sub>LTR</sub> <sup>(9)</sup>                                            | —                               | —                            | —             | 10     | —                            | —             | 10     | $\mu$ s   |
| t <sub>LTD</sub> <sup>(10)</sup>                                           | —                               | 4                            | —             | —      | 4                            | —             | —      | $\mu$ s   |
| t <sub>LTD_manual</sub> <sup>(11)</sup>                                    | —                               | 4                            | —             | —      | 4                            | —             | —      | $\mu$ s   |
| t <sub>LTR_LTD_manual</sub> <sup>(12)</sup>                                | —                               | 15                           | —             | —      | 15                           | —             | —      | $\mu$ s   |
| Run Length                                                                 | GT channels                     | —                            | —             | 72     | —                            | —             | 72     | CID       |
|                                                                            | GX channels                     | <sup>(8)</sup>               |               |        |                              |               |        |           |
| CDR PPM                                                                    | GT channels                     | —                            | —             | 1000   | —                            | —             | 1000   | $\pm$ PPM |
|                                                                            | GX channels                     | <sup>(8)</sup>               |               |        |                              |               |        |           |
| Programmable equalization (AC Gain) <sup>(5)</sup>                         | GT channels                     | —                            | —             | 14     | —                            | —             | 14     | dB        |
|                                                                            | GX channels                     | <sup>(8)</sup>               |               |        |                              |               |        |           |
| Programmable DC gain <sup>(6)</sup>                                        | GT channels                     | —                            | —             | 7.5    | —                            | —             | 7.5    | dB        |
|                                                                            | GX channels                     | <sup>(8)</sup>               |               |        |                              |               |        |           |
| Differential on-chip termination resistors <sup>(7)</sup>                  | GT channels                     | —                            | 100           | —      | —                            | 100           | —      | $\Omega$  |
| <b>Transmitter</b>                                                         |                                 |                              |               |        |                              |               |        |           |
| Supported I/O Standards                                                    | —                               | 1.4-V and 1.5-V PCML         |               |        |                              |               |        |           |
| Data rate (Standard PCS)                                                   | GX channels                     | 600                          | —             | 8500   | 600                          | —             | 8500   | Mbps      |
| Data rate (10G PCS)                                                        | GX channels                     | 600                          | —             | 12,500 | 600                          | —             | 12,500 | Mbps      |

**Table 28. Transceiver Specifications for Stratix V GT Devices (Part 4 of 5) <sup>(1)</sup>**

| Symbol/<br>Description                                             | Conditions                                   | Transceiver<br>Speed Grade 2 |     |                                | Transceiver<br>Speed Grade 3 |     |                                | Unit |
|--------------------------------------------------------------------|----------------------------------------------|------------------------------|-----|--------------------------------|------------------------------|-----|--------------------------------|------|
|                                                                    |                                              | Min                          | Typ | Max                            | Min                          | Typ | Max                            |      |
| Data rate                                                          | GT channels                                  | 19,600                       | —   | 28,050                         | 19,600                       | —   | 25,780                         | Mbps |
| Differential on-chip<br>termination resistors                      | GT channels                                  | —                            | 100 | —                              | —                            | 100 | —                              | Ω    |
|                                                                    | GX channels                                  | (8)                          |     |                                |                              |     |                                |      |
| V <sub>OCM</sub> (AC coupled)                                      | GT channels                                  | —                            | 500 | —                              | —                            | 500 | —                              | mV   |
|                                                                    | GX channels                                  | (8)                          |     |                                |                              |     |                                |      |
| Rise/Fall time                                                     | GT channels                                  | —                            | 15  | —                              | —                            | 15  | —                              | ps   |
|                                                                    | GX channels                                  | (8)                          |     |                                |                              |     |                                |      |
| Intra-differential pair<br>skew                                    | GX channels                                  | (8)                          |     |                                |                              |     |                                |      |
| Intra-transceiver block<br>transmitter channel-to-<br>channel skew | GX channels                                  | (8)                          |     |                                |                              |     |                                |      |
| Inter-transceiver block<br>transmitter channel-to-<br>channel skew | GX channels                                  | (8)                          |     |                                |                              |     |                                |      |
| CMU PLL                                                            |                                              |                              |     |                                |                              |     |                                |      |
| Supported Data Range                                               | —                                            | 600                          | —   | 12500                          | 600                          | —   | 8500                           | Mbps |
| t <sub>pll_powerdown</sub> <sup>(13)</sup>                         | —                                            | 1                            | —   | —                              | 1                            | —   | —                              | μs   |
| t <sub>pll_lock</sub> <sup>(14)</sup>                              | —                                            | —                            | —   | 10                             | —                            | —   | 10                             | μs   |
| ATX PLL                                                            |                                              |                              |     |                                |                              |     |                                |      |
| Supported Data Rate<br>Range for GX Channels                       | VCO post-<br>divider L=2                     | 8000                         | —   | 12500                          | 8000                         | —   | 8500                           | Mbps |
|                                                                    | L=4                                          | 4000                         | —   | 6600                           | 4000                         | —   | 6600                           | Mbps |
|                                                                    | L=8                                          | 2000                         | —   | 3300                           | 2000                         | —   | 3300                           | Mbps |
|                                                                    | L=8,<br>Local/Central<br>Clock Divider<br>=2 | 1000                         | —   | 1762.5                         | 1000                         | —   | 1762.5                         | Mbps |
| Supported Data Rate<br>Range for GT Channels                       | VCO post-<br>divider L=2                     | 9800                         | —   | 14025                          | 9800                         | —   | 12890                          | Mbps |
| t <sub>pll_powerdown</sub> <sup>(13)</sup>                         | —                                            | 1                            | —   | —                              | 1                            | —   | —                              | μs   |
| t <sub>pll_lock</sub> <sup>(14)</sup>                              | —                                            | —                            | —   | 10                             | —                            | —   | 10                             | μs   |
| fPLL                                                               |                                              |                              |     |                                |                              |     |                                |      |
| Supported Data Range                                               | —                                            | 600                          | —   | 3250/<br>3.125 <sup>(23)</sup> | 600                          | —   | 3250/<br>3.125 <sup>(23)</sup> | Mbps |
| t <sub>pll_powerdown</sub> <sup>(13)</sup>                         | —                                            | 1                            | —   | —                              | 1                            | —   | —                              | μs   |

Figure 4 shows the differential transmitter output waveform.

**Figure 4. Differential Transmitter/Receiver Output/Input Waveform**

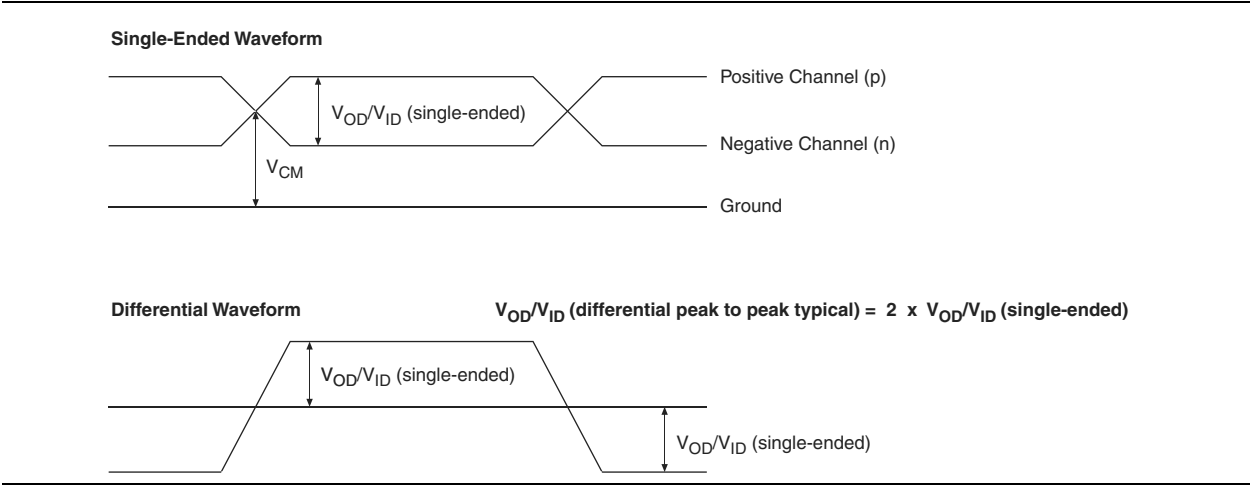


Figure 5 shows the Stratix V AC gain curves for GT channels.

**Figure 5. AC Gain Curves for GT Channels**

**Table 31. PLL Specifications for Stratix V Devices (Part 3 of 3)**

| Symbol    | Parameter                                            | Min    | Typ  | Max   | Unit |
|-----------|------------------------------------------------------|--------|------|-------|------|
| $f_{RES}$ | Resolution of VCO frequency ( $f_{INPFD} = 100$ MHz) | 390625 | 5.96 | 0.023 | Hz   |

**Notes to Table 31:**

- (1) This specification is limited in the Quartus II software by the I/O maximum frequency. The maximum I/O frequency is different for each I/O standard.
- (2) This specification is limited by the lower of the two: I/O  $f_{MAX}$  or  $f_{OUT}$  of the PLL.
- (3) A high input jitter directly affects the PLL output jitter. To have low PLL output clock jitter, you must provide a clean clock source < 120 ps.
- (4)  $f_{REF}$  is  $f_{IN}/N$  when  $N = 1$ .
- (5) Peak-to-peak jitter with a probability level of  $10^{-12}$  (14 sigma, 99.9999999974404% confidence level). The output jitter specification applies to the intrinsic jitter of the PLL, when an input jitter of 30 ps is applied. The external memory interface clock output jitter specifications use a different measurement method and are available in Table 44 on page 52.
- (6) The cascaded PLL specification is only applicable with the following condition:
  - a. Upstream PLL:  $0.59\text{MHz} \leq \text{Upstream PLL BW} < 1$  MHz
  - b. Downstream PLL: Downstream PLL BW > 2 MHz
- (7) High bandwidth PLL settings are not supported in external feedback mode.
- (8) The external memory interface clock output jitter specifications use a different measurement method, which is available in Table 42 on page 50.
- (9) The VCO frequency reported by the Quartus II software in the PLL Usage Summary section of the compilation report takes into consideration the VCO post-scale counter K value. Therefore, if the counter K has a value of 2, the frequency reported can be lower than the  $f_{VCO}$  specification.
- (10) This specification only covers fractional PLL for low bandwidth. The  $f_{VCO}$  for fractional value range 0.05 - 0.95 must be  $\geq 1000$  MHz, while  $f_{VCO}$  for fractional value range 0.20 - 0.80 must be  $\geq 1200$  MHz.
- (11) This specification only covered fractional PLL for low bandwidth. The  $f_{VCO}$  for fractional value range 0.05-0.95 must be  $\geq 1000$  MHz.
- (12) This specification only covered fractional PLL for low bandwidth. The  $f_{VCO}$  for fractional value range 0.20-0.80 must be  $\geq 1200$  MHz.

## DSP Block Specifications

Table 32 lists the Stratix V DSP block performance specifications.

**Table 32. Block Performance Specifications for Stratix V DSP Devices (Part 1 of 2)**

| Mode                                         | Peformance |         |         |     |               |     |     | Unit |
|----------------------------------------------|------------|---------|---------|-----|---------------|-----|-----|------|
|                                              | C1         | C2, C2L | I2, I2L | C3  | I3, I3L, I3YY | C4  | I4  |      |
| Modes using one DSP                          |            |         |         |     |               |     |     |      |
| Three 9 x 9                                  | 600        | 600     | 600     | 480 | 480           | 420 | 420 | MHz  |
| One 18 x 18                                  | 600        | 600     | 600     | 480 | 480           | 420 | 400 | MHz  |
| Two partial 18 x 18 (or 16 x 16)             | 600        | 600     | 600     | 480 | 480           | 420 | 400 | MHz  |
| One 27 x 27                                  | 500        | 500     | 500     | 400 | 400           | 350 | 350 | MHz  |
| One 36 x 18                                  | 500        | 500     | 500     | 400 | 400           | 350 | 350 | MHz  |
| One sum of two 18 x 18(One sum of 2 16 x 16) | 500        | 500     | 500     | 400 | 400           | 350 | 350 | MHz  |
| One sum of square                            | 500        | 500     | 500     | 400 | 400           | 350 | 350 | MHz  |
| One 18 x 18 plus 36 (a x b) + c              | 500        | 500     | 500     | 400 | 400           | 350 | 350 | MHz  |
| Modes using two DSPs                         |            |         |         |     |               |     |     |      |
| Three 18 x 18                                | 500        | 500     | 500     | 400 | 400           | 350 | 350 | MHz  |
| One sum of four 18 x 18                      | 475        | 475     | 475     | 380 | 380           | 300 | 300 | MHz  |
| One sum of two 27 x 27                       | 465        | 465     | 450     | 380 | 380           | 300 | 290 | MHz  |
| One sum of two 36 x 18                       | 475        | 475     | 475     | 380 | 380           | 300 | 300 | MHz  |
| One complex 18 x 18                          | 500        | 500     | 500     | 400 | 400           | 350 | 350 | MHz  |
| One 36 x 36                                  | 475        | 475     | 475     | 380 | 380           | 300 | 300 | MHz  |

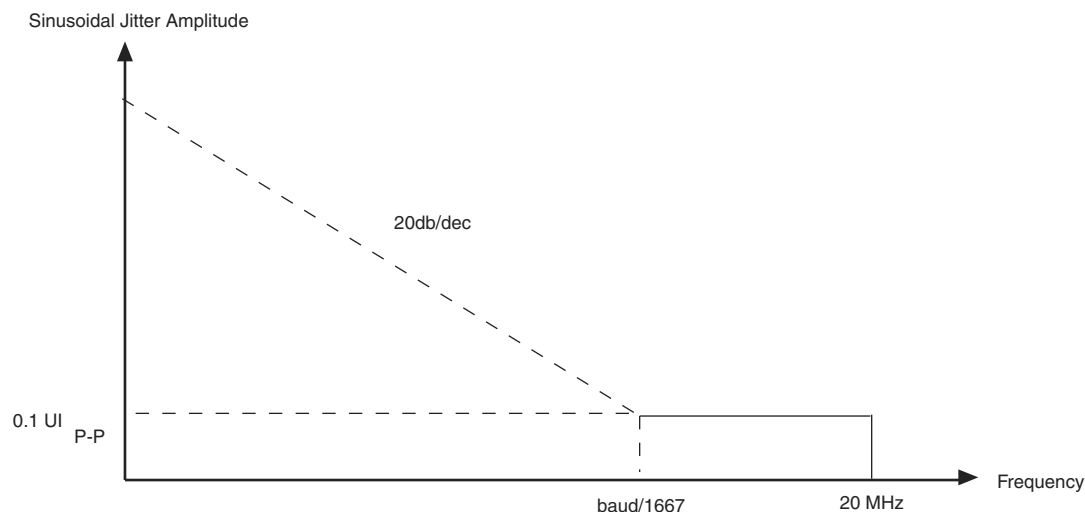
**Table 36. High-Speed I/O Specifications for Stratix V Devices <sup>(1)</sup>, <sup>(2)</sup> (Part 3 of 4)**

| Symbol                                                      | Conditions                                                                                                                          | C1             |     |                | C2, C2L, I2, I2L |     |                | C3, I3, I3L, I3YY |     |                | C4, I4         |     |                | Unit |
|-------------------------------------------------------------|-------------------------------------------------------------------------------------------------------------------------------------|----------------|-----|----------------|------------------|-----|----------------|-------------------|-----|----------------|----------------|-----|----------------|------|
|                                                             |                                                                                                                                     | Min            | Typ | Max            | Min              | Typ | Max            | Min               | Typ | Max            | Min            | Typ | Max            |      |
| $t_{DUTY}$                                                  | Transmitter output clock duty cycle for both True and Emulated Differential I/O Standards                                           | 45             | 50  | 55             | 45               | 50  | 55             | 45                | 50  | 55             | 45             | 50  | 55             | %    |
| $t_{RISE}$ & $t_{FALL}$                                     | True Differential I/O Standards                                                                                                     | —              | —   | 160            | —                | —   | 160            | —                 | —   | 200            | —              | —   | 200            | ps   |
|                                                             | Emulated Differential I/O Standards with three external output resistor networks                                                    | —              | —   | 250            | —                | —   | 250            | —                 | —   | 250            | —              | —   | 300            | ps   |
| TCCS                                                        | True Differential I/O Standards                                                                                                     | —              | —   | 150            | —                | —   | 150            | —                 | —   | 150            | —              | —   | 150            | ps   |
|                                                             | Emulated Differential I/O Standards                                                                                                 | —              | —   | 300            | —                | —   | 300            | —                 | —   | 300            | —              | —   | 300            | ps   |
| <b>Receiver</b>                                             |                                                                                                                                     |                |     |                |                  |     |                |                   |     |                |                |     |                |      |
| True Differential I/O Standards - $f_{HSDRDPA}$ (data rate) | SERDES factor J = 3 to 10 <sup>(11)</sup> , <sup>(12)</sup> , <sup>(13)</sup> , <sup>(14)</sup> , <sup>(15)</sup> , <sup>(16)</sup> | 150            | —   | 1434           | 150              | —   | 1434           | 150               | —   | 1250           | 150            | —   | 1050           | Mbps |
|                                                             | SERDES factor J $\geq 4$                                                                                                            | 150            | —   | 1600           | 150              | —   | 1600           | 150               | —   | 1600           | 150            | —   | 1250           | Mbps |
|                                                             | LVDS RX with DPA <sup>(12)</sup> , <sup>(14)</sup> , <sup>(15)</sup> , <sup>(16)</sup>                                              | 150            | —   | 1600           | 150              | —   | 1600           | 150               | —   | 1600           | 150            | —   | 1250           | Mbps |
|                                                             | SERDES factor J = 2, uses DDR Registers                                                                                             | <sup>(6)</sup> | —   | <sup>(7)</sup> | <sup>(6)</sup>   | —   | <sup>(7)</sup> | <sup>(6)</sup>    | —   | <sup>(7)</sup> | <sup>(6)</sup> | —   | <sup>(7)</sup> | Mbps |
|                                                             | SERDES factor J = 1, uses SDR Register                                                                                              | <sup>(6)</sup> | —   | <sup>(7)</sup> | <sup>(6)</sup>   | —   | <sup>(7)</sup> | <sup>(6)</sup>    | —   | <sup>(7)</sup> | <sup>(6)</sup> | —   | <sup>(7)</sup> | Mbps |

**Table 38. LVDS Soft-CDR/DPA Sinusoidal Jitter Mask Values for a Data Rate  $\geq 1.25$  Gbps**

| Jitter Frequency (Hz) |            | Sinusoidal Jitter (UI) |
|-----------------------|------------|------------------------|
| F1                    | 10,000     | 25.000                 |
| F2                    | 17,565     | 25.000                 |
| F3                    | 1,493,000  | 0.350                  |
| F4                    | 50,000,000 | 0.350                  |

Figure 9 shows the LVDS soft-CDR/DPA sinusoidal jitter tolerance specification for a data rate  $< 1.25$  Gbps.

**Figure 9. LVDS Soft-CDR/DPA Sinusoidal Jitter Tolerance Specification for a Data Rate  $< 1.25$  Gbps**

### DLL Range, DQS Logic Block, and Memory Output Clock Jitter Specifications

Table 39 lists the DLL range specification for Stratix V devices. The DLL is always in 8-tap mode in Stratix V devices.

**Table 39. DLL Range Specifications for Stratix V Devices <sup>(1)</sup>**

| C1      | C2, C2L, I2, I2L | C3, I3, I3L, I3YY | C4,I4   | Unit |
|---------|------------------|-------------------|---------|------|
| 300-933 | 300-933          | 300-890           | 300-890 | MHz  |

**Note to Table 39:**

- (1) Stratix V devices support memory interface frequencies lower than 300 MHz, although the reference clock that feeds the DLL must be at least 300 MHz. To support interfaces below 300 MHz, multiply the reference clock feeding the DLL to ensure the frequency is within the supported range of the DLL.

Table 40 lists the DQS phase offset delay per stage for Stratix V devices.

**Table 40. DQS Phase Offset Delay Per Setting for Stratix V Devices <sup>(1), (2)</sup> (Part 1 of 2)**

| Speed Grade      | Min | Max | Unit |
|------------------|-----|-----|------|
| C1               | 8   | 14  | ps   |
| C2, C2L, I2, I2L | 8   | 14  | ps   |
| C3,I3, I3L, I3YY | 8   | 15  | ps   |

**Table 46. JTAG Timing Parameters and Values for Stratix V Devices**

| Symbol     | Description                              | Min | Max               | Unit |
|------------|------------------------------------------|-----|-------------------|------|
| $t_{JPH}$  | JTAG port hold time                      | 5   | —                 | ns   |
| $t_{JPCO}$ | JTAG port clock to output                | —   | 11 <sup>(1)</sup> | ns   |
| $t_{JPZX}$ | JTAG port high impedance to valid output | —   | 14 <sup>(1)</sup> | ns   |
| $t_{JPXZ}$ | JTAG port valid output to high impedance | —   | 14 <sup>(1)</sup> | ns   |

**Notes to Table 46:**

- (1) A 1 ns adder is required for each  $V_{CCIO}$  voltage step down from 3.0 V. For example,  $t_{JPCO}$  = 12 ns if  $V_{CCIO}$  of the TDO I/O bank = 2.5 V, or 13 ns if it equals 1.8 V.
- (2) The minimum TCK clock period is 167 ns if VCCBAT is within the range 1.2V-1.5V when you perform the volatile key programming.

## Raw Binary File Size

For the POR delay specification, refer to the “POR Delay Specification” section of the “Configuration, Design Security, and Remote System Upgrades in Stratix V Devices”.

Table 47 lists the uncompressed raw binary file (.rbf) sizes for Stratix V devices.

**Table 47. Uncompressed .rbf Sizes for Stratix V Devices**

| Family       | Device | Package                      | Configuration .rbf Size (bits) | IOCSR .rbf Size (bits) <sup>(4), (5)</sup> |
|--------------|--------|------------------------------|--------------------------------|--------------------------------------------|
| Stratix V GX | 5SGXA3 | H35, F40, F35 <sup>(2)</sup> | 213,798,880                    | 562,392                                    |
|              |        | H29, F35 <sup>(3)</sup>      | 137,598,880                    | 564,504                                    |
|              | 5SGXA4 | —                            | 213,798,880                    | 563,672                                    |
|              | 5SGXA5 | —                            | 269,979,008                    | 562,392                                    |
|              | 5SGXA7 | —                            | 269,979,008                    | 562,392                                    |
|              | 5SGXA9 | —                            | 342,742,976                    | 700,888                                    |
|              | 5SGXAB | —                            | 342,742,976                    | 700,888                                    |
|              | 5SGXB5 | —                            | 270,528,640                    | 584,344                                    |
|              | 5SGXB6 | —                            | 270,528,640                    | 584,344                                    |
|              | 5SGXB9 | —                            | 342,742,976                    | 700,888                                    |
|              | 5SGXBB | —                            | 342,742,976                    | 700,888                                    |
| Stratix V GT | 5SGTC5 | —                            | 269,979,008                    | 562,392                                    |
|              | 5SGTC7 | —                            | 269,979,008                    | 562,392                                    |
| Stratix V GS | 5SGSD3 | —                            | 137,598,880                    | 564,504                                    |
|              | 5SGSD4 | F1517                        | 213,798,880                    | 563,672                                    |
|              |        | —                            | 137,598,880                    | 564,504                                    |
|              | 5SGSD5 | —                            | 213,798,880                    | 563,672                                    |
|              | 5SGSD6 | —                            | 293,441,888                    | 565,528                                    |
|              | 5SGSD8 | —                            | 293,441,888                    | 565,528                                    |

**Table 47. Uncompressed .rbf Sizes for Stratix V Devices**

| Family                     | Device | Package | Configuration .rbf Size (bits) | IOCSR .rbf Size (bits) <sup>(4), (5)</sup> |
|----------------------------|--------|---------|--------------------------------|--------------------------------------------|
| Stratix V E <sup>(1)</sup> | 5SEE9  | —       | 342,742,976                    | 700,888                                    |
|                            | 5SEEB  | —       | 342,742,976                    | 700,888                                    |

**Notes to Table 47:**

- (1) Stratix V E devices do not have PCI Express® (PCIe®) hard IP. Stratix V E devices do not support the CvP configuration scheme.
- (2) 36-transceiver devices.
- (3) 24-transceiver devices.
- (4) File size for the periphery image.
- (5) The IOCSR .rbf size is specifically for the CvP feature.

Use the data in Table 47 to estimate the file size before design compilation. Different configuration file formats, such as a hexadecimal (.hex) or tabular text file (.tff) format, have different file sizes. For the different types of configuration file and file sizes, refer to the Quartus II software. However, for a specific version of the Quartus II software, any design targeted for the same device has the same uncompressed configuration file size. If you are using compression, the file size can vary after each compilation because the compression ratio depends on your design.



For more information about setting device configuration options, refer to *Configuration, Design Security, and Remote System Upgrades in Stratix V Devices*. For creating configuration files, refer to the *Quartus II Help*.

Table 48 lists the minimum configuration time estimates for Stratix V devices.

**Table 48. Minimum Configuration Time Estimation for Stratix V Devices**

| Variant | Member Code | Active Serial <sup>(1)</sup> |            |                     | Fast Passive Parallel <sup>(2)</sup> |            |                     |
|---------|-------------|------------------------------|------------|---------------------|--------------------------------------|------------|---------------------|
|         |             | Width                        | DCLK (MHz) | Min Config Time (s) | Width                                | DCLK (MHz) | Min Config Time (s) |
| GX      | A3          | 4                            | 100        | 0.534               | 32                                   | 100        | 0.067               |
|         |             | 4                            | 100        | 0.344               | 32                                   | 100        | 0.043               |
|         | A4          | 4                            | 100        | 0.534               | 32                                   | 100        | 0.067               |
|         | A5          | 4                            | 100        | 0.675               | 32                                   | 100        | 0.084               |
|         | A7          | 4                            | 100        | 0.675               | 32                                   | 100        | 0.084               |
|         | A9          | 4                            | 100        | 0.857               | 32                                   | 100        | 0.107               |
|         | AB          | 4                            | 100        | 0.857               | 32                                   | 100        | 0.107               |
|         | B5          | 4                            | 100        | 0.676               | 32                                   | 100        | 0.085               |
|         | B6          | 4                            | 100        | 0.676               | 32                                   | 100        | 0.085               |
|         | B9          | 4                            | 100        | 0.857               | 32                                   | 100        | 0.107               |
|         | BB          | 4                            | 100        | 0.857               | 32                                   | 100        | 0.107               |
| GT      | C5          | 4                            | 100        | 0.675               | 32                                   | 100        | 0.084               |
|         | C7          | 4                            | 100        | 0.675               | 32                                   | 100        | 0.084               |

Table 50 lists the timing parameters for Stratix V devices for FPP configuration when the DCLK-to-DATA [] ratio is 1.

**Table 50. FPP Timing Parameters for Stratix V Devices <sup>(1)</sup>**

| Symbol                            | Parameter                                         | Minimum                                                    | Maximum              | Units |
|-----------------------------------|---------------------------------------------------|------------------------------------------------------------|----------------------|-------|
| t <sub>CF2CD</sub>                | nCONFIG low to CONF_DONE low                      | —                                                          | 600                  | ns    |
| t <sub>CF2ST0</sub>               | nCONFIG low to nSTATUS low                        | —                                                          | 600                  | ns    |
| t <sub>CFG</sub>                  | nCONFIG low pulse width                           | 2                                                          | —                    | μs    |
| t <sub>STATUS</sub>               | nSTATUS low pulse width                           | 268                                                        | 1,506 <sup>(2)</sup> | μs    |
| t <sub>CF2ST1</sub>               | nCONFIG high to nSTATUS high                      | —                                                          | 1,506 <sup>(3)</sup> | μs    |
| t <sub>CF2CK</sub> <sup>(6)</sup> | nCONFIG high to first rising edge on DCLK         | 1,506                                                      | —                    | μs    |
| t <sub>ST2CK</sub> <sup>(6)</sup> | nSTATUS high to first rising edge of DCLK         | 2                                                          | —                    | μs    |
| t <sub>DSU</sub>                  | DATA [] setup time before rising edge on DCLK     | 5.5                                                        | —                    | ns    |
| t <sub>DH</sub>                   | DATA [] hold time after rising edge on DCLK       | 0                                                          | —                    | ns    |
| t <sub>CH</sub>                   | DCLK high time                                    | $0.45 \times 1/f_{\text{MAX}}$                             | —                    | s     |
| t <sub>CL</sub>                   | DCLK low time                                     | $0.45 \times 1/f_{\text{MAX}}$                             | —                    | s     |
| t <sub>CLK</sub>                  | DCLK period                                       | $1/f_{\text{MAX}}$                                         | —                    | s     |
| f <sub>MAX</sub>                  | DCLK frequency (FPP $\times 8/\times 16$ )        | —                                                          | 125                  | MHz   |
|                                   | DCLK frequency (FPP $\times 32$ )                 | —                                                          | 100                  | MHz   |
| t <sub>CD2UM</sub>                | CONF_DONE high to user mode <sup>(4)</sup>        | 175                                                        | 437                  | μs    |
| t <sub>CD2CU</sub>                | CONF_DONE high to CLKUSR enabled                  | 4 × maximum DCLK period                                    | —                    | —     |
| t <sub>CD2UMC</sub>               | CONF_DONE high to user mode with CLKUSR option on | t <sub>CD2CU</sub> + (8576 × CLKUSR period) <sup>(5)</sup> | —                    | —     |

**Notes to Table 50:**

- (1) Use these timing parameters when the decompression and design security features are disabled.
- (2) This value is applicable if you do not delay configuration by extending the nCONFIG or nSTATUS low pulse width.
- (3) This value is applicable if you do not delay configuration by externally holding the nSTATUS low.
- (4) The minimum and maximum numbers apply only if you chose the internal oscillator as the clock source for initializing the device.
- (5) To enable the CLKUSR pin as the initialization clock source and to obtain the maximum frequency specification on these pins, refer to the Initialization section of the “Configuration, Design Security, and Remote System Upgrades in Stratix V Devices” chapter.
- (6) If nSTATUS is monitored, follow the t<sub>ST2CK</sub> specification. If nSTATUS is not monitored, follow the t<sub>CF2CK</sub> specification.

### FPP Configuration Timing when DCLK-to-DATA [] > 1

Figure 13 shows the timing waveform for FPP configuration when using a MAX II device, MAX V device, or microprocessor as an external host. This waveform shows timing when the DCLK-to-DATA [] ratio is more than 1.

Table 51 lists the timing parameters for Stratix V devices for FPP configuration when the DCLK-to-DATA [ ] ratio is more than 1.

**Table 51. FPP Timing Parameters for Stratix V Devices When the DCLK-to-DATA[ ] Ratio is >1 <sup>(1)</sup>**

| Symbol                     | Parameter                                         | Minimum                                                         | Maximum              | Units   |
|----------------------------|---------------------------------------------------|-----------------------------------------------------------------|----------------------|---------|
| $t_{CF2CD}$                | nCONFIG low to CONF_DONE low                      | —                                                               | 600                  | ns      |
| $t_{CF2ST0}$               | nCONFIG low to nSTATUS low                        | —                                                               | 600                  | ns      |
| $t_{CFG}$                  | nCONFIG low pulse width                           | 2                                                               | —                    | $\mu$ s |
| $t_{STATUS}$               | nSTATUS low pulse width                           | 268                                                             | 1,506 <sup>(2)</sup> | $\mu$ s |
| $t_{CF2ST1}$               | nCONFIG high to nSTATUS high                      | —                                                               | 1,506 <sup>(2)</sup> | $\mu$ s |
| $t_{CF2CK}$ <sup>(5)</sup> | nCONFIG high to first rising edge on DCLK         | 1,506                                                           | —                    | $\mu$ s |
| $t_{ST2CK}$ <sup>(5)</sup> | nSTATUS high to first rising edge of DCLK         | 2                                                               | —                    | $\mu$ s |
| $t_{DSU}$                  | DATA [ ] setup time before rising edge on DCLK    | 5.5                                                             | —                    | ns      |
| $t_{DH}$                   | DATA [ ] hold time after rising edge on DCLK      | $N-1/f_{DCLK}$ <sup>(5)</sup>                                   | —                    | s       |
| $t_{CH}$                   | DCLK high time                                    | $0.45 \times 1/f_{MAX}$                                         | —                    | s       |
| $t_{CL}$                   | DCLK low time                                     | $0.45 \times 1/f_{MAX}$                                         | —                    | s       |
| $t_{CLK}$                  | DCLK period                                       | $1/f_{MAX}$                                                     | —                    | s       |
| $f_{MAX}$                  | DCLK frequency (FPP $\times 8/\times 16$ )        | —                                                               | 125                  | MHz     |
|                            | DCLK frequency (FPP $\times 32$ )                 | —                                                               | 100                  | MHz     |
| $t_R$                      | Input rise time                                   | —                                                               | 40                   | ns      |
| $t_F$                      | Input fall time                                   | —                                                               | 40                   | ns      |
| $t_{CD2UM}$                | CONF_DONE high to user mode <sup>(3)</sup>        | 175                                                             | 437                  | $\mu$ s |
| $t_{CD2CU}$                | CONF_DONE high to CLKUSR enabled                  | $4 \times$ maximum DCLK period                                  | —                    | —       |
| $t_{CD2UMC}$               | CONF_DONE high to user mode with CLKUSR option on | $t_{CD2CU} + (8576 \times \text{CLKUSR period})$ <sup>(4)</sup> | —                    | —       |

**Notes to Table 51:**

- (1) Use these timing parameters when you use the decompression and design security features.
- (2) You can obtain this value if you do not delay configuration by extending the nCONFIG or nSTATUS low pulse width.
- (3) The minimum and maximum numbers apply only if you use the internal oscillator as the clock source for initializing the device.
- (4) To enable the CLKUSR pin as the initialization clock source and to obtain the maximum frequency specification on these pins, refer to the Initialization section of the “Configuration, Design Security, and Remote System Upgrades in Stratix V Devices” chapter.
- (5) N is the DCLK-to-DATA ratio and  $f_{DCLK}$  is the DCLK frequency the system is operating.
- (6) If nSTATUS is monitored, follow the  $t_{ST2CK}$  specification. If nSTATUS is not monitored, follow the  $t_{CF2CK}$  specification.

**Table 61. Document Revision History (Part 2 of 3)**

| Date          | Version | Changes                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      |
|---------------|---------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| November 2014 | 3.3     | <ul style="list-style-type: none"> <li>■ Added the I3YY speed grade and changed the data rates for the GX channel in Table 1.</li> <li>■ Added the I3YY speed grade to the <math>V_{CC}</math> description in Table 6.</li> <li>■ Added the I3YY speed grade to <math>V_{CCHIP\_L}</math>, <math>V_{CCHIP\_R}</math>, <math>V_{CCHSSI\_L}</math>, and <math>V_{CCHSSI\_R}</math> descriptions in Table 7.</li> <li>■ Added 240-<math>\Omega</math> to Table 11.</li> <li>■ Changed CDR PPM tolerance in Table 23.</li> <li>■ Added additional max data rate for fPLL in Table 23.</li> <li>■ Added the I3YY speed grade and changed the data rates for transceiver speed grade 3 in Table 25.</li> <li>■ Added the I3YY speed grade and changed the data rates for transceiver speed grade 3 in Table 26.</li> <li>■ Changed CDR PPM tolerance in Table 28.</li> <li>■ Added additional max data rate for fPLL in Table 28.</li> <li>■ Changed the mode descriptions for MLAB and M20K in Table 33.</li> <li>■ Changed the Max value of <math>f_{HCLK\_OUT}</math> for the C2, C2L, I2, I2L speed grades in Table 36.</li> <li>■ Changed the frequency ranges for C1 and C2 in Table 39.</li> <li>■ Changed the .rbf file sizes for 5SGSD6 and 5SGSD8 in Table 47.</li> <li>■ Added note about nSTATUS to Table 50, Table 51, Table 54.</li> <li>■ Changed the available settings in Table 58.</li> <li>■ Changed the note in “Periphery Performance”.</li> <li>■ Updated the “I/O Standard Specifications” section.</li> <li>■ Updated the “Raw Binary File Size” section.</li> <li>■ Updated the receiver voltage input range in Table 22.</li> <li>■ Updated the max frequency for the LVDS clock network in Table 36.</li> <li>■ Updated the DCLK note to Figure 11.</li> <li>■ Updated Table 23 <math>VO_{CM}</math> (DC Coupled) condition.</li> <li>■ Updated Table 6 and Table 7.</li> <li>■ Added the DCLK specification to Table 55.</li> <li>■ Updated the notes for Table 47.</li> <li>■ Updated the list of parameters for Table 56.</li> </ul> |
| November 2013 | 3.2     | ■ Updated Table 28                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           |
| November 2013 | 3.1     | ■ Updated Table 33                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           |
| November 2013 | 3.0     | ■ Updated Table 23 and Table 28                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              |
| October 2013  | 2.9     | ■ Updated the “Transceiver Characterization” section                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         |
| October 2013  | 2.8     | <ul style="list-style-type: none"> <li>■ Updated Table 3, Table 12, Table 14, Table 19, Table 20, Table 23, Table 24, Table 28, Table 30, Table 31, Table 32, Table 33, Table 36, Table 39, Table 40, Table 41, Table 42, Table 47, Table 53, Table 58, and Table 59</li> <li>■ Added Figure 1 and Figure 3</li> <li>■ Added the “Transceiver Characterization” section</li> <li>■ Removed all “Preliminary” designations.</li> </ul>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        |