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Intel - 5SGXEB5R2F43I2N Datasheet



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Understanding <u>Embedded - FPGAs (Field</u> <u>Programmable Gate Array)</u>

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Obsolete
Number of LABs/CLBs	185000
Number of Logic Elements/Cells	490000
Total RAM Bits	41984000
Number of I/O	600
Number of Gates	· .
Voltage - Supply	0.87V ~ 0.93V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	1760-BBGA, FCBGA
Supplier Device Package	1760-FCBGA (42.5x42.5)
Purchase URL	https://www.e-xfl.com/product-detail/intel/5sgxeb5r2f43i2n

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

								·			
Transceiver Speed	Core Speed Grade										
Grade	C1	C2, C2L	C3	C4	12, 12L	13, 13L	I 3YY	14			
3 GX channel—8.5 Gbps	_	Yes	Yes	Yes	_	Yes	Yes ⁽⁴⁾	Yes			

Table 1. Stratix V GX and GS Commercial and Industrial Speed Grade Offering ^{(1), (2), (3)} (Part 2 of 2)

Notes to Table 1:

(1) C = Commercial temperature grade; I = Industrial temperature grade.

(2) Lower number refers to faster speed grade.

(3) C2L, I2L, and I3L speed grades are for low-power devices.

(4) I3YY speed grades can achieve up to 10.3125 Gbps.

Table 2 lists the industrial and commercial speed grades for the Stratix V GT devices. **Table 2. Stratix V GT Commercial and Industrial Speed Grade Offering** ⁽¹⁾, ⁽²⁾

Transseiver Speed Grade	Core Speed Grade							
Transceiver Speeu draue	C1	C2	12	13				
2 GX channel—12.5 Gbps GT channel—28.05 Gbps	Yes	Yes	_	_				
3 GX channel—12.5 Gbps GT channel—25.78 Gbps	Yes	Yes	Yes	Yes				

Notes to Table 2:

(1) C = Commercial temperature grade; I = Industrial temperature grade.

(2) Lower number refers to faster speed grade.

Absolute Maximum Ratings

Absolute maximum ratings define the maximum operating conditions for Stratix V devices. The values are based on experiments conducted with the devices and theoretical modeling of breakdown and damage mechanisms. The functional operation of the device is not implied for these conditions.



Conditions other than those listed in Table 3 may cause permanent damage to the device. Additionally, device operation at the absolute maximum ratings for extended periods of time may have adverse effects on the device.

TANIC J. ANSULULC MAXIMUM NALINYS IVI SUALIX V DEVICES (FAIL I UI Z)	Table 3.	Absolute Maximum	Ratings	for Stratix \	/ Devices	(Part 1 of 2)
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Symbol	Description	Minimum	Maximum	Unit
V _{CC}	Power supply for core voltage and periphery circuitry	-0.5	1.35	V
V _{CCPT}	Power supply for programmable power technology	-0.5	1.8	V
V _{CCPGM}	Power supply for configuration pins	-0.5	3.9	V
V _{CC_AUX}	Auxiliary supply for the programmable power technology	-0.5	3.4	V
V _{CCBAT}	Battery back-up power supply for design security volatile key register	-0.5	3.9	V
V _{CCPD}	I/O pre-driver power supply	-0.5	3.9	V
V _{CCIO}	I/O power supply	-0.5	3.9	V

Symbol	Description	Minimum	Maximum	Unit
V _{CCD_FPLL}	PLL digital power supply	-0.5	1.8	V
V _{CCA_FPLL}	PLL analog power supply	-0.5	3.4	V
VI	DC input voltage	-0.5	3.8	V
TJ	Operating junction temperature	-55	125	°C
T _{STG}	Storage temperature (No bias)	-65	150	°C
I _{OUT}	DC output current per pin	-25	40	mA

Table 3. Absolute Maximum Ratings for Stratix V Devices (Part 2 of 2)

Table 4 lists the absolute conditions for the transceiver power supply for Stratix V GX, GS, and GT devices.

Table 4. Transceiver Power Supply Absolute Conditions for Stratix V GX, GS, and GT Devices

Symbol	Description	Devices	Minimum	Maximum	Unit
V _{CCA_GXBL}	Transceiver channel PLL power supply (left side)	GX, GS, GT	-0.5	3.75	V
V _{CCA_GXBR}	Transceiver channel PLL power supply (right side)	GX, GS	-0.5	3.75	V
V _{CCA_GTBR}	Transceiver channel PLL power supply (right side)	GT	-0.5	3.75	V
V _{CCHIP_L}	Transceiver hard IP power supply (left side)	GX, GS, GT	-0.5	1.35	V
V _{CCHIP_R}	Transceiver hard IP power supply (right side)	GX, GS, GT	-0.5	1.35	V
V _{CCHSSI_L}	Transceiver PCS power supply (left side)	GX, GS, GT	-0.5	1.35	V
V _{CCHSSI_R}	Transceiver PCS power supply (right side)	GX, GS, GT	-0.5	1.35	V
V _{CCR_GXBL}	Receiver analog power supply (left side)	GX, GS, GT	-0.5	1.35	V
V _{CCR_GXBR}	Receiver analog power supply (right side)	GX, GS, GT	-0.5	1.35	V
V _{CCR_GTBR}	Receiver analog power supply for GT channels (right side)	GT	-0.5	1.35	V
V _{CCT_GXBL}	Transmitter analog power supply (left side)	GX, GS, GT	-0.5	1.35	V
V _{CCT_GXBR}	Transmitter analog power supply (right side)	GX, GS, GT	-0.5	1.35	V
V _{CCT_GTBR}	Transmitter analog power supply for GT channels (right side)	GT	-0.5	1.35	V
V _{CCL_GTBR}	Transmitter clock network power supply (right side)	GT	-0.5	1.35	V
V _{CCH_GXBL}	Transmitter output buffer power supply (left side)	GX, GS, GT	-0.5	1.8	V
V _{CCH_GXBR}	Transmitter output buffer power supply (right side)	GX, GS, GT	-0.5	1.8	V

Maximum Allowed Overshoot and Undershoot Voltage

During transitions, input signals may overshoot to the voltage shown in Table 5 and undershoot to -2.0 V for input currents less than 100 mA and periods shorter than 20 ns.

I/O Pin Leakage Current

Table 9 lists the Stratix V I/O pin leakage current specifications.

Table 9.	I/O Pin	Leakage	Current for	Stratix V	Devices (1)
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Symbol	Description	Conditions	Min	Тур	Max	Unit
I _I	Input pin	$V_I = 0 V \text{ to } V_{CCIOMAX}$	-30	_	30	μA
I _{OZ}	Tri-stated I/O pin	$V_0 = 0 V \text{ to } V_{\text{CCIOMAX}}$	-30		30	μA

Note to Table 9:

(1) If $V_0 = V_{CCI0}$ to $V_{CCI0Max}$, 100 μ A of leakage current per I/O is expected.

Bus Hold Specifications

Table 10 lists the Stratix V device family bus hold specifications.

Table 10. Bus Hold Parameters for Stratix V Devices

				V _{CCIO}									
Parameter	Symbol	Conditions	1.2 V		1.5 V		1.8 V		2.5 V		3.0 V		Unit
			Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Low sustaining current	I _{SUSL}	V _{IN} > V _{IL} (maximum)	22.5	_	25.0	_	30.0	_	50.0	_	70.0	_	μA
High sustaining current	I _{SUSH}	V _{IN} < V _{IH} (minimum)	-22.5		-25.0	_	-30.0	_	-50.0	_	-70.0		μA
Low overdrive current	I _{odl}	$0V < V_{IN} < V_{CCIO}$		120		160		200	_	300		500	μA
High overdrive current	I _{odh}	$0V < V_{IN} < V_{CCIO}$		-120		-160		-200		-300		-500	μΑ
Bus-hold trip point	V _{TRIP}	_	0.45	0.95	0.50	1.00	0.68	1.07	0.70	1.70	0.80	2.00	۷

On-Chip Termination (OCT) Specifications

If you enable OCT calibration, calibration is automatically performed at power-up for I/Os connected to the calibration block. Table 11 lists the Stratix V OCT termination calibration accuracy specifications.

Table 11. OCT Calibration Accuracy Specifications for Stratix V Devices ⁽¹⁾ (Part 1 of 2)

			Calibration Accuracy					
Symbol	Description	Conditions	C1	C2,12	C3,I3, I3YY	C4,14	Unit	
25- $Ω$ R _S	Internal series termination with calibration (25- Ω setting)	V _{CCI0} = 3.0, 2.5, 1.8, 1.5, 1.2 V	±15	±15	±15	±15	%	

- You typically use the interactive Excel-based Early Power Estimator before designing the FPGA to get a magnitude estimate of the device power. The Quartus II PowerPlay Power Analyzer provides better quality estimates based on the specifics of the design after you complete place-and-route. The PowerPlay Power Analyzer can apply a combination of user-entered, simulation-derived, and estimated signal activities that, when combined with detailed circuit models, yields very accurate power estimates.
- ***** For more information about power estimation tools, refer to the *PowerPlay Early Power Estimator User Guide* and the *PowerPlay Power Analysis* chapter in the *Quartus II Handbook*.

Symbol/ Description	Conditions	Tra	nsceive Grade	r Speed 1	Transceiver Speed Grade 2			Trai	Unit		
Description		Min	Тур	Max	Min	Тур	Max	Min	Тур	Max	
	85– Ω setting	_	85 ± 30%		_	85 ± 30%		—	85 ± 30%		Ω
Differential on- chip termination resistors ⁽²¹⁾	100–Ω setting	_	100 ± 30%		_	100 ± 30%		_	100 ± 30%	_	Ω
	120–Ω setting	_	120 ± 30%		_	120 ± 30%		_	120 ± 30%	_	Ω
	150-Ω setting	_	150 ± 30%		_	150 ± 30%	_	_	150 ± 30%	_	Ω
V _{ICM} (AC and DC	V _{CCR_GXB} = 0.85 V or 0.9 V full bandwidth	_	600	_	_	600	_		600	_	mV
	V _{CCR_GXB} = 0.85 V or 0.9 V half bandwidth		600	_		600	_		600	_	mV
(oupled)	V _{CCR_GXB} = 1.0 V/1.05 V full bandwidth	_	700	_	_	700	_	_	700	_	mV
	V _{CCR_GXB} = 1.0 V half bandwidth		750	_	_	750	_	_	750	_	mV
t _{LTR} ⁽¹¹⁾	—	_	_	10	_	—	10	_	—	10	μs
t _{LTD} ⁽¹²⁾	—	4	_		4	—		4	-	—	μs
t _{LTD_manual} ⁽¹³⁾	—	4			4	—		4	—	—	μs
t _{LTR_LTD_manual} ⁽¹⁴⁾	—	15	_		15	—		15	—	—	μs
Run Length		_		200	_	—	200	_	—	200	UI
Programmable equalization (AC Gain) ⁽¹⁰⁾	Full bandwidth (6.25 GHz) Half bandwidth (3.125 GHz)		_	16	_	_	16	_		16	dB

 Table 23. Transceiver Specifications for Stratix V GX and GS Devices ⁽¹⁾ (Part 4 of 7)

Mada (2)	Transceiver	PMA Width	20	20	16	16	10	10	8	8
	Speed Grade	PCS/Core Width	40	20	32	16	20	10	16	8
	1	C1, C2, C2L, I2, I2L core speed grade	12.2	11.4	9.76	9.12	6.5	5.8	5.2	4.72
	ŋ	C1, C2, C2L, I2, I2L core speed grade	12.2	11.4	9.76	9.12	6.5	5.8	5.2	4.72
	۷	C3, I3, I3L core speed grade	9.8	9.0	7.84	7.2	5.3	4.7	4.24	3.76
FIFO		C1, C2, C2L, I2, I2L core speed grade	8.5	8.5	8.5	8.5	6.5	5.8	5.2	4.72
	3	I3YY core speed grade	10.3125	10.3125	7.84	7.2	5.3	4.7	4.24	3.76
	5	C3, I3, I3L core speed grade	8.5	8.5	7.84	7.2	5.3	4.7	4.24	3.76
		C4, I4 core speed grade	8.5	8.2	7.04	6.56	4.8	4.2	3.84	3.44
	1	C1, C2, C2L, I2, I2L core speed grade	12.2	11.4	9.76	9.12	6.1	5.7	4.88	4.56
	ŋ	C1, C2, C2L, I2, I2L core speed grade	12.2	11.4	9.76	9.12	6.1	5.7	4.88	4.56
	۷	C3, I3, I3L core speed grade	9.8	9.0	7.92	7.2	4.9	4.5	3.96	3.6
Register		C1, C2, C2L, I2, I2L core speed grade	10.3125	10.3125	10.3125	10.3125	6.1	5.7	4.88	4.56
	3	I3YY core speed grade	10.3125	10.3125	7.92	7.2	4.9	4.5	3.96	3.6
	J	C3, I3, I3L core speed grade	8.5	8.5	7.92	7.2	4.9	4.5	3.96	3.6
		C4, I4 core speed grade	8.5	8.2	7.04	6.56	4.4	4.1	3.52	3.28

Table 25 shows the approximate maximum data rate using the standard PCS.

Table 25. Stratix V Standard PCS Approximate Maximum Date Rate (1), (3)

Notes to Table 25:

(1) The maximum data rate is in Gbps.

(2) The Phase Compensation FIFO can be configured in FIFO mode or register mode. In the FIFO mode, the pointers are not fixed, and the latency can vary. In the register mode the pointers are fixed for low latency.

(3) The maximum data rate is also constrained by the transceiver speed grade. Refer to Table 1 for the transceiver speed grade.

Table 27 shows the V_{OD} settings for the GX channel.

Symbol	V _{op} Setting	V _{od} Value (mV)	V _{op} Setting	V _{op} Value (mV)
	0 (1)	0	32	640
	1 (1)	20	33	660
	2 (1)	40	34	680
	3 (1)	60	35	700
	4 (1)	80	36	720
	5 ⁽¹⁾	100	37	740
	6	120	38	760
	7	140	39	780
	8	160	40	800
	9	180	41	820
	10	200	42	840
	11	220	43	860
	12	240	44	880
	13	260	45	900
	14	280	46	920
V_{0D} differential peak to peak	15	300	47	940
typical ⁽³⁾	16	320	48	960
	17	340	49	980
	18	360	50	1000
	19	380	51	1020
	20	400	52	1040
	21	420	53	1060
	22	440	54	1080
	23	460	55	1100
	24	480	56	1120
	25	500	57	1140
	26	520	58	1160
	27	540	59	1180
	28	560	60	1200
	29	580	61	1220
	30	600	62	1240
	31	620	63	1260

Table 27. Typical V_{0D} Setting for GX Channel, TX Termination = 100 $\Omega^{\left(2\right)}$

Note to Table 27:

(1) If TX termination resistance = 100Ω , this VOD setting is illegal.

(2) The tolerance is +/-20% for all VOD settings except for settings 2 and below.

(3) Refer to Figure 2.

Symbol/	Conditions	s	Transceive peed Grade	r 2	S	Transceive peed Grade	r 3	Unit
Description		Min	Тур	Max	Min	Тур	Max	
Reference Clock								1
Supported I/O Standards	Dedicated reference clock pin	1.2-V PCN	IL, 1.4-V PC	ML, 1.5-V P(CML, 2.5-V I and HCSL	PCML, Diffe	rential LVPE	ECL, LVDS,
otanuarus	RX reference clock pin		1.4-V PCML	., 1.5-V PCM	IL, 2.5-V PC	ML, LVPEC	L, and LVDS	6
Input Reference Clock Frequency (CMU PLL) ⁽⁶⁾	_	40	_	710	40	_	710	MHz
Input Reference Clock Frequency (ATX PLL) ⁽⁶⁾	_	100	_	710	100	_	710	MHz
Rise time	20% to 80%	_		400	_	_	400	
Fall time	80% to 20%			400	—	_	400	ps
Duty cycle	—	45	_	55	45	_	55	%
Spread-spectrum modulating clock frequency	PCI Express (PCIe)	30	_	33	30	_	33	kHz
Spread-spectrum downspread	PCle	_	0 to -0.5	_	_	0 to -0.5	_	%
On-chip termination resistors ⁽¹⁹⁾	_	_	100	_	_	100	_	Ω
Absolute V _{MAX} ⁽³⁾	Dedicated reference clock pin	_	_	1.6	_	_	1.6	V
	RX reference clock pin	_	_	1.2	_	_	1.2	
Absolute V _{MIN}	—	-0.4		—	-0.4	—		V
Peak-to-peak differential input voltage	_	200	_	1600	200	_	1600	mV
V _{ICM} (AC coupled)	Dedicated reference clock pin		1050/1000 ^{(,}	2)	1	050/1000 (2)	mV
	RX reference clock pin	1	.0/0.9/0.85 (22)	1.	0/0.9/0.85 ((22)	V
V _{ICM} (DC coupled)	HCSL I/O standard for PCIe reference clock	250	_	550	250	_	550	mV

Table 28. Transceiver Specifications for Stratix V GT Devices (Part 1 of 5)⁽¹⁾

Symbol	Parameter	Min	Тур	Max	Unit
+ (3) (4)	Input clock cycle-to-cycle jitter ($f_{REF} \ge 100 \text{ MHz}$)			0.15	UI (p-p)
LINCCJ (0), (1)	Input clock cycle-to-cycle jitter (f _{REF} < 100 MHz)	-750		+750	ps (p-p)
+ (5)	Period Jitter for dedicated clock output (f_{OUT} \geq 100 MHz)	_	_	175 ⁽¹⁾	ps (p-p)
CUTPJ_DC	Period Jitter for dedicated clock output (f _{OUT} < 100 MHz)	_	_	17.5 ⁽¹⁾	mUI (p-p)
+ (5)	Period Jitter for dedicated clock output in fractional PLL ($f_{OUT} \ge 100 \text{ MHz}$)	_	_	250 ⁽¹¹⁾ , 175 ⁽¹²⁾	ps (p-p)
^L FOUTPJ_DC	Period Jitter for dedicated clock output in fractional PLL (f _{OUT} < 100 MHz)	_	_	25 ⁽¹¹⁾ , 17.5 ⁽¹²⁾	mUI (p-p)
+ (5)	Cycle-to-Cycle Jitter for a dedicated clock output ($f_{\text{OUT}} \geq 100 \text{ MHz})$		_	175	ps (p-p)
COUTCCJ_DC	Cycle-to-Cycle Jitter for a dedicated clock output $(f_{OUT} < 100 \text{ MHz})$		_	17.5	mUI (p-p)
+ (5)	Cycle-to-cycle Jitter for a dedicated clock output in fractional PLL ($f_{OUT} \ge 100 \text{ MHz}$)		_	250 ⁽¹¹⁾ , 175 ⁽¹²⁾	ps (p-p)
FOUTCCJ_DC	Cycle-to-cycle Jitter for a dedicated clock output in fractional PLL ($f_{OUT} < 100 \text{ MHz}$)+		_	25 ⁽¹¹⁾ , 17.5 ⁽¹²⁾	mUI (p-p)
t _{outpj 10} (5),	Period Jitter for a clock output on a regular I/O in integer PLL ($f_{OUT} \ge 100 \text{ MHz}$)		_	600	ps (p-p)
(8)	Period Jitter for a clock output on a regular I/O $(f_{OUT} < 100 \text{ MHz})$		_	60	mUI (p-p)
t _{foutpj 10} ^{(5),}	Period Jitter for a clock output on a regular I/O in fractional PLL ($f_{OUT} \ge 100 \text{ MHz}$)	_	_	600 ⁽¹⁰⁾	ps (p-p)
(8), (11)	Period Jitter for a clock output on a regular I/O in fractional PLL (f _{OUT} < 100 MHz)	_	_	60 ⁽¹⁰⁾	mUI (p-p)
t _{outccj_io} (5),	Cycle-to-cycle Jitter for a clock output on a regular I/O in integer PLL ($f_{OUT} \geq 100 \mbox{ MHz})$	_	_	600	ps (p-p)
(8)	Cycle-to-cycle Jitter for a clock output on a regular I/O in integer PLL (f _{OUT} < 100 MHz)	_	_	60 ⁽¹⁰⁾	mUI (p-p)
t _{FOUTCCJ 10} (5),	Cycle-to-cycle Jitter for a clock output on a regular I/O in fractional PLL ($f_{OUT} \ge 100$ MHz)		_	600 ⁽¹⁰⁾	ps (p-p)
(8), (11)	Cycle-to-cycle Jitter for a clock output on a regular I/O in fractional PLL (f _{OUT} < 100 MHz)	_	_	60	mUI (p-p)
t _{CASC OUTPJ DC}	Period Jitter for a dedicated clock output in cascaded PLLs ($f_{OUT} \ge 100 \text{ MHz}$)	_	_	175	ps (p-p)
(5), (6)	Period Jitter for a dedicated clock output in cascaded PLLs (f_{OUT} < 100 MHz)	_	_	17.5	mUI (p-p)
f _{DRIFT}	Frequency drift after PFDENA is disabled for a duration of 100 μs		_	±10	%
dK _{BIT}	Bit number of Delta Sigma Modulator (DSM)	8	24	32	Bits
k _{VALUE}	Numerator of Fraction	128	8388608	2147483648	—

Table 31. PLL Specifications for Stratix V Devices (Part 2 of 3)

Table 31. PLL Specifications for Stratix V Devices (Part 3 of 3)

Symbol	Parameter	Min	Тур	Max	Unit
f _{RES}	Resolution of VCO frequency ($f_{INPFD} = 100 \text{ MHz}$)	390625	5.96	0.023	Hz

Notes to Table 31:

(1) This specification is limited in the Quartus II software by the I/O maximum frequency. The maximum I/O frequency is different for each I/O standard.

(2) This specification is limited by the lower of the two: I/O f_{MAX} or f_{OUT} of the PLL.

- (3) A high input jitter directly affects the PLL output jitter. To have low PLL output clock jitter, you must provide a clean clock source < 120 ps.
- (4) f_{REF} is fIN/N when N = 1.
- (5) Peak-to-peak jitter with a probability level of 10⁻¹² (14 sigma, 99.9999999974404% confidence level). The output jitter specification applies to the intrinsic jitter of the PLL, when an input jitter of 30 ps is applied. The external memory interface clock output jitter specifications use a different measurement method and are available in Table 44 on page 52.
- (6) The cascaded PLL specification is only applicable with the following condition: a. Upstream PLL: 0.59Mhz ≤ Upstream PLL BW < 1 MHz b. Downstream PLL: Downstream PLL BW > 2 MHz
- (7) High bandwidth PLL settings are not supported in external feedback mode.
- (8) The external memory interface clock output jitter specifications use a different measurement method, which is available in Table 42 on page 50.
- (9) The VCO frequency reported by the Quartus II software in the PLL Usage Summary section of the compilation report takes into consideration the VCO post-scale counter K value. Therefore, if the counter K has a value of 2, the frequency reported can be lower than the f_{VCO} specification.
- (10) This specification only covers fractional PLL for low bandwidth. The f_{VCO} for fractional value range 0.05 0.95 must be \geq 1000 MHz, while f_{VCO} for fractional value range 0.20 0.80 must be \geq 1200 MHz.
- (11) This specification only covered fractional PLL for low bandwidth. The f_{VC0} for fractional value range 0.05-0.95 must be \geq 1000 MHz.
- (12) This specification only covered fractional PLL for low bandwidth. The f_{VC0} for fractional value range 0.20-0.80 must be \geq 1200 MHz.

DSP Block Specifications

Table 32 lists the Stratix V DSP block performance specifications.

			F	Peformanc	e			
Mode	C1	C2, C2L	12, 12L	C3	13, 13L, 13YY	C4	14	Unit
		Modes ı	using one	DSP				
Three 9 x 9	600	600	600	480	480	420	420	MHz
One 18 x 18	600	600	600	480	480	420	400	MHz
Two partial 18 x 18 (or 16 x 16)	600	600	600	480	480	420	400	MHz
One 27 x 27	500	500	500	400	400	350	350	MHz
One 36 x 18	500	500	500	400	400	350	350	MHz
One sum of two 18 x 18(One sum of 2 16 x 16)	500	500	500	400	400	350	350	MHz
One sum of square	500	500	500	400	400	350	350	MHz
One 18 x 18 plus 36 (a x b) + c	500	500	500	400	400	350	350	MHz
		Modes u	sing two l	DSPs				·
Three 18 x 18	500	500	500	400	400	350	350	MHz
One sum of four 18 x 18	475	475	475	380	380	300	300	MHz
One sum of two 27 x 27	465	465	450	380	380	300	290	MHz
One sum of two 36 x 18	475	475	475	380	380	300	300	MHz
One complex 18 x 18	500	500	500	400	400	350	350	MHz
One 36 x 36	475	475	475	380	380	300	300	MHz

Table 32. Block Performance Specifications for Stratix V DSP Devices (Part 1 of 2)

Figure 7 shows the dynamic phase alignment (DPA) lock time specifications with the DPA PLL calibration option enabled.

Figure 7. DPA Lock Time Specification with DPA PLL Calibration Enabled

rx_reset			
rx_dpa_locked			<u> </u>
			-

Table 37 lists the DPA lock time specifications for Stratix V devices.

Table 37. DPA Lock Time Specifications for Stratix V GX Devices Only (1), (2), (3)

Standard	Training Pattern	Number of Data Transitions in One Repetition of the Training Pattern	Number of Repetitions per 256 Data Transitions ⁽⁴⁾	Maximum
SPI-4	00000000001111111111	2	128	640 data transitions
Parallel Rapid I/O	00001111	2	128	640 data transitions
	10010000	4	64	640 data transitions
Miscollanoous	10101010	8	32	640 data transitions
Wiscenareous	01010101	8	32	640 data transitions

Notes to Table 37:

(1) The DPA lock time is for one channel.

(2) One data transition is defined as a 0-to-1 or 1-to-0 transition.

(3) The DPA lock time stated in this table applies to both commercial and industrial grade.

(4) This is the number of repetitions for the stated training pattern to achieve the 256 data transitions.

Figure 8 shows the **LVDS** soft-clock data recovery (CDR)/DPA sinusoidal jitter tolerance specification for a data rate \geq 1.25 Gbps. Table 38 lists the **LVDS** soft-CDR/DPA sinusoidal jitter tolerance specification for a data rate \geq 1.25 Gbps.





Jitter Free	quency (Hz)	Sinusoidal Jitter (UI)
F1	10,000	25.000
F2	17,565	25.000
F3	1,493,000	0.350
F4	50,000,000	0.350

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Figure 9 shows the **LVDS** soft-CDR/DPA sinusoidal jitter tolerance specification for a data rate < 1.25 Gbps.





DLL Range, DQS Logic Block, and Memory Output Clock Jitter Specifications

Table 39 lists the DLL range specification for Stratix V devices. The DLL is always in 8-tap mode in Stratix V devices.

Table 39. DLL Range Specifications for Stratix V Devices (1)

C1	C2, C2L, I2, I2L	C3, I3, I3L, I3YY	C4,I4	Unit
300-933	300-933	300-890	300-890	MHz

Note to Table 39:

(1) Stratix V devices support memory interface frequencies lower than 300 MHz, although the reference clock that feeds the DLL must be at least 300 MHz. To support interfaces below 300 MHz, multiply the reference clock feeding the DLL to ensure the frequency is within the supported range of the DLL.

Table 40 lists the DQS phase offset delay per stage for Stratix V devices.

Table 40. DQS Phase Offset Delay Per Setting for Stratix V Devices ^{(1), (2)} (Part 1 of 2)

Speed Grade	Min	Max	Unit
C1	8	14	ps
C2, C2L, I2, I2L	8	14	ps
C3,I3, I3L, I3YY	8	15	ps

Clock Network	Parameter	Symbol	C	1	C2, C2L	, 12, 12L	C3, I3, I3L, I3YY C4,I		,14	Unit	
			Min	Max	Min	Max	Min	Max	Min	Max	
PHY Clock	Clock period jitter	$t_{JIT(per)}$	-25	25	-25	25	-30	30	-35	35	ps
	Cycle-to-cycle period jitter	$t_{\rm JIT(cc)}$	-50	50	-50	50	-60	60	-70	70	ps
	Duty cycle jitter	$t_{JIT(duty)}$	-37.5	37.5	-37.5	37.5	-45	45	-56	56	ps

Table 42. Memory Output Clock Jitter Specification for Stratix V Devices (1), (Part 2 of 2) (2), (3)

Notes to Table 42:

(1) The clock jitter specification applies to the memory output clock pins generated using differential signal-splitter and DDIO circuits clocked by a PLL output routed on a PHY, regional, or global clock network as specified. Altera recommends using PHY clock networks whenever possible.

(2) The clock jitter specification applies to the memory output clock pins clocked by an integer PLL.

(3) The memory output clock jitter is applicable when an input jitter of 30 ps peak-to-peak is applied with bit error rate (BER) -12, equivalent to 14 sigma.

OCT Calibration Block Specifications

Table 43 lists the OCT calibration block specifications for Stratix V devices.

Table 43. OCT Calibration Block Specifications for Stratix V Devices

Symbol	Description	Min	Тур	Max	Unit
OCTUSRCLK	Clock required by the OCT calibration blocks	—	—	20	MHz
T _{OCTCAL}	Number of OCTUSRCLK clock cycles required for OCT $\rm R_S/R_T$ calibration		1000	_	Cycles
T _{OCTSHIFT}	Number of OCTUSRCLK clock cycles required for the OCT code to shift out	_	32	_	Cycles
T _{RS_RT}	Time required between the dyn_term_ctrl and oe signal transitions in a bidirectional I/O buffer to dynamically switch between OCT R_S and R_T (Figure 10)		2.5		ns

Figure 10 shows the timing diagram for the oe and dyn_term_ctrl signals.

Figure 10. Timing Diagram for oe and dyn_term_ctrl Signals



Symbol	Description	Min	Max	Unit
t _{JPH}	JTAG port hold time	5	—	ns
t _{JPCO}	JTAG port clock to output	—	11 ⁽¹⁾	ns
t _{JPZX}	JTAG port high impedance to valid output	—	14 ⁽¹⁾	ns
t _{JPXZ}	JTAG port valid output to high impedance	—	14 ⁽¹⁾	ns

Table 46. JTAG Timing Parameters and Values for Stratix V Devices

Notes to Table 46:

(1) A 1 ns adder is required for each V_{CCI0} voltage step down from 3.0 V. For example, $t_{JPC0} = 12$ ns if V_{CCI0} of the TDO I/O bank = 2.5 V, or 13 ns if it equals 1.8 V.

(2) The minimum TCK clock period is 167 ns if VCCBAT is within the range 1.2V-1.5V when you perform the volatile key programming.

Raw Binary File Size

For the POR delay specification, refer to the "POR Delay Specification" section of the "Configuration, Design Security, and Remote System Upgrades in Stratix V Devices".

Table 47 lists the uncompressed raw binary file (.rbf) sizes for Stratix V devices.

Family	y Device Package		Configuration .rbf Size (bits)	IOCSR .rbf Size (bits) ^{(4), (5)}		
	500742	H35, F40, F35 ⁽²⁾	213,798,880	562,392		
	JOUNAS	H29, F35 ⁽³⁾	137,598,880	564,504		
	5SGXA4	—	213,798,880	563,672		
	5SGXA5	—	269,979,008	562,392		
	5SGXA7	—	269,979,008	562,392		
Stratix V GX	5SGXA9	—	342,742,976	700,888		
	5SGXAB	—	342,742,976	700,888		
	5SGXB5	—	270,528,640	584,344		
	5SGXB6	—	270,528,640	584,344		
	5SGXB9	_	342,742,976	700,888		
	5SGXBB	—	342,742,976	700,888		
Stratix V CT	5SGTC5	—	269,979,008	562,392		
Stratix V GX	5SGTC7	_	269,979,008	562,392		
	5SGSD3	—	137,598,880	564,504		
	590904	F1517	213,798,880	563,672		
Stratix V GS	J303D4		137,598,880	564,504		
	5SGSD5		213,798,880	563,672		
	5SGSD6		293,441,888	565,528		
	5SGSD8	—	293,441,888	565,528		

Table 47. Uncompressed .rbf Sizes for Stratix V Devices

FPP Configuration Timing when DCLK-to-DATA [] = 1

Figure 12 shows the timing waveform for FPP configuration when using a MAX II or MAX V device as an external host. This waveform shows timing when the DCLK-to-DATA[] ratio is 1.





Notes to Figure 12:

- (1) Use this timing waveform when the DCLK-to-DATA [] ratio is 1.
- (2) The beginning of this waveform shows the device in user mode. In user mode, nCONFIG, nSTATUS, and CONF_DONE are at logic-high levels. When nCONFIG is pulled low, a reconfiguration cycle begins.
- (3) After power-up, the Stratix V device holds nstatus low for the time of the POR delay.
- (4) After power-up, before and during configuration, CONF_DONE is low.
- (5) Do not leave DCLK floating after configuration. DCLK is ignored after configuration is complete. It can toggle high or low if required.
- (6) For FPP ×16, use DATA [15..0]. For FPP ×8, use DATA [7..0]. DATA [31..0] are available as a user I/O pin after configuration. The state of this pin depends on the dual-purpose pin settings.
- (7) To ensure a successful configuration, send the entire configuration data to the Stratix V device. CONF_DONE is released high when the Stratix V device receives all the configuration data successfully. After CONF_DONE goes high, send two additional falling edges on DCLK to begin initialization and enter user mode.
- (8) After the option bit to enable the INIT_DONE pin is configured into the device, the INIT DONE goes low.

Table 50 lists the timing parameters for Stratix V devices for FPP configuration when the DCLK-to-DATA[] ratio is 1.

Table 50. FPP Timing Parameters for Stratix V Devices (1)

Symbol	Parameter	Minimum	Maximum	Units
t _{CF2CD}	nCONFIG low to CONF_DONE low	—	600	ns
t _{CF2ST0}	nCONFIG low to nSTATUS low		600	ns
t _{CFG}	nCONFIG low pulse width	2		μS
t _{status}	nSTATUS low pulse width	268	1,506 ⁽²⁾	μS
t _{CF2ST1}	nCONFIG high to nSTATUS high	—	1,506 ⁽³⁾	μS
t _{CF2CK} (6)	nCONFIG high to first rising edge on DCLK	1,506		μS
t _{ST2CK} (6)	(6) nSTATUS high to first rising edge of DCLK 2			μS
t _{DSU}	DATA [] setup time before rising edge on DCLK	5.5	_	ns
t _{DH}	DATA [] hold time after rising edge on DCLK	0	_	ns
t _{CH}	DCLK high time	$0.45\times1/f_{MAX}$		S
t _{CL}	DCLK low time	$0.45\times1/f_{MAX}$	_	S
t _{CLK}	DCLK period	1/f _{MAX}		S
4	DCLK frequency (FPP ×8/×16)	—	125	MHz
IMAX	DCLK frequency (FPP ×32)	—	600 	MHz
t _{CD2UM}	CONF_DONE high to user mode ⁽⁴⁾	175	437	μS
+	CONTR DOWN high to CT WARD analysis	4 × maximum		
LCD2CU	CONF_DONE HIGH to CLEOSE enabled	DCLK period	—	_
t _{cD2UMC}	CONF_DONE high to user mode with CLKUSR option on	$\begin{array}{c} t_{\text{CD2CU}} + \\ (8576 \times \text{CLKUSR} \\ \text{period}) \ ^{(5)} \end{array}$		_

Notes to Table 50:

(1) Use these timing parameters when the decompression and design security features are disabled.

(2) This value is applicable if you do not delay configuration by extending the nCONFIG or nSTATUS low pulse width.

(3) This value is applicable if you do not delay configuration by externally holding the nSTATUS low.

- (4) The minimum and maximum numbers apply only if you chose the internal oscillator as the clock source for initializing the device.
- (5) To enable the CLKUSR pin as the initialization clock source and to obtain the maximum frequency specification on these pins, refer to the Initialization section of the "Configuration, Design Security, and Remote System Upgrades in Stratix V Devices" chapter.
- (6) If nSTATUS is monitored, follow the t_{ST2CK} specification. If nSTATUS is not monitored, follow the t_{CF2CK} specification.

FPP Configuration Timing when DCLK-to-DATA [] > 1

Figure 13 shows the timing waveform for FPP configuration when using a MAX II device, MAX V device, or microprocessor as an external host. This waveform shows timing when the DCLK-to-DATA [] ratio is more than 1.

Symbol	Parameter	Minimum	Maximum	Units
t _{CD2UM}	CONF_DONE high to user mode (3)	175	437	μS
t _{CD2CU}	CONF_DONE high to CLKUSR enabled	4 × maximum DCLK period	_	—
t _{CD2UMC}	CONF_DONE high to user mode with CLKUSR option on	t _{cd2cu} + (8576 × clkusr period)	_	—

Table 53. AS Timing Parameters for AS \times 1 and AS \times 4 Configurations in Stratix V Devices ^{(1), (2)} (Part 2 of 2)

Notes to Table 53:

(1) The minimum and maximum numbers apply only if you choose the internal oscillator as the clock source for initializing the device.

(2) t_{CF2CD}, t_{CF2ST0}, t_{CF2ST0}, t_{CF6}, t_{STATUS}, and t_{CF2ST1} timing parameters are identical to the timing parameters for PS mode listed in Table 54 on page 63.

(3) To enable the CLKUSR pin as the initialization clock source and to obtain the maximum frequency specification on this pin, refer to the Initialization section of the "Configuration, Design Security, and Remote System Upgrades in Stratix V Devices" chapter.

Passive Serial Configuration Timing

Figure 15 shows the timing waveform for a passive serial (PS) configuration when using a MAX II device, MAX V device, or microprocessor as an external host.

Figure 15. PS Configuration Timing Waveform ⁽¹⁾



Notes to Figure 15:

- (1) The beginning of this waveform shows the device in user mode. In user mode, nCONFIG, nSTATUS, and CONF_DONE are at logic high levels. When nCONFIG is pulled low, a reconfiguration cycle begins.
- (2) After power-up, the Stratix V device holds nSTATUS low for the time of the POR delay.
- (3) After power-up, before and during configuration, CONF DONE is low.
- (4) Do not leave DCLK floating after configuration. You can drive it high or low, whichever is more convenient.
- (5) DATAO is available as a user I/O pin after configuration. The state of this pin depends on the dual-purpose pin settings in the **Device and Pins Option**.
- (6) To ensure a successful configuration, send the entire configuration data to the Stratix V device. CONF_DONE is released high after the Stratix V device receives all the configuration data successfully. After CONF_DONE goes high, send two additional falling edges on DCLK to begin initialization and enter user mode.
- (7) After the option bit to enable the INIT DONE pin is configured into the device, the INIT DONE goes low.

Remote System Upgrades

Table 56 lists the timing parameter specifications for the remote system upgrade circuitry.

Table 56. Remote System Upgrade Circuitry Timing Specificatio

Parameter	Minimum	Maximum	Unit
t _{RU_nCONFIG} ⁽¹⁾	250	—	ns
t _{RU_nRSTIMER} ⁽²⁾	250	_	ns

Notes to Table 56:

- (1) This is equivalent to strobing the reconfiguration input of the ALTREMOTE_UPDATE megafunction high for the minimum timing specification. For more information, refer to the Remote System Upgrade State Machine section of the "Configuration, Design Security, and Remote System Upgrades in Stratix V Devices" chapter.
- (2) This is equivalent to strobing the reset_timer input of the ALTREMOTE_UPDATE megafunction high for the minimum timing specification. For more information, refer to the User Watchdog Timer section of the "Configuration, Design Security, and Remote System Upgrades in Stratix V Devices" chapter.

User Watchdog Internal Circuitry Timing Specification

Table 57 lists the operating range of the 12.5-MHz internal oscillator.

Table 57. 12.5-MHz Internal Oscillator Specifications

Minimum	Typical	Maximum	Units
5.3	7.9	12.5	MHz

I/O Timing

Altera offers two ways to determine I/O timing—the Excel-based I/O Timing and the Quartus II Timing Analyzer.

Excel-based I/O timing provides pin timing performance for each device density and speed grade. The data is typically used prior to designing the FPGA to get an estimate of the timing budget as part of the link timing analysis. The Quartus II Timing Analyzer provides a more accurate and precise I/O timing data based on the specifics of the design after you complete place-and-route.

 You can download the Excel-based I/O Timing spreadsheet from the Stratix V Devices Documentation web page.

Programmable IOE Delay

Table 58 lists the Stratix V IOE programmable delay settings.

Table 58. IOE Programmable Delay for Stratix V Devices (Part 1 of 2)

Parameter (1) Available Settings	Available	Min	Fast	Model				Slow N	lodel			
	Offset	Industrial	Commercial	C1	C2	C3	C4	12	13, 13YY	14	Unit	
D1	64	0	0.464	0.493	0.838	0.838	0.924	1.011	0.844	0.921	1.006	ns
D2	32	0	0.230	0.244	0.415	0.415	0.459	0.503	0.417	0.456	0.500	ns

Parameter Available (1) Settings	Available Min		Fast Model		Slow Model							
	Offset (2)	Industrial	Commercial	C1	C2	C3	C4	12	13, 13YY	14	Unit	
D3	8	0	1.587	1.699	2.793	2.793	2.992	3.192	2.811	3.047	3.257	ns
D4	64	0	0.464	0.492	0.838	0.838	0.924	1.011	0.843	0.920	1.006	ns
D5	64	0	0.464	0.493	0.838	0.838	0.924	1.011	0.844	0.921	1.006	ns
D6	32	0	0.229	0.244	0.415	0.415	0.458	0.503	0.418	0.456	0.499	ns

Table 58.	IOE Pro	grammable De	lay for	Stratix V	V Devices	(Part 2 of 2)
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Notes to Table 58:

(1) You can set this value in the Quartus II software by selecting D1, D2, D3, D5, and D6 in the Assignment Name column of Assignment Editor.

(2) Minimum offset does not include the intrinsic delay.

Programmable Output Buffer Delay

Table 59 lists the delay chain settings that control the rising and falling edge delays of the output buffer. The default delay is 0 ps.

Symbol	Parameter	Typical	Unit
	Rising and/or falling edge delay	0 (default)	ps
D _{outbuf}		25	ps
		50	ps
		75	ps

Note to Table 59:

(1) You can set the programmable output buffer delay in the Quartus II software by setting the Output Buffer Delay Control assignment to either positive, negative, or both edges, with the specific values stated here (in ps) for the Output Buffer Delay assignment.

Glossary

Table 60 lists the glossary for this chapter.

Table 60. Glossary (Part 1 of 4)

Letter	Subject	Definitions	
Α			
В	—	—	
С			
D	—	_	
E	—	—	
F	f _{HSCLK}	Left and right PLL input clock frequency.	
	f _{HSDR}	High-speed I/O block—Maximum and minimum LVDS data transfer rate (f _{HSDR} = 1/TUI), non-DPA.	
	f _{hsdrdpa}	High-speed I/O block—Maximum and minimum LVDS data transfer rate (f _{HSDRDPA} = 1/TUI), DPA.	

Table 60. Glossary (Part 2 of 4)

Letter	Subject	Definitions	
G H I	JTAG Timing Specifications	High-speed I/O block—Deserialization factor (width of parallel data bus). JTAG Timing Specifications: TMS	
K L M N O			
Ρ	PLL Specifications	Diagram of PLL Specifications (1)	
Q	_	—	
R	RL	Receiver differential input discrete resistor (external to the Stratix V device).	