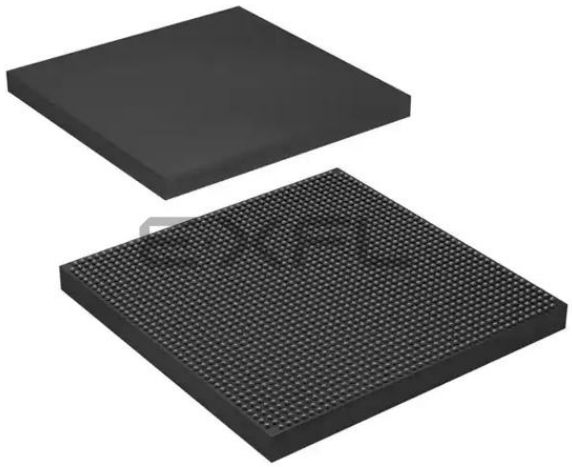

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## Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

## Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

| Details | |
|---|---|
| Product Status | Obsolete |
| Number of LABs/CLBs | 185000 |
| Number of Logic Elements/Cells | 490000 |
| Total RAM Bits | 41984000 |
| Number of I/O | 600 |
| Number of Gates | - |
| Voltage - Supply | 0.82V ~ 0.88V |
| Mounting Type | Surface Mount |
| Operating Temperature | 0°C ~ 85°C (TJ) |
| Package / Case | 1760-BBGA, FCBGA |
| Supplier Device Package | 1760-FCBGA (42.5x42.5) |
| Purchase URL | https://www.e-xfl.com/product-detail/intel/5sgxeb5r3f43c3n |

**Table 3. Absolute Maximum Ratings for Stratix V Devices (Part 2 of 2)**

| Symbol | Description | Minimum | Maximum | Unit |
|---|---|---|---|---|
| $V_{CCD\_FPLL}$ | PLL digital power supply | –0.5 | 1.8 | V |
| $V_{CCA\_FPLL}$ | PLL analog power supply | –0.5 | 3.4 | V |
| $V_I$ | DC input voltage | –0.5 | 3.8 | V |
| $T_J$ | Operating junction temperature | –55 | 125 | °C |
| $T_{STG}$ | Storage temperature (No bias) | –65 | 150 | °C |
| $I_{OUT}$ | DC output current per pin | –25 | 40 | mA |

Table 4 lists the absolute conditions for the transceiver power supply for Stratix V GX, GS, and GT devices.

**Table 4. Transceiver Power Supply Absolute Conditions for Stratix V GX, GS, and GT Devices**

| Symbol | Description | Devices | Minimum | Maximum | Unit |
|---|---|---|---|---|---|
| $V_{CCA\_GXBL}$ | Transceiver channel PLL power supply (left side) | GX, GS, GT | –0.5 | 3.75 | V |
| $V_{CCA\_GXBR}$ | Transceiver channel PLL power supply (right side) | GX, GS | –0.5 | 3.75 | V |
| $V_{CCA\_GTBR}$ | Transceiver channel PLL power supply (right side) | GT | –0.5 | 3.75 | V |
| $V_{CCHIP\_L}$ | Transceiver hard IP power supply (left side) | GX, GS, GT | –0.5 | 1.35 | V |
| $V_{CCHIP\_R}$ | Transceiver hard IP power supply (right side) | GX, GS, GT | –0.5 | 1.35 | V |
| $V_{CCHSSI\_L}$ | Transceiver PCS power supply (left side) | GX, GS, GT | –0.5 | 1.35 | V |
| $V_{CCHSSI\_R}$ | Transceiver PCS power supply (right side) | GX, GS, GT | –0.5 | 1.35 | V |
| $V_{CCR\_GXBL}$ | Receiver analog power supply (left side) | GX, GS, GT | –0.5 | 1.35 | V |
| $V_{CCR\_GXBR}$ | Receiver analog power supply (right side) | GX, GS, GT | –0.5 | 1.35 | V |
| $V_{CCR\_GTBR}$ | Receiver analog power supply for GT channels (right side) | GT | –0.5 | 1.35 | V |
| $V_{CCT\_GXBL}$ | Transmitter analog power supply (left side) | GX, GS, GT | –0.5 | 1.35 | V |
| $V_{CCT\_GXBR}$ | Transmitter analog power supply (right side) | GX, GS, GT | –0.5 | 1.35 | V |
| $V_{CCT\_GTBR}$ | Transmitter analog power supply for GT channels (right side) | GT | –0.5 | 1.35 | V |
| $V_{CCL\_GTBR}$ | Transmitter clock network power supply (right side) | GT | –0.5 | 1.35 | V |
| $V_{CCH\_GXBL}$ | Transmitter output buffer power supply (left side) | GX, GS, GT | –0.5 | 1.8 | V |
| $V_{CCH\_GXBR}$ | Transmitter output buffer power supply (right side) | GX, GS, GT | –0.5 | 1.8 | V |

### Maximum Allowed Overshoot and Undershoot Voltage

During transitions, input signals may overshoot to the voltage shown in Table 5 and undershoot to –2.0 V for input currents less than 100 mA and periods shorter than 20 ns.

Table 8 shows the transceiver power supply voltage requirements for various conditions.

**Table 8. Transceiver Power Supply Voltage Requirements**

| Conditions | Core Speed Grade | VCCR_GXB & VCCT_GXB (2) | VCCA_GXB | VCCH_GXB | Unit |
|---|---|---|---|---|---|
| If BOTH of the following conditions are true:<br>■ Data rate > 10.3 Gbps.<br>■ DFE is used. | All | 1.05 | 3.0 | 1.5 | V |
| If ANY of the following conditions are true (1):<br>■ ATX PLL is used.<br>■ Data rate > 6.5Gbps.<br>■ DFE (data rate ≤ 10.3 Gbps), AEQ, or EyeQ feature is used. | All | 1.0 | | | |
| If ALL of the following conditions are true:<br>■ ATX PLL is not used.<br>■ Data rate ≤ 6.5Gbps.<br>■ DFE, AEQ, and EyeQ are not used. | C1, C2, I2, and I3YY | 0.90 | 2.5 | | |
| | C2L, C3, C4, I2L, I3, I3L, and I4 | 0.85 | 2.5 | | |

**Notes to Table 8:**

(1) Choose this power supply voltage requirement option if you plan to upgrade your design later with any of the listed conditions.

(2) If the VCCR_GXB and VCCT_GXB supplies are set to 1.0 V or 1.05 V, they cannot be shared with the VCC core supply. If the VCCR_GXB and VCCT_GXB are set to either 0.90 V or 0.85 V, they can be shared with the VCC core supply.

## DC Characteristics

This section lists the supply current, I/O pin leakage current, input pin capacitance, on-chip termination tolerance, and hot socketing specifications.

### Supply Current

Supply current is the current drawn from the respective power rails used for power budgeting. Use the Excel-based Early Power Estimator (EPE) to get supply current estimates for your design because these currents vary greatly with the resources you use.

For more information about power estimation tools, refer to the *PowerPlay Early Power Estimator User Guide* and the *PowerPlay Power Analysis* chapter in the *Quartus II Handbook*.

### I/O Pin Leakage Current

Table 9 lists the Stratix V I/O pin leakage current specifications.

**Table 9. I/O Pin Leakage Current for Stratix V Devices (1)**

| Symbol | Description | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $I_I$ | Input pin | $V_I$ = 0 V to $V_{CCIOMAX}$ | –30 | — | 30 | µA |
| $I_{OZ}$ | Tri-stated I/O pin | $V_O$ = 0 V to $V_{CCIOMAX}$ | –30 | — | 30 | µA |

**Note to Table 9:**

(1) If $V_O = V_{CCIO}$ to $V_{CCIOMax}$, 100 µA of leakage current per I/O is expected.

### Bus Hold Specifications

Table 10 lists the Stratix V device family bus hold specifications.

**Table 10. Bus Hold Parameters for Stratix V Devices**

| Parameter | Symbol | Conditions | $V_{CCIO}$ | | | | | | | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | 1.2 V | | 1.5 V | | 1.8 V | | 2.5 V | | 3.0 V | | |
| | | | Min | Max | Min | Max | Min | Max | Min | Max | Min | Max | |
| Low sustaining current | $I_{SUSL}$ | $V_{IN} > V_{IL}$ (maximum) | 22.5 | — | 25.0 | — | 30.0 | — | 50.0 | — | 70.0 | — | µA |
| High sustaining current | $I_{SUSH}$ | $V_{IN} < V_{IH}$ (minimum) | –22.5 | — | –25.0 | — | –30.0 | — | –50.0 | — | –70.0 | — | µA |
| Low overdrive current | $I_{ODL}$ | $0V < V_{IN} < V_{CCIO}$ | — | 120 | — | 160 | — | 200 | — | 300 | — | 500 | µA |
| High overdrive current | $I_{ODH}$ | $0V < V_{IN} < V_{CCIO}$ | — | –120 | — | –160 | — | –200 | — | –300 | — | –500 | µA |
| Bus-hold trip point | $V_{TRIP}$ | — | 0.45 | 0.95 | 0.50 | 1.00 | 0.68 | 1.07 | 0.70 | 1.70 | 0.80 | 2.00 | V |

### On-Chip Termination (OCT) Specifications

If you enable OCT calibration, calibration is automatically performed at power-up for I/Os connected to the calibration block. Table 11 lists the Stratix V OCT termination calibration accuracy specifications.

**Table 11. OCT Calibration Accuracy Specifications for Stratix V Devices (1) (Part 1 of 2)**

| Symbol | Description | Conditions | Calibration Accuracy | | | | Unit |
|---|---|---|---|---|---|---|---|
| | | | C1 | C2,I2 | C3,I3, I3YY | C4,I4 | |
| 25-Ω $R_S$ | Internal series termination with calibration (25-Ω setting) | $V_{CCIO}$ = 3.0, 2.5, 1.8, 1.5, 1.2 V | ±15 | ±15 | ±15 | ±15 | % |

**Table 11. OCT Calibration Accuracy Specifications for Stratix V Devices (1) (Part 2 of 2)**

| Symbol | Description | Conditions | Calibration Accuracy | | | | Unit |
|---|---|---|---|---|---|---|---|
| | | | C1 | C2,I2 | C3,I3, I3YY | C4,I4 | |
| 50-Ω $R_S$ | Internal series termination with calibration (50-Ω setting) | $V_{CCIO}$ = 3.0, 2.5, 1.8, 1.5, 1.2 V | ±15 | ±15 | ±15 | ±15 | % |
| 34-Ω and 40-Ω $R_S$ | Internal series termination with calibration (34-Ω and 40-Ω setting) | $V_{CCIO}$ = 1.5, 1.35, 1.25, 1.2 V | ±15 | ±15 | ±15 | ±15 | % |
| 48-Ω, 60-Ω, 80-Ω, and 240-Ω $R_S$ | Internal series termination with calibration (48-Ω, 60-Ω, 80-Ω, and 240-Ω setting) | $V_{CCIO}$ = 1.2 V | ±15 | ±15 | ±15 | ±15 | % |
| 50-Ω $R_T$ | Internal parallel termination with calibration (50-Ω setting) | $V_{CCIO}$ = 2.5, 1.8, 1.5, 1.2 V | –10 to +40 | –10 to +40 | –10 to +40 | –10 to +40 | % |
| 20-Ω, 30-Ω, 40-Ω,60-Ω, and 120-Ω $R_T$ | Internal parallel termination with calibration (20-Ω, 30-Ω, 40-Ω, 60-Ω, and 120-Ω setting) | $V_{CCIO}$ = 1.5, 1.35, 1.25 V | –10 to +40 | –10 to +40 | –10 to +40 | –10 to +40 | % |
| 60-Ω and 120-Ω $R_T$ | Internal parallel termination with calibration (60-Ω and 120-Ω setting) | $V_{CCIO}$ = 1.2 | –10 to +40 | –10 to +40 | –10 to +40 | –10 to +40 | % |
| 25-Ω $R_{S\_left\_shift}$ | Internal left shift series termination with calibration (25-Ω $R_{S\_left\_shift}$ setting) | $V_{CCIO}$ = 3.0, 2.5, 1.8, 1.5, 1.2 V | ±15 | ±15 | ±15 | ±15 | % |

**Note to Table 11:**

(1) OCT calibration accuracy is valid at the time of calibration only.

Table 12 lists the Stratix V OCT without calibration resistance tolerance to PVT changes.

**Table 12. OCT Without Calibration Resistance Tolerance Specifications for Stratix V Devices (Part 1 of 2)**

| Symbol | Description | Conditions | Resistance Tolerance | | | | Unit |
|---|---|---|---|---|---|---|---|
| | | | C1 | C2,I2 | C3, I3, I3YY | C4, I4 | |
| 25-Ω R, 50-Ω $R_S$ | Internal series termination without calibration (25-Ω setting) | $V_{CCIO}$ = 3.0 and 2.5 V | ±30 | ±30 | ±40 | ±40 | % |
| 25-Ω $R_S$ | Internal series termination without calibration (25-Ω setting) | $V_{CCIO}$ = 1.8 and 1.5 V | ±30 | ±30 | ±40 | ±40 | % |
| 25-Ω $R_S$ | Internal series termination without calibration (25-Ω setting) | $V_{CCIO}$ = 1.2 V | ±35 | ±35 | ±50 | ±50 | % |

## Internal Weak Pull-Up Resistor

Table 16 lists the weak pull-up resistor values for Stratix V devices.

**Table 16. Internal Weak Pull-Up Resistor for Stratix V Devices (1), (2)**

| Symbol | Description | $V_{CCIO}$ Conditions (V) (3) | Value (4) | Unit |
|---|---|---|---|---|
| $R_{PU}$ | Value of the I/O pin pull-up resistor before and during configuration, as well as user mode if you enable the programmable pull-up resistor option. | 3.0 ±5% | 25 | kΩ |
| | | 2.5 ±5% | 25 | kΩ |
| | | 1.8 ±5% | 25 | kΩ |
| | | 1.5 ±5% | 25 | kΩ |
| | | 1.35 ±5% | 25 | kΩ |
| | | 1.25 ±5% | 25 | kΩ |
| | | 1.2 ±5% | 25 | kΩ |

**Notes to Table 16:**

(1) All I/O pins have an option to enable the weak pull-up resistor except the configuration, test, and JTAG pins.

(2) The internal weak pull-down feature is only available for the JTAG TCK pin. The typical value for this internal weak pull-down resistor is approximately 25 kΩ.

(3) The pin pull-up resistance values may be lower if an external source drives the pin higher than $V_{CCIO}$.

(4) These specifications are valid with a ±10% tolerance to cover changes over PVT.

## I/O Standard Specifications

Table 17 through Table 22 list the input voltage ($V_{IH}$ and $V_{IL}$), output voltage ($V_{OH}$ and $V_{OL}$), and current drive characteristics ($I_{OH}$ and $I_{OL}$) for various I/O standards supported by Stratix V devices. These tables also show the Stratix V device family I/O standard specifications. The $V_{OL}$ and $V_{OH}$ values are valid at the corresponding $I_{OH}$ and $I_{OL}$, respectively.

For an explanation of the terms used in Table 17 through Table 22, refer to "Glossary" on page 65. For tolerance calculations across all SSTL and HSTL I/O standards, refer to Altera knowledge base solution rd07262012_486.

**Table 17. Single-Ended I/O Standards for Stratix V Devices**

| I/O Standard | $V_{CCIO}$ (V) | | | $V_{IL}$ (V) | | $V_{IH}$ (V) | | $V_{OL}$ (V) | $V_{OH}$ (V) | $I_{OL}$ (mA) | $I_{OH}$ (mA) |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | Min | Typ | Max | Min | Max | Min | Max | Max | Min | | |
| LVTTL | 2.85 | 3 | 3.15 | –0.3 | 0.8 | 1.7 | 3.6 | 0.4 | 2.4 | 2 | –2 |
| LVCMOS | 2.85 | 3 | 3.15 | –0.3 | 0.8 | 1.7 | 3.6 | 0.2 | $V_{CCIO}$ – 0.2 | 0.1 | –0.1 |
| 2.5 V | 2.375 | 2.5 | 2.625 | –0.3 | 0.7 | 1.7 | 3.6 | 0.4 | 2 | 1 | –1 |
| 1.8 V | 1.71 | 1.8 | 1.89 | –0.3 | 0.35 * $V_{CCIO}$ | 0.65 * $V_{CCIO}$ | $V_{CCIO}$ + 0.3 | 0.45 | $V_{CCIO}$ – 0.45 | 2 | –2 |
| 1.5 V | 1.425 | 1.5 | 1.575 | –0.3 | 0.35 * $V_{CCIO}$ | 0.65 * $V_{CCIO}$ | $V_{CCIO}$ + 0.3 | 0.25 * $V_{CCIO}$ | 0.75 * $V_{CCIO}$ | 2 | –2 |
| 1.2 V | 1.14 | 1.2 | 1.26 | –0.3 | 0.35 * $V_{CCIO}$ | 0.65 * $V_{CCIO}$ | $V_{CCIO}$ + 0.3 | 0.25 * $V_{CCIO}$ | 0.75 * $V_{CCIO}$ | 2 | –2 |

**Table 18. Single-Ended SSTL, HSTL, and HSUL I/O Reference Voltage Specifications for Stratix V Devices**

| I/O Standard | $V_{CCIO}$ (V) | | | $V_{REF}$ (V) | | | $V_{TT}$ (V) | | |
|---|---|---|---|---|---|---|---|---|---|
| | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max |
| SSTL-2 Class I, II | 2.375 | 2.5 | 2.625 | 0.49 * $V_{CCIO}$ | 0.5 * $V_{CCIO}$ | 0.51 * $V_{CCIO}$ | $V_{REF}$ – 0.04 | $V_{REF}$ | $V_{REF}$ + 0.04 |
| SSTL-18 Class I, II | 1.71 | 1.8 | 1.89 | 0.833 | 0.9 | 0.969 | $V_{REF}$ – 0.04 | $V_{REF}$ | $V_{REF}$ + 0.04 |
| SSTL-15 Class I, II | 1.425 | 1.5 | 1.575 | 0.49 * $V_{CCIO}$ | 0.5 * $V_{CCIO}$ | 0.51 * $V_{CCIO}$ | 0.49 * $V_{CCIO}$ | 0.5 * VCCIO | 0.51 * $V_{CCIO}$ |
| SSTL-135 Class I, II | 1.283 | 1.35 | 1.418 | 0.49 * $V_{CCIO}$ | 0.5 * $V_{CCIO}$ | 0.51 * $V_{CCIO}$ | 0.49 * $V_{CCIO}$ | 0.5 * $V_{CCIO}$ | 0.51 * $V_{CCIO}$ |
| SSTL-125 Class I, II | 1.19 | 1.25 | 1.26 | 0.49 * $V_{CCIO}$ | 0.5 * $V_{CCIO}$ | 0.51 * $V_{CCIO}$ | 0.49 * $V_{CCIO}$ | 0.5 * VCCIO | 0.51 * $V_{CCIO}$ |
| SSTL-12 Class I, II | 1.14 | 1.20 | 1.26 | 0.49 * $V_{CCIO}$ | 0.5 * $V_{CCIO}$ | 0.51 * $V_{CCIO}$ | 0.49 * $V_{CCIO}$ | 0.5 * VCCIO | 0.51 * $V_{CCIO}$ |
| HSTL-18 Class I, II | 1.71 | 1.8 | 1.89 | 0.85 | 0.9 | 0.95 | — | $V_{CCIO}$/2 | — |
| HSTL-15 Class I, II | 1.425 | 1.5 | 1.575 | 0.68 | 0.75 | 0.9 | — | $V_{CCIO}$/2 | — |
| HSTL-12 Class I, II | 1.14 | 1.2 | 1.26 | 0.47 * $V_{CCIO}$ | 0.5 * $V_{CCIO}$ | 0.53 * $V_{CCIO}$ | — | $V_{CCIO}$/2 | — |
| HSUL-12 | 1.14 | 1.2 | 1.3 | 0.49 * $V_{CCIO}$ | 0.5 * $V_{CCIO}$ | 0.51 * $V_{CCIO}$ | — | — | — |

**Table 19. Single-Ended SSTL, HSTL, and HSUL I/O Standards Signal Specifications for Stratix V Devices (Part 1 of 2)**

| I/O Standard | $V_{IL(DC)}$ (V) | | $V_{IH(DC)}$ (V) | | $V_{IL(AC)}$ (V) | $V_{IH(AC)}$ (V) | $V_{OL}$ (V) | $V_{OH}$ (V) | $I_{ol}$ (mA) | $I_{oh}$ (mA) |
|---|---|---|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Max | Min | Max | Min | | |
| SSTL-2 Class I | –0.3 | $V_{REF}$ – 0.15 | $V_{REF}$ + 0.15 | $V_{CCIO}$ + 0.3 | $V_{REF}$ – 0.31 | $V_{REF}$ + 0.31 | $V_{TT}$ – 0.608 | $V_{TT}$ + 0.608 | 8.1 | –8.1 |
| SSTL-2 Class II | –0.3 | $V_{REF}$ – 0.15 | $V_{REF}$ + 0.15 | $V_{CCIO}$ + 0.3 | $V_{REF}$ – 0.31 | $V_{REF}$ + 0.31 | $V_{TT}$ – 0.81 | $V_{TT}$ + 0.81 | 16.2 | –16.2 |
| SSTL-18 Class I | –0.3 | $V_{REF}$ – 0.125 | $V_{REF}$ + 0.125 | $V_{CCIO}$ + 0.3 | $V_{REF}$ – 0.25 | $V_{REF}$ + 0.25 | $V_{TT}$ – 0.603 | $V_{TT}$ + 0.603 | 6.7 | –6.7 |
| SSTL-18 Class II | –0.3 | $V_{REF}$ – 0.125 | $V_{REF}$ + 0.125 | $V_{CCIO}$ + 0.3 | $V_{REF}$ – 0.25 | $V_{REF}$ + 0.25 | 0.28 | $V_{CCIO}$ – 0.28 | 13.4 | –13.4 |
| SSTL-15 Class I | — | $V_{REF}$ – 0.1 | $V_{REF}$ + 0.1 | — | $V_{REF}$ – 0.175 | $V_{REF}$ + 0.175 | 0.2 * $V_{CCIO}$ | 0.8 * $V_{CCIO}$ | 8 | –8 |
| SSTL-15 Class II | — | $V_{REF}$ – 0.1 | $V_{REF}$ + 0.1 | — | $V_{REF}$ – 0.175 | $V_{REF}$ + 0.175 | 0.2 * $V_{CCIO}$ | 0.8 * $V_{CCIO}$ | 16 | –16 |
| SSTL-135 Class I, II | — | $V_{REF}$ – 0.09 | $V_{REF}$ + 0.09 | — | $V_{REF}$ – 0.16 | $V_{REF}$ + 0.16 | 0.2 * $V_{CCIO}$ | 0.8 * $V_{CCIO}$ | — | — |
| SSTL-125 Class I, II | — | $V_{REF}$ – 0.85 | $V_{REF}$ + 0.85 | — | $V_{REF}$ – 0.15 | $V_{REF}$ + 0.15 | 0.2 * $V_{CCIO}$ | 0.8 * $V_{CCIO}$ | — | — |
| SSTL-12 Class I, II | — | $V_{REF}$ – 0.1 | $V_{REF}$ + 0.1 | — | $V_{REF}$ – 0.15 | $V_{REF}$ + 0.15 | 0.2 * $V_{CCIO}$ | 0.8 * $V_{CCIO}$ | — | — |

You typically use the interactive Excel-based Early Power Estimator before designing the FPGA to get a magnitude estimate of the device power. The Quartus II PowerPlay Power Analyzer provides better quality estimates based on the specifics of the design after you complete place-and-route. The PowerPlay Power Analyzer can apply a combination of user-entered, simulation-derived, and estimated signal activities that, when combined with detailed circuit models, yields very accurate power estimates.

For more information about power estimation tools, refer to the *PowerPlay Early Power Estimator User Guide* and the *PowerPlay Power Analysis* chapter in the *Quartus II Handbook*.

**Table 23. Transceiver Specifications for Stratix V GX and GS Devices (1) (Part 5 of 7)**

| Symbol/ Description | Conditions | Transceiver Speed Grade 1 | | | Transceiver Speed Grade 2 | | | Transceiver Speed Grade 3 | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| Programmable DC gain | DC Gain Setting = 0 | — | 0 | — | — | 0 | — | — | 0 | — | dB |
| | DC Gain Setting = 1 | — | 2 | — | — | 2 | — | — | 2 | — | dB |
| | DC Gain Setting = 2 | — | 4 | — | — | 4 | — | — | 4 | — | dB |
| | DC Gain Setting = 3 | — | 6 | — | — | 6 | — | — | 6 | — | dB |
| | DC Gain Setting = 4 | — | 8 | — | — | 8 | — | — | 8 | — | dB |
| **Transmitter** | | | | | | | | | | | |
| Supported I/O Standards | — | 1.4-V and 1.5-V PCML | | | | | | | | | |
| Data rate (Standard PCS) | — | 600 | — | 12200 | 600 | — | 12200 | 600 | — | 8500/ 10312.5 (24) | Mbps |
| Data rate (10G PCS) | — | 600 | — | 14100 | 600 | — | 12500 | 600 | — | 8500/ 10312.5 (24) | Mbps |
| Differential on-chip termination resistors | 85-Ω setting | — | 85 ± 20% | — | — | 85 ± 20% | — | — | 85 ± 20% | — | Ω |
| | 100-Ω setting | — | 100 ± 20% | — | — | 100 ± 20% | — | — | 100 ± 20% | — | Ω |
| | 120-Ω setting | — | 120 ± 20% | — | — | 120 ± 20% | — | — | 120 ± 20% | — | Ω |
| | 150-Ω setting | — | 150 ± 20% | — | — | 150 ± 20% | — | — | 150 ± 20% | — | Ω |
| $V_{OCM}$ (AC coupled) | 0.65-V setting | — | 650 | — | — | 650 | — | — | 650 | — | mV |
| $V_{OCM}$ (DC coupled) | — | — | 650 | — | — | 650 | — | — | 650 | — | mV |
| Rise time (7) | 20% to 80% | 30 | — | 160 | 30 | — | 160 | 30 | — | 160 | ps |
| Fall time (7) | 80% to 20% | 30 | — | 160 | 30 | — | 160 | 30 | — | 160 | ps |
| Intra-differential pair skew | Tx $V_{CM}$ = 0.5 V and slew rate of 15 ps | — | — | 15 | — | — | 15 | — | — | 15 | ps |
| Intra-transceiver block transmitter channel-to-channel skew | x6 PMA bonded mode | — | — | 120 | — | — | 120 | — | — | 120 | ps |

**Table 23. Transceiver Specifications for Stratix V GX and GS Devices (1) (Part 6 of 7)**

| Symbol/ Description | Conditions | Transceiver Speed Grade 1 | | | Transceiver Speed Grade 2 | | | Transceiver Speed Grade 3 | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| Inter-transceiver block transmitter channel-to-channel skew | xN PMA bonded mode | — | — | 500 | — | — | 500 | — | — | 500 | ps |
| **CMU PLL** | | | | | | | | | | | |
| Supported Data Range | — | 600 | — | 12500 | 600 | — | 12500 | 600 | — | 8500/ 10312.5 (24) | Mbps |
| $t_{pll\_powerdown}$ (15) | — | 1 | — | — | 1 | — | — | 1 | — | — | µs |
| $t_{pll\_lock}$ (16) | — | — | — | 10 | — | — | 10 | — | — | 10 | µs |
| **ATX PLL** | | | | | | | | | | | |
| Supported Data Rate Range | VCO post-divider L=2 | 8000 | — | 14100 | 8000 | — | 12500 | 8000 | — | 8500/ 10312.5 (24) | Mbps |
| | L=4 | 4000 | — | 7050 | 4000 | — | 6600 | 4000 | — | 6600 | Mbps |
| | L=8 | 2000 | — | 3525 | 2000 | — | 3300 | 2000 | — | 3300 | Mbps |
| | L=8, Local/Central Clock Divider =2 | 1000 | — | 1762.5 | 1000 | — | 1762.5 | 1000 | — | 1762.5 | Mbps |
| $t_{pll\_powerdown}$ (15) | — | 1 | — | — | 1 | — | — | 1 | — | — | µs |
| $t_{pll\_lock}$ (16) | — | — | — | 10 | — | — | 10 | — | — | 10 | µs |
| **fPLL** | | | | | | | | | | | |
| Supported Data Range | — | 600 | — | 3250/ 3125 (25) | 600 | — | 3250/ 3125 (25) | 600 | — | 3250/ 3125 (25) | Mbps |
| $t_{pll\_powerdown}$ (15) | — | 1 | — | — | 1 | — | — | 1 | — | — | µs |

**Table 23. Transceiver Specifications for Stratix V GX and GS Devices (1) (Part 7 of 7)**

| Symbol/ Description | Conditions | Transceiver Speed Grade 1 | | | Transceiver Speed Grade 2 | | | Transceiver Speed Grade 3 | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| $t_{pll\_lock}$ (16) | — | — | — | 10 | — | — | 10 | — | — | 10 | µs |

**Notes to Table 23:**

(1) Speed grades shown in Table 23 refer to the PMA Speed Grade in the device ordering code. The maximum data rate could be restricted by the Core/PCS speed grade. Contact your Altera Sales Representative for the maximum data rate specifications in each speed grade combination offered. For more information about device ordering codes, refer to the *Stratix V Device Overview*.

(2) The reference clock common mode voltage is equal to the $V_{CCR\_GXB}$ power supply level.

(3) This supply must be connected to 1.0 V if the transceiver is configured at a data rate > 6.5 Gbps, and to 1.05 V if configured at a data rate > 10.3 Gbps when DFE is used. For data rates up to 6.5 Gbps, you can connect this supply to 0.85 V.

(4) This supply follows VCCR_GXB.

(5) The device cannot tolerate prolonged operation at this absolute maximum.

(6) The differential eye opening specification at the receiver input pins assumes that **Receiver Equalization** is disabled. If you enable **Receiver Equalization**, the receiver circuitry can tolerate a lower minimum eye opening, depending on the equalization level.

(7) The Quartus II software automatically selects the appropriate slew rate depending on the configured data rate or functional mode.

(8) The input reference clock frequency options depend on the data rate and the device speed grade.

(9) The line data rate may be limited by PCS-FPGA interface speed grade.

(10) Refer to Figure 1 for the GX channel AC gain curves. The total effective AC gain is the AC gain minus the DC gain.

(11) $t_{LTR}$ is the time required for the receive CDR to lock to the input reference clock frequency after coming out of reset.

(12) $t_{LTD}$ is time required for the receiver CDR to start recovering valid data after the rx_is_lockedtodata signal goes high.

(13) $t_{LTD\_manual}$ is the time required for the receiver CDR to start recovering valid data after the rx_is_lockedtodata signal goes high when the CDR is functioning in the manual mode.

(14) $t_{LTR\_LTD\_manual}$ is the time the receiver CDR must be kept in lock to reference (LTR) mode after the rx_is_lockedtoref signal goes high when the CDR is functioning in the manual mode.

(15) $t_{pll\_powerdown}$ is the PLL powerdown minimum pulse width.

(16) $t_{pll\_lock}$ is the time required for the transmitter CMU/ATX PLL to lock to the input reference clock frequency after coming out of reset.

(17) To calculate the REFCLK rms phase jitter requirement for PCIe at reference clock frequencies other than 100 MHz, use the following formula: REFCLK rms phase jitter at f(MHz) = REFCLK rms phase jitter at 100 MHz × 100/f.

(18) The maximum peak to peak differential input voltage $V_{ID}$ after device configuration is equal to 4 × (absolute $V_{MAX}$ for receiver pin - $V_{ICM}$).

(19) For ES devices, $R_{REF}$ is 2000 Ω ±1%.

(20) To calculate the REFCLK phase noise requirement at frequencies other than 622 MHz, use the following formula: REFCLK phase noise at f(MHz) = REFCLK phase noise at 622 MHz + 20*log(f/622).

(21) SFP/+ optical modules require the host interface to have RD+/- differentially terminated with 100 Ω. The internal OCT feature is available after the Stratix V FPGA configuration is completed. Altera recommends that FPGA configuration is completed before inserting the optical module. Otherwise, minimize unnecessary removal and insertion with unconfigured devices.

(22) Refer to Figure 2.

(23) For oversampling designs to support data rates less than the minimum specification, the CDR needs to be in LTR mode only.

(24) I3YY devices can achieve data rates up to 10.3125 Gbps.

(25) When you use fPLL as a TXPLL of the transceiver.

(26) `REFCLK` performance requires to meet transmitter `REFCLK` phase noise specification.

(27) Minimum eye opening of 85 mV is only for the unstressed input eye condition.

Table 25 shows the approximate maximum data rate using the standard PCS.

**Table 25. Stratix V Standard PCS Approximate Maximum Date Rate** *(1), (3)*

| Mode *(2)* | Transceiver Speed Grade | PMA Width | 20 | 20 | 16 | 16 | 10 | 10 | 8 | 8 |
|---|---|---|---|---|---|---|---|---|---|---|
| | | PCS/Core Width | 40 | 20 | 32 | 16 | 20 | 10 | 16 | 8 |
| FIFO | 1 | C1, C2, C2L, I2, I2L core speed grade | 12.2 | 11.4 | 9.76 | 9.12 | 6.5 | 5.8 | 5.2 | 4.72 |
| | 2 | C1, C2, C2L, I2, I2L core speed grade | 12.2 | 11.4 | 9.76 | 9.12 | 6.5 | 5.8 | 5.2 | 4.72 |
| | | C3, I3, I3L core speed grade | 9.8 | 9.0 | 7.84 | 7.2 | 5.3 | 4.7 | 4.24 | 3.76 |
| | 3 | C1, C2, C2L, I2, I2L core speed grade | 8.5 | 8.5 | 8.5 | 8.5 | 6.5 | 5.8 | 5.2 | 4.72 |
| | | I3YY core speed grade | 10.3125 | 10.3125 | 7.84 | 7.2 | 5.3 | 4.7 | 4.24 | 3.76 |
| | | C3, I3, I3L core speed grade | 8.5 | 8.5 | 7.84 | 7.2 | 5.3 | 4.7 | 4.24 | 3.76 |
| | | C4, I4 core speed grade | 8.5 | 8.2 | 7.04 | 6.56 | 4.8 | 4.2 | 3.84 | 3.44 |
| Register | 1 | C1, C2, C2L, I2, I2L core speed grade | 12.2 | 11.4 | 9.76 | 9.12 | 6.1 | 5.7 | 4.88 | 4.56 |
| | 2 | C1, C2, C2L, I2, I2L core speed grade | 12.2 | 11.4 | 9.76 | 9.12 | 6.1 | 5.7 | 4.88 | 4.56 |
| | | C3, I3, I3L core speed grade | 9.8 | 9.0 | 7.92 | 7.2 | 4.9 | 4.5 | 3.96 | 3.6 |
| | 3 | C1, C2, C2L, I2, I2L core speed grade | 10.3125 | 10.3125 | 10.3125 | 10.3125 | 6.1 | 5.7 | 4.88 | 4.56 |
| | | I3YY core speed grade | 10.3125 | 10.3125 | 7.92 | 7.2 | 4.9 | 4.5 | 3.96 | 3.6 |
| | | C3, I3, I3L core speed grade | 8.5 | 8.5 | 7.92 | 7.2 | 4.9 | 4.5 | 3.96 | 3.6 |
| | | C4, I4 core speed grade | 8.5 | 8.2 | 7.04 | 6.56 | 4.4 | 4.1 | 3.52 | 3.28 |

**Notes to Table 25**:

(1) The maximum data rate is in Gbps.

(2) The Phase Compensation FIFO can be configured in FIFO mode or register mode. In the FIFO mode, the pointers are not fixed, and the latency can vary. In the register mode the pointers are fixed for low latency.

(3) The maximum data rate is also constrained by the transceiver speed grade. Refer to Table 1 for the transceiver speed grade.

**Table 28. Transceiver Specifications for Stratix V GT Devices (Part 4 of 5) (1)**

| Symbol/ Description | Conditions | Transceiver Speed Grade 2 | | | Transceiver Speed Grade 3 | | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | Min | Typ | Max | Min | Typ | Max | |
| Data rate | GT channels | 19,600 | — | 28,050 | 19,600 | — | 25,780 | Mbps |
| Differential on-chip termination resistors | GT channels | — | 100 | — | — | 100 | — | Ω |
| | GX channels | (8) | | | | | | |
| $V_{OCM}$ (AC coupled) | GT channels | — | 500 | — | — | 500 | — | mV |
| | GX channels | (8) | | | | | | |
| Rise/Fall time | GT channels | — | 15 | — | — | 15 | — | ps |
| | GX channels | (8) | | | | | | |
| Intra-differential pair skew | GX channels | (8) | | | | | | |
| Intra-transceiver block transmitter channel-to-channel skew | GX channels | (8) | | | | | | |
| Inter-transceiver block transmitter channel-to-channel skew | GX channels | (8) | | | | | | |
| **CMU PLL** | | | | | | | | |
| Supported Data Range | — | 600 | — | 12500 | 600 | — | 8500 | Mbps |
| $t_{pll\_powerdown}$ (13) | — | 1 | — | — | 1 | — | — | µs |
| $t_{pll\_lock}$ (14) | — | — | — | 10 | — | — | 10 | µs |
| **ATX PLL** | | | | | | | | |
| Supported Data Rate Range for GX Channels | VCO post-divider L=2 | 8000 | — | 12500 | 8000 | — | 8500 | Mbps |
| | L=4 | 4000 | — | 6600 | 4000 | — | 6600 | Mbps |
| | L=8 | 2000 | — | 3300 | 2000 | — | 3300 | Mbps |
| | L=8, Local/Central Clock Divider =2 | 1000 | — | 1762.5 | 1000 | — | 1762.5 | Mbps |
| Supported Data Rate Range for GT Channels | VCO post-divider L=2 | 9800 | — | 14025 | 9800 | — | 12890 | Mbps |
| $t_{pll\_powerdown}$ (13) | — | 1 | — | — | 1 | — | — | µs |
| $t_{pll\_lock}$ (14) | — | — | — | 10 | — | — | 10 | µs |
| **fPLL** | | | | | | | | |
| Supported Data Range | — | 600 | — | 3250/ 3.125 (23) | 600 | — | 3250/ 3.125 (23) | Mbps |
| $t_{pll\_powerdown}$ (13) | — | 1 | — | — | 1 | — | — | µs |

Table 29 shows the $V_{OD}$ settings for the GT channel.

**Table 29. Typical $V_{OD}$ Setting for GT Channel, TX Termination = 100 Ω**

| Symbol | $V_{OD}$ Setting | $V_{OD}$ Value (mV) |
|---|---|---|
| $V_{OD}$ differential peak to peak typical (1) | 0 | 0 |
| | 1 | 200 |
| | 2 | 400 |
| | 3 | 600 |
| | 4 | 800 |
| | 5 | 1000 |

**Note:**

(1) Refer to Figure 4.

Figure 6 shows the Stratix V DC gain curves for GT channels.

**Figure 6. DC Gain Curves for GT Channels**

## Transceiver Characterization

This section summarizes the Stratix V transceiver characterization results for compliance with the following protocols:

- Interlaken
- 40G (XLAUI)/100G (CAUI)
- 10GBase-KR
- QSGMII
- XAUI
- SFI
- Gigabit Ethernet (Gbe / GIGE)
- SPAUI
- Serial Rapid IO (SRIO)
- CPRI
- OBSAI
- Hyper Transport (HT)
- SATA
- SAS
- CEI

- XFI
- ASI
- HiGig/HiGig+
- HiGig2/HiGig2+
- Serial Data Converter (SDC)
- GPON
- SDI
- SONET
- Fibre Channel (FC)
- PCIe
- QPI
- SFF-8431

Download the Stratix V Characterization Report Tool to view the characterization report summary for these protocols.

# Core Performance Specifications

This section describes the clock tree, phase-locked loop (PLL), digital signal processing (DSP), memory blocks, configuration, and JTAG specifications.

## Clock Tree Specifications

Table 30 lists the clock tree specifications for Stratix V devices.

**Table 30. Clock Tree Performance for Stratix V Devices** *(1)*

| Symbol | Performance | | | Unit |
|---|---|---|---|---|
| | C1, C2, C2L, I2, and I2L | C3, I3, I3L, and I3YY | C4, I4 | |
| Global and Regional Clock | 717 | 650 | 580 | MHz |
| Periphery Clock | 550 | 500 | 500 | MHz |

**Note to Table 30:**

(1) The Stratix V ES devices are limited to 600 MHz core clock tree performance.

**Table 31. PLL Specifications for Stratix V Devices (Part 3 of 3)**

| Symbol | Parameter | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| $f_{RES}$ | Resolution of VCO frequency ($f_{INPFD}$ = 100 MHz) | 390625 | 5.96 | 0.023 | Hz |

**Notes to Table 31:**

(1) This specification is limited in the Quartus II software by the I/O maximum frequency. The maximum I/O frequency is different for each I/O standard.

(2) This specification is limited by the lower of the two: I/O $f_{MAX}$ or $f_{OUT}$ of the PLL.

(3) A high input jitter directly affects the PLL output jitter. To have low PLL output clock jitter, you must provide a clean clock source < 120 ps.

(4) $f_{REF}$ is fIN/N when N = 1.

(5) Peak-to-peak jitter with a probability level of $10^{-12}$ (14 sigma, 99.99999999974404% confidence level). The output jitter specification applies to the intrinsic jitter of the PLL, when an input jitter of 30 ps is applied. The external memory interface clock output jitter specifications use a different measurement method and are available in Table 44 on page 52.

(6) The cascaded PLL specification is only applicable with the following condition:
a. Upstream PLL: 0.59Mhz ≤ Upstream PLL BW < 1 MHz
b. Downstream PLL: Downstream PLL BW > 2 MHz

(7) High bandwidth PLL settings are not supported in external feedback mode.

(8) The external memory interface clock output jitter specifications use a different measurement method, which is available in Table 42 on page 50.

(9) The VCO frequency reported by the Quartus II software in the PLL Usage Summary section of the compilation report takes into consideration the VCO post-scale counter K value. Therefore, if the counter K has a value of 2, the frequency reported can be lower than the $f_{VCO}$ specification.

(10) This specification only covers fractional PLL for low bandwidth. The $f_{VCO}$ for fractional value range 0.05 - 0.95 must be ≥ 1000 MHz, while $f_{VCO}$ for fractional value range 0.20 - 0.80 must be ≥ 1200 MHz.

(11) This specification only covered fractional PLL for low bandwidth. The $f_{VCO}$ for fractional value range 0.05-0.95 must be ≥ 1000 MHz.

(12) This specification only covered fractional PLL for low bandwidth. The $f_{VCO}$ for fractional value range 0.20-0.80 must be ≥ 1200 MHz.

## DSP Block Specifications

Table 32 lists the Stratix V DSP block performance specifications.

**Table 32. Block Performance Specifications for Stratix V DSP Devices (Part 1 of 2)**

| Mode | Peformance | | | | | | | Unit |
|---|---|---|---|---|---|---|---|---|
| | C1 | C2, C2L | I2, I2L | C3 | I3, I3L, I3YY | C4 | I4 | |
| **Modes using one DSP** | | | | | | | | |
| Three 9 x 9 | 600 | 600 | 600 | 480 | 480 | 420 | 420 | MHz |
| One 18 x 18 | 600 | 600 | 600 | 480 | 480 | 420 | 400 | MHz |
| Two partial 18 x 18 (or 16 x 16) | 600 | 600 | 600 | 480 | 480 | 420 | 400 | MHz |
| One 27 x 27 | 500 | 500 | 500 | 400 | 400 | 350 | 350 | MHz |
| One 36 x 18 | 500 | 500 | 500 | 400 | 400 | 350 | 350 | MHz |
| One sum of two 18 x 18(One sum of 2 16 x 16) | 500 | 500 | 500 | 400 | 400 | 350 | 350 | MHz |
| One sum of square | 500 | 500 | 500 | 400 | 400 | 350 | 350 | MHz |
| One 18 x 18 plus 36 (a x b) + c | 500 | 500 | 500 | 400 | 400 | 350 | 350 | MHz |
| **Modes using two DSPs** | | | | | | | | |
| Three 18 x 18 | 500 | 500 | 500 | 400 | 400 | 350 | 350 | MHz |
| One sum of four 18 x 18 | 475 | 475 | 475 | 380 | 380 | 300 | 300 | MHz |
| One sum of two 27 x 27 | 465 | 465 | 450 | 380 | 380 | 300 | 290 | MHz |
| One sum of two 36 x 18 | 475 | 475 | 475 | 380 | 380 | 300 | 300 | MHz |
| One complex 18 x 18 | 500 | 500 | 500 | 400 | 400 | 350 | 350 | MHz |
| One 36 x 36 | 475 | 475 | 475 | 380 | 380 | 300 | 300 | MHz |

**Table 40. DQS Phase Offset Delay Per Setting for Stratix V Devices (1), (2) (Part 2 of 2)**

| Speed Grade | Min | Max | Unit |
|---|---|---|---|
| C4,I4 | 8 | 16 | ps |

**Notes to Table 40:**

(1) The typical value equals the average of the minimum and maximum values.

(2) The delay settings are linear with a cumulative delay variation of 40 ps for all speed grades. For example, when using a –2 speed grade and applying a 10-phase offset setting to a 90° phase shift at 400 MHz, the expected average cumulative delay is [625 ps + (10 × 10 ps) ± 20 ps] = 725 ps ± 20 ps.

Table 41 lists the DQS phase shift error for Stratix V devices.

**Table 41. DQS Phase Shift Error Specification for DLL-Delayed Clock ($t_{DQS\_PSERR}$) for Stratix V Devices (1)**

| Number of DQS Delay Buffers | C1 | C2, C2L, I2, I2L | C3, I3, I3L, I3YY | C4,I4 | Unit |
|---|---|---|---|---|---|
| 1 | 28 | 28 | 30 | 32 | ps |
| 2 | 56 | 56 | 60 | 64 | ps |
| 3 | 84 | 84 | 90 | 96 | ps |
| 4 | 112 | 112 | 120 | 128 | ps |

**Notes to Table 41:**

(1) This error specification is the absolute maximum and minimum error. For example, skew on three DQS delay buffers in a –2 speed grade is ±78 ps or ±39 ps.

Table 42 lists the memory output clock jitter specifications for Stratix V devices.

**Table 42. Memory Output Clock Jitter Specification for Stratix V Devices (1), (2), (3) (Part 1 of 2)**

| Clock Network | Parameter | Symbol | C1 | | C2, C2L, I2, I2L | | C3, I3, I3L, I3YY | | C4,I4 | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | Min | Max | Min | Max | Min | Max | Min | Max | |
| Regional | Clock period jitter | $t_{JIT(per)}$ | –50 | 50 | –50 | 50 | –55 | 55 | –55 | 55 | ps |
| | Cycle-to-cycle period jitter | $t_{JIT(cc)}$ | –100 | 100 | –100 | 100 | –110 | 110 | –110 | 110 | ps |
| | Duty cycle jitter | $t_{JIT(duty)}$ | –50 | 50 | –50 | 50 | –82.5 | 82.5 | –82.5 | 82.5 | ps |
| Global | Clock period jitter | $t_{JIT(per)}$ | –75 | 75 | –75 | 75 | –82.5 | 82.5 | –82.5 | 82.5 | ps |
| | Cycle-to-cycle period jitter | $t_{JIT(cc)}$ | –150 | 150 | –150 | 150 | –165 | 165 | –165 | 165 | ps |
| | Duty cycle jitter | $t_{JIT(duty)}$ | –75 | 75 | –75 | 75 | –90 | 90 | –90 | 90 | ps |

**Table 48. Minimum Configuration Time Estimation for Stratix V Devices**

| Variant | Member Code | Active Serial (1) | | | Fast Passive Parallel (2) | | |
|---|---|---|---|---|---|---|---|
| | | Width | DCLK (MHz) | Min Config Time (s) | Width | DCLK (MHz) | Min Config Time (s) |
| GS | D3 | 4 | 100 | 0.344 | 32 | 100 | 0.043 |
| | D4 | 4 | 100 | 0.534 | 32 | 100 | 0.067 |
| | | 4 | 100 | 0.344 | 32 | 100 | 0.043 |
| | D5 | 4 | 100 | 0.534 | 32 | 100 | 0.067 |
| | D6 | 4 | 100 | 0.741 | 32 | 100 | 0.093 |
| | D8 | 4 | 100 | 0.741 | 32 | 100 | 0.093 |
| E | E9 | 4 | 100 | 0.857 | 32 | 100 | 0.107 |
| | EB | 4 | 100 | 0.857 | 32 | 100 | 0.107 |

**Notes to Table 48:**

(1) DCLK frequency of 100 MHz using external CLKUSR.

(2) Max FPGA FPP bandwidth may exceed bandwidth available from some external storage or control logic.

# Fast Passive Parallel Configuration Timing

This section describes the fast passive parallel (FPP) configuration timing parameters for Stratix V devices.

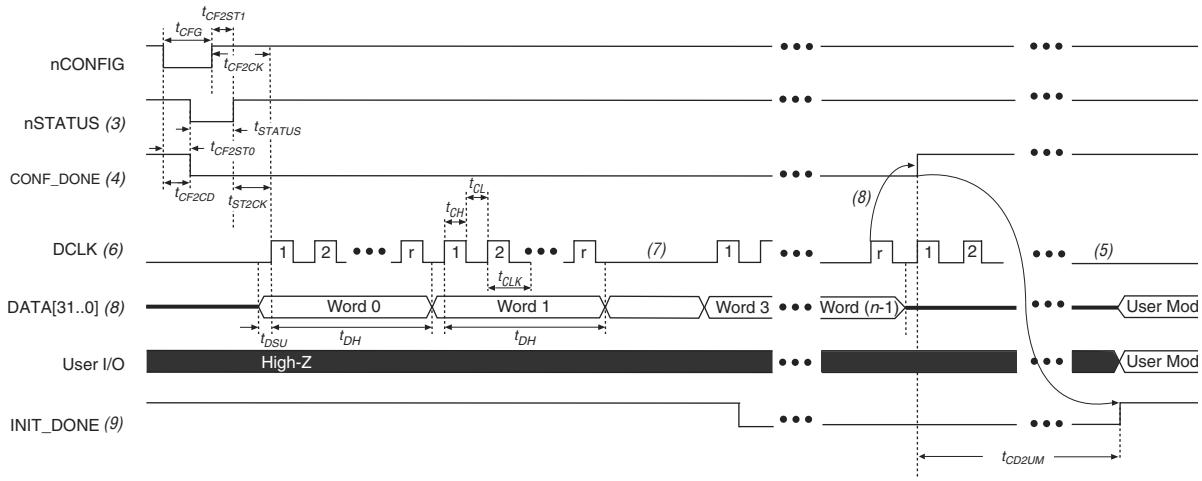
## DCLK-to-DATA[] Ratio for FPP Configuration

FPP configuration requires a different DCLK-to-DATA[] ratio when you enable the design security, decompression, or both features. Table 49 lists the DCLK-to-DATA[] ratio for each combination.

**Table 49. DCLK-to-DATA[] Ratio (1) (Part 1 of 2)**

| Configuration Scheme | Decompression | Design Security | DCLK-to-DATA[] Ratio |
|---|---|---|---|
| FPP ×8 | Disabled | Disabled | 1 |
| | Disabled | Enabled | 1 |
| | Enabled | Disabled | 2 |
| | Enabled | Enabled | 2 |
| FPP ×16 | Disabled | Disabled | 1 |
| | Disabled | Enabled | 2 |
| | Enabled | Disabled | 4 |
| | Enabled | Enabled | 4 |

**Figure 13. FPP Configuration Timing Waveform When the DCLK-to-DATA[] Ratio is >1** *(1), (2)*




**Notes to Figure 13:**

(1) Use this timing waveform and parameters when the DCLK-to-DATA[] ratio is >1. To find out the DCLK-to-DATA[] ratio for your system, refer to Table 49 on page 55.

(2) The beginning of this waveform shows the device in user mode. In user mode, nCONFIG, nSTATUS, and CONF_DONE are at logic high levels. When nCONFIG is pulled low, a reconfiguration cycle begins.

(3) After power-up, the Stratix V device holds nSTATUS low for the time as specified by the POR delay.

(4) After power-up, before and during configuration, CONF_DONE is low.

(5) Do not leave DCLK floating after configuration. You can drive it high or low, whichever is more convenient.

(6) "r" denotes the DCLK-to-DATA[] ratio. For the DCLK-to-DATA[] ratio based on the decompression and the design security feature enable settings, refer to Table 49 on page 55.

(7) If needed, pause DCLK by holding it low. When DCLK restarts, the external host must provide data on the DATA[31..0] pins prior to sending the first DCLK rising edge.

(8) To ensure a successful configuration, send the entire configuration data to the Stratix V device. CONF_DONE is released high after the Stratix V device receives all the configuration data successfully. After CONF_DONE goes high, send two additional falling edges on DCLK to begin initialization and enter user mode.

(9) After the option bit to enable the INIT_DONE pin is configured into the device, the INIT_DONE goes low.

Table 51 lists the timing parameters for Stratix V devices for FPP configuration when the DCLK-to-DATA[] ratio is more than 1.

**Table 51. FPP Timing Parameters for Stratix V Devices When the DCLK-to-DATA[] Ratio is >1 (1)**

| Symbol | Parameter | Minimum | Maximum | Units |
|---|---|---|---|---|
| $t_{CF2CD}$ | nCONFIG low to CONF_DONE low | — | 600 | ns |
| $t_{CF2ST0}$ | nCONFIG low to nSTATUS low | — | 600 | ns |
| $t_{CFG}$ | nCONFIG low pulse width | 2 | — | µs |
| $t_{STATUS}$ | nSTATUS low pulse width | 268 | 1,506 (2) | µs |
| $t_{CF2ST1}$ | nCONFIG high to nSTATUS high | — | 1,506 (2) | µs |
| $t_{CF2CK}$ (5) | nCONFIG high to first rising edge on DCLK | 1,506 | — | µs |
| $t_{ST2CK}$ (5) | nSTATUS high to first rising edge of DCLK | 2 | — | µs |
| $t_{DSU}$ | DATA[] setup time before rising edge on DCLK | 5.5 | — | ns |
| $t_{DH}$ | DATA[] hold time after rising edge on DCLK | N–1/$f_{DCLK}$ (5) | — | s |
| $t_{CH}$ | DCLK high time | 0.45 × 1/$f_{MAX}$ | — | s |
| $t_{CL}$ | DCLK low time | 0.45 × 1/$f_{MAX}$ | — | s |
| $t_{CLK}$ | DCLK period | 1/$f_{MAX}$ | — | s |
| $f_{MAX}$ | DCLK frequency (FPP ×8/×16) | — | 125 | MHz |
| | DCLK frequency (FPP ×32) | — | 100 | MHz |
| $t_R$ | Input rise time | — | 40 | ns |
| $t_F$ | Input fall time | — | 40 | ns |
| $t_{CD2UM}$ | CONF_DONE high to user mode (3) | 175 | 437 | µs |
| $t_{CD2CU}$ | CONF_DONE high to CLKUSR enabled | 4 × maximum DCLK period | — | — |
| $t_{CD2UMC}$ | CONF_DONE high to user mode with CLKUSR option on | $t_{CD2CU}$ + (8576 × CLKUSR period) (4) | — | — |

**Notes to Table 51:**

(1) Use these timing parameters when you use the decompression and design security features.

(2) You can obtain this value if you do not delay configuration by extending the nCONFIG or nSTATUS low pulse width.

(3) The minimum and maximum numbers apply only if you use the internal oscillator as the clock source for initializing the device.

(4) To enable the CLKUSR pin as the initialization clock source and to obtain the maximum frequency specification on these pins, refer to the Initialization section of the "Configuration, Design Security, and Remote System Upgrades in Stratix V Devices" chapter.

(5) N is the DCLK-to-DATA ratio and $f_{DCLK}$ is the DCLK frequency the system is operating.

(6) If nSTATUS is monitored, follow the $t_{ST2CK}$ specification. If nSTATUS is not monitored, follow the $t_{CF2CK}$ specification.