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### Understanding **Embedded - FPGAs (Field Programmable Gate Array)**

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

### Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

#### Details

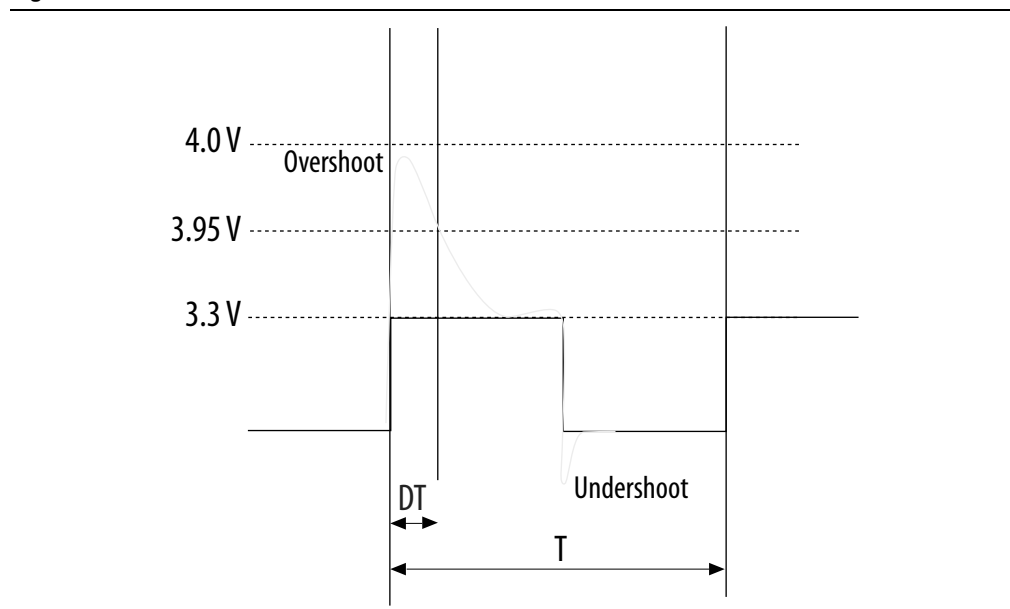
Product Status	Obsolete
Number of LABs/CLBs	225400
Number of Logic Elements/Cells	597000
Total RAM Bits	53248000
Number of I/O	432
Number of Gates	-
Voltage - Supply	0.82V ~ 0.88V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	1517-FBGA (40x40)
Supplier Device Package	1517-FBGA (40x40)
Purchase URL	<a href="https://www.e-xfl.com/product-detail/intel/5sgxeb6r3f40c3n">https://www.e-xfl.com/product-detail/intel/5sgxeb6r3f40c3n</a>

Table 5 lists the maximum allowed input overshoot voltage and the duration of the overshoot voltage as a percentage of device lifetime. The maximum allowed overshoot duration is specified as a percentage of high time over the lifetime of the device. A DC signal is equivalent to 100% of the duty cycle. For example, a signal that overshoots to 3.95 V can be at 3.95 V for only ~21% over the lifetime of the device; for a device lifetime of 10 years, the overshoot duration amounts to ~2 years.

**Table 5. Maximum Allowed Overshoot During Transitions**

Symbol	Description	Condition (V)	Overshoot Duration as % @ $T_J = 100^{\circ}\text{C}$	Unit
$V_i$ (AC)	AC input voltage	3.8	100	%
		3.85	64	%
		3.9	36	%
		3.95	21	%
		4	12	%
		4.05	7	%
		4.1	4	%
		4.15	2	%
		4.2	1	%

**Figure 1. Stratix V Device Overshoot Duration**



**Table 6. Recommended Operating Conditions for Stratix V Devices (Part 2 of 2)**

Symbol	Description	Condition	Min <sup>(4)</sup>	Typ	Max <sup>(4)</sup>	Unit
t <sub>RAMP</sub>	Power supply ramp time	Standard POR	200 $\mu$ s	—	100 ms	—
		Fast POR	200 $\mu$ s	—	4 ms	—

**Notes to Table 6:**

- (1) V<sub>CCPD</sub> must be 2.5 V when V<sub>CCIO</sub> is 2.5, 1.8, 1.5, 1.35, 1.25 or 1.2 V. V<sub>CCPD</sub> must be 3.0 V when V<sub>CCIO</sub> is 3.0 V.
- (2) If you do not use the design security feature in Stratix V devices, connect V<sub>CCBAT</sub> to a 1.2- to 3.0-V power supply. Stratix V power-on-reset (POR) circuitry monitors V<sub>CCBAT</sub>. Stratix V devices will not exit POR if V<sub>CCBAT</sub> stays at logic low.
- (3) C2L and I2L can also be run at 0.90 V for legacy boards that were designed for the C2 and I2 speed grades.
- (4) The power supply value describes the budget for the DC (static) power supply tolerance and does not include the dynamic tolerance requirements. Refer to the PDN tool for the additional budget for the dynamic tolerance requirements.

Table 7 lists the transceiver power supply recommended operating conditions for Stratix V GX, GS, and GT devices.

**Table 7. Recommended Transceiver Power Supply Operating Conditions for Stratix V GX, GS, and GT Devices (Part 1 of 2)**

Symbol	Description	Devices	Minimum <sup>(4)</sup>	Typical	Maximum <sup>(4)</sup>	Unit
V <sub>CCA_GXBL</sub> (1), (3)	Transceiver channel PLL power supply (left side)	GX, GS, GT	2.85	3.0	3.15	V
			2.375	2.5	2.625	
V <sub>CCA_GXBR</sub> (1), (3)	Transceiver channel PLL power supply (right side)	GX, GS	2.85	3.0	3.15	V
			2.375	2.5	2.625	
V <sub>CCA_GTBR</sub>	Transceiver channel PLL power supply (right side)	GT	2.85	3.0	3.15	V
V <sub>CCHIP_L</sub>	Transceiver hard IP power supply (left side; C1, C2, I2, and I3YY speed grades)	GX, GS, GT	0.87	0.9	0.93	V
	Transceiver hard IP power supply (left side; C2L, C3, C4, I2L, I3, I3L, and I4 speed grades)	GX, GS, GT	0.82	0.85	0.88	V
V <sub>CCHIP_R</sub>	Transceiver hard IP power supply (right side; C1, C2, I2, and I3YY speed grades)	GX, GS, GT	0.87	0.9	0.93	V
	Transceiver hard IP power supply (right side; C2L, C3, C4, I2L, I3, I3L, and I4 speed grades)	GX, GS, GT	0.82	0.85	0.88	V
V <sub>CCHSSI_L</sub>	Transceiver PCS power supply (left side; C1, C2, I2, and I3YY speed grades)	GX, GS, GT	0.87	0.9	0.93	V
	Transceiver PCS power supply (left side; C2L, C3, C4, I2L, I3, I3L, and I4 speed grades)	GX, GS, GT	0.82	0.85	0.88	V
V <sub>CCHSSI_R</sub>	Transceiver PCS power supply (right side; C1, C2, I2, and I3YY speed grades)	GX, GS, GT	0.87	0.9	0.93	V
	Transceiver PCS power supply (right side; C2L, C3, C4, I2L, I3, I3L, and I4 speed grades)	GX, GS, GT	0.82	0.85	0.88	V
V <sub>CCR_GXBL</sub> (2)	Receiver analog power supply (left side)	GX, GS, GT	0.82	0.85	0.88	V
			0.87	0.90	0.93	
			0.97	1.0	1.03	
			1.03	1.05	1.07	

**Table 7. Recommended Transceiver Power Supply Operating Conditions for Stratix V GX, GS, and GT Devices (Part 2 of 2)**

Symbol	Description	Devices	Minimum <sup>(4)</sup>	Typical	Maximum <sup>(4)</sup>	Unit
$V_{CCR\_GXBR}$ (2)	Receiver analog power supply (right side)	GX, GS, GT	0.82	0.85	0.88	V
			0.87	0.90	0.93	
			0.97	1.0	1.03	
			1.03	1.05	1.07	
$V_{CCR\_GTBR}$	Receiver analog power supply for GT channels (right side)	GT	1.02	1.05	1.08	V
$V_{CCT\_GXBL}$ (2)	Transmitter analog power supply (left side)	GX, GS, GT	0.82	0.85	0.88	V
			0.87	0.90	0.93	
			0.97	1.0	1.03	
			1.03	1.05	1.07	
$V_{CCT\_GXBR}$ (2)	Transmitter analog power supply (right side)	GX, GS, GT	0.82	0.85	0.88	V
			0.87	0.90	0.93	
			0.97	1.0	1.03	
			1.03	1.05	1.07	
$V_{CCT\_GTBR}$	Transmitter analog power supply for GT channels (right side)	GT	1.02	1.05	1.08	V
$V_{CCL\_GTBR}$	Transmitter clock network power supply	GT	1.02	1.05	1.08	V
$V_{CCH\_GXBL}$	Transmitter output buffer power supply (left side)	GX, GS, GT	1.425	1.5	1.575	V
$V_{CCH\_GXBR}$	Transmitter output buffer power supply (right side)	GX, GS, GT	1.425	1.5	1.575	V

**Notes to Table 7:**

- (1) This supply must be connected to 3.0 V if the CMU PLL, receiver CDR, or both, are configured at a base data rate > 6.5 Gbps. Up to 6.5 Gbps, you can connect this supply to either 3.0 V or 2.5 V.
- (2) Refer to Table 8 to select the correct power supply level for your design.
- (3) When using ATX PLLs, the supply must be 3.0 V.
- (4) This value describes the budget for the DC (static) power supply tolerance and does not include the dynamic tolerance requirements. Refer to the PDN tool for the additional budget for the dynamic tolerance requirements.

### I/O Pin Leakage Current

Table 9 lists the Stratix V I/O pin leakage current specifications.

**Table 9. I/O Pin Leakage Current for Stratix V Devices <sup>(1)</sup>**

Symbol	Description	Conditions	Min	Typ	Max	Unit
$I_I$	Input pin	$V_I = 0 \text{ V to } V_{CCIO\text{MAX}}$	-30	—	30	$\mu\text{A}$
$I_{OZ}$	Tri-stated I/O pin	$V_O = 0 \text{ V to } V_{CCIO\text{MAX}}$	-30	—	30	$\mu\text{A}$

**Note to Table 9:**

(1) If  $V_O = V_{CCIO}$  to  $V_{CCIO\text{MAX}}$ , 100  $\mu\text{A}$  of leakage current per I/O is expected.

### Bus Hold Specifications

Table 10 lists the Stratix V device family bus hold specifications.

**Table 10. Bus Hold Parameters for Stratix V Devices**

Parameter	Symbol	Conditions	V <sub>CCIO</sub>										Unit
			1.2 V		1.5 V		1.8 V		2.5 V		3.0 V		
			Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Low sustaining current	I <sub>SUSL</sub>	V <sub>IN</sub> > V <sub>IL</sub> (maximum)	22.5	—	25.0	—	30.0	—	50.0	—	70.0	—	μA
High sustaining current	I <sub>SUSH</sub>	V <sub>IN</sub> < V <sub>IH</sub> (minimum)	−22.5	—	−25.0	—	−30.0	—	−50.0	—	−70.0	—	μA
Low overdrive current	I <sub>ODL</sub>	0V < V <sub>IN</sub> < V <sub>CCIO</sub>	—	120	—	160	—	200	—	300	—	500	μA
High overdrive current	I <sub>ODH</sub>	0V < V <sub>IN</sub> < V <sub>CCIO</sub>	—	−120	—	−160	—	−200	—	−300	—	−500	μA
Bus-hold trip point	V <sub>TRIP</sub>	—	0.45	0.95	0.50	1.00	0.68	1.07	0.70	1.70	0.80	2.00	V

### On-Chip Termination (OCT) Specifications

If you enable OCT calibration, calibration is automatically performed at power-up for I/Os connected to the calibration block. Table 11 lists the Stratix V OCT termination calibration accuracy specifications.

**Table 11. OCT Calibration Accuracy Specifications for Stratix V Devices <sup>(1)</sup> (Part 1 of 2)**

Symbol	Description	Conditions	Calibration Accuracy				Unit
			C1	C2,I2	C3,I3, I3YY	C4,I4	
25- $\Omega$ $R_S$	Internal series termination with calibration (25- $\Omega$ setting)	$V_{\text{CCIO}} = 3.0, 2.5, 1.8, 1.5, 1.2 \text{ V}$	$\pm 15$	$\pm 15$	$\pm 15$	$\pm 15$	%

**Table 23. Transceiver Specifications for Stratix V GX and GS Devices <sup>(1)</sup> (Part 3 of 7)**

Symbol/ Description	Conditions	Transceiver Speed Grade 1			Transceiver Speed Grade 2			Transceiver Speed Grade 3			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Reconfiguration clock ( <code>mgmt_clk_clk</code> ) frequency	—	100	—	125	100	—	125	100	—	125	MHz
<b>Receiver</b>											
Supported I/O Standards	—	1.4-V PCML, 1.5-V PCML, 2.5-V PCML, LVPECL, and LVDS									
Data rate (Standard PCS) (9), (23)	—	600	—	12200	600	—	12200	600	—	8500/ 10312.5 (24)	Mbps
Data rate (10G PCS) (9), (23)	—	600	—	14100	600	—	12500	600	—	8500/ 10312.5 (24)	Mbps
Absolute $V_{MAX}$ for a receiver pin <sup>(5)</sup>	—	—	—	1.2	—	—	1.2	—	—	1.2	V
Absolute $V_{MIN}$ for a receiver pin	—	−0.4	—	—	−0.4	—	—	−0.4	—	—	V
Maximum peak- to-peak differential input voltage $V_{ID}$ (diff p- p) before device configuration <sup>(22)</sup>	—	—	—	1.6	—	—	1.6	—	—	1.6	V
Maximum peak- to-peak differential input voltage $V_{ID}$ (diff p- p) after device configuration <sup>(18)</sup> , (22)	$V_{CCR\_GXB} =$ 1.0 V/1.05 V ( $V_{ICM} =$ 0.70 V)	—	—	2.0	—	—	2.0	—	—	2.0	V
	$V_{CCR\_GXB} =$ 0.90 V ( $V_{ICM} = 0.6$ V)	—	—	2.4	—	—	2.4	—	—	2.4	V
	$V_{CCR\_GXB} =$ 0.85 V ( $V_{ICM} = 0.6$ V)	—	—	2.4	—	—	2.4	—	—	2.4	V
Minimum differential eye opening at receiver serial input pins <sup>(6)</sup> , (22), (27)	—	85	—	—	85	—	—	85	—	—	mV

**Table 23. Transceiver Specifications for Stratix V GX and GS Devices <sup>(1)</sup> (Part 4 of 7)**

Symbol/ Description	Conditions	Transceiver Speed Grade 1			Transceiver Speed Grade 2			Transceiver Speed Grade 3			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Differential on-chip termination resistors <sup>(21)</sup>	85- $\Omega$ setting	—	85 $\pm$ 30%	—	—	85 $\pm$ 30%	—	—	85 $\pm$ 30%	—	$\Omega$
	100- $\Omega$ setting	—	100 $\pm$ 30%	—	—	100 $\pm$ 30%	—	—	100 $\pm$ 30%	—	$\Omega$
	120- $\Omega$ setting	—	120 $\pm$ 30%	—	—	120 $\pm$ 30%	—	—	120 $\pm$ 30%	—	$\Omega$
	150- $\Omega$ setting	—	150 $\pm$ 30%	—	—	150 $\pm$ 30%	—	—	150 $\pm$ 30%	—	$\Omega$
$V_{ICM}$ (AC and DC coupled)	$V_{CCR\_GXB} = 0.85\text{ V}$ or 0.9 V full bandwidth	—	600	—	—	600	—	—	600	—	mV
	$V_{CCR\_GXB} = 0.85\text{ V}$ or 0.9 V half bandwidth	—	600	—	—	600	—	—	600	—	mV
	$V_{CCR\_GXB} = 1.0\text{ V}/1.05\text{ V}$ full bandwidth	—	700	—	—	700	—	—	700	—	mV
	$V_{CCR\_GXB} = 1.0\text{ V}$ half bandwidth	—	750	—	—	750	—	—	750	—	mV
$t_{LTR}$ <sup>(11)</sup>	—	—	—	10	—	—	10	—	—	10	$\mu\text{s}$
$t_{LTD}$ <sup>(12)</sup>	—	4	—	—	4	—	—	4	—	—	$\mu\text{s}$
$t_{LTD\_manual}$ <sup>(13)</sup>	—	4	—	—	4	—	—	4	—	—	$\mu\text{s}$
$t_{LTR\_LTD\_manual}$ <sup>(14)</sup>	—	15	—	—	15	—	—	15	—	—	$\mu\text{s}$
Run Length	—	—	—	200	—	—	200	—	—	200	UI
Programmable equalization (AC Gain) <sup>(10)</sup>	Full bandwidth (6.25 GHz) Half bandwidth (3.125 GHz)	—	—	16	—	—	16	—	—	16	dB

**Table 23. Transceiver Specifications for Stratix V GX and GS Devices <sup>(1)</sup> (Part 7 of 7)**

Symbol/ Description	Conditions	Transceiver Speed Grade 1			Transceiver Speed Grade 2			Transceiver Speed Grade 3			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
$t_{pll\_lock}^{(16)}$	—	—	—	10	—	—	10	—	—	10	μs

**Notes to Table 23:**

- (1) Speed grades shown in Table 23 refer to the PMA Speed Grade in the device ordering code. The maximum data rate could be restricted by the Core/PCS speed grade. Contact your Altera Sales Representative for the maximum data rate specifications in each speed grade combination offered. For more information about device ordering codes, refer to the *Stratix V Device Overview*.
- (2) The reference clock common mode voltage is equal to the  $V_{CCR\_GXB}$  power supply level.
- (3) This supply must be connected to 1.0 V if the transceiver is configured at a data rate > 6.5 Gbps, and to 1.05 V if configured at a data rate > 10.3 Gbps when DFE is used. For data rates up to 6.5 Gbps, you can connect this supply to 0.85 V.
- (4) This supply follows  $V_{CCR\_GXB}$ .
- (5) The device cannot tolerate prolonged operation at this absolute maximum.
- (6) The differential eye opening specification at the receiver input pins assumes that **Receiver Equalization** is disabled. If you enable **Receiver Equalization**, the receiver circuitry can tolerate a lower minimum eye opening, depending on the equalization level.
- (7) The Quartus II software automatically selects the appropriate slew rate depending on the configured data rate or functional mode.
- (8) The input reference clock frequency options depend on the data rate and the device speed grade.
- (9) The line data rate may be limited by PCS-FPGA interface speed grade.
- (10) Refer to Figure 1 for the GX channel AC gain curves. The total effective AC gain is the AC gain minus the DC gain.
- (11)  $t_{LTR}$  is the time required for the receive CDR to lock to the input reference clock frequency after coming out of reset.
- (12)  $t_{LTD}$  is time required for the receiver CDR to start recovering valid data after the rx\_is\_lockedtodata signal goes high.
- (13)  $t_{LTD\_manual}$  is the time required for the receiver CDR to start recovering valid data after the rx\_is\_lockedtodata signal goes high when the CDR is functioning in the manual mode.
- (14)  $t_{LTR\_LTD\_manual}$  is the time the receiver CDR must be kept in lock to reference (LTR) mode after the rx\_is\_lockedtoref signal goes high when the CDR is functioning in the manual mode.
- (15)  $t_{pll\_powerdown}$  is the PLL powerdown minimum pulse width.
- (16)  $t_{pll\_lock}$  is the time required for the transmitter CMU/ATX PLL to lock to the input reference clock frequency after coming out of reset.
- (17) To calculate the REFCLK rms phase jitter requirement for PCIe at reference clock frequencies other than 100 MHz, use the following formula: REFCLK rms phase jitter at f(MHz) = REFCLK rms phase jitter at 100 MHz  $\times$  100/f.
- (18) The maximum peak to peak differential input voltage  $V_{ID}$  after device configuration is equal to  $4 \times (\text{absolute } V_{MAX} \text{ for receiver pin} - V_{ICM})$ .
- (19) For ES devices,  $R_{REF}$  is  $2000 \Omega \pm 1\%$ .
- (20) To calculate the REFCLK phase noise requirement at frequencies other than 622 MHz, use the following formula: REFCLK phase noise at f(MHz) = REFCLK phase noise at 622 MHz +  $20 \times \log(f/622)$ .
- (21) SFP/+ optical modules require the host interface to have RD+/- differentially terminated with  $100 \Omega$ . The internal OCT feature is available after the Stratix V FPGA configuration is completed. Altera recommends that FPGA configuration is completed before inserting the optical module. Otherwise, minimize unnecessary removal and insertion with unconfigured devices.
- (22) Refer to Figure 2.
- (23) For oversampling designs to support data rates less than the minimum specification, the CDR needs to be in LTR mode only.
- (24) I3YY devices can achieve data rates up to 10.3125 Gbps.
- (25) When you use fPLL as a TXPLL of the transceiver.
- (26) REFCLK performance requires to meet transmitter REFCLK phase noise specification.
- (27) Minimum eye opening of 85 mV is only for the unstressed input eye condition.



Table 24 shows the maximum transmitter data rate for the clock network.

**Table 24. Clock Network Maximum Data Rate Transmitter Specifications <sup>(1)</sup>**

Clock Network	ATX PLL			CMU PLL <sup>(2)</sup>			fPLL		
	Non-bonded Mode (Gbps)	Bonded Mode (Gbps)	Channel Span	Non-bonded Mode (Gbps)	Bonded Mode (Gbps)	Channel Span	Non-bonded Mode (Gbps)	Bonded Mode (Gbps)	Channel Span
x1 <sup>(3)</sup>	14.1	—	6	12.5	—	6	3.125	—	3
x6 <sup>(3)</sup>	—	14.1	6	—	12.5	6	—	3.125	6
x6 PLL Feedback <sup>(4)</sup>	—	14.1	Side-wide	—	12.5	Side-wide	—	—	—
xN (PCIe)	—	8.0	8	—	5.0	8	—	—	—
xN (Native PHY IP)	8.0	8.0	Up to 13 channels above and below PLL	7.99	7.99	Up to 13 channels above and below PLL	3.125	3.125	Up to 13 channels above and below PLL
	—	8.01 to 9.8304	Up to 7 channels above and below PLL						

**Notes to Table 24:**

- (1) Valid data rates below the maximum specified in this table depend on the reference clock frequency and the PLL counter settings. Check the MegaWizard message during the PHY IP instantiation.
- (2) ATX PLL is recommended at 8 Gbps and above data rates for improved jitter performance.
- (3) Channel span is within a transceiver bank.
- (4) Side-wide channel bonding is allowed up to the maximum supported by the PHY IP.

Table 26 shows the approximate maximum data rate using the 10G PCS.

**Table 26. Stratix V 10G PCS Approximate Maximum Data Rate <sup>(1)</sup>**

Mode <sup>(2)</sup>	Transceiver Speed Grade	PMA Width	64	40	40	40	32	32
		PCS Width	64	66/67	50	40	64/66/67	32
FIFO or Register	1	C1, C2, C2L, I2, I2L core speed grade	14.1	14.1	10.69	14.1	13.6	13.6
	2	C1, C2, C2L, I2, I2L core speed grade	12.5	12.5	10.69	12.5	12.5	12.5
		C3, I3, I3L core speed grade	12.5	12.5	10.69	12.5	10.88	10.88
	3	C1, C2, C2L, I2, I2L core speed grade	8.5 Gbps					
		C3, I3, I3L core speed grade						
		C4, I4 core speed grade						
		I3YY core speed grade	10.3125 Gbps					

**Notes to Table 26:**

- (1) The maximum data rate is in Gbps.
- (2) The Phase Compensation FIFO can be configured in FIFO mode or register mode. In the FIFO mode, the pointers are not fixed, and the latency can vary. In the register mode the pointers are fixed for low latency.

Table 27 shows the  $V_{OD}$  settings for the GX channel.

**Table 27. Typical  $V_{OD}$  Setting for GX Channel, TX Termination = 100  $\Omega$  <sup>(2)</sup>**

Symbol	$V_{OD}$ Setting	$V_{OD}$ Value (mV)	$V_{OD}$ Setting	$V_{OD}$ Value (mV)
<b><math>V_{OD}</math> differential peak to peak typical <sup>(3)</sup></b>	0 <sup>(1)</sup>	0	32	640
	1 <sup>(1)</sup>	20	33	660
	2 <sup>(1)</sup>	40	34	680
	3 <sup>(1)</sup>	60	35	700
	4 <sup>(1)</sup>	80	36	720
	5 <sup>(1)</sup>	100	37	740
	6	120	38	760
	7	140	39	780
	8	160	40	800
	9	180	41	820
	10	200	42	840
	11	220	43	860
	12	240	44	880
	13	260	45	900
	14	280	46	920
	15	300	47	940
	16	320	48	960
	17	340	49	980
	18	360	50	1000
	19	380	51	1020
	20	400	52	1040
	21	420	53	1060
	22	440	54	1080
	23	460	55	1100
	24	480	56	1120
	25	500	57	1140
	26	520	58	1160
	27	540	59	1180
	28	560	60	1200
	29	580	61	1220
	30	600	62	1240
	31	620	63	1260

**Note to Table 27:**

- (1) If TX termination resistance = 100 $\Omega$ , this VOD setting is illegal.
- (2) The tolerance is +/-20% for all VOD settings except for settings 2 and below.
- (3) Refer to Figure 2.

**Table 28. Transceiver Specifications for Stratix V GT Devices (Part 1 of 5) <sup>(1)</sup>**

Symbol/ Description	Conditions	Transceiver Speed Grade 2			Transceiver Speed Grade 3			Unit
		Min	Typ	Max	Min	Typ	Max	
Reference Clock								
Supported I/O Standards	Dedicated reference clock pin	1.2-V PCML, 1.4-V PCML, 1.5-V PCML, 2.5-V PCML, Differential LVPECL, LVDS, and HCSL						
	RX reference clock pin	1.4-V PCML, 1.5-V PCML, 2.5-V PCML, LVPECL, and LVDS						
Input Reference Clock Frequency (CMU PLL) <sup>(6)</sup>	—	40	—	710	40	—	710	MHz
Input Reference Clock Frequency (ATX PLL) <sup>(6)</sup>	—	100	—	710	100	—	710	MHz
Rise time	20% to 80%	—	—	400	—	—	400	ps
Fall time	80% to 20%	—	—	400	—	—	400	
Duty cycle	—	45	—	55	45	—	55	%
Spread-spectrum modulating clock frequency	PCI Express (PCIe)	30	—	33	30	—	33	kHz
Spread-spectrum downspread	PCIe	—	0 to −0.5	—	—	0 to −0.5	—	%
On-chip termination resistors <sup>(19)</sup>	—	—	100	—	—	100	—	Ω
Absolute V <sub>MAX</sub> <sup>(3)</sup>	Dedicated reference clock pin	—	—	1.6	—	—	1.6	V
	RX reference clock pin	—	—	1.2	—	—	1.2	
Absolute V <sub>MIN</sub>	—	-0.4	—	—	-0.4	—	—	V
Peak-to-peak differential input voltage	—	200	—	1600	200	—	1600	mV
V <sub>ICM</sub> (AC coupled)	Dedicated reference clock pin	1050/1000 <sup>(2)</sup>			1050/1000 <sup>(2)</sup>			mV
	RX reference clock pin	1.0/0.9/0.85 <sup>(22)</sup>			1.0/0.9/0.85 <sup>(22)</sup>			V
V <sub>ICM</sub> (DC coupled)	HCSL I/O standard for PCIe reference clock	250	—	550	250	—	550	mV

Table 29 shows the  $V_{OD}$  settings for the GT channel.

**Table 29. Typical  $V_{OD}$  Setting for GT Channel, TX Termination = 100  $\Omega$**

Symbol	$V_{OD}$ Setting	$V_{OD}$ Value (mV)
<b><math>V_{OD}</math> differential peak to peak typical <sup>(1)</sup></b>	0	0
	1	200
	2	400
	3	600
	4	800
	5	1000

**Note:**

(1) Refer to Figure 4.

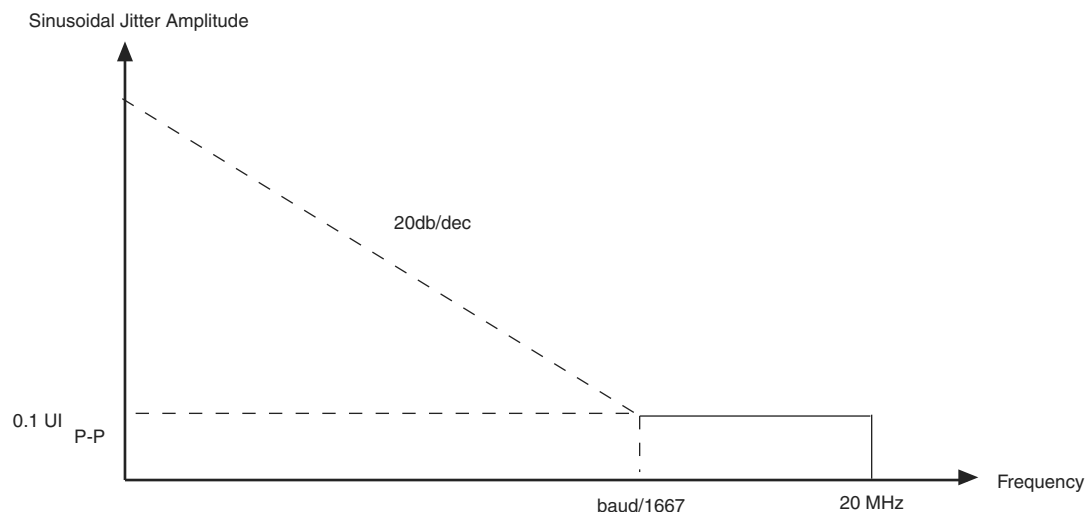
**Table 36. High-Speed I/O Specifications for Stratix V Devices <sup>(1)</sup>, <sup>(2)</sup> (Part 2 of 4)**

Symbol	Conditions	C1			C2, C2L, I2, I2L			C3, I3, I3L, I3YY			C4,I4			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Transmitter														
True Differential I/O Standards - f <sub>HSDR</sub> (data rate)	SERDES factor J = 3 to 10 <sup>(9), (11), (12), (13), (14), (15), (16)</sup>	(6)	—	1600	(6)	—	1434	(6)	—	1250	(6)	—	1050	Mbps
	SERDES factor J ≥ 4  LVDS TX with DPA <sup>(12), (14), (15), (16)</sup>	(6)	—	1600	(6)	—	1600	(6)	—	1600	(6)	—	1250	Mbps
	SERDES factor J = 2, uses DDR Registers	(6)	—	(7)	(6)	—	(7)	(6)	—	(7)	(6)	—	(7)	Mbps
	SERDES factor J = 1, uses SDR Register	(6)	—	(7)	(6)	—	(7)	(6)	—	(7)	(6)	—	(7)	Mbps
Emulated Differential I/O Standards with Three External Output Resistor Networks - f <sub>HSDR</sub> (data rate) <sup>(10)</sup>	SERDES factor J = 4 to 10 <sup>(17)</sup>	(6)	—	1100	(6)	—	1100	(6)	—	840	(6)	—	840	Mbps
t <sub>x Jitter</sub> - True Differential I/O Standards	Total Jitter for Data Rate 600 Mbps - 1.25 Gbps	—	—	160	—	—	160	—	—	160	—	—	160	ps
	Total Jitter for Data Rate < 600 Mbps	—	—	0.1	—	—	0.1	—	—	0.1	—	—	0.1	UI
t <sub>x Jitter</sub> - Emulated Differential I/O Standards with Three External Output Resistor Network	Total Jitter for Data Rate 600 Mbps - 1.25 Gbps	—	—	300	—	—	300	—	—	300	—	—	325	ps
	Total Jitter for Data Rate < 600 Mbps	—	—	0.2	—	—	0.2	—	—	0.2	—	—	0.25	UI

**Table 38. LVDS Soft-CDR/DPA Sinusoidal Jitter Mask Values for a Data Rate  $\geq 1.25$  Gbps**

Jitter Frequency (Hz)		Sinusoidal Jitter (UI)
F1	10,000	25.000
F2	17,565	25.000
F3	1,493,000	0.350
F4	50,000,000	0.350

Figure 9 shows the LVDS soft-CDR/DPA sinusoidal jitter tolerance specification for a data rate  $< 1.25$  Gbps.

**Figure 9. LVDS Soft-CDR/DPA Sinusoidal Jitter Tolerance Specification for a Data Rate  $< 1.25$  Gbps**

### DLL Range, DQS Logic Block, and Memory Output Clock Jitter Specifications

Table 39 lists the DLL range specification for Stratix V devices. The DLL is always in 8-tap mode in Stratix V devices.

**Table 39. DLL Range Specifications for Stratix V Devices <sup>(1)</sup>**

C1	C2, C2L, I2, I2L	C3, I3, I3L, I3YY	C4,I4	Unit
300-933	300-933	300-890	300-890	MHz

**Note to Table 39:**

- (1) Stratix V devices support memory interface frequencies lower than 300 MHz, although the reference clock that feeds the DLL must be at least 300 MHz. To support interfaces below 300 MHz, multiply the reference clock feeding the DLL to ensure the frequency is within the supported range of the DLL.

Table 40 lists the DQS phase offset delay per stage for Stratix V devices.

**Table 40. DQS Phase Offset Delay Per Setting for Stratix V Devices <sup>(1), (2)</sup> (Part 1 of 2)**

Speed Grade	Min	Max	Unit
C1	8	14	ps
C2, C2L, I2, I2L	8	14	ps
C3,I3, I3L, I3YY	8	15	ps

## Duty Cycle Distortion (DCD) Specifications

Table 44 lists the worst-case DCD for Stratix V devices.

**Table 44. Worst-Case DCD on Stratix V I/O Pins <sup>(1)</sup>**

Symbol	C1		C2, C2L, I2, I2L		C3, I3, I3L, I3YY		C4, I4		Unit
	Min	Max	Min	Max	Min	Max	Min	Max	
Output Duty Cycle	45	55	45	55	45	55	45	55	%

**Note to Table 44:**

(1) The DCD numbers do not cover the core clock network.

## Configuration Specification

### POR Delay Specification

Power-on reset (POR) delay is defined as the delay between the time when all the power supplies monitored by the POR circuitry reach the minimum recommended operating voltage to the time when the nSTATUS is released high and your device is ready to begin configuration.



For more information about the POR delay, refer to the *Hot Socketing and Power-On Reset in Stratix V Devices* chapter.

Table 45 lists the fast and standard POR delay specification.

**Table 45. Fast and Standard POR Delay Specification <sup>(1)</sup>**

POR Delay	Minimum	Maximum
Fast	4 ms	12 ms
Standard	100 ms	300 ms

**Note to Table 45:**

(1) You can select the POR delay based on the MSEL settings as described in the MSEL Pin Settings section of the “Configuration, Design Security, and Remote System Upgrades in Stratix V Devices” chapter.

### JTAG Configuration Specifications

Table 46 lists the JTAG timing parameters and values for Stratix V devices.

**Table 46. JTAG Timing Parameters and Values for Stratix V Devices**

Symbol	Description	Min	Max	Unit
t <sub>JCP</sub>	TCK clock period <sup>(2)</sup>	30	—	ns
t <sub>JCP</sub>	TCK clock period <sup>(2)</sup>	167	—	ns
t <sub>JCH</sub>	TCK clock high time <sup>(2)</sup>	14	—	ns
t <sub>JCL</sub>	TCK clock low time <sup>(2)</sup>	14	—	ns
t <sub>JPSU (TDI)</sub>	TDI JTAG port setup time	2	—	ns
t <sub>JPSU (TMS)</sub>	TMS JTAG port setup time	3	—	ns



Table 50 lists the timing parameters for Stratix V devices for FPP configuration when the DCLK-to-DATA [] ratio is 1.

**Table 50. FPP Timing Parameters for Stratix V Devices <sup>(1)</sup>**

Symbol	Parameter	Minimum	Maximum	Units
t <sub>CF2CD</sub>	nCONFIG low to CONF_DONE low	—	600	ns
t <sub>CF2ST0</sub>	nCONFIG low to nSTATUS low	—	600	ns
t <sub>CFG</sub>	nCONFIG low pulse width	2	—	μs
t <sub>STATUS</sub>	nSTATUS low pulse width	268	1,506 <sup>(2)</sup>	μs
t <sub>CF2ST1</sub>	nCONFIG high to nSTATUS high	—	1,506 <sup>(3)</sup>	μs
t <sub>CF2CK</sub> <sup>(6)</sup>	nCONFIG high to first rising edge on DCLK	1,506	—	μs
t <sub>ST2CK</sub> <sup>(6)</sup>	nSTATUS high to first rising edge of DCLK	2	—	μs
t <sub>DSU</sub>	DATA [] setup time before rising edge on DCLK	5.5	—	ns
t <sub>DH</sub>	DATA [] hold time after rising edge on DCLK	0	—	ns
t <sub>CH</sub>	DCLK high time	$0.45 \times 1/f_{\text{MAX}}$	—	s
t <sub>CL</sub>	DCLK low time	$0.45 \times 1/f_{\text{MAX}}$	—	s
t <sub>CLK</sub>	DCLK period	$1/f_{\text{MAX}}$	—	s
f <sub>MAX</sub>	DCLK frequency (FPP $\times 8/\times 16$ )	—	125	MHz
	DCLK frequency (FPP $\times 32$ )	—	100	MHz
t <sub>CD2UM</sub>	CONF_DONE high to user mode <sup>(4)</sup>	175	437	μs
t <sub>CD2CU</sub>	CONF_DONE high to CLKUSR enabled	4 × maximum DCLK period	—	—
t <sub>CD2UMC</sub>	CONF_DONE high to user mode with CLKUSR option on	t <sub>CD2CU</sub> + (8576 × CLKUSR period) <sup>(5)</sup>	—	—

**Notes to Table 50:**

- (1) Use these timing parameters when the decompression and design security features are disabled.
- (2) This value is applicable if you do not delay configuration by extending the nCONFIG or nSTATUS low pulse width.
- (3) This value is applicable if you do not delay configuration by externally holding the nSTATUS low.
- (4) The minimum and maximum numbers apply only if you chose the internal oscillator as the clock source for initializing the device.
- (5) To enable the CLKUSR pin as the initialization clock source and to obtain the maximum frequency specification on these pins, refer to the Initialization section of the “Configuration, Design Security, and Remote System Upgrades in Stratix V Devices” chapter.
- (6) If nSTATUS is monitored, follow the t<sub>ST2CK</sub> specification. If nSTATUS is not monitored, follow the t<sub>CF2CK</sub> specification.

### FPP Configuration Timing when DCLK-to-DATA [] > 1

Figure 13 shows the timing waveform for FPP configuration when using a MAX II device, MAX V device, or microprocessor as an external host. This waveform shows timing when the DCLK-to-DATA [] ratio is more than 1.

Table 51 lists the timing parameters for Stratix V devices for FPP configuration when the DCLK-to-DATA [ ] ratio is more than 1.

**Table 51. FPP Timing Parameters for Stratix V Devices When the DCLK-to-DATA[ ] Ratio is >1 <sup>(1)</sup>**

Symbol	Parameter	Minimum	Maximum	Units
$t_{CF2CD}$	nCONFIG low to CONF_DONE low	—	600	ns
$t_{CF2ST0}$	nCONFIG low to nSTATUS low	—	600	ns
$t_{CFG}$	nCONFIG low pulse width	2	—	$\mu$ s
$t_{STATUS}$	nSTATUS low pulse width	268	1,506 <sup>(2)</sup>	$\mu$ s
$t_{CF2ST1}$	nCONFIG high to nSTATUS high	—	1,506 <sup>(2)</sup>	$\mu$ s
$t_{CF2CK}$ <sup>(5)</sup>	nCONFIG high to first rising edge on DCLK	1,506	—	$\mu$ s
$t_{ST2CK}$ <sup>(5)</sup>	nSTATUS high to first rising edge of DCLK	2	—	$\mu$ s
$t_{DSU}$	DATA [ ] setup time before rising edge on DCLK	5.5	—	ns
$t_{DH}$	DATA [ ] hold time after rising edge on DCLK	$N-1/f_{DCLK}$ <sup>(5)</sup>	—	s
$t_{CH}$	DCLK high time	$0.45 \times 1/f_{MAX}$	—	s
$t_{CL}$	DCLK low time	$0.45 \times 1/f_{MAX}$	—	s
$t_{CLK}$	DCLK period	$1/f_{MAX}$	—	s
$f_{MAX}$	DCLK frequency (FPP $\times 8/\times 16$ )	—	125	MHz
	DCLK frequency (FPP $\times 32$ )	—	100	MHz
$t_R$	Input rise time	—	40	ns
$t_F$	Input fall time	—	40	ns
$t_{CD2UM}$	CONF_DONE high to user mode <sup>(3)</sup>	175	437	$\mu$ s
$t_{CD2CU}$	CONF_DONE high to CLKUSR enabled	$4 \times$ maximum DCLK period	—	—
$t_{CD2UMC}$	CONF_DONE high to user mode with CLKUSR option on	$t_{CD2CU} + (8576 \times \text{CLKUSR period})$ <sup>(4)</sup>	—	—

**Notes to Table 51:**

- (1) Use these timing parameters when you use the decompression and design security features.
- (2) You can obtain this value if you do not delay configuration by extending the nCONFIG or nSTATUS low pulse width.
- (3) The minimum and maximum numbers apply only if you use the internal oscillator as the clock source for initializing the device.
- (4) To enable the CLKUSR pin as the initialization clock source and to obtain the maximum frequency specification on these pins, refer to the Initialization section of the “Configuration, Design Security, and Remote System Upgrades in Stratix V Devices” chapter.
- (5) N is the DCLK-to-DATA ratio and  $f_{DCLK}$  is the DCLK frequency the system is operating.
- (6) If nSTATUS is monitored, follow the  $t_{ST2CK}$  specification. If nSTATUS is not monitored, follow the  $t_{CF2CK}$  specification.

## Remote System Upgrades

Table 56 lists the timing parameter specifications for the remote system upgrade circuitry.

**Table 56. Remote System Upgrade Circuitry Timing Specifications**

Parameter	Minimum	Maximum	Unit
$t_{RU\_nCONFIG}^{(1)}$	250	—	ns
$t_{RU\_nRSTIMER}^{(2)}$	250	—	ns

**Notes to Table 56:**

- (1) This is equivalent to strobing the reconfiguration input of the ALTREMOTE\_UPDATE megafunction high for the minimum timing specification. For more information, refer to the Remote System Upgrade State Machine section of the “Configuration, Design Security, and Remote System Upgrades in Stratix V Devices” chapter.
- (2) This is equivalent to strobing the reset\_timer input of the ALTREMOTE\_UPDATE megafunction high for the minimum timing specification. For more information, refer to the User Watchdog Timer section of the “Configuration, Design Security, and Remote System Upgrades in Stratix V Devices” chapter.

## User Watchdog Internal Circuitry Timing Specification

Table 57 lists the operating range of the 12.5-MHz internal oscillator.

**Table 57. 12.5-MHz Internal Oscillator Specifications**

Minimum	Typical	Maximum	Units
5.3	7.9	12.5	MHz

## I/O Timing

Altera offers two ways to determine I/O timing—the Excel-based I/O Timing and the Quartus II Timing Analyzer.

Excel-based I/O timing provides pin timing performance for each device density and speed grade. The data is typically used prior to designing the FPGA to get an estimate of the timing budget as part of the link timing analysis. The Quartus II Timing Analyzer provides a more accurate and precise I/O timing data based on the specifics of the design after you complete place-and-route.



You can download the Excel-based I/O Timing spreadsheet from the Stratix V Devices Documentation web page.

## Programmable IOE Delay

Table 58 lists the Stratix V IOE programmable delay settings.

**Table 58. IOE Programmable Delay for Stratix V Devices (Part 1 of 2)**

Parameter (1)	Available Settings	Min Offset (2)	Fast Model		Slow Model							
			Industrial	Commercial	C1	C2	C3	C4	I2	I3, I3YY	I4	Unit
D1	64	0	0.464	0.493	0.838	0.838	0.924	1.011	0.844	0.921	1.006	ns
D2	32	0	0.230	0.244	0.415	0.415	0.459	0.503	0.417	0.456	0.500	ns

**Table 60. Glossary (Part 4 of 4)**

Letter	Subject	Definitions
<b>V</b>	$V_{CM(DC)}$	DC common mode input voltage.
	$V_{ICM}$	Input common mode voltage—The common mode of the differential signal at the receiver.
	$V_{ID}$	Input differential voltage swing—The difference in voltage between the positive and complementary conductors of a differential transmission at the receiver.
	$V_{DIF(AC)}$	AC differential input voltage—Minimum AC input differential voltage required for switching.
	$V_{DIF(DC)}$	DC differential input voltage— Minimum DC input differential voltage required for switching.
	$V_{IH}$	Voltage input high—The minimum positive voltage applied to the input which is accepted by the device as a logic high.
	$V_{IH(AC)}$	High-level AC input voltage
	$V_{IH(DC)}$	High-level DC input voltage
	$V_{IL}$	Voltage input low—The maximum positive voltage applied to the input which is accepted by the device as a logic low.
	$V_{IL(AC)}$	Low-level AC input voltage
	$V_{IL(DC)}$	Low-level DC input voltage
	$V_{OCM}$	Output common mode voltage—The common mode of the differential signal at the transmitter.
	$V_{OD}$	Output differential voltage swing—The difference in voltage between the positive and complementary conductors of a differential transmission at the transmitter.
	$V_{SWING}$	Differential input voltage
	$V_X$	Input differential cross point voltage
	$V_{OX}$	Output differential cross point voltage
<b>W</b>	W	High-speed I/O block—clock boost factor
<b>X</b>	—	—
<b>Y</b>		
<b>Z</b>		

**Table 61. Document Revision History (Part 3 of 3)**

Date	Version	Changes
May 2013	2.7	<ul style="list-style-type: none"> <li>■ Updated Table 2, Table 6, Table 7, Table 20, Table 23, Table 27, Table 47, Table 60</li> <li>■ Added Table 24, Table 48</li> <li>■ Updated Figure 9, Figure 10, Figure 11, Figure 12</li> </ul>
February 2013	2.6	<ul style="list-style-type: none"> <li>■ Updated Table 7, Table 9, Table 20, Table 23, Table 27, Table 30, Table 31, Table 35, Table 46</li> <li>■ Updated “Maximum Allowed Overshoot and Undershoot Voltage”</li> </ul>
December 2012	2.5	<ul style="list-style-type: none"> <li>■ Updated Table 3, Table 6, Table 7, Table 8, Table 23, Table 24, Table 25, Table 27, Table 30, Table 32, Table 35</li> <li>■ Added Table 33</li> <li>■ Added “Fast Passive Parallel Configuration Timing”</li> <li>■ Added “Active Serial Configuration Timing”</li> <li>■ Added “Passive Serial Configuration Timing”</li> <li>■ Added “Remote System Upgrades”</li> <li>■ Added “User Watchdog Internal Circuitry Timing Specification”</li> <li>■ Added “Initialization”</li> <li>■ Added “Raw Binary File Size”</li> </ul>
June 2012	2.4	<ul style="list-style-type: none"> <li>■ Added Figure 1, Figure 2, and Figure 3.</li> <li>■ Updated Table 1, Table 2, Table 3, Table 6, Table 11, Table 22, Table 23, Table 27, Table 29, Table 30, Table 31, Table 32, Table 35, Table 38, Table 39, Table 40, Table 41, Table 43, Table 56, and Table 59.</li> <li>■ Various edits throughout to fix bugs.</li> <li>■ Changed title of document to <i>Stratix V Device Datasheet</i>.</li> <li>■ Removed document from the Stratix V handbook and made it a separate document.</li> </ul>
February 2012	2.3	<ul style="list-style-type: none"> <li>■ Updated Table 1–22, Table 1–29, Table 1–31, and Table 1–31.</li> </ul>
December 2011	2.2	<ul style="list-style-type: none"> <li>■ Added Table 2–31.</li> <li>■ Updated Table 2–28 and Table 2–34.</li> </ul>
November 2011	2.1	<ul style="list-style-type: none"> <li>■ Added Table 2–2 and Table 2–21 and updated Table 2–5 with information about Stratix V GT devices.</li> <li>■ Updated Table 2–11, Table 2–13, Table 2–20, and Table 2–25.</li> <li>■ Various edits throughout to fix SPRs.</li> </ul>
May 2011	2.0	<ul style="list-style-type: none"> <li>■ Updated Table 2–4, Table 2–18, Table 2–19, Table 2–21, Table 2–22, Table 2–23, and Table 2–24.</li> <li>■ Updated the “DQ Logic Block and Memory Output Clock Jitter Specifications” title.</li> <li>■ Chapter moved to Volume 1.</li> <li>■ Minor text edits.</li> </ul>
December 2010	1.1	<ul style="list-style-type: none"> <li>■ Updated Table 1–2, Table 1–4, Table 1–19, and Table 1–23.</li> <li>■ Converted chapter to the new template.</li> <li>■ Minor text edits.</li> </ul>
July 2010	1.0	Initial release.