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Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Obsolete
Number of LABs/CLBs	225400
Number of Logic Elements/Cells	597000
Total RAM Bits	53248000
Number of I/O	600
Number of Gates	-
Voltage - Supply	0.87V ~ 0.93V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	1760-BBGA, FCBGA
Supplier Device Package	1760-FCBGA (42.5x42.5)
Purchase URL	https://www.e-xfl.com/product-detail/intel/5sgxeb6r3f43c2

Table 1. Stratix V GX and GS Commercial and Industrial Speed Grade Offering ^{(1), (2), (3)} (Part 2 of 2)

Transceiver Speed Grade	Core Speed Grade							
	C1	C2, C2L	C3	C4	I2, I2L	I3, I3L	I3YY	I4
3 GX channel—8.5 Gbps	—	Yes	Yes	Yes	—	Yes	Yes ⁽⁴⁾	Yes

Notes to Table 1:

- (1) C = Commercial temperature grade; I = Industrial temperature grade.
 (2) Lower number refers to faster speed grade.
 (3) C2L, I2L, and I3L speed grades are for low-power devices.
 (4) I3YY speed grades can achieve up to 10.3125 Gbps.

Table 2 lists the industrial and commercial speed grades for the Stratix V GT devices.

Table 2. Stratix V GT Commercial and Industrial Speed Grade Offering ^{(1), (2)}

Transceiver Speed Grade	Core Speed Grade			
	C1	C2	I2	I3
2 GX channel—12.5 Gbps GT channel—28.05 Gbps	Yes	Yes	—	—
3 GX channel—12.5 Gbps GT channel—25.78 Gbps	Yes	Yes	Yes	Yes

Notes to Table 2:

- (1) C = Commercial temperature grade; I = Industrial temperature grade.
 (2) Lower number refers to faster speed grade.

Absolute Maximum Ratings

Absolute maximum ratings define the maximum operating conditions for Stratix V devices. The values are based on experiments conducted with the devices and theoretical modeling of breakdown and damage mechanisms. The functional operation of the device is not implied for these conditions.



Conditions other than those listed in Table 3 may cause permanent damage to the device. Additionally, device operation at the absolute maximum ratings for extended periods of time may have adverse effects on the device.

Table 3. Absolute Maximum Ratings for Stratix V Devices (Part 1 of 2)

Symbol	Description	Minimum	Maximum	Unit
V _{CC}	Power supply for core voltage and periphery circuitry	−0.5	1.35	V
V _{CCPT}	Power supply for programmable power technology	−0.5	1.8	V
V _{CCPGM}	Power supply for configuration pins	−0.5	3.9	V
V _{CC_AUX}	Auxiliary supply for the programmable power technology	−0.5	3.4	V
V _{CCBAT}	Battery back-up power supply for design security volatile key register	−0.5	3.9	V
V _{CCPD}	I/O pre-driver power supply	−0.5	3.9	V
V _{CCIO}	I/O power supply	−0.5	3.9	V

Table 3. Absolute Maximum Ratings for Stratix V Devices (Part 2 of 2)

Symbol	Description	Minimum	Maximum	Unit
V _{CCD_FPLL}	PLL digital power supply	−0.5	1.8	V
V _{CCA_FPLL}	PLL analog power supply	−0.5	3.4	V
V _I	DC input voltage	−0.5	3.8	V
T _J	Operating junction temperature	−55	125	°C
T _{STG}	Storage temperature (No bias)	−65	150	°C
I _{OUT}	DC output current per pin	−25	40	mA

Table 4 lists the absolute conditions for the transceiver power supply for Stratix V GX, GS, and GT devices.

Table 4. Transceiver Power Supply Absolute Conditions for Stratix V GX, GS, and GT Devices

Symbol	Description	Devices	Minimum	Maximum	Unit
V _{CCA_GXBL}	Transceiver channel PLL power supply (left side)	GX, GS, GT	−0.5	3.75	V
V _{CCA_GXBR}	Transceiver channel PLL power supply (right side)	GX, GS	−0.5	3.75	V
V _{CCA_GTBR}	Transceiver channel PLL power supply (right side)	GT	−0.5	3.75	V
V _{CCHIP_L}	Transceiver hard IP power supply (left side)	GX, GS, GT	−0.5	1.35	V
V _{CCHIP_R}	Transceiver hard IP power supply (right side)	GX, GS, GT	−0.5	1.35	V
V _{CCHSSI_L}	Transceiver PCS power supply (left side)	GX, GS, GT	−0.5	1.35	V
V _{CCHSSI_R}	Transceiver PCS power supply (right side)	GX, GS, GT	−0.5	1.35	V
V _{CCR_GXBL}	Receiver analog power supply (left side)	GX, GS, GT	−0.5	1.35	V
V _{CCR_GXBR}	Receiver analog power supply (right side)	GX, GS, GT	−0.5	1.35	V
V _{CCR_GTBR}	Receiver analog power supply for GT channels (right side)	GT	−0.5	1.35	V
V _{CCT_GXBL}	Transmitter analog power supply (left side)	GX, GS, GT	−0.5	1.35	V
V _{CCT_GXBR}	Transmitter analog power supply (right side)	GX, GS, GT	−0.5	1.35	V
V _{CCT_GTBR}	Transmitter analog power supply for GT channels (right side)	GT	−0.5	1.35	V
V _{CCL_GTBR}	Transmitter clock network power supply (right side)	GT	−0.5	1.35	V
V _{CCH_GXBL}	Transmitter output buffer power supply (left side)	GX, GS, GT	−0.5	1.8	V
V _{CCH_GXBR}	Transmitter output buffer power supply (right side)	GX, GS, GT	−0.5	1.8	V

Maximum Allowed Overshoot and Undershoot Voltage

During transitions, input signals may overshoot to the voltage shown in Table 5 and undershoot to −2.0 V for input currents less than 100 mA and periods shorter than 20 ns.

Table 7. Recommended Transceiver Power Supply Operating Conditions for Stratix V GX, GS, and GT Devices (Part 2 of 2)

Symbol	Description	Devices	Minimum ⁽⁴⁾	Typical	Maximum ⁽⁴⁾	Unit
V_{CCR_GXBR} (2)	Receiver analog power supply (right side)	GX, GS, GT	0.82	0.85	0.88	V
			0.87	0.90	0.93	
			0.97	1.0	1.03	
			1.03	1.05	1.07	
V_{CCR_GTBR}	Receiver analog power supply for GT channels (right side)	GT	1.02	1.05	1.08	V
V_{CCT_GXBL} (2)	Transmitter analog power supply (left side)	GX, GS, GT	0.82	0.85	0.88	V
			0.87	0.90	0.93	
			0.97	1.0	1.03	
			1.03	1.05	1.07	
V_{CCT_GXBR} (2)	Transmitter analog power supply (right side)	GX, GS, GT	0.82	0.85	0.88	V
			0.87	0.90	0.93	
			0.97	1.0	1.03	
			1.03	1.05	1.07	
V_{CCT_GTBR}	Transmitter analog power supply for GT channels (right side)	GT	1.02	1.05	1.08	V
V_{CCL_GTBR}	Transmitter clock network power supply	GT	1.02	1.05	1.08	V
V_{CCH_GXBL}	Transmitter output buffer power supply (left side)	GX, GS, GT	1.425	1.5	1.575	V
V_{CCH_GXBR}	Transmitter output buffer power supply (right side)	GX, GS, GT	1.425	1.5	1.575	V

Notes to Table 7:

- (1) This supply must be connected to 3.0 V if the CMU PLL, receiver CDR, or both, are configured at a base data rate > 6.5 Gbps. Up to 6.5 Gbps, you can connect this supply to either 3.0 V or 2.5 V.
- (2) Refer to Table 8 to select the correct power supply level for your design.
- (3) When using ATX PLLs, the supply must be 3.0 V.
- (4) This value describes the budget for the DC (static) power supply tolerance and does not include the dynamic tolerance requirements. Refer to the PDN tool for the additional budget for the dynamic tolerance requirements.

Table 18. Single-Ended SSTL, HSTL, and HSUL I/O Reference Voltage Specifications for Stratix V Devices

I/O Standard	V_{CCIO} (V)			V_{REF} (V)			V_{TT} (V)		
	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max
SSTL-2 Class I, II	2.375	2.5	2.625	$0.49 * V_{CCIO}$	$0.5 * V_{CCIO}$	$0.51 * V_{CCIO}$	$V_{REF} - 0.04$	V_{REF}	$V_{REF} + 0.04$
SSTL-18 Class I, II	1.71	1.8	1.89	0.833	0.9	0.969	$V_{REF} - 0.04$	V_{REF}	$V_{REF} + 0.04$
SSTL-15 Class I, II	1.425	1.5	1.575	$0.49 * V_{CCIO}$	$0.5 * V_{CCIO}$	$0.51 * V_{CCIO}$	$0.49 * V_{CCIO}$	$0.5 * V_{CCIO}$	$0.51 * V_{CCIO}$
SSTL-135 Class I, II	1.283	1.35	1.418	$0.49 * V_{CCIO}$	$0.5 * V_{CCIO}$	$0.51 * V_{CCIO}$	$0.49 * V_{CCIO}$	$0.5 * V_{CCIO}$	$0.51 * V_{CCIO}$
SSTL-125 Class I, II	1.19	1.25	1.26	$0.49 * V_{CCIO}$	$0.5 * V_{CCIO}$	$0.51 * V_{CCIO}$	$0.49 * V_{CCIO}$	$0.5 * V_{CCIO}$	$0.51 * V_{CCIO}$
SSTL-12 Class I, II	1.14	1.20	1.26	$0.49 * V_{CCIO}$	$0.5 * V_{CCIO}$	$0.51 * V_{CCIO}$	$0.49 * V_{CCIO}$	$0.5 * V_{CCIO}$	$0.51 * V_{CCIO}$
HSTL-18 Class I, II	1.71	1.8	1.89	0.85	0.9	0.95	—	$V_{CCIO}/2$	—
HSTL-15 Class I, II	1.425	1.5	1.575	0.68	0.75	0.9	—	$V_{CCIO}/2$	—
HSTL-12 Class I, II	1.14	1.2	1.26	$0.47 * V_{CCIO}$	$0.5 * V_{CCIO}$	$0.53 * V_{CCIO}$	—	$V_{CCIO}/2$	—
HSUL-12	1.14	1.2	1.3	$0.49 * V_{CCIO}$	$0.5 * V_{CCIO}$	$0.51 * V_{CCIO}$	—	—	—

Table 19. Single-Ended SSTL, HSTL, and HSUL I/O Standards Signal Specifications for Stratix V Devices (Part 1 of 2)

I/O Standard	$V_{IL(DC)}$ (V)		$V_{IH(DC)}$ (V)		$V_{IL(AC)}$ (V)	$V_{IH(AC)}$ (V)	V_{OL} (V)	V_{OH} (V)	I_{OI} (mA)	I_{OH} (mA)
	Min	Max	Min	Max	Max	Min	Max	Min		
SSTL-2 Class I	-0.3	$V_{REF} - 0.15$	$V_{REF} + 0.15$	$V_{CCIO} + 0.3$	$V_{REF} - 0.31$	$V_{REF} + 0.31$	$V_{TT} - 0.608$	$V_{TT} + 0.608$	8.1	-8.1
SSTL-2 Class II	-0.3	$V_{REF} - 0.15$	$V_{REF} + 0.15$	$V_{CCIO} + 0.3$	$V_{REF} - 0.31$	$V_{REF} + 0.31$	$V_{TT} - 0.81$	$V_{TT} + 0.81$	16.2	-16.2
SSTL-18 Class I	-0.3	$V_{REF} - 0.125$	$V_{REF} + 0.125$	$V_{CCIO} + 0.3$	$V_{REF} - 0.25$	$V_{REF} + 0.25$	$V_{TT} - 0.603$	$V_{TT} + 0.603$	6.7	-6.7
SSTL-18 Class II	-0.3	$V_{REF} - 0.125$	$V_{REF} + 0.125$	$V_{CCIO} + 0.3$	$V_{REF} - 0.25$	$V_{REF} + 0.25$	0.28	$V_{CCIO} - 0.28$	13.4	-13.4
SSTL-15 Class I	—	$V_{REF} - 0.1$	$V_{REF} + 0.1$	—	$V_{REF} - 0.175$	$V_{REF} + 0.175$	$0.2 * V_{CCIO}$	$0.8 * V_{CCIO}$	8	-8
SSTL-15 Class II	—	$V_{REF} - 0.1$	$V_{REF} + 0.1$	—	$V_{REF} - 0.175$	$V_{REF} + 0.175$	$0.2 * V_{CCIO}$	$0.8 * V_{CCIO}$	16	-16
SSTL-135 Class I, II	—	$V_{REF} - 0.09$	$V_{REF} + 0.09$	—	$V_{REF} - 0.16$	$V_{REF} + 0.16$	$0.2 * V_{CCIO}$	$0.8 * V_{CCIO}$	—	—
SSTL-125 Class I, II	—	$V_{REF} - 0.85$	$V_{REF} + 0.85$	—	$V_{REF} - 0.15$	$V_{REF} + 0.15$	$0.2 * V_{CCIO}$	$0.8 * V_{CCIO}$	—	—
SSTL-12 Class I, II	—	$V_{REF} - 0.1$	$V_{REF} + 0.1$	—	$V_{REF} - 0.15$	$V_{REF} + 0.15$	$0.2 * V_{CCIO}$	$0.8 * V_{CCIO}$	—	—

Table 21. Differential HSTL and HSUL I/O Standards for Stratix V Devices (Part 2 of 2)

I/O Standard	V_{CCIO} (V)			$V_{DIF(DC)}$ (V)		$V_{X(AC)}$ (V)			$V_{CM(DC)}$ (V)			$V_{DIF(AC)}$ (V)	
	Min	Typ	Max	Min	Max	Min	Typ	Max	Min	Typ	Max	Min	Max
HSTL-12 Class I, II	1.14	1.2	1.26	0.16	$V_{CCIO} + 0.3$	—	$0.5^* V_{CCIO}$	—	$0.4^* V_{CCIO}$	$0.5^* V_{CCIO}$	$0.6^* V_{CCIO}$	0.3	$V_{CCIO} + 0.48$
HSUL-12	1.14	1.2	1.3	0.26	0.26	$0.5^* V_{CCIO} - 0.12$	$0.5^* V_{CCIO}$	$0.5^* V_{CCIO} + 0.12$	$0.4^* V_{CCIO}$	$0.5^* V_{CCIO}$	$0.6^* V_{CCIO}$	0.44	0.44

Table 22. Differential I/O Standard Specifications for Stratix V Devices ⁽⁷⁾

I/O Standard	V_{CCIO} (V) ⁽¹⁰⁾			V_{ID} (mV) ⁽⁸⁾			$V_{ICM(DC)}$ (V)			V_{OD} (V) ⁽⁶⁾			V_{OCM} (V) ⁽⁶⁾		
	Min	Typ	Max	Min	Condition	Max	Min	Condition	Max	Min	Typ	Max	Min	Typ	Max
PCML	Transmitter, receiver, and input reference clock pins of the high-speed transceivers use the PCML I/O standard. For transmitter, receiver, and reference clock I/O pin specifications, refer to Table 23 on page 18.														
2.5 V LVDS ⁽¹⁾	2.375	2.5	2.625	100	$V_{CM} = 1.25$ V	—	0.05	$D_{MAX} \leq 700$ Mbps	1.8	0.247	—	0.6	1.125	1.25	1.375
						—	1.05	$D_{MAX} > 700$ Mbps	1.55	0.247	—	0.6	1.125	1.25	1.375
BLVDS ⁽⁵⁾	2.375	2.5	2.625	100	—	—	—	—	—	—	—	—	—	—	—
RSDS (HIO) ⁽²⁾	2.375	2.5	2.625	100	$V_{CM} = 1.25$ V	—	0.3	—	1.4	0.1	0.2	0.6	0.5	1.2	1.4
Mini-LVDS (HIO) ⁽³⁾	2.375	2.5	2.625	200	—	600	0.4	—	1.325	0.25	—	0.6	1	1.2	1.4
LVPECL ^{(4), (9)}	—	—	—	300	—	—	0.6	$D_{MAX} \leq 700$ Mbps	1.8	—	—	—	—	—	—
	—	—	—	300	—	—	1	$D_{MAX} > 700$ Mbps	1.6	—	—	—	—	—	—

Notes to Table 22:

- (1) For optimized LVDS receiver performance, the receiver voltage input range must be between 1.0 V to 1.6 V for data rates above 700 Mbps, and 0 V to 1.85 V for data rates below 700 Mbps.
- (2) For optimized RSDS receiver performance, the receiver voltage input range must be between 0.25 V to 1.45 V.
- (3) For optimized Mini-LVDS receiver performance, the receiver voltage input range must be between 0.3 V to 1.425 V.
- (4) For optimized LVPECL receiver performance, the receiver voltage input range must be between 0.85 V to 1.75 V for data rate above 700 Mbps and 0.45 V to 1.95 V for data rate below 700 Mbps.
- (5) There are no fixed V_{ICM} , V_{OD} , and V_{OCM} specifications for BLVDS. They depend on the system topology.
- (6) RL range: $90 \leq RL \leq 110 \Omega$.
- (7) The 1.4-V and 1.5-V PCML transceiver I/O standard specifications are described in "Transceiver Performance Specifications" on page 18.
- (8) The minimum VID value is applicable over the entire common mode range, VCM.
- (9) LVPECL is only supported on dedicated clock input pins.
- (10) Differential inputs are powered by VCCPD which requires 2.5 V.

Power Consumption

Altera offers two ways to estimate power consumption for a design—the Excel-based Early Power Estimator and the Quartus® II PowerPlay Power Analyzer feature.

Table 23. Transceiver Specifications for Stratix V GX and GS Devices ⁽¹⁾ (Part 5 of 7)

Symbol/ Description	Conditions	Transceiver Speed Grade 1			Transceiver Speed Grade 2			Transceiver Speed Grade 3			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Programmable DC gain	DC Gain Setting = 0	—	0	—	—	0	—	—	0	—	dB
	DC Gain Setting = 1	—	2	—	—	2	—	—	2	—	dB
	DC Gain Setting = 2	—	4	—	—	4	—	—	4	—	dB
	DC Gain Setting = 3	—	6	—	—	6	—	—	6	—	dB
	DC Gain Setting = 4	—	8	—	—	8	—	—	8	—	dB
Transmitter											
Supported I/O Standards	—	1.4-V and 1.5-V PCML									
Data rate (Standard PCS)	—	600	—	12200	600	—	12200	600	—	8500/ 10312.5 ⁽²⁴⁾	Mbps
Data rate (10G PCS)	—	600	—	14100	600	—	12500	600	—	8500/ 10312.5 ⁽²⁴⁾	Mbps
Differential on- chip termination resistors	85- Ω setting	—	85 \pm 20%	—	—	85 \pm 20%	—	—	85 \pm 20%	—	Ω
	100- Ω setting	—	100 \pm 20%	—	—	100 \pm 20%	—	—	100 \pm 20%	—	Ω
	120- Ω setting	—	120 \pm 20%	—	—	120 \pm 20%	—	—	120 \pm 20%	—	Ω
	150- Ω setting	—	150 \pm 20%	—	—	150 \pm 20%	—	—	150 \pm 20%	—	Ω
V _{OCM} (AC coupled)	0.65-V setting	—	650	—	—	650	—	—	650	—	mV
V _{OCM} (DC coupled)	—	—	650	—	—	650	—	—	650	—	mV
Rise time ⁽⁷⁾	20% to 80%	30	—	160	30	—	160	30	—	160	ps
Fall time ⁽⁷⁾	80% to 20%	30	—	160	30	—	160	30	—	160	ps
Intra-differential pair skew	Tx V _{CM} = 0.5 V and slew rate of 15 ps	—	—	15	—	—	15	—	—	15	ps
Intra-transceiver block transmitter channel-to- channel skew	x6 PMA bonded mode	—	—	120	—	—	120	—	—	120	ps

Table 23. Transceiver Specifications for Stratix V GX and GS Devices ⁽¹⁾ (Part 7 of 7)

Symbol/ Description	Conditions	Transceiver Speed Grade 1			Transceiver Speed Grade 2			Transceiver Speed Grade 3			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
$t_{pll_lock}^{(16)}$	—	—	—	10	—	—	10	—	—	10	μs

Notes to Table 23:

- (1) Speed grades shown in Table 23 refer to the PMA Speed Grade in the device ordering code. The maximum data rate could be restricted by the Core/PCS speed grade. Contact your Altera Sales Representative for the maximum data rate specifications in each speed grade combination offered. For more information about device ordering codes, refer to the *Stratix V Device Overview*.
- (2) The reference clock common mode voltage is equal to the V_{CCR_GXB} power supply level.
- (3) This supply must be connected to 1.0 V if the transceiver is configured at a data rate > 6.5 Gbps, and to 1.05 V if configured at a data rate > 10.3 Gbps when DFE is used. For data rates up to 6.5 Gbps, you can connect this supply to 0.85 V.
- (4) This supply follows $VCCR_GXB$.
- (5) The device cannot tolerate prolonged operation at this absolute maximum.
- (6) The differential eye opening specification at the receiver input pins assumes that **Receiver Equalization** is disabled. If you enable **Receiver Equalization**, the receiver circuitry can tolerate a lower minimum eye opening, depending on the equalization level.
- (7) The Quartus II software automatically selects the appropriate slew rate depending on the configured data rate or functional mode.
- (8) The input reference clock frequency options depend on the data rate and the device speed grade.
- (9) The line data rate may be limited by PCS-FPGA interface speed grade.
- (10) Refer to Figure 1 for the GX channel AC gain curves. The total effective AC gain is the AC gain minus the DC gain.
- (11) t_{LTR} is the time required for the receive CDR to lock to the input reference clock frequency after coming out of reset.
- (12) t_{LTD} is time required for the receiver CDR to start recovering valid data after the rx_is_lockedtodata signal goes high.
- (13) t_{LTD_manual} is the time required for the receiver CDR to start recovering valid data after the rx_is_lockedtodata signal goes high when the CDR is functioning in the manual mode.
- (14) $t_{LTR_LTD_manual}$ is the time the receiver CDR must be kept in lock to reference (LTR) mode after the rx_is_lockedtoref signal goes high when the CDR is functioning in the manual mode.
- (15) $t_{pll_powerdown}$ is the PLL powerdown minimum pulse width.
- (16) t_{pll_lock} is the time required for the transmitter CMU/ATX PLL to lock to the input reference clock frequency after coming out of reset.
- (17) To calculate the REFCLK rms phase jitter requirement for PCIe at reference clock frequencies other than 100 MHz, use the following formula: REFCLK rms phase jitter at f(MHz) = REFCLK rms phase jitter at 100 MHz \times 100/f.
- (18) The maximum peak to peak differential input voltage V_{ID} after device configuration is equal to $4 \times (\text{absolute } V_{MAX} \text{ for receiver pin} - V_{ICM})$.
- (19) For ES devices, R_{REF} is $2000 \Omega \pm 1\%$.
- (20) To calculate the REFCLK phase noise requirement at frequencies other than 622 MHz, use the following formula: REFCLK phase noise at f(MHz) = REFCLK phase noise at 622 MHz + $20 \times \log(f/622)$.
- (21) SFP/+ optical modules require the host interface to have RD+/- differentially terminated with 100Ω . The internal OCT feature is available after the Stratix V FPGA configuration is completed. Altera recommends that FPGA configuration is completed before inserting the optical module. Otherwise, minimize unnecessary removal and insertion with unconfigured devices.
- (22) Refer to Figure 2.
- (23) For oversampling designs to support data rates less than the minimum specification, the CDR needs to be in LTR mode only.
- (24) I3YY devices can achieve data rates up to 10.3125 Gbps.
- (25) When you use fPLL as a TXPLL of the transceiver.
- (26) REFCLK performance requires to meet transmitter REFCLK phase noise specification.
- (27) Minimum eye opening of 85 mV is only for the unstressed input eye condition.

Figure 2 shows the differential transmitter output waveform.

Figure 2. Differential Transmitter Output Waveform

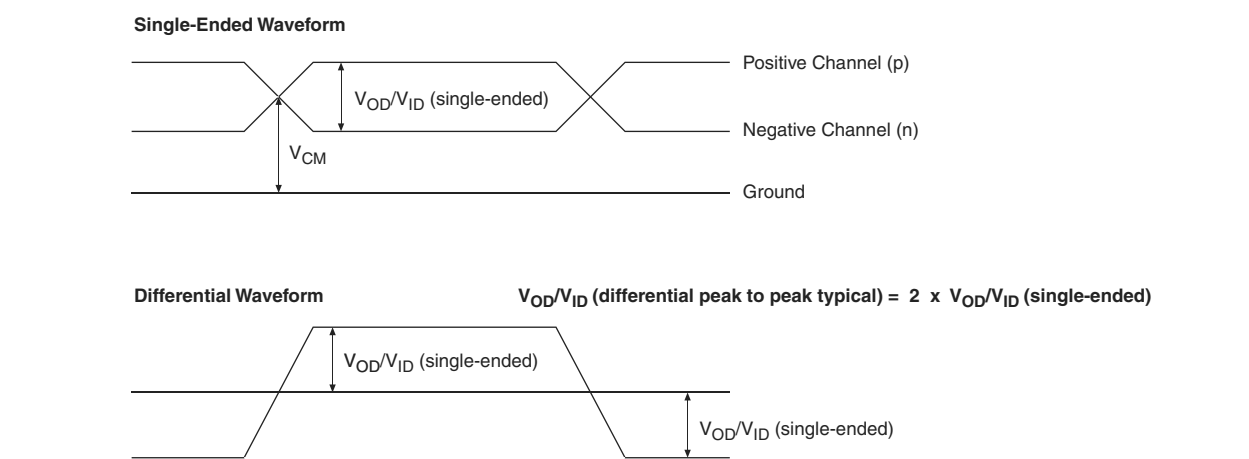


Figure 3 shows the Stratix V AC gain curves for GX channels.

Figure 3. AC Gain Curves for GX Channels (full bandwidth)



Stratix V GT devices contain both GX and GT channels. All transceiver specifications for the GX channels not listed in Table 28 are the same as those listed in Table 23.

Table 28 lists the Stratix V GT transceiver specifications.

Table 28. Transceiver Specifications for Stratix V GT Devices (Part 1 of 5) ⁽¹⁾

Symbol/ Description	Conditions	Transceiver Speed Grade 2			Transceiver Speed Grade 3			Unit
		Min	Typ	Max	Min	Typ	Max	
Reference Clock								
Supported I/O Standards	Dedicated reference clock pin	1.2-V PCML, 1.4-V PCML, 1.5-V PCML, 2.5-V PCML, Differential LVPECL, LVDS, and HCSL						
	RX reference clock pin	1.4-V PCML, 1.5-V PCML, 2.5-V PCML, LVPECL, and LVDS						
Input Reference Clock Frequency (CMU PLL) ⁽⁶⁾	—	40	—	710	40	—	710	MHz
Input Reference Clock Frequency (ATX PLL) ⁽⁶⁾	—	100	—	710	100	—	710	MHz
Rise time	20% to 80%	—	—	400	—	—	400	ps
Fall time	80% to 20%	—	—	400	—	—	400	
Duty cycle	—	45	—	55	45	—	55	%
Spread-spectrum modulating clock frequency	PCI Express (PCIe)	30	—	33	30	—	33	kHz
Spread-spectrum downspread	PCIe	—	0 to −0.5	—	—	0 to −0.5	—	%
On-chip termination resistors ⁽¹⁹⁾	—	—	100	—	—	100	—	Ω
Absolute V _{MAX} ⁽³⁾	Dedicated reference clock pin	—	—	1.6	—	—	1.6	V
	RX reference clock pin	—	—	1.2	—	—	1.2	
Absolute V _{MIN}	—	-0.4	—	—	-0.4	—	—	V
Peak-to-peak differential input voltage	—	200	—	1600	200	—	1600	mV
V _{ICM} (AC coupled)	Dedicated reference clock pin	1050/1000 ⁽²⁾			1050/1000 ⁽²⁾			mV
	RX reference clock pin	1.0/0.9/0.85 ⁽²²⁾			1.0/0.9/0.85 ⁽²²⁾			V
V _{ICM} (DC coupled)	HCSL I/O standard for PCIe reference clock	250	—	550	250	—	550	mV

Table 28. Transceiver Specifications for Stratix V GT Devices (Part 4 of 5) ⁽¹⁾

Symbol/ Description	Conditions	Transceiver Speed Grade 2			Transceiver Speed Grade 3			Unit
		Min	Typ	Max	Min	Typ	Max	
Data rate	GT channels	19,600	—	28,050	19,600	—	25,780	Mbps
Differential on-chip termination resistors	GT channels	—	100	—	—	100	—	Ω
	GX channels	(8)						
V _{OCM} (AC coupled)	GT channels	—	500	—	—	500	—	mV
	GX channels	(8)						
Rise/Fall time	GT channels	—	15	—	—	15	—	ps
	GX channels	(8)						
Intra-differential pair skew	GX channels	(8)						
Intra-transceiver block transmitter channel-to- channel skew	GX channels	(8)						
Inter-transceiver block transmitter channel-to- channel skew	GX channels	(8)						
CMU PLL								
Supported Data Range	—	600	—	12500	600	—	8500	Mbps
t _{pll_powerdown} ⁽¹³⁾	—	1	—	—	1	—	—	μs
t _{pll_lock} ⁽¹⁴⁾	—	—	—	10	—	—	10	μs
ATX PLL								
Supported Data Rate Range for GX Channels	VCO post- divider L=2	8000	—	12500	8000	—	8500	Mbps
	L=4	4000	—	6600	4000	—	6600	Mbps
	L=8	2000	—	3300	2000	—	3300	Mbps
	L=8, Local/Central Clock Divider =2	1000	—	1762.5	1000	—	1762.5	Mbps
Supported Data Rate Range for GT Channels	VCO post- divider L=2	9800	—	14025	9800	—	12890	Mbps
t _{pll_powerdown} ⁽¹³⁾	—	1	—	—	1	—	—	μs
t _{pll_lock} ⁽¹⁴⁾	—	—	—	10	—	—	10	μs
fPLL								
Supported Data Range	—	600	—	3250/ 3.125 ⁽²³⁾	600	—	3250/ 3.125 ⁽²³⁾	Mbps
t _{pll_powerdown} ⁽¹³⁾	—	1	—	—	1	—	—	μs

Table 28. Transceiver Specifications for Stratix V GT Devices (Part 5 of 5) ⁽¹⁾

Symbol/ Description	Conditions	Transceiver Speed Grade 2			Transceiver Speed Grade 3			Unit
		Min	Typ	Max	Min	Typ	Max	
t_{pll_lock} ⁽¹⁴⁾	—	—	—	10	—	—	10	μs

Notes to Table 28:

- (1) Speed grades shown refer to the PMA Speed Grade in the device ordering code. The maximum data rate could be restricted by the Core/PCS speed grade. Contact your Altera Sales Representative for the maximum data rate specifications in each speed grade combination offered. For more information about device ordering codes, refer to the *Stratix V Device Overview*.
- (2) The reference clock common mode voltage is equal to the VCCR_GXB power supply level.
- (3) The device cannot tolerate prolonged operation at this absolute maximum.
- (4) The differential eye opening specification at the receiver input pins assumes that receiver equalization is disabled. If you enable receiver equalization, the receiver circuitry can tolerate a lower minimum eye opening, depending on the equalization level.
- (5) Refer to Figure 5 for the GT channel AC gain curves. The total effective AC gain is the AC gain minus the DC gain.
- (6) Refer to Figure 6 for the GT channel DC gain curves.
- (7) CFP2 optical modules require the host interface to have the receiver data pins differentially terminated with 100 Ω. The internal OCT feature is available after the Stratix V FPGA configuration is completed. Altera recommends that FPGA configuration is completed before inserting the optical module. Otherwise, minimize unnecessary removal and insertion with unconfigured devices.
- (8) Specifications for this parameter are the same as for Stratix V GX and GS devices. See Table 23 for specifications.
- (9) t_{LTR} is the time required for the receive CDR to lock to the input reference clock frequency after coming out of reset.
- (10) t_{LTD} is time required for the receiver CDR to start recovering valid data after the $rx_is_lockedto\ data$ signal goes high.
- (11) t_{LTD_manual} is the time required for the receiver CDR to start recovering valid data after the $rx_is_lockedto\ data$ signal goes high when the CDR is functioning in the manual mode.
- (12) $t_{LTR_LTD_manual}$ is the time the receiver CDR must be kept in lock to reference (LTR) mode after the $rx_is_lockedto\ ref$ signal goes high when the CDR is functioning in the manual mode.
- (13) $tp11_powerdown$ is the PLL powerdown minimum pulse width.
- (14) $tp11_lock$ is the time required for the transmitter CMU/ATX PLL to lock to the input reference clock frequency after coming out of reset.
- (15) To calculate the REFCLK rms phase jitter requirement for PCIe at reference clock frequencies other than 100 MHz, use the following formula:
REFCLK rms phase jitter at f(MHz) = REFCLK rms phase jitter at 100 MHz × 100/f.
- (16) The maximum peak to peak differential input voltage V_{ID} after device configuration is equal to $4 \times (\text{absolute } V_{MAX} \text{ for receiver pin} - V_{ICM})$.
- (17) For ES devices, RREF is 2000 Ω ±1%.
- (18) To calculate the REFCLK phase noise requirement at frequencies other than 622 MHz, use the following formula: REFCLK phase noise at f(MHz) = REFCLK phase noise at 622 MHz + 20*log(f/622).
- (19) SFP/+ optical modules require the host interface to have RD+/- differentially terminated with 100 Ω. The internal OCT feature is available after the Stratix V FPGA configuration is completed. Altera recommends that FPGA configuration is completed before inserting the optical module. Otherwise, minimize unnecessary removal and insertion with unconfigured devices.
- (20) Refer to Figure 4.
- (21) For oversampling design to support data rates less than the minimum specification, the CDR needs to be in LTR mode only.
- (22) This supply follows VCCR_GXB for both GX and GT channels.
- (23) When you use fPLL as a TXPLL of the transceiver.

Figure 4 shows the differential transmitter output waveform.

Figure 4. Differential Transmitter/Receiver Output/Input Waveform



Figure 5 shows the Stratix V AC gain curves for GT channels.

Figure 5. AC Gain Curves for GT Channels

Figure 6 shows the Stratix V DC gain curves for GT channels.

Figure 6. DC Gain Curves for GT Channels

Transceiver Characterization

This section summarizes the Stratix V transceiver characterization results for compliance with the following protocols:

- Interlaken
- 40G (XLAUI)/100G (CAUI)
- 10GBase-KR
- QSGMII
- XAUI
- SFI
- Gigabit Ethernet (Gbe / GIGE)
- SPAUI
- Serial Rapid IO (SRIO)
- CPRI
- OBSAI
- Hyper Transport (HT)
- SATA
- SAS
- CEI

Table 31. PLL Specifications for Stratix V Devices (Part 3 of 3)

Symbol	Parameter	Min	Typ	Max	Unit
f_{RES}	Resolution of VCO frequency ($f_{INPFD} = 100$ MHz)	390625	5.96	0.023	Hz

Notes to Table 31:

- (1) This specification is limited in the Quartus II software by the I/O maximum frequency. The maximum I/O frequency is different for each I/O standard.
- (2) This specification is limited by the lower of the two: I/O f_{MAX} or f_{OUT} of the PLL.
- (3) A high input jitter directly affects the PLL output jitter. To have low PLL output clock jitter, you must provide a clean clock source < 120 ps.
- (4) f_{REF} is f_{IN}/N when $N = 1$.
- (5) Peak-to-peak jitter with a probability level of 10^{-12} (14 sigma, 99.9999999974404% confidence level). The output jitter specification applies to the intrinsic jitter of the PLL, when an input jitter of 30 ps is applied. The external memory interface clock output jitter specifications use a different measurement method and are available in Table 44 on page 52.
- (6) The cascaded PLL specification is only applicable with the following condition:
 - a. Upstream PLL: $0.59\text{MHz} \leq \text{Upstream PLL BW} < 1$ MHz
 - b. Downstream PLL: Downstream PLL BW > 2 MHz
- (7) High bandwidth PLL settings are not supported in external feedback mode.
- (8) The external memory interface clock output jitter specifications use a different measurement method, which is available in Table 42 on page 50.
- (9) The VCO frequency reported by the Quartus II software in the PLL Usage Summary section of the compilation report takes into consideration the VCO post-scale counter K value. Therefore, if the counter K has a value of 2, the frequency reported can be lower than the f_{VCO} specification.
- (10) This specification only covers fractional PLL for low bandwidth. The f_{VCO} for fractional value range 0.05 - 0.95 must be ≥ 1000 MHz, while f_{VCO} for fractional value range 0.20 - 0.80 must be ≥ 1200 MHz.
- (11) This specification only covered fractional PLL for low bandwidth. The f_{VCO} for fractional value range 0.05-0.95 must be ≥ 1000 MHz.
- (12) This specification only covered fractional PLL for low bandwidth. The f_{VCO} for fractional value range 0.20-0.80 must be ≥ 1200 MHz.

DSP Block Specifications

Table 32 lists the Stratix V DSP block performance specifications.

Table 32. Block Performance Specifications for Stratix V DSP Devices (Part 1 of 2)

Mode	Peformance							Unit
	C1	C2, C2L	I2, I2L	C3	I3, I3L, I3YY	C4	I4	
Modes using one DSP								
Three 9 x 9	600	600	600	480	480	420	420	MHz
One 18 x 18	600	600	600	480	480	420	400	MHz
Two partial 18 x 18 (or 16 x 16)	600	600	600	480	480	420	400	MHz
One 27 x 27	500	500	500	400	400	350	350	MHz
One 36 x 18	500	500	500	400	400	350	350	MHz
One sum of two 18 x 18(One sum of 2 16 x 16)	500	500	500	400	400	350	350	MHz
One sum of square	500	500	500	400	400	350	350	MHz
One 18 x 18 plus 36 (a x b) + c	500	500	500	400	400	350	350	MHz
Modes using two DSPs								
Three 18 x 18	500	500	500	400	400	350	350	MHz
One sum of four 18 x 18	475	475	475	380	380	300	300	MHz
One sum of two 27 x 27	465	465	450	380	380	300	290	MHz
One sum of two 36 x 18	475	475	475	380	380	300	300	MHz
One complex 18 x 18	500	500	500	400	400	350	350	MHz
One 36 x 36	475	475	475	380	380	300	300	MHz

Periphery Performance

This section describes periphery performance, including high-speed I/O and external memory interface.

I/O performance supports several system interfaces, such as the **LVDS** high-speed I/O interface, external memory interface, and the **PCI/PCI-X** bus interface.

General-purpose I/O standards such as 3.3-, 2.5-, 1.8-, and 1.5-**LVTTL/LVCMOS** are capable of a typical 167 MHz and 1.2-**LVCMOS** at 100 MHz interfacing frequency with a 10 pF load.



The actual achievable frequency depends on design- and system-specific factors. Ensure proper timing closure in your design and perform HSPICE/IBIS simulations based on your specific design and system setup to determine the maximum achievable frequency in your system.

High-Speed I/O Specification

Table 36 lists high-speed I/O timing for Stratix V devices.

Table 36. High-Speed I/O Specifications for Stratix V Devices ⁽¹⁾, ⁽²⁾ (Part 1 of 4)

Symbol	Conditions	C1			C2, C2L, I2, I2L			C3, I3, I3L, I3YY			C4,I4			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
$f_{\text{HCLK_in}}$ (input clock frequency) True Differential I/O Standards	Clock boost factor $W = 1$ to 40 ⁽⁴⁾	5	—	800	5	—	800	5	—	625	5	—	525	MHz
$f_{\text{HCLK_in}}$ (input clock frequency) Single Ended I/O Standards ⁽³⁾	Clock boost factor $W = 1$ to 40 ⁽⁴⁾	5	—	800	5	—	800	5	—	625	5	—	525	MHz
$f_{\text{HCLK_in}}$ (input clock frequency) Single Ended I/O Standards	Clock boost factor $W = 1$ to 40 ⁽⁴⁾	5	—	520	5	—	520	5	—	420	5	—	420	MHz
$f_{\text{HCLK_OUT}}$ (output clock frequency)	—	5	—	800	5	—	800	5	—	625 ⁽⁵⁾	5	—	525 ⁽⁵⁾	MHz

Table 36. High-Speed I/O Specifications for Stratix V Devices ^{(1), (2)} (Part 2 of 4)

Symbol	Conditions	C1			C2, C2L, I2, I2L			C3, I3, I3L, I3YY			C4,I4			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Transmitter														
True Differential I/O Standards - f _{HSDR} (data rate)	SERDES factor J = 3 to 10 ^{(9), (11), (12), (13), (14), (15), (16)}	(6)	—	1600	(6)	—	1434	(6)	—	1250	(6)	—	1050	Mbps
	SERDES factor J ≥ 4 LVDS TX with DPA ^{(12), (14), (15), (16)}	(6)	—	1600	(6)	—	1600	(6)	—	1600	(6)	—	1250	Mbps
	SERDES factor J = 2, uses DDR Registers	(6)	—	(7)	(6)	—	(7)	(6)	—	(7)	(6)	—	(7)	Mbps
	SERDES factor J = 1, uses SDR Register	(6)	—	(7)	(6)	—	(7)	(6)	—	(7)	(6)	—	(7)	Mbps
Emulated Differential I/O Standards with Three External Output Resistor Networks - f _{HSDR} (data rate) ⁽¹⁰⁾	SERDES factor J = 4 to 10 ⁽¹⁷⁾	(6)	—	1100	(6)	—	1100	(6)	—	840	(6)	—	840	Mbps
t _{x Jitter} - True Differential I/O Standards	Total Jitter for Data Rate 600 Mbps - 1.25 Gbps	—	—	160	—	—	160	—	—	160	—	—	160	ps
	Total Jitter for Data Rate < 600 Mbps	—	—	0.1	—	—	0.1	—	—	0.1	—	—	0.1	UI
t _{x Jitter} - Emulated Differential I/O Standards with Three External Output Resistor Network	Total Jitter for Data Rate 600 Mbps - 1.25 Gbps	—	—	300	—	—	300	—	—	300	—	—	325	ps
	Total Jitter for Data Rate < 600 Mbps	—	—	0.2	—	—	0.2	—	—	0.2	—	—	0.25	UI

Table 54 lists the PS configuration timing parameters for Stratix V devices.

Table 54. PS Timing Parameters for Stratix V Devices

Symbol	Parameter	Minimum	Maximum	Units
t_{CF2CD}	nCONFIG low to CONF_DONE low	—	600	ns
t_{CF2ST0}	nCONFIG low to nSTATUS low	—	600	ns
t_{CFG}	nCONFIG low pulse width	2	—	μ s
t_{STATUS}	nSTATUS low pulse width	268	1,506 ⁽¹⁾	μ s
t_{CF2ST1}	nCONFIG high to nSTATUS high	—	1,506 ⁽²⁾	μ s
t_{CF2CK} ⁽⁵⁾	nCONFIG high to first rising edge on DCLK	1,506	—	μ s
t_{ST2CK} ⁽⁵⁾	nSTATUS high to first rising edge of DCLK	2	—	μ s
t_{DSU}	DATA [] setup time before rising edge on DCLK	5.5	—	ns
t_{DH}	DATA [] hold time after rising edge on DCLK	0	—	ns
t_{CH}	DCLK high time	$0.45 \times 1/f_{MAX}$	—	s
t_{CL}	DCLK low time	$0.45 \times 1/f_{MAX}$	—	s
t_{CLK}	DCLK period	$1/f_{MAX}$	—	s
f_{MAX}	DCLK frequency	—	125	MHz
t_{CD2UM}	CONF_DONE high to user mode ⁽³⁾	175	437	μ s
t_{CD2CU}	CONF_DONE high to CLKUSR enabled	4 × maximum DCLK period	—	—
t_{CD2UMC}	CONF_DONE high to user mode with CLKUSR option on	$t_{CD2CU} + (8576 \times \text{CLKUSR period})$ ⁽⁴⁾	—	—

Notes to Table 54:

- (1) This value is applicable if you do not delay configuration by extending the nCONFIG or nSTATUS low pulse width.
- (2) This value is applicable if you do not delay configuration by externally holding the nSTATUS low.
- (3) The minimum and maximum numbers apply only if you choose the internal oscillator as the clock source for initializing the device.
- (4) To enable the CLKUSR pin as the initialization clock source and to obtain the maximum frequency specification on these pins, refer to the “Initialization” section.
- (5) If nSTATUS is monitored, follow the t_{ST2CK} specification. If nSTATUS is not monitored, follow the t_{CF2CK} specification.

Initialization

Table 55 lists the initialization clock source option, the applicable configuration schemes, and the maximum frequency.

Table 55. Initialization Clock Source Option and the Maximum Frequency

Initialization Clock Source	Configuration Schemes	Maximum Frequency	Minimum Number of Clock Cycles ⁽¹⁾
Internal Oscillator	AS, PS, FPP	12.5 MHz	8576
CLKUSR	AS, PS, FPP ⁽²⁾	125 MHz	
DCLK	PS, FPP	125 MHz	

Notes to Table 55:

- (1) The minimum number of clock cycles required for device initialization.
- (2) To enable CLKUSR as the initialization clock source, turn on the **Enable user-supplied start-up clock (CLKUSR)** option in the Quartus II software from the **General** panel of the **Device and Pin Options** dialog box.

Document Revision History

Table 61 lists the revision history for this chapter.

Table 61. Document Revision History (Part 1 of 3)

Date	Version	Changes
June 2018	3.9	<ul style="list-style-type: none"> Added the “Stratix V Device Overshoot Duration” figure.
April 2017	3.8	<ul style="list-style-type: none"> Added a footnote to the “High-Speed I/O Specifications for Stratix V Devices” table. Changed the minimum value for t_{CD2UMC} in the “PS Timing Parameters for Stratix V Devices” table. Changed the condition for $100\text{-}\Omega$ R_D in the “OCT Without Calibration Resistance Tolerance Specifications for Stratix V Devices” table. Changed the minimum value for t_{CD2UMC} in the “AS Timing Parameters for AS ‘1 and AS ‘4 Configurations in Stratix V Devices” table Changed the minimum value for t_{CD2UMC} in the “FPP Timing Parameters for Stratix V Devices When the DCLK-to-DATA[] Ratio is >1” table. Changed the minimum value for t_{CD2UMC} in the “FPP Timing Parameters for Stratix V Devices When the DCLK-to-DATA[] Ratio is >1” table. Changed the minimum number of clock cycles value in the “Initialization Clock Source Option and the Maximum Frequency” table.
June 2016	3.7	<ul style="list-style-type: none"> Added the V_{ID} minimum specification for LVPECL in the “Differential I/O Standard Specifications for Stratix V Devices” table Added the I_{OUT} specification to the “Absolute Maximum Ratings for Stratix V Devices” table.
December 2015	3.6	<ul style="list-style-type: none"> Added a footnote to the “High-Speed I/O Specifications for Stratix V Devices” table.
December 2015	3.5	<ul style="list-style-type: none"> Changed the transmitter, receiver, and ATX PLL data rate specifications in the “Transceiver Specifications for Stratix V GX and GS Devices” table. Changed the configuration .rbf sizes in the “Uncompressed .rbf Sizes for Stratix V Devices” table.
July 2015	3.4	<ul style="list-style-type: none"> Changed the data rate specification for transceiver speed grade 3 in the following tables: <ul style="list-style-type: none"> “Transceiver Specifications for Stratix V GX and GS Devices” “Stratix V Standard PCS Approximate Maximum Date Rate” “Stratix V 10G PCS Approximate Maximum Data Rate” Changed the conditions for reference clock rise and fall time, and added a note to the “Transceiver Specifications for Stratix V GX and GS Devices” table. Added a note to the “Minimum differential eye opening at receiver serial input pins” specification in the “Transceiver Specifications for Stratix V GX and GS Devices” table. Changed the t_{CO} maximum value in the “AS Timing Parameters for AS ‘1 and AS ‘4 Configurations in Stratix V Devices” table. Removed the CDR ppm tolerance specification from the “Transceiver Specifications for Stratix V GX and GS Devices” table.

Table 61. Document Revision History (Part 2 of 3)

Date	Version	Changes
November 2014	3.3	<ul style="list-style-type: none"> ■ Added the I3YY speed grade and changed the data rates for the GX channel in Table 1. ■ Added the I3YY speed grade to the V_{CC} description in Table 6. ■ Added the I3YY speed grade to V_{CCHIP_L}, V_{CCHIP_R}, V_{CCHSSI_L}, and V_{CCHSSI_R} descriptions in Table 7. ■ Added 240-Ω to Table 11. ■ Changed CDR PPM tolerance in Table 23. ■ Added additional max data rate for fPLL in Table 23. ■ Added the I3YY speed grade and changed the data rates for transceiver speed grade 3 in Table 25. ■ Added the I3YY speed grade and changed the data rates for transceiver speed grade 3 in Table 26. ■ Changed CDR PPM tolerance in Table 28. ■ Added additional max data rate for fPLL in Table 28. ■ Changed the mode descriptions for MLAB and M20K in Table 33. ■ Changed the Max value of f_{HCLK_OUT} for the C2, C2L, I2, I2L speed grades in Table 36. ■ Changed the frequency ranges for C1 and C2 in Table 39. ■ Changed the .rbf file sizes for 5SGSD6 and 5SGSD8 in Table 47. ■ Added note about nSTATUS to Table 50, Table 51, Table 54. ■ Changed the available settings in Table 58. ■ Changed the note in “Periphery Performance”. ■ Updated the “I/O Standard Specifications” section. ■ Updated the “Raw Binary File Size” section. ■ Updated the receiver voltage input range in Table 22. ■ Updated the max frequency for the LVDS clock network in Table 36. ■ Updated the DCLK note to Figure 11. ■ Updated Table 23 VO_{CM} (DC Coupled) condition. ■ Updated Table 6 and Table 7. ■ Added the DCLK specification to Table 55. ■ Updated the notes for Table 47. ■ Updated the list of parameters for Table 56.
November 2013	3.2	■ Updated Table 28
November 2013	3.1	■ Updated Table 33
November 2013	3.0	■ Updated Table 23 and Table 28
October 2013	2.9	■ Updated the “Transceiver Characterization” section
October 2013	2.8	<ul style="list-style-type: none"> ■ Updated Table 3, Table 12, Table 14, Table 19, Table 20, Table 23, Table 24, Table 28, Table 30, Table 31, Table 32, Table 33, Table 36, Table 39, Table 40, Table 41, Table 42, Table 47, Table 53, Table 58, and Table 59 ■ Added Figure 1 and Figure 3 ■ Added the “Transceiver Characterization” section ■ Removed all “Preliminary” designations.