# Intel - 5SGXEB6R3F43C4 Datasheet

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## Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

## Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications,

| **Details** | |
|---|---|
| Product Status | Obsolete |
| Number of LABs/CLBs | 225400 |
| Number of Logic Elements/Cells | 597000 |
| Total RAM Bits | 53248000 |
| Number of I/O | 600 |
| Number of Gates | - |
| Voltage - Supply | 0.82V ~ 0.88V |
| Mounting Type | Surface Mount |
| Operating Temperature | 0°C ~ 85°C (TJ) |
| Package / Case | 1760-BBGA, FCBGA |
| Supplier Device Package | 1760-FCBGA (42.5x42.5) |
| Purchase URL | https://www.e-xfl.com/product-detail/intel/5sgxeb6r3f43c4 |

## Recommended Operating Conditions

This section lists the functional operating limits for the AC and DC parameters for Stratix V devices. Table 6 lists the steady-state voltage and current values expected from Stratix V devices. Power supply ramps must all be strictly monotonic, without plateaus.

**Table 6. Recommended Operating Conditions for Stratix V Devices (Part 1 of 2)**

| Symbol | Description | Condition | Min (4) | Typ | Max (4) | Unit |
|---|---|---|---|---|---|---|
| $V_{CC}$ | Core voltage and periphery circuitry power supply (C1, C2, I2, and I3YY speed grades) | — | 0.87 | 0.9 | 0.93 | V |
| | Core voltage and periphery circuitry power supply (C2L, C3, C4, I2L, I3, I3L, and I4 speed grades) (3) | — | 0.82 | 0.85 | 0.88 | V |
| $V_{CCPT}$ | Power supply for programmable power technology | — | 1.45 | 1.50 | 1.55 | V |
| $V_{CC\_AUX}$ | Auxiliary supply for the programmable power technology | — | 2.375 | 2.5 | 2.625 | V |
| $V_{CCPD}$ (1) | I/O pre-driver (3.0 V) power supply | — | 2.85 | 3.0 | 3.15 | V |
| | I/O pre-driver (2.5 V) power supply | — | 2.375 | 2.5 | 2.625 | V |
| $V_{CCIO}$ | I/O buffers (3.0 V) power supply | — | 2.85 | 3.0 | 3.15 | V |
| | I/O buffers (2.5 V) power supply | — | 2.375 | 2.5 | 2.625 | V |
| | I/O buffers (1.8 V) power supply | — | 1.71 | 1.8 | 1.89 | V |
| | I/O buffers (1.5 V) power supply | — | 1.425 | 1.5 | 1.575 | V |
| | I/O buffers (1.35 V) power supply | — | 1.283 | 1.35 | 1.45 | V |
| | I/O buffers (1.25 V) power supply | — | 1.19 | 1.25 | 1.31 | V |
| | I/O buffers (1.2 V) power supply | — | 1.14 | 1.2 | 1.26 | V |
| $V_{CCPGM}$ | Configuration pins (3.0 V) power supply | — | 2.85 | 3.0 | 3.15 | V |
| | Configuration pins (2.5 V) power supply | — | 2.375 | 2.5 | 2.625 | V |
| | Configuration pins (1.8 V) power supply | — | 1.71 | 1.8 | 1.89 | V |
| $V_{CCA\_FPLL}$ | PLL analog voltage regulator power supply | — | 2.375 | 2.5 | 2.625 | V |
| $V_{CCD\_FPLL}$ | PLL digital voltage regulator power supply | — | 1.45 | 1.5 | 1.55 | V |
| $V_{CCBAT}$ (2) | Battery back-up power supply (For design security volatile key register) | — | 1.2 | — | 3.0 | V |
| $V_I$ | DC input voltage | — | –0.5 | — | 3.6 | V |
| $V_O$ | Output voltage | — | 0 | — | $V_{CCIO}$ | V |
| $T_J$ | Operating junction temperature | Commercial | 0 | — | 85 | °C |
| | | Industrial | –40 | — | 100 | °C |

Table 8 shows the transceiver power supply voltage requirements for various conditions.

**Table 8. Transceiver Power Supply Voltage Requirements**

| Conditions | Core Speed Grade | VCCR_GXB & VCCT_GXB (2) | VCCA_GXB | VCCH_GXB | Unit |
|---|---|---|---|---|---|
| If BOTH of the following conditions are true:<br>■ Data rate > 10.3 Gbps.<br>■ DFE is used. | All | 1.05 | 3.0 | 1.5 | V |
| If ANY of the following conditions are true (1):<br>■ ATX PLL is used.<br>■ Data rate > 6.5Gbps.<br>■ DFE (data rate ≤ 10.3 Gbps), AEQ, or EyeQ feature is used. | All | 1.0 | | | |
| If ALL of the following conditions are true:<br>■ ATX PLL is not used.<br>■ Data rate ≤ 6.5Gbps.<br>■ DFE, AEQ, and EyeQ are not used. | C1, C2, I2, and I3YY | 0.90 | 2.5 | | |
| | C2L, C3, C4, I2L, I3, I3L, and I4 | 0.85 | 2.5 | | |

**Notes to Table 8:**

(1) Choose this power supply voltage requirement option if you plan to upgrade your design later with any of the listed conditions.

(2) If the VCCR_GXB and VCCT_GXB supplies are set to 1.0 V or 1.05 V, they cannot be shared with the VCC core supply. If the VCCR_GXB and VCCT_GXB are set to either 0.90 V or 0.85 V, they can be shared with the VCC core supply.

## DC Characteristics

This section lists the supply current, I/O pin leakage current, input pin capacitance, on-chip termination tolerance, and hot socketing specifications.

### Supply Current

Supply current is the current drawn from the respective power rails used for power budgeting. Use the Excel-based Early Power Estimator (EPE) to get supply current estimates for your design because these currents vary greatly with the resources you use.

For more information about power estimation tools, refer to the *PowerPlay Early Power Estimator User Guide* and the *PowerPlay Power Analysis* chapter in the *Quartus II Handbook*.

**Table 18. Single-Ended SSTL, HSTL, and HSUL I/O Reference Voltage Specifications for Stratix V Devices**

| I/O Standard | $V_{CCIO}$ (V) | | | $V_{REF}$ (V) | | | $V_{TT}$ (V) | | |
|---|---|---|---|---|---|---|---|---|---|
| | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max |
| SSTL-2 Class I, II | 2.375 | 2.5 | 2.625 | 0.49 * $V_{CCIO}$ | 0.5 * $V_{CCIO}$ | 0.51 * $V_{CCIO}$ | $V_{REF}$ – 0.04 | $V_{REF}$ | $V_{REF}$ + 0.04 |
| SSTL-18 Class I, II | 1.71 | 1.8 | 1.89 | 0.833 | 0.9 | 0.969 | $V_{REF}$ – 0.04 | $V_{REF}$ | $V_{REF}$ + 0.04 |
| SSTL-15 Class I, II | 1.425 | 1.5 | 1.575 | 0.49 * $V_{CCIO}$ | 0.5 * $V_{CCIO}$ | 0.51 * $V_{CCIO}$ | 0.49 * $V_{CCIO}$ | 0.5 * VCCIO | 0.51 * $V_{CCIO}$ |
| SSTL-135 Class I, II | 1.283 | 1.35 | 1.418 | 0.49 * $V_{CCIO}$ | 0.5 * $V_{CCIO}$ | 0.51 * $V_{CCIO}$ | 0.49 * $V_{CCIO}$ | 0.5 * $V_{CCIO}$ | 0.51 * $V_{CCIO}$ |
| SSTL-125 Class I, II | 1.19 | 1.25 | 1.26 | 0.49 * $V_{CCIO}$ | 0.5 * $V_{CCIO}$ | 0.51 * $V_{CCIO}$ | 0.49 * $V_{CCIO}$ | 0.5 * VCCIO | 0.51 * $V_{CCIO}$ |
| SSTL-12 Class I, II | 1.14 | 1.20 | 1.26 | 0.49 * $V_{CCIO}$ | 0.5 * $V_{CCIO}$ | 0.51 * $V_{CCIO}$ | 0.49 * $V_{CCIO}$ | 0.5 * VCCIO | 0.51 * $V_{CCIO}$ |
| HSTL-18 Class I, II | 1.71 | 1.8 | 1.89 | 0.85 | 0.9 | 0.95 | — | $V_{CCIO}$/2 | — |
| HSTL-15 Class I, II | 1.425 | 1.5 | 1.575 | 0.68 | 0.75 | 0.9 | — | $V_{CCIO}$/2 | — |
| HSTL-12 Class I, II | 1.14 | 1.2 | 1.26 | 0.47 * $V_{CCIO}$ | 0.5 * $V_{CCIO}$ | 0.53 * $V_{CCIO}$ | — | $V_{CCIO}$/2 | — |
| HSUL-12 | 1.14 | 1.2 | 1.3 | 0.49 * $V_{CCIO}$ | 0.5 * $V_{CCIO}$ | 0.51 * $V_{CCIO}$ | — | — | — |

**Table 19. Single-Ended SSTL, HSTL, and HSUL I/O Standards Signal Specifications for Stratix V Devices (Part 1 of 2)**

| I/O Standard | $V_{IL(DC)}$ (V) | | $V_{IH(DC)}$ (V) | | $V_{IL(AC)}$ (V) | $V_{IH(AC)}$ (V) | $V_{OL}$ (V) | $V_{OH}$ (V) | $I_{ol}$ (mA) | $I_{oh}$ (mA) |
|---|---|---|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Max | Min | Max | Min | | |
| SSTL-2 Class I | –0.3 | $V_{REF}$ – 0.15 | $V_{REF}$ + 0.15 | $V_{CCIO}$ + 0.3 | $V_{REF}$ – 0.31 | $V_{REF}$ + 0.31 | $V_{TT}$ – 0.608 | $V_{TT}$ + 0.608 | 8.1 | –8.1 |
| SSTL-2 Class II | –0.3 | $V_{REF}$ – 0.15 | $V_{REF}$ + 0.15 | $V_{CCIO}$ + 0.3 | $V_{REF}$ – 0.31 | $V_{REF}$ + 0.31 | $V_{TT}$ – 0.81 | $V_{TT}$ + 0.81 | 16.2 | –16.2 |
| SSTL-18 Class I | –0.3 | $V_{REF}$ – 0.125 | $V_{REF}$ + 0.125 | $V_{CCIO}$ + 0.3 | $V_{REF}$ – 0.25 | $V_{REF}$ + 0.25 | $V_{TT}$ – 0.603 | $V_{TT}$ + 0.603 | 6.7 | –6.7 |
| SSTL-18 Class II | –0.3 | $V_{REF}$ – 0.125 | $V_{REF}$ + 0.125 | $V_{CCIO}$ + 0.3 | $V_{REF}$ – 0.25 | $V_{REF}$ + 0.25 | 0.28 | $V_{CCIO}$ – 0.28 | 13.4 | –13.4 |
| SSTL-15 Class I | — | $V_{REF}$ – 0.1 | $V_{REF}$ + 0.1 | — | $V_{REF}$ – 0.175 | $V_{REF}$ + 0.175 | 0.2 * $V_{CCIO}$ | 0.8 * $V_{CCIO}$ | 8 | –8 |
| SSTL-15 Class II | — | $V_{REF}$ – 0.1 | $V_{REF}$ + 0.1 | — | $V_{REF}$ – 0.175 | $V_{REF}$ + 0.175 | 0.2 * $V_{CCIO}$ | 0.8 * $V_{CCIO}$ | 16 | –16 |
| SSTL-135 Class I, II | — | $V_{REF}$ – 0.09 | $V_{REF}$ + 0.09 | — | $V_{REF}$ – 0.16 | $V_{REF}$ + 0.16 | 0.2 * $V_{CCIO}$ | 0.8 * $V_{CCIO}$ | — | — |
| SSTL-125 Class I, II | — | $V_{REF}$ – 0.85 | $V_{REF}$ + 0.85 | — | $V_{REF}$ – 0.15 | $V_{REF}$ + 0.15 | 0.2 * $V_{CCIO}$ | 0.8 * $V_{CCIO}$ | — | — |
| SSTL-12 Class I, II | — | $V_{REF}$ – 0.1 | $V_{REF}$ + 0.1 | — | $V_{REF}$ – 0.15 | $V_{REF}$ + 0.15 | 0.2 * $V_{CCIO}$ | 0.8 * $V_{CCIO}$ | — | — |

**Table 21. Differential HSTL and HSUL I/O Standards for Stratix V Devices (Part 2 of 2)**

| I/O Standard | $V_{CCIO}$ (V) | | | $V_{DIF(DC)}$ (V) | | $V_{X(AC)}$ (V) | | | $V_{CM(DC)}$ (V) | | | $V_{DIF(AC)}$ (V) | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | Min | Typ | Max | Min | Max | Min | Typ | Max | Min | Typ | Max | Min | Max |
| HSTL-12 Class I, II | 1.14 | 1.2 | 1.26 | 0.16 | $V_{CCIO}$ + 0.3 | — | 0.5* $V_{CCIO}$ | — | 0.4* $V_{CCIO}$ | 0.5* $V_{CCIO}$ | 0.6* $V_{CCIO}$ | 0.3 | $V_{CCIO}$ + 0.48 |
| HSUL-12 | 1.14 | 1.2 | 1.3 | 0.26 | 0.26 | 0.5*$V_{CCIO}$ – 0.12 | 0.5* $V_{CCIO}$ | 0.5*$V_{CCIO}$ + 0.12 | 0.4* $V_{CCIO}$ | 0.5* $V_{CCIO}$ | 0.6* $V_{CCIO}$ | 0.44 | 0.44 |

**Table 22. Differential I/O Standard Specifications for Stratix V Devices** *(7)*

| I/O Standard | $V_{CCIO}$ (V) *(10)* | | | $V_{ID}$ (mV) *(8)* | | | $V_{ICM(DC)}$ (V) | | | $V_{OD}$ (V) *(6)* | | | $V_{OCM}$ (V) *(6)* | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | Min | Typ | Max | Min | Condition | Max | Min | Condition | Max | Min | Typ | Max | Min | Typ | Max |
| PCML | Transmitter, receiver, and input reference clock pins of the high-speed transceivers use the PCML I/O standard. For transmitter, receiver, and reference clock I/O pin specifications, refer to Table 23 on page 18. | | | | | | | | | | | | | | |
| 2.5 V LVDS *(1)* | 2.375 | 2.5 | 2.625 | 100 | $V_{CM}$ = 1.25 V | — | 0.05 | $D_{MAX} \leq$ 700 Mbps | 1.8 | 0.247 | — | 0.6 | 1.125 | 1.25 | 1.375 |
| | | | | | | — | 1.05 | $D_{MAX} >$ 700 Mbps | 1.55 | 0.247 | — | 0.6 | 1.125 | 1.25 | 1.375 |
| BLVDS *(5)* | 2.375 | 2.5 | 2.625 | 100 | — | — | — | — | — | — | — | — | — | — | — |
| RSDS (HIO) *(2)* | 2.375 | 2.5 | 2.625 | 100 | $V_{CM}$ = 1.25 V | — | 0.3 | — | 1.4 | 0.1 | 0.2 | 0.6 | 0.5 | 1.2 | 1.4 |
| Mini-LVDS (HIO) *(3)* | 2.375 | 2.5 | 2.625 | 200 | — | 600 | 0.4 | — | 1.325 | 0.25 | — | 0.6 | 1 | 1.2 | 1.4 |
| LVPECL *(4), (9)* | — | — | — | 300 | — | — | 0.6 | $D_{MAX} \leq$ 700 Mbps | 1.8 | — | — | — | — | — | — |
| | — | — | — | 300 | — | — | 1 | $D_{MAX} >$ 700 Mbps | 1.6 | — | — | — | — | — | — |

**Notes to Table 22*:***

(1) For optimized LVDS receiver performance, the receiver voltage input range must be between 1.0 V to 1.6 V for data rates above 700 Mbps, and 0 V to 1.85 V for data rates below 700 Mbps.

(2) For optimized RSDS receiver performance, the receiver voltage input range must be between 0.25 V to 1.45 V.

(3) For optimized Mini-LVDS receiver performance, the receiver voltage input range must be between 0.3 V to 1.425 V.

(4) For optimized LVPECL receiver performance, the receiver voltage input range must be between 0.85 V to 1.75 V for data rate above 700 Mbps and 0.45 V to 1.95 V for data rate below 700 Mbps.

(5) There are no fixed $V_{ICM}$, $V_{OD}$, and $V_{OCM}$ specifications for BLVDS. They depend on the system topology.

(6) RL range: $90 \leq RL \leq 110\ \Omega$ .

(7) The 1.4-V and 1.5-V PCML transceiver I/O standard specifications are described in "Transceiver Performance Specifications" on page 18.

(8) The minimum VID value is applicable over the entire common mode range, VCM.

(9) LVPECL is only supported on dedicated clock input pins.

(10) Differential inputs are powered by VCCPD which requires 2.5 V.

## Power Consumption

Altera offers two ways to estimate power consumption for a design—the Excel-based Early Power Estimator and the Quartus® II PowerPlay Power Analyzer feature.

**Table 23. Transceiver Specifications for Stratix V GX and GS Devices** *(1)* **(Part 5 of 7)**

| Symbol/ Description | Conditions | Transceiver Speed Grade 1 | | | Transceiver Speed Grade 2 | | | Transceiver Speed Grade 3 | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| Programmable DC gain | DC Gain Setting = 0 | — | 0 | — | — | 0 | — | — | 0 | — | dB |
| | DC Gain Setting = 1 | — | 2 | — | — | 2 | — | — | 2 | — | dB |
| | DC Gain Setting = 2 | — | 4 | — | — | 4 | — | — | 4 | — | dB |
| | DC Gain Setting = 3 | — | 6 | — | — | 6 | — | — | 6 | — | dB |
| | DC Gain Setting = 4 | — | 8 | — | — | 8 | — | — | 8 | — | dB |
| **Transmitter** | | | | | | | | | | | |
| Supported I/O Standards | — | 1.4-V and 1.5-V PCML | | | | | | | | | |
| Data rate (Standard PCS) | — | 600 | — | 12200 | 600 | — | 12200 | 600 | — | 8500/ 10312.5 *(24)* | Mbps |
| Data rate (10G PCS) | — | 600 | — | 14100 | 600 | — | 12500 | 600 | — | 8500/ 10312.5 *(24)* | Mbps |
| Differential on-chip termination resistors | 85-Ω setting | — | 85 ± 20% | — | — | 85 ± 20% | — | — | 85 ± 20% | — | Ω |
| | 100-Ω setting | — | 100 ± 20% | — | — | 100 ± 20% | — | — | 100 ± 20% | — | Ω |
| | 120-Ω setting | — | 120 ± 20% | — | — | 120 ± 20% | — | — | 120 ± 20% | — | Ω |
| | 150-Ω setting | — | 150 ± 20% | — | — | 150 ± 20% | — | — | 150 ± 20% | — | Ω |
| $V_{OCM}$ (AC coupled) | 0.65-V setting | — | 650 | — | — | 650 | — | — | 650 | — | mV |
| $V_{OCM}$ (DC coupled) | — | — | 650 | — | — | 650 | — | — | 650 | — | mV |
| Rise time *(7)* | 20% to 80% | 30 | — | 160 | 30 | — | 160 | 30 | — | 160 | ps |
| Fall time *(7)* | 80% to 20% | 30 | — | 160 | 30 | — | 160 | 30 | — | 160 | ps |
| Intra-differential pair skew | Tx $V_{CM}$ = 0.5 V and slew rate of 15 ps | — | — | 15 | — | — | 15 | — | — | 15 | ps |
| Intra-transceiver block transmitter channel-to-channel skew | x6 PMA bonded mode | — | — | 120 | — | — | 120 | — | — | 120 | ps |

Table 24 shows the maximum transmitter data rate for the clock network.

**Table 24. Clock Network Maximum Data Rate Transmitter Specifications** *(1)*

| Clock Network | ATX PLL | | | CMU PLL *(2)* | | | fPLL | | |
|---|---|---|---|---|---|---|---|---|---|
| | Non-bonded Mode (Gbps) | Bonded Mode (Gbps) | Channel Span | Non-bonded Mode (Gbps) | Bonded Mode (Gbps) | Channel Span | Non-bonded Mode (Gbps) | Bonded Mode (Gbps) | Channel Span |
| x1 *(3)* | 14.1 | — | 6 | 12.5 | — | 6 | 3.125 | — | 3 |
| x6 *(3)* | — | 14.1 | 6 | — | 12.5 | 6 | — | 3.125 | 6 |
| x6 PLL Feedback *(4)* | — | 14.1 | Side-wide | — | 12.5 | Side-wide | — | — | — |
| xN (PCIe) | — | 8.0 | 8 | — | 5.0 | 8 | — | — | — |
| xN (Native PHY IP) | 8.0 | 8.0 | Up to 13 channels above and below PLL | 7.99 | 7.99 | Up to 13 channels above and below PLL | 3.125 | 3.125 | Up to 13 channels above and below PLL |
| | — | 8.01 to 9.8304 | Up to 7 channels above and below PLL | | | | | | |

**Notes to Table 24:**

(1) Valid data rates below the maximum specified in this table depend on the reference clock frequency and the PLL counter settings. Check the MegaWizard message during the PHY IP instantiation.

(2) ATX PLL is recommended at 8 Gbps and above data rates for improved jitter performance.

(3) Channel span is within a transceiver bank.

(4) Side-wide channel bonding is allowed up to the maximum supported by the PHY IP.

Table 25 shows the approximate maximum data rate using the standard PCS.

**Table 25. Stratix V Standard PCS Approximate Maximum Date Rate (1), (3)**

| Mode (2) | Transceiver Speed Grade | PMA Width | 20 | 20 | 16 | 16 | 10 | 10 | 8 | 8 |
|---|---|---|---|---|---|---|---|---|---|---|
| | | PCS/Core Width | 40 | 20 | 32 | 16 | 20 | 10 | 16 | 8 |
| FIFO | 1 | C1, C2, C2L, I2, I2L core speed grade | 12.2 | 11.4 | 9.76 | 9.12 | 6.5 | 5.8 | 5.2 | 4.72 |
| | 2 | C1, C2, C2L, I2, I2L core speed grade | 12.2 | 11.4 | 9.76 | 9.12 | 6.5 | 5.8 | 5.2 | 4.72 |
| | | C3, I3, I3L core speed grade | 9.8 | 9.0 | 7.84 | 7.2 | 5.3 | 4.7 | 4.24 | 3.76 |
| | 3 | C1, C2, C2L, I2, I2L core speed grade | 8.5 | 8.5 | 8.5 | 8.5 | 6.5 | 5.8 | 5.2 | 4.72 |
| | | I3YY core speed grade | 10.3125 | 10.3125 | 7.84 | 7.2 | 5.3 | 4.7 | 4.24 | 3.76 |
| | | C3, I3, I3L core speed grade | 8.5 | 8.5 | 7.84 | 7.2 | 5.3 | 4.7 | 4.24 | 3.76 |
| | | C4, I4 core speed grade | 8.5 | 8.2 | 7.04 | 6.56 | 4.8 | 4.2 | 3.84 | 3.44 |
| Register | 1 | C1, C2, C2L, I2, I2L core speed grade | 12.2 | 11.4 | 9.76 | 9.12 | 6.1 | 5.7 | 4.88 | 4.56 |
| | 2 | C1, C2, C2L, I2, I2L core speed grade | 12.2 | 11.4 | 9.76 | 9.12 | 6.1 | 5.7 | 4.88 | 4.56 |
| | | C3, I3, I3L core speed grade | 9.8 | 9.0 | 7.92 | 7.2 | 4.9 | 4.5 | 3.96 | 3.6 |
| | 3 | C1, C2, C2L, I2, I2L core speed grade | 10.3125 | 10.3125 | 10.3125 | 10.3125 | 6.1 | 5.7 | 4.88 | 4.56 |
| | | I3YY core speed grade | 10.3125 | 10.3125 | 7.92 | 7.2 | 4.9 | 4.5 | 3.96 | 3.6 |
| | | C3, I3, I3L core speed grade | 8.5 | 8.5 | 7.92 | 7.2 | 4.9 | 4.5 | 3.96 | 3.6 |
| | | C4, I4 core speed grade | 8.5 | 8.2 | 7.04 | 6.56 | 4.4 | 4.1 | 3.52 | 3.28 |

**Notes to Table 25**:

(1) The maximum data rate is in Gbps.

(2) The Phase Compensation FIFO can be configured in FIFO mode or register mode. In the FIFO mode, the pointers are not fixed, and the latency can vary. In the register mode the pointers are fixed for low latency.

(3) The maximum data rate is also constrained by the transceiver speed grade. Refer to Table 1 for the transceiver speed grade.

**Table 28. Transceiver Specifications for Stratix V GT Devices (Part 1 of 5) (1)**

| Symbol/ Description | Conditions | Transceiver Speed Grade 2 | | | Transceiver Speed Grade 3 | | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | Min | Typ | Max | Min | Typ | Max | |
| **Reference Clock** | | | | | | | | |
| Supported I/O Standards | Dedicated reference clock pin | 1.2-V PCML, 1.4-V PCML, 1.5-V PCML, 2.5-V PCML, Differential LVPECL, LVDS, and HCSL | | | | | | |
| | RX reference clock pin | 1.4-V PCML, 1.5-V PCML, 2.5-V PCML, LVPECL, and LVDS | | | | | | |
| Input Reference Clock Frequency (CMU PLL) (6) | — | 40 | — | 710 | 40 | — | 710 | MHz |
| Input Reference Clock Frequency (ATX PLL) (6) | — | 100 | — | 710 | 100 | — | 710 | MHz |
| Rise time | 20% to 80% | — | — | 400 | — | — | 400 | ps |
| Fall time | 80% to 20% | — | — | 400 | — | — | 400 | |
| Duty cycle | — | 45 | — | 55 | 45 | — | 55 | % |
| Spread-spectrum modulating clock frequency | PCI Express (PCIe) | 30 | — | 33 | 30 | — | 33 | kHz |
| Spread-spectrum downspread | PCIe | — | 0 to –0.5 | — | — | 0 to –0.5 | — | % |
| On-chip termination resistors (19) | — | — | 100 | — | — | 100 | — | Ω |
| Absolute $V_{MAX}$ (3) | Dedicated reference clock pin | — | — | 1.6 | — | — | 1.6 | V |
| | RX reference clock pin | — | — | 1.2 | — | — | 1.2 | |
| Absolute $V_{MIN}$ | — | -0.4 | — | — | -0.4 | — | — | V |
| Peak-to-peak differential input voltage | — | 200 | — | 1600 | 200 | — | 1600 | mV |
| $V_{ICM}$ (AC coupled) | Dedicated reference clock pin | 1050/1000 (2) | | | 1050/1000 (2) | | | mV |
| | RX reference clock pin | 1.0/0.9/0.85 (22) | | | 1.0/0.9/0.85 (22) | | | V |
| $V_{ICM}$ (DC coupled) | HCSL I/O standard for PCIe reference clock | 250 | — | 550 | 250 | — | 550 | mV |

Figure 4 shows the differential transmitter output waveform.

**Figure 4. Differential Transmitter/Receiver Output/Input Waveform**

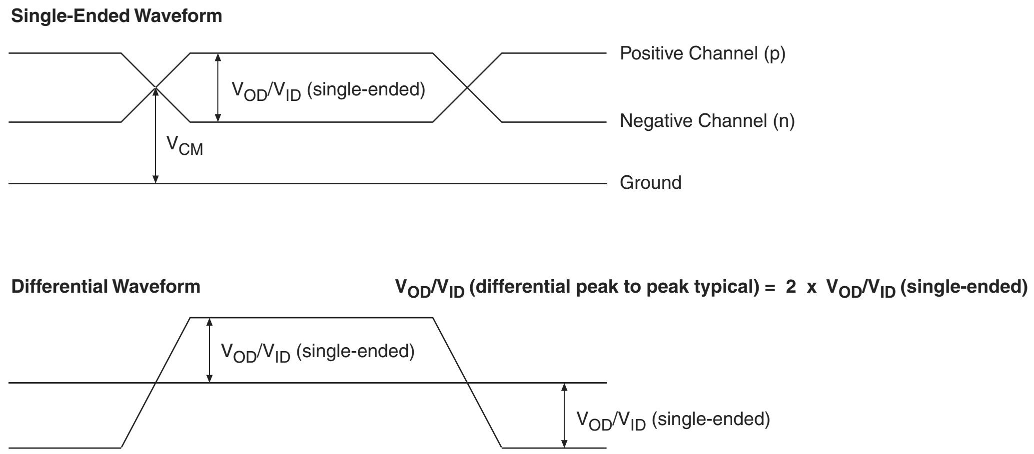


Figure 5 shows the Stratix V AC gain curves for GT channels.

**Figure 5. AC Gain Curves for GT Channels**

**Table 31. PLL Specifications for Stratix V Devices (Part 2 of 3)**

| Symbol | Parameter | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| $t_{INCCJ}$ (3), (4) | Input clock cycle-to-cycle jitter ($f_{REF} \geq 100$ MHz) | — | — | 0.15 | UI (p-p) |
| | Input clock cycle-to-cycle jitter ($f_{REF} < 100$ MHz) | –750 | — | +750 | ps (p-p) |
| $t_{OUTPJ\_DC}$ (5) | Period Jitter for dedicated clock output ($f_{OUT} \geq$ 100 MHz) | — | — | 175 (1) | ps (p-p) |
| | Period Jitter for dedicated clock output ($f_{OUT} <$ 100 MHz) | — | — | 17.5 (1) | mUI (p-p) |
| $t_{FOUTPJ\_DC}$ (5) | Period Jitter for dedicated clock output in fractional PLL ($f_{OUT} \geq 100$ MHz) | — | — | 250 (11), 175 (12) | ps (p-p) |
| | Period Jitter for dedicated clock output in fractional PLL ($f_{OUT} < 100$ MHz) | — | — | 25 (11), 17.5 (12) | mUI (p-p) |
| $t_{OUTCCJ\_DC}$ (5) | Cycle-to-Cycle Jitter for a dedicated clock output ($f_{OUT} \geq 100$ MHz) | — | — | 175 | ps (p-p) |
| | Cycle-to-Cycle Jitter for a dedicated clock output ($f_{OUT} < 100$ MHz) | — | — | 17.5 | mUI (p-p) |
| $t_{FOUTCCJ\_DC}$ (5) | Cycle-to-cycle Jitter for a dedicated clock output in fractional PLL ($f_{OUT} \geq 100$ MHz) | — | — | 250 (11), 175 (12) | ps (p-p) |
| | Cycle-to-cycle Jitter for a dedicated clock output in fractional PLL ($f_{OUT} < 100$ MHz)+ | — | — | 25 (11), 17.5 (12) | mUI (p-p) |
| $t_{OUTPJ\_IO}$ (5), (8) | Period Jitter for a clock output on a regular I/O in integer PLL ($f_{OUT} \geq 100$ MHz) | — | — | 600 | ps (p-p) |
| | Period Jitter for a clock output on a regular I/O ($f_{OUT} < 100$ MHz) | — | — | 60 | mUI (p-p) |
| $t_{FOUTPJ\_IO}$ (5), (8), (11) | Period Jitter for a clock output on a regular I/O in fractional PLL ($f_{OUT} \geq 100$ MHz) | — | — | 600 (10) | ps (p-p) |
| | Period Jitter for a clock output on a regular I/O in fractional PLL ($f_{OUT} < 100$ MHz) | — | — | 60 (10) | mUI (p-p) |
| $t_{OUTCCJ\_IO}$ (5), (8) | Cycle-to-cycle Jitter for a clock output on a regular I/O in integer PLL ($f_{OUT} \geq 100$ MHz) | — | — | 600 | ps (p-p) |
| | Cycle-to-cycle Jitter for a clock output on a regular I/O in integer PLL ($f_{OUT} < 100$ MHz) | — | — | 60 (10) | mUI (p-p) |
| $t_{FOUTCCJ\_IO}$ (5), (8), (11) | Cycle-to-cycle Jitter for a clock output on a regular I/O in fractional PLL ($f_{OUT} \geq 100$ MHz) | — | — | 600 (10) | ps (p-p) |
| | Cycle-to-cycle Jitter for a clock output on a regular I/O in fractional PLL ($f_{OUT} < 100$ MHz) | — | — | 60 | mUI (p-p) |
| $t_{CASC\_OUTPJ\_DC}$ (5), (6) | Period Jitter for a dedicated clock output in cascaded PLLs ($f_{OUT} \geq 100$ MHz) | — | — | 175 | ps (p-p) |
| | Period Jitter for a dedicated clock output in cascaded PLLs ($f_{OUT} < 100$ MHz) | — | — | 17.5 | mUI (p-p) |
| $f_{DRIFT}$ | Frequency drift after PFDENA is disabled for a duration of 100 µs | — | — | ±10 | % |
| $dK_{BIT}$ | Bit number of Delta Sigma Modulator (DSM) | 8 | 24 | 32 | Bits |
| $k_{VALUE}$ | Numerator of Fraction | 128 | 8388608 | 2147483648 | — |

Figure 7 shows the dynamic phase alignment (DPA) lock time specifications with the DPA PLL calibration option enabled.

**Figure 7. DPA Lock Time Specification with DPA PLL Calibration Enabled**

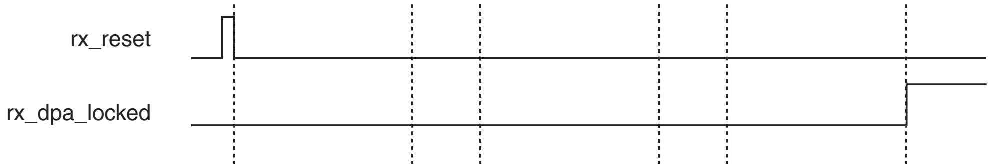


Table 37 lists the DPA lock time specifications for Stratix V devices.

**Table 37. DPA Lock Time Specifications for Stratix V GX Devices Only (1), (2), (3)**

| Standard | Training Pattern | Number of Data Transitions in One Repetition of the Training Pattern | Number of Repetitions per 256 Data Transitions (4) | Maximum |
|---|---|---|---|---|
| SPI-4 | 00000000001111111111 | 2 | 128 | 640 data transitions |
| Parallel Rapid I/O | 00001111 | 2 | 128 | 640 data transitions |
| | 10010000 | 4 | 64 | 640 data transitions |
| Miscellaneous | 10101010 | 8 | 32 | 640 data transitions |
| | 01010101 | 8 | 32 | 640 data transitions |

**Notes to Table 37:**

(1) The DPA lock time is for one channel.

(2) One data transition is defined as a 0-to-1 or 1-to-0 transition.

(3) The DPA lock time stated in this table applies to both commercial and industrial grade.

(4) This is the number of repetitions for the stated training pattern to achieve the 256 data transitions.

Figure 8 shows the **LVDS** soft-clock data recovery (CDR)/DPA sinusoidal jitter tolerance specification for a data rate ≥ 1.25 Gbps. Table 38 lists the **LVDS** soft-CDR/DPA sinusoidal jitter tolerance specification for a data rate ≥ 1.25 Gbps.

**Figure 8. LVDS Soft-CDR/DPA Sinusoidal Jitter Tolerance Specification for a Data Rate ≥ 1.25 Gbps**

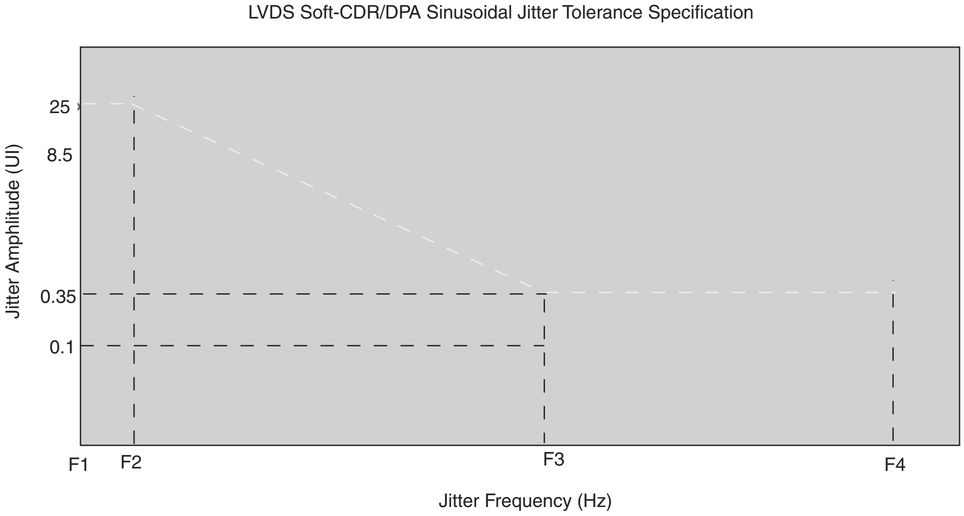


**Table 46. JTAG Timing Parameters and Values for Stratix V Devices**

| Symbol | Description | Min | Max | Unit |
|---|---|---|---|---|
| $t_{JPH}$ | JTAG port hold time | 5 | — | ns |
| $t_{JPCO}$ | JTAG port clock to output | — | 11 (1) | ns |
| $t_{JPZX}$ | JTAG port high impedance to valid output | — | 14 (1) | ns |
| $t_{JPXZ}$ | JTAG port valid output to high impedance | — | 14 (1) | ns |

**Notes to Table 46:**

(1) A 1 ns adder is required for each $V_{CCIO}$ voltage step down from 3.0 V. For example, $t_{JPCO}$ = 12 ns if $V_{CCIO}$ of the TDO I/O bank = 2.5 V, or 13 ns if it equals 1.8 V.

(2) The minimum TCK clock period is 167 ns if VCCBAT is within the range 1.2V-1.5V when you perform the volatile key programming.

## Raw Binary File Size

For the POR delay specification, refer to the "POR Delay Specification" section of the "Configuration, Design Security, and Remote System Upgrades in Stratix V Devices".

Table 47 lists the uncompressed raw binary file (**.rbf**) sizes for Stratix V devices.

**Table 47. Uncompressed .rbf Sizes for Stratix V Devices**

| Family | Device | Package | Configuration .rbf Size (bits) | IOCSR .rbf Size (bits) (4), (5) |
|---|---|---|---|---|
| Stratix V GX | 5SGXA3 | H35, F40, F35 (2) | 213,798,880 | 562,392 |
| | | H29, F35 (3) | 137,598,880 | 564,504 |
| | 5SGXA4 | — | 213,798,880 | 563,672 |
| | 5SGXA5 | — | 269,979,008 | 562,392 |
| | 5SGXA7 | — | 269,979,008 | 562,392 |
| | 5SGXA9 | — | 342,742,976 | 700,888 |
| | 5SGXAB | — | 342,742,976 | 700,888 |
| | 5SGXB5 | — | 270,528,640 | 584,344 |
| | 5SGXB6 | — | 270,528,640 | 584,344 |
| | 5SGXB9 | — | 342,742,976 | 700,888 |
| | 5SGXBB | — | 342,742,976 | 700,888 |
| Stratix V GT | 5SGTC5 | — | 269,979,008 | 562,392 |
| | 5SGTC7 | — | 269,979,008 | 562,392 |
| Stratix V GS | 5SGSD3 | — | 137,598,880 | 564,504 |
| | 5SGSD4 | F1517 | 213,798,880 | 563,672 |
| | | — | 137,598,880 | 564,504 |
| | 5SGSD5 | — | 213,798,880 | 563,672 |
| | 5SGSD6 | — | 293,441,888 | 565,528 |
| | 5SGSD8 | — | 293,441,888 | 565,528 |

**Table 47. Uncompressed .rbf Sizes for Stratix V Devices**

| Family | Device | Package | Configuration .rbf Size (bits) | IOCSR .rbf Size (bits) (4), (5) |
|---|---|---|---|---|
| Stratix V E (1) | 5SEE9 | — | 342,742,976 | 700,888 |
|  | 5SEEB | — | 342,742,976 | 700,888 |

**Notes to Table 47:**

(1) Stratix V E devices do not have PCI Express® (PCIe®) hard IP. Stratix V E devices do not support the CvP configuration scheme.
(2) 36-transceiver devices.
(3) 24-transceiver devices.
(4) File size for the periphery image.
(5) The IOCSR **.rbf** size is specifically for the CvP feature.

Use the data in Table 47 to estimate the file size before design compilation. Different configuration file formats, such as a hexadecimal (**.hex**) or tabular text file (**.ttf**) format, have different file sizes. For the different types of configuration file and file sizes, refer to the Quartus II software. However, for a specific version of the Quartus II software, any design targeted for the same device has the same uncompressed configuration file size. If you are using compression, the file size can vary after each compilation because the compression ratio depends on your design.

For more information about setting device configuration options, refer to *Configuration, Design Security, and Remote System Upgrades in Stratix V Devices*. For creating configuration files, refer to the *Quartus II Help*.

Table 48 lists the minimum configuration time estimates for Stratix V devices.

**Table 48. Minimum Configuration Time Estimation for Stratix V Devices**

| Variant | Member Code | Active Serial (1) |  |  | Fast Passive Parallel (2) |  |  |
|---|---|---|---|---|---|---|---|
|  |  | Width | DCLK (MHz) | Min Config Time (s) | Width | DCLK (MHz) | Min Config Time (s) |
| GX | A3 | 4 | 100 | 0.534 | 32 | 100 | 0.067 |
|  |  | 4 | 100 | 0.344 | 32 | 100 | 0.043 |
|  | A4 | 4 | 100 | 0.534 | 32 | 100 | 0.067 |
|  | A5 | 4 | 100 | 0.675 | 32 | 100 | 0.084 |
|  | A7 | 4 | 100 | 0.675 | 32 | 100 | 0.084 |
|  | A9 | 4 | 100 | 0.857 | 32 | 100 | 0.107 |
|  | AB | 4 | 100 | 0.857 | 32 | 100 | 0.107 |
|  | B5 | 4 | 100 | 0.676 | 32 | 100 | 0.085 |
|  | B6 | 4 | 100 | 0.676 | 32 | 100 | 0.085 |
|  | B9 | 4 | 100 | 0.857 | 32 | 100 | 0.107 |
|  | BB | 4 | 100 | 0.857 | 32 | 100 | 0.107 |
| GT | C5 | 4 | 100 | 0.675 | 32 | 100 | 0.084 |
|  | C7 | 4 | 100 | 0.675 | 32 | 100 | 0.084 |

**Table 48. Minimum Configuration Time Estimation for Stratix V Devices**

| Variant | Member Code | Active Serial (1) | | | Fast Passive Parallel (2) | | |
|---|---|---|---|---|---|---|---|
| | | Width | DCLK (MHz) | Min Config Time (s) | Width | DCLK (MHz) | Min Config Time (s) |
| GS | D3 | 4 | 100 | 0.344 | 32 | 100 | 0.043 |
| | D4 | 4 | 100 | 0.534 | 32 | 100 | 0.067 |
| | | 4 | 100 | 0.344 | 32 | 100 | 0.043 |
| | D5 | 4 | 100 | 0.534 | 32 | 100 | 0.067 |
| | D6 | 4 | 100 | 0.741 | 32 | 100 | 0.093 |
| | D8 | 4 | 100 | 0.741 | 32 | 100 | 0.093 |
| E | E9 | 4 | 100 | 0.857 | 32 | 100 | 0.107 |
| | EB | 4 | 100 | 0.857 | 32 | 100 | 0.107 |

**Notes to Table 48:**

(1) DCLK frequency of 100 MHz using external CLKUSR.

(2) Max FPGA FPP bandwidth may exceed bandwidth available from some external storage or control logic.

# Fast Passive Parallel Configuration Timing

This section describes the fast passive parallel (FPP) configuration timing parameters for Stratix V devices.

## DCLK-to-DATA[] Ratio for FPP Configuration

FPP configuration requires a different `DCLK`-to-`DATA[]` ratio when you enable the design security, decompression, or both features. Table 49 lists the `DCLK`-to-`DATA[]` ratio for each combination.

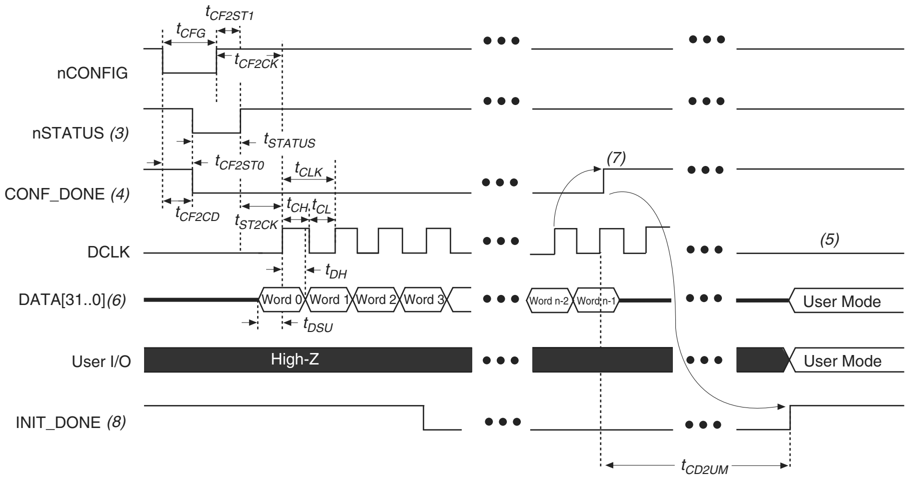
**Table 49. DCLK-to-DATA[] Ratio (1) (Part 1 of 2)**

| Configuration Scheme | Decompression | Design Security | DCLK-to-DATA[] Ratio |
|---|---|---|---|
| FPP ×8 | Disabled | Disabled | 1 |
| | Disabled | Enabled | 1 |
| | Enabled | Disabled | 2 |
| | Enabled | Enabled | 2 |
| FPP ×16 | Disabled | Disabled | 1 |
| | Disabled | Enabled | 2 |
| | Enabled | Disabled | 4 |
| | Enabled | Enabled | 4 |

## FPP Configuration Timing when DCLK-to-DATA [] = 1

Figure 12 shows the timing waveform for FPP configuration when using a MAX II or MAX V device as an external host. This waveform shows timing when the `DCLK`-to-`DATA[]` ratio is 1.

**Figure 12. FPP Configuration Timing Waveform When the DCLK-to-DATA[] Ratio is 1** *(1), (2)*



**Notes to Figure 12:**

1. (1) Use this timing waveform when the `DCLK`-to-`DATA[]` ratio is 1.
2. (2) The beginning of this waveform shows the device in user mode. In user mode, `nCONFIG`, `nSTATUS`, and `CONF_DONE` are at logic-high levels. When `nCONFIG` is pulled low, a reconfiguration cycle begins.
3. (3) After power-up, the Stratix V device holds `nSTATUS` low for the time of the POR delay.
4. (4) After power-up, before and during configuration, `CONF_DONE` is low.
5. (5) Do not leave `DCLK` floating after configuration. `DCLK` is ignored after configuration is complete. It can toggle high or low if required.
6. (6) For FPP ×16, use `DATA[15..0]`. For FPP ×8, use `DATA[7..0]`. `DATA[31..0]` are available as a user I/O pin after configuration. The state of this pin depends on the dual-purpose pin settings.
7. (7) To ensure a successful configuration, send the entire configuration data to the Stratix V device. `CONF_DONE` is released high when the Stratix V device receives all the configuration data successfully. After `CONF_DONE` goes high, send two additional falling edges on `DCLK` to begin initialization and enter user mode.
8. (8) After the option bit to enable the `INIT_DONE` pin is configured into the device, the `INIT_DONE` goes low.

Table 54 lists the PS configuration timing parameters for Stratix V devices.

**Table 54. PS Timing Parameters for Stratix V Devices**

| Symbol | Parameter | Minimum | Maximum | Units |
|---|---|---|---|---|
| $t_{CF2CD}$ | `nCONFIG` low to `CONF_DONE` low | — | 600 | ns |
| $t_{CF2ST0}$ | `nCONFIG` low to `nSTATUS` low | — | 600 | ns |
| $t_{CFG}$ | `nCONFIG` low pulse width | 2 | — | µs |
| $t_{STATUS}$ | `nSTATUS` low pulse width | 268 | 1,506 *(1)* | µs |
| $t_{CF2ST1}$ | `nCONFIG` high to `nSTATUS` high | — | 1,506 *(2)* | µs |
| $t_{CF2CK}$ *(5)* | `nCONFIG` high to first rising edge on `DCLK` | 1,506 | — | µs |
| $t_{ST2CK}$ *(5)* | `nSTATUS` high to first rising edge of `DCLK` | 2 | — | µs |
| $t_{DSU}$ | `DATA[]` setup time before rising edge on `DCLK` | 5.5 | — | ns |
| $t_{DH}$ | `DATA[]` hold time after rising edge on `DCLK` | 0 | — | ns |
| $t_{CH}$ | `DCLK` high time | $0.45 \times 1/f_{MAX}$ | — | s |
| $t_{CL}$ | `DCLK` low time | $0.45 \times 1/f_{MAX}$ | — | s |
| $t_{CLK}$ | `DCLK` period | $1/f_{MAX}$ | — | s |
| $f_{MAX}$ | `DCLK` frequency | — | 125 | MHz |
| $t_{CD2UM}$ | `CONF_DONE` high to user mode *(3)* | 175 | 437 | µs |
| $t_{CD2CU}$ | `CONF_DONE` high to `CLKUSR` enabled | 4 × maximum `DCLK` period | — | — |
| $t_{CD2UMC}$ | `CONF_DONE` high to user mode with `CLKUSR` option on | $t_{CD2CU}$ + (8576 × `CLKUSR` period) *(4)* | — | — |

**Notes to Table 54:**

(1) This value is applicable if you do not delay configuration by extending the `nCONFIG` or `nSTATUS` low pulse width.

(2) This value is applicable if you do not delay configuration by externally holding the `nSTATUS` low.

(3) The minimum and maximum numbers apply only if you choose the internal oscillator as the clock source for initializing the device.

(4) To enable the `CLKUSR` pin as the initialization clock source and to obtain the maximum frequency specification on these pins, refer to the "Initialization" section.

(5) If `nSTATUS` is monitored, follow the $t_{ST2CK}$ specification. If `nSTATUS` is not monitored, follow the $t_{CF2CK}$ specification.

# Initialization

Table 55 lists the initialization clock source option, the applicable configuration schemes, and the maximum frequency.

**Table 55. Initialization Clock Source Option and the Maximum Frequency**

| Initialization Clock Source | Configuration Schemes | Maximum Frequency | Minimum Number of Clock Cycles *(1)* |
|---|---|---|---|
| Internal Oscillator | AS, PS, FPP | 12.5 MHz | 8576 |
| `CLKUSR` | AS, PS, FPP *(2)* | 125 MHz | |
| `DCLK` | PS, FPP | 125 MHz | |

**Notes to Table 55:**

(1) The minimum number of clock cycles required for device initialization.

(2) To enable `CLKUSR` as the initialization clock source, turn on the **Enable user-supplied start-up clock (`CLKUSR`)** option in the Quartus II software from the **General** panel of the **Device and Pin Options** dialog box.

**Table 58. IOE Programmable Delay for Stratix V Devices (Part 2 of 2)**

| Parameter (1) | Available Settings | Min Offset (2) | Fast Model |  | Slow Model |  |  |  |  |  |  |  |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
|  |  |  | Industrial | Commercial | C1 | C2 | C3 | C4 | I2 | I3, I3YY | I4 | Unit |
| D3 | 8 | 0 | 1.587 | 1.699 | 2.793 | 2.793 | 2.992 | 3.192 | 2.811 | 3.047 | 3.257 | ns |
| D4 | 64 | 0 | 0.464 | 0.492 | 0.838 | 0.838 | 0.924 | 1.011 | 0.843 | 0.920 | 1.006 | ns |
| D5 | 64 | 0 | 0.464 | 0.493 | 0.838 | 0.838 | 0.924 | 1.011 | 0.844 | 0.921 | 1.006 | ns |
| D6 | 32 | 0 | 0.229 | 0.244 | 0.415 | 0.415 | 0.458 | 0.503 | 0.418 | 0.456 | 0.499 | ns |

**Notes to Table 58:**

(1) You can set this value in the Quartus II software by selecting **D1**, **D2**, **D3**, **D5**, and **D6** in the **Assignment Name** column of **Assignment Editor**.

(2) Minimum offset does not include the intrinsic delay.

## Programmable Output Buffer Delay

Table 59 lists the delay chain settings that control the rising and falling edge delays of the output buffer. The default delay is 0 ps.

**Table 59. Programmable Output Buffer Delay for Stratix V Devices** *(1)*

| Symbol | Parameter | Typical | Unit |
|---|---|---|---|
| $D_{OUTBUF}$ | Rising and/or falling edge delay | 0 (default) | ps |
|  |  | 25 | ps |
|  |  | 50 | ps |
|  |  | 75 | ps |

**Note to Table 59:**

(1) You can set the programmable output buffer delay in the Quartus II software by setting the **Output Buffer Delay Control** assignment to either positive, negative, or both edges, with the specific values stated here (in ps) for the **Output Buffer Delay** assignment.

# Glossary

Table 60 lists the glossary for this chapter.

**Table 60. Glossary (Part 1 of 4)**

| Letter | Subject | Definitions |
|---|---|---|
| **A**<br>B<br>C | — | — |
| **D** | — | — |
| **E** | — | — |
| **F** | $f_{HSCLK}$ | Left and right PLL input clock frequency. |
|  | $f_{HSDR}$ | High-speed I/O block—Maximum and minimum **LVDS** data transfer rate ($f_{HSDR}$ = 1/TUI), non-DPA. |
|  | $f_{HSDRDPA}$ | High-speed I/O block—Maximum and minimum **LVDS** data transfer rate ($f_{HSDRDPA}$ = 1/TUI), DPA. |

**Table 60. Glossary (Part 2 of 4)**

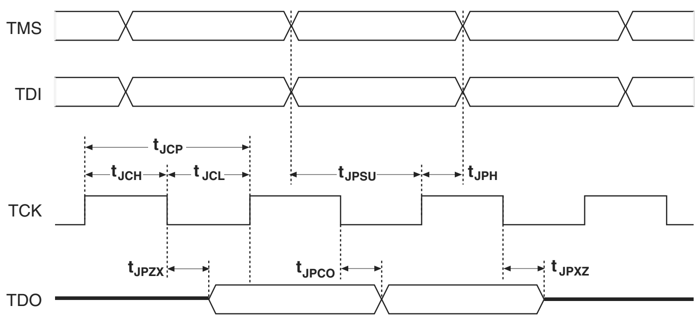
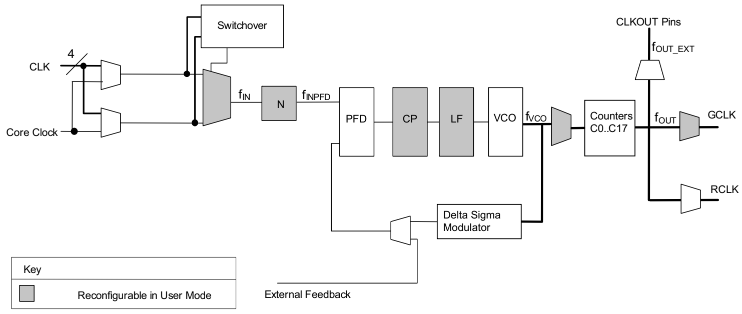
| Letter | Subject | Definitions |
|---|---|---|
| **G**<br>H<br>I | — | — |
| **J** | J | High-speed I/O block—Deserialization factor (width of parallel data bus). |
| | JTAG Timing Specifications | JTAG Timing Specifications:  |
| **K**<br>L<br>M<br>N<br>O | — | — |
| **P** | **PLL Specifications** | **Diagram of PLL Specifications** (1)  <br>**Note:**<br>(1) `Core Clock` can only be fed by dedicated clock input pins or PLL outputs. |
| **Q** | — | — |
| **R** | **$R_L$** | Receiver differential input discrete resistor (external to the Stratix V device). |

**Table 60. Glossary (Part 4 of 4)**

| Letter | Subject | Definitions |
|---|---|---|
| **V** | $\mathbf{V}_{CM(DC)}$ | DC common mode input voltage. |
| | $\mathbf{V}_{ICM}$ | Input common mode voltage—The common mode of the differential signal at the receiver. |
| | $\mathbf{V}_{ID}$ | Input differential voltage swing—The difference in voltage between the positive and complementary conductors of a differential transmission at the receiver. |
| | $\mathbf{V}_{DIF(AC)}$ | AC differential input voltage—Minimum AC input differential voltage required for switching. |
| | $\mathbf{V}_{DIF(DC)}$ | DC differential input voltage— Minimum DC input differential voltage required for switching. |
| | $\mathbf{V}_{IH}$ | Voltage input high—The minimum positive voltage applied to the input which is accepted by the device as a logic high. |
| | $\mathbf{V}_{IH(AC)}$ | High-level AC input voltage |
| | $\mathbf{V}_{IH(DC)}$ | High-level DC input voltage |
| | $\mathbf{V}_{IL}$ | Voltage input low—The maximum positive voltage applied to the input which is accepted by the device as a logic low. |
| | $\mathbf{V}_{IL(AC)}$ | Low-level AC input voltage |
| | $\mathbf{V}_{IL(DC)}$ | Low-level DC input voltage |
| | $\mathbf{V}_{OCM}$ | Output common mode voltage—The common mode of the differential signal at the transmitter. |
| | $\mathbf{V}_{OD}$ | Output differential voltage swing—The difference in voltage between the positive and complementary conductors of a differential transmission at the transmitter. |
| | $\mathbf{V}_{SWING}$ | Differential input voltage |
| | $\mathbf{V}_{X}$ | Input differential cross point voltage |
| | $\mathbf{V}_{OX}$ | Output differential cross point voltage |
| **W** | W | High-speed I/O block—clock boost factor |
| **X**<br>Y<br>Z | — | — |

# Document Revision History

Table 61 lists the revision history for this chapter.

**Table 61. Document Revision History (Part 1 of 3)**

| Date | Version | Changes |
|---|---|---|
| June 2018 | 3.9 | ■ Added the “Stratix V Device Overshoot Duration” figure. |
| April 2017 | 3.8 | ■ Added a footnote to the “High-Speed I/O Specifications for Stratix V Devices” table.<br>■ Changed the minimum value for $t_{CD2UMC}$ in the “PS Timing Parameters for Stratix V Devices” table.<br>■ Changed the condition for 100-Ω $R_D$ in the “OCT Without Calibration Resistance Tolerance Specifications for Stratix V Devices” table.<br>■ Changed the minimum value for $t_{CD2UMC}$ in the “AS Timing Parameters for AS ´1 and AS ´4 Configurations in Stratix V Devices” table<br>■ Changed the minimum value for $t_{CD2UMC}$ in the “FPP Timing Parameters for Stratix V Devices When the DCLK-to-DATA[] Ratio is >1” table.<br>■ Changed the minimum value for $t_{CD2UMC}$ in the “FPP Timing Parameters for Stratix V Devices When the DCLK-to-DATA[] Ratio is >1” table.<br>■ Changed the minimum number of clock cycles value in the “Initialization Clock Source Option and the Maximum Frequency” table. |
| June 2016 | 3.7 | ■ Added the $V_{ID}$ minimum specification for LVPECL in the “Differential I/O Standard Specifications for Stratix V Devices” table<br>■ Added the $I_{OUT}$ specification to the “Absolute Maximum Ratings for Stratix V Devices” table. |
| December 2015 | 3.6 | ■ Added a footnote to the “High-Speed I/O Specifications for Stratix V Devices” table. |
| December 2015 | 3.5 | ■ Changed the transmitter, receiver, and ATX PLL data rate specifications in the “Transceiver Specifications for Stratix V GX and GS Devices” table.<br>■ Changed the configuration .rbf sizes in the “Uncompressed .rbf Sizes for Stratix V Devices” table. |
| July 2015 | 3.4 | ■ Changed the data rate specification for transceiver speed grade 3 in the following tables:<br>  ■ “Transceiver Specifications for Stratix V GX and GS Devices”<br>  ■ “Stratix V Standard PCS Approximate Maximum Date Rate”<br>  ■ “Stratix V 10G PCS Approximate Maximum Data Rate”<br>■ Changed the conditions for reference clock rise and fall time, and added a note to the “Transceiver Specifications for Stratix V GX and GS Devices” table.<br>■ Added a note to the “Minimum differential eye opening at receiver serial input pins” specification in the “Transceiver Specifications for Stratix V GX and GS Devices” table.<br>■ Changed the $t_{CO}$ maximum value in the “AS Timing Parameters for AS ´1 and AS ´4 Configurations in Stratix V Devices” table.<br>■ Removed the CDR ppm tolerance specification from the “Transceiver Specifications for Stratix V GX and GS Devices” table. |