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### Understanding [Embedded - FPGAs \(Field Programmable Gate Array\)](#)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

### Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

#### Details

|                                |   |
|--------------------------------|---|
| Product Status                 | Obsolete  |
| Number of LABs/CLBs            | 317000  |
| Number of Logic Elements/Cells | 840000  |
| Total RAM Bits                 | 53248000  |
| Number of I/O                  | 600   |
| Number of Gates                | -   |
| Voltage - Supply               | 0.87V ~ 0.93V   |
| Mounting Type                  | Surface Mount   |
| Operating Temperature          | 0°C ~ 85°C (TJ)   |
| Package / Case                 | 1760-BBGA, FCBGA  |
| Supplier Device Package        | 1760-HBGA (45x45)   |
| Purchase URL                   | <a href="https://www.e-xfl.com/product-detail/intel/5sgxeb9r3h43c2n">https://www.e-xfl.com/product-detail/intel/5sgxeb9r3h43c2n</a> |

**Table 1. Stratix V GX and GS Commercial and Industrial Speed Grade Offering <sup>(1), (2), (3)</sup> (Part 2 of 2)**

| Transceiver Speed Grade  | Core Speed Grade |         |     |     |         |         |                    |     |
|--------------------------|------------------|---------|-----|-----|---------|---------|--------------------|-----|
|                          | C1               | C2, C2L | C3  | C4  | I2, I2L | I3, I3L | I3YY               | I4  |
| 3<br>GX channel—8.5 Gbps | —                | Yes     | Yes | Yes | —       | Yes     | Yes <sup>(4)</sup> | Yes |

**Notes to Table 1:**

- (1) C = Commercial temperature grade; I = Industrial temperature grade.  
 (2) Lower number refers to faster speed grade.  
 (3) C2L, I2L, and I3L speed grades are for low-power devices.  
 (4) I3YY speed grades can achieve up to 10.3125 Gbps.

Table 2 lists the industrial and commercial speed grades for the Stratix V GT devices.

**Table 2. Stratix V GT Commercial and Industrial Speed Grade Offering <sup>(1), (2)</sup>**

| Transceiver Speed Grade                            | Core Speed Grade |     |     |     |
|--|------------------|-----|-----|-----|
|  | C1               | C2  | I2  | I3  |
| 2<br>GX channel—12.5 Gbps<br>GT channel—28.05 Gbps | Yes              | Yes | —   | —   |
| 3<br>GX channel—12.5 Gbps<br>GT channel—25.78 Gbps | Yes              | Yes | Yes | Yes |

**Notes to Table 2:**

- (1) C = Commercial temperature grade; I = Industrial temperature grade.  
 (2) Lower number refers to faster speed grade.

**Absolute Maximum Ratings**

Absolute maximum ratings define the maximum operating conditions for Stratix V devices. The values are based on experiments conducted with the devices and theoretical modeling of breakdown and damage mechanisms. The functional operation of the device is not implied for these conditions.



Conditions other than those listed in Table 3 may cause permanent damage to the device. Additionally, device operation at the absolute maximum ratings for extended periods of time may have adverse effects on the device.

**Table 3. Absolute Maximum Ratings for Stratix V Devices (Part 1 of 2)**

| Symbol              | Description  | Minimum | Maximum | Unit |
|---------------------|--|---------|---------|------|
| V <sub>CC</sub>     | Power supply for core voltage and periphery circuitry                  | −0.5    | 1.35    | V    |
| V <sub>CCPT</sub>   | Power supply for programmable power technology                         | −0.5    | 1.8     | V    |
| V <sub>CCPGM</sub>  | Power supply for configuration pins                                    | −0.5    | 3.9     | V    |
| V <sub>CC_AUX</sub> | Auxiliary supply for the programmable power technology                 | −0.5    | 3.4     | V    |
| V <sub>CCBAT</sub>  | Battery back-up power supply for design security volatile key register | −0.5    | 3.9     | V    |
| V <sub>CCPD</sub>   | I/O pre-driver power supply  | −0.5    | 3.9     | V    |
| V <sub>CCIO</sub>   | I/O power supply   | −0.5    | 3.9     | V    |

Table 8 shows the transceiver power supply voltage requirements for various conditions.

**Table 8. Transceiver Power Supply Voltage Requirements**

| Conditions  | Core Speed Grade                  | VCCR_GXB & VCCT_GXB <sup>(2)</sup> | VCCA_GXB | VCCH_GXB | Unit |
|---|-----------------------------------|------------------------------------|----------|----------|------|
| If BOTH of the following conditions are true:<br><ul style="list-style-type: none"> <li>■ Data rate &gt; 10.3 Gbps.</li> <li>■ DFE is used.</li> </ul>  | All                               | 1.05                               | 3.0      | 1.5      | V    |
| If ANY of the following conditions are true <sup>(1)</sup> :<br><ul style="list-style-type: none"> <li>■ ATX PLL is used.</li> <li>■ Data rate &gt; 6.5Gbps.</li> <li>■ DFE (data rate ≤ 10.3 Gbps), AEQ, or EyeQ feature is used.</li> </ul> | All                               | 1.0                                |          |          |      |
| If ALL of the following conditions are true:<br><ul style="list-style-type: none"> <li>■ ATX PLL is not used.</li> <li>■ Data rate ≤ 6.5Gbps.</li> <li>■ DFE, AEQ, and EyeQ are not used.</li> </ul>  | C1, C2, I2, and I3YY              | 0.90                               | 2.5      |          |      |
|   | C2L, C3, C4, I2L, I3, I3L, and I4 | 0.85                               | 2.5      |          |      |

**Notes to Table 8:**

- (1) Choose this power supply voltage requirement option if you plan to upgrade your design later with any of the listed conditions.
- (2) If the VCCR\_GXB and VCCT\_GXB supplies are set to 1.0 V or 1.05 V, they cannot be shared with the VCC core supply. If the VCCR\_GXB and VCCT\_GXB are set to either 0.90 V or 0.85 V, they can be shared with the VCC core supply.

## DC Characteristics

This section lists the supply current, I/O pin leakage current, input pin capacitance, on-chip termination tolerance, and hot socketing specifications.

### Supply Current

Supply current is the current drawn from the respective power rails used for power budgeting. Use the Excel-based Early Power Estimator (EPE) to get supply current estimates for your design because these currents vary greatly with the resources you use.



For more information about power estimation tools, refer to the *PowerPlay Early Power Estimator User Guide* and the *PowerPlay Power Analysis* chapter in the *Quartus II Handbook*.

-  You typically use the interactive Excel-based Early Power Estimator before designing the FPGA to get a magnitude estimate of the device power. The Quartus II PowerPlay Power Analyzer provides better quality estimates based on the specifics of the design after you complete place-and-route. The PowerPlay Power Analyzer can apply a combination of user-entered, simulation-derived, and estimated signal activities that, when combined with detailed circuit models, yields very accurate power estimates.
-  For more information about power estimation tools, refer to the *PowerPlay Early Power Estimator User Guide* and the *PowerPlay Power Analysis* chapter in the *Quartus II Handbook*.

**Table 23. Transceiver Specifications for Stratix V GX and GS Devices <sup>(1)</sup> (Part 3 of 7)**

| Symbol/<br>Description  | Conditions   | Transceiver Speed<br>Grade 1                         |     |       | Transceiver Speed<br>Grade 2 |     |       | Transceiver Speed<br>Grade 3 |     |                          | Unit |
|---|--|--|-----|-------|------------------------------|-----|-------|------------------------------|-----|--------------------------|------|
|   |  | Min  | Typ | Max   | Min                          | Typ | Max   | Min                          | Typ | Max                      |      |
| Reconfiguration clock<br>( <code>mgmt_clk_clk</code> )<br>frequency   | —  | 100  | —   | 125   | 100                          | —   | 125   | 100                          | —   | 125                      | MHz  |
| <b>Receiver</b>   |  |  |     |       |                              |     |       |                              |     |                          |      |
| Supported I/O Standards   | —  | 1.4-V PCML, 1.5-V PCML, 2.5-V PCML, LVPECL, and LVDS |     |       |                              |     |       |                              |     |                          |      |
| Data rate<br>(Standard PCS)<br>(9), (23)  | —  | 600  | —   | 12200 | 600                          | —   | 12200 | 600                          | —   | 8500/<br>10312.5<br>(24) | Mbps |
| Data rate<br>(10G PCS) (9), (23)  | —  | 600  | —   | 14100 | 600                          | —   | 12500 | 600                          | —   | 8500/<br>10312.5<br>(24) | Mbps |
| Absolute $V_{MAX}$ for<br>a receiver pin <sup>(5)</sup>   | —  | —  | —   | 1.2   | —                            | —   | 1.2   | —                            | —   | 1.2                      | V    |
| Absolute $V_{MIN}$ for<br>a receiver pin  | —  | −0.4   | —   | —     | −0.4                         | —   | —     | −0.4                         | —   | —                        | V    |
| Maximum peak-<br>to-peak<br>differential input<br>voltage $V_{ID}$ (diff p-<br>p) before device<br>configuration <sup>(22)</sup>          | —  | —  | —   | 1.6   | —                            | —   | 1.6   | —                            | —   | 1.6                      | V    |
| Maximum peak-<br>to-peak<br>differential input<br>voltage $V_{ID}$ (diff p-<br>p) after device<br>configuration <sup>(18)</sup> ,<br>(22) | $V_{CCR\_GXB} =$<br>1.0 V/1.05 V<br>( $V_{ICM} =$<br>0.70 V) | —  | —   | 2.0   | —                            | —   | 2.0   | —                            | —   | 2.0                      | V    |
|   | $V_{CCR\_GXB} =$<br>0.90 V<br>( $V_{ICM} = 0.6$ V)           | —  | —   | 2.4   | —                            | —   | 2.4   | —                            | —   | 2.4                      | V    |
|   | $V_{CCR\_GXB} =$<br>0.85 V<br>( $V_{ICM} = 0.6$ V)           | —  | —   | 2.4   | —                            | —   | 2.4   | —                            | —   | 2.4                      | V    |
| Minimum<br>differential eye<br>opening at<br>receiver serial<br>input pins <sup>(6)</sup> , (22),<br>(27)                                 | —  | 85   | —   | —     | 85                           | —   | —     | 85                           | —   | —                        | mV   |

**Table 23. Transceiver Specifications for Stratix V GX and GS Devices <sup>(1)</sup> (Part 6 of 7)**

| Symbol/<br>Description  | Conditions                                   | Transceiver Speed<br>Grade 1 |     |                               | Transceiver Speed<br>Grade 2 |     |                               | Transceiver Speed<br>Grade 3 |     |                                     | Unit |
|---|--|------------------------------|-----|-------------------------------|------------------------------|-----|-------------------------------|------------------------------|-----|-------------------------------------|------|
|   |  | Min                          | Typ | Max                           | Min                          | Typ | Max                           | Min                          | Typ | Max                                 |      |
| Inter-transceiver<br>block transmitter<br>channel-to-<br>channel skew | xN PMA<br>bonded mode                        | —                            | —   | 500                           | —                            | —   | 500                           | —                            | —   | 500                                 | ps   |
| <b>CMU PLL</b>  |  |                              |     |                               |                              |     |                               |                              |     |                                     |      |
| Supported Data<br>Range   | —  | 600                          | —   | 12500                         | 600                          | —   | 12500                         | 600                          | —   | 8500/<br>10312.5<br><sup>(24)</sup> | Mbps |
| t <sub>pll_powerdown</sub> <sup>(15)</sup>                            | —  | 1                            | —   | —                             | 1                            | —   | —                             | 1                            | —   | —                                   | μs   |
| t <sub>pll_lock</sub> <sup>(16)</sup>                                 | —  | —                            | —   | 10                            | —                            | —   | 10                            | —                            | —   | 10                                  | μs   |
| <b>ATX PLL</b>  |  |                              |     |                               |                              |     |                               |                              |     |                                     |      |
| Supported Data<br>Rate Range  | VCO<br>post-divider<br>L=2                   | 8000                         | —   | 14100                         | 8000                         | —   | 12500                         | 8000                         | —   | 8500/<br>10312.5<br><sup>(24)</sup> | Mbps |
|   | L=4  | 4000                         | —   | 7050                          | 4000                         | —   | 6600                          | 4000                         | —   | 6600                                | Mbps |
|   | L=8  | 2000                         | —   | 3525                          | 2000                         | —   | 3300                          | 2000                         | —   | 3300                                | Mbps |
|   | L=8,<br>Local/Central<br>Clock Divider<br>=2 | 1000                         | —   | 1762.5                        | 1000                         | —   | 1762.5                        | 1000                         | —   | 1762.5                              | Mbps |
| t <sub>pll_powerdown</sub> <sup>(15)</sup>                            | —  | 1                            | —   | —                             | 1                            | —   | —                             | 1                            | —   | —                                   | μs   |
| t <sub>pll_lock</sub> <sup>(16)</sup>                                 | —  | —                            | —   | 10                            | —                            | —   | 10                            | —                            | —   | 10                                  | μs   |
| <b>fPLL</b>   |  |                              |     |                               |                              |     |                               |                              |     |                                     |      |
| Supported Data<br>Range   | —  | 600                          | —   | 3250/<br>3125 <sup>(25)</sup> | 600                          | —   | 3250/<br>3125 <sup>(25)</sup> | 600                          | —   | 3250/<br>3125 <sup>(25)</sup>       | Mbps |
| t <sub>pll_powerdown</sub> <sup>(15)</sup>                            | —  | 1                            | —   | —                             | 1                            | —   | —                             | 1                            | —   | —                                   | μs   |

**Table 23. Transceiver Specifications for Stratix V GX and GS Devices <sup>(1)</sup> (Part 7 of 7)**

| Symbol/<br>Description | Conditions | Transceiver Speed<br>Grade 1 |     |     | Transceiver Speed<br>Grade 2 |     |     | Transceiver Speed<br>Grade 3 |     |     | Unit |
|------------------------|------------|------------------------------|-----|-----|------------------------------|-----|-----|------------------------------|-----|-----|------|
|                        |            | Min                          | Typ | Max | Min                          | Typ | Max | Min                          | Typ | Max |      |
| $t_{pll\_lock}^{(16)}$ | —          | —                            | —   | 10  | —                            | —   | 10  | —                            | —   | 10  | μs   |

**Notes to Table 23:**

- (1) Speed grades shown in Table 23 refer to the PMA Speed Grade in the device ordering code. The maximum data rate could be restricted by the Core/PCS speed grade. Contact your Altera Sales Representative for the maximum data rate specifications in each speed grade combination offered. For more information about device ordering codes, refer to the *Stratix V Device Overview*.
- (2) The reference clock common mode voltage is equal to the  $V_{CCR\_GXB}$  power supply level.
- (3) This supply must be connected to 1.0 V if the transceiver is configured at a data rate > 6.5 Gbps, and to 1.05 V if configured at a data rate > 10.3 Gbps when DFE is used. For data rates up to 6.5 Gbps, you can connect this supply to 0.85 V.
- (4) This supply follows  $V_{CCR\_GXB}$ .
- (5) The device cannot tolerate prolonged operation at this absolute maximum.
- (6) The differential eye opening specification at the receiver input pins assumes that **Receiver Equalization** is disabled. If you enable **Receiver Equalization**, the receiver circuitry can tolerate a lower minimum eye opening, depending on the equalization level.
- (7) The Quartus II software automatically selects the appropriate slew rate depending on the configured data rate or functional mode.
- (8) The input reference clock frequency options depend on the data rate and the device speed grade.
- (9) The line data rate may be limited by PCS-FPGA interface speed grade.
- (10) Refer to Figure 1 for the GX channel AC gain curves. The total effective AC gain is the AC gain minus the DC gain.
- (11)  $t_{LTR}$  is the time required for the receive CDR to lock to the input reference clock frequency after coming out of reset.
- (12)  $t_{LTD}$  is time required for the receiver CDR to start recovering valid data after the rx\_is\_lockedtodata signal goes high.
- (13)  $t_{LTD\_manual}$  is the time required for the receiver CDR to start recovering valid data after the rx\_is\_lockedtodata signal goes high when the CDR is functioning in the manual mode.
- (14)  $t_{LTR\_LTD\_manual}$  is the time the receiver CDR must be kept in lock to reference (LTR) mode after the rx\_is\_lockedtoref signal goes high when the CDR is functioning in the manual mode.
- (15)  $t_{pll\_powerdown}$  is the PLL powerdown minimum pulse width.
- (16)  $t_{pll\_lock}$  is the time required for the transmitter CMU/ATX PLL to lock to the input reference clock frequency after coming out of reset.
- (17) To calculate the REFCLK rms phase jitter requirement for PCIe at reference clock frequencies other than 100 MHz, use the following formula: REFCLK rms phase jitter at f(MHz) = REFCLK rms phase jitter at 100 MHz  $\times$  100/f.
- (18) The maximum peak to peak differential input voltage  $V_{ID}$  after device configuration is equal to  $4 \times (\text{absolute } V_{MAX} \text{ for receiver pin} - V_{ICM})$ .
- (19) For ES devices,  $R_{REF}$  is  $2000 \Omega \pm 1\%$ .
- (20) To calculate the REFCLK phase noise requirement at frequencies other than 622 MHz, use the following formula: REFCLK phase noise at f(MHz) = REFCLK phase noise at 622 MHz +  $20 \times \log(f/622)$ .
- (21) SFP/+ optical modules require the host interface to have RD+/- differentially terminated with  $100 \Omega$ . The internal OCT feature is available after the Stratix V FPGA configuration is completed. Altera recommends that FPGA configuration is completed before inserting the optical module. Otherwise, minimize unnecessary removal and insertion with unconfigured devices.
- (22) Refer to Figure 2.
- (23) For oversampling designs to support data rates less than the minimum specification, the CDR needs to be in LTR mode only.
- (24) I3YY devices can achieve data rates up to 10.3125 Gbps.
- (25) When you use fPLL as a TXPLL of the transceiver.
- (26) REFCLK performance requires to meet transmitter REFCLK phase noise specification.
- (27) Minimum eye opening of 85 mV is only for the unstressed input eye condition.

Table 25 shows the approximate maximum data rate using the standard PCS.

**Table 25. Stratix V Standard PCS Approximate Maximum Date Rate <sup>(1)</sup>, <sup>(3)</sup>**

| Mode <sup>(2)</sup> | Transceiver Speed Grade | PMA Width                             | 20      | 20      | 16      | 16      | 10  | 10  | 8    | 8    |
|---------------------|-------------------------|---------------------------------------|---------|---------|---------|---------|-----|-----|------|------|
|                     |                         | PCS/Core Width                        | 40      | 20      | 32      | 16      | 20  | 10  | 16   | 8    |
| FIFO                | 1                       | C1, C2, C2L, I2, I2L core speed grade | 12.2    | 11.4    | 9.76    | 9.12    | 6.5 | 5.8 | 5.2  | 4.72 |
|                     | 2                       | C1, C2, C2L, I2, I2L core speed grade | 12.2    | 11.4    | 9.76    | 9.12    | 6.5 | 5.8 | 5.2  | 4.72 |
|                     |                         | C3, I3, I3L core speed grade          | 9.8     | 9.0     | 7.84    | 7.2     | 5.3 | 4.7 | 4.24 | 3.76 |
|                     | 3                       | C1, C2, C2L, I2, I2L core speed grade | 8.5     | 8.5     | 8.5     | 8.5     | 6.5 | 5.8 | 5.2  | 4.72 |
|                     |                         | I3YY core speed grade                 | 10.3125 | 10.3125 | 7.84    | 7.2     | 5.3 | 4.7 | 4.24 | 3.76 |
|                     |                         | C3, I3, I3L core speed grade          | 8.5     | 8.5     | 7.84    | 7.2     | 5.3 | 4.7 | 4.24 | 3.76 |
|                     |                         | C4, I4 core speed grade               | 8.5     | 8.2     | 7.04    | 6.56    | 4.8 | 4.2 | 3.84 | 3.44 |
| Register            | 1                       | C1, C2, C2L, I2, I2L core speed grade | 12.2    | 11.4    | 9.76    | 9.12    | 6.1 | 5.7 | 4.88 | 4.56 |
|                     | 2                       | C1, C2, C2L, I2, I2L core speed grade | 12.2    | 11.4    | 9.76    | 9.12    | 6.1 | 5.7 | 4.88 | 4.56 |
|                     |                         | C3, I3, I3L core speed grade          | 9.8     | 9.0     | 7.92    | 7.2     | 4.9 | 4.5 | 3.96 | 3.6  |
|                     | 3                       | C1, C2, C2L, I2, I2L core speed grade | 10.3125 | 10.3125 | 10.3125 | 10.3125 | 6.1 | 5.7 | 4.88 | 4.56 |
|                     |                         | I3YY core speed grade                 | 10.3125 | 10.3125 | 7.92    | 7.2     | 4.9 | 4.5 | 3.96 | 3.6  |
|                     |                         | C3, I3, I3L core speed grade          | 8.5     | 8.5     | 7.92    | 7.2     | 4.9 | 4.5 | 3.96 | 3.6  |
|                     |                         | C4, I4 core speed grade               | 8.5     | 8.2     | 7.04    | 6.56    | 4.4 | 4.1 | 3.52 | 3.28 |

**Notes to Table 25:**

- (1) The maximum data rate is in Gbps.
- (2) The Phase Compensation FIFO can be configured in FIFO mode or register mode. In the FIFO mode, the pointers are not fixed, and the latency can vary. In the register mode the pointers are fixed for low latency.
- (3) The maximum data rate is also constrained by the transceiver speed grade. Refer to Table 1 for the transceiver speed grade.



Table 27 shows the  $V_{OD}$  settings for the GX channel.

**Table 27. Typical  $V_{OD}$  Setting for GX Channel, TX Termination = 100  $\Omega$  <sup>(2)</sup>**

| Symbol  | $V_{OD}$ Setting | $V_{OD}$ Value (mV) | $V_{OD}$ Setting | $V_{OD}$ Value (mV) |
|---|------------------|---------------------|------------------|---------------------|
| <b><math>V_{OD}</math> differential peak to peak typical <sup>(3)</sup></b> | 0 <sup>(1)</sup> | 0                   | 32               | 640                 |
|   | 1 <sup>(1)</sup> | 20                  | 33               | 660                 |
|   | 2 <sup>(1)</sup> | 40                  | 34               | 680                 |
|   | 3 <sup>(1)</sup> | 60                  | 35               | 700                 |
|   | 4 <sup>(1)</sup> | 80                  | 36               | 720                 |
|   | 5 <sup>(1)</sup> | 100                 | 37               | 740                 |
|   | 6                | 120                 | 38               | 760                 |
|   | 7                | 140                 | 39               | 780                 |
|   | 8                | 160                 | 40               | 800                 |
|   | 9                | 180                 | 41               | 820                 |
|   | 10               | 200                 | 42               | 840                 |
|   | 11               | 220                 | 43               | 860                 |
|   | 12               | 240                 | 44               | 880                 |
|   | 13               | 260                 | 45               | 900                 |
|   | 14               | 280                 | 46               | 920                 |
|   | 15               | 300                 | 47               | 940                 |
|   | 16               | 320                 | 48               | 960                 |
|   | 17               | 340                 | 49               | 980                 |
|   | 18               | 360                 | 50               | 1000                |
|   | 19               | 380                 | 51               | 1020                |
|   | 20               | 400                 | 52               | 1040                |
|   | 21               | 420                 | 53               | 1060                |
|   | 22               | 440                 | 54               | 1080                |
|   | 23               | 460                 | 55               | 1100                |
|   | 24               | 480                 | 56               | 1120                |
|   | 25               | 500                 | 57               | 1140                |
|   | 26               | 520                 | 58               | 1160                |
|   | 27               | 540                 | 59               | 1180                |
|   | 28               | 560                 | 60               | 1200                |
|   | 29               | 580                 | 61               | 1220                |
|   | 30               | 600                 | 62               | 1240                |
|   | 31               | 620                 | 63               | 1260                |

**Note to Table 27:**

- (1) If TX termination resistance = 100 $\Omega$ , this VOD setting is illegal.
- (2) The tolerance is +/-20% for all VOD settings except for settings 2 and below.
- (3) Refer to Figure 2.

Table 29 shows the  $V_{OD}$  settings for the GT channel.

**Table 29. Typical  $V_{OD}$  Setting for GT Channel, TX Termination = 100  $\Omega$**

| Symbol  | $V_{OD}$ Setting | $V_{OD}$ Value (mV) |
|---|------------------|---------------------|
| $V_{OD}$ differential peak to peak typical <sup>(1)</sup> | 0                | 0                   |
|   | 1                | 200                 |
|   | 2                | 400                 |
|   | 3                | 600                 |
|   | 4                | 800                 |
|   | 5                | 1000                |

**Note:**

(1) Refer to Figure 4.

Figure 4 shows the differential transmitter output waveform.

**Figure 4. Differential Transmitter/Receiver Output/Input Waveform**



Figure 5 shows the Stratix V AC gain curves for GT channels.

**Figure 5. AC Gain Curves for GT Channels**

Figure 6 shows the Stratix V DC gain curves for GT channels.

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**Figure 6. DC Gain Curves for GT Channels**

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**Transceiver Characterization**

This section summarizes the Stratix V transceiver characterization results for compliance with the following protocols:

- Interlaken
- 40G (XLAUI)/100G (CAUI)
- 10GBase-KR
- QSGMII
- XAUI
- SFI
- Gigabit Ethernet (Gbe / GIGE)
- SPAUI
- Serial Rapid IO (SRIO)
- CPRI
- OBSAI
- Hyper Transport (HT)
- SATA
- SAS
- CEI

**Table 36. High-Speed I/O Specifications for Stratix V Devices <sup>(1), (2)</sup> (Part 3 of 4)**

| Symbol   | Conditions  | C1             |     |                | C2, C2L, I2, I2L |     |                | C3, I3, I3L, I3YY |     |                | C4, I4         |     |                | Unit |
|--|---|----------------|-----|----------------|------------------|-----|----------------|-------------------|-----|----------------|----------------|-----|----------------|------|
|  |   | Min            | Typ | Max            | Min              | Typ | Max            | Min               | Typ | Max            | Min            | Typ | Max            |      |
| $t_{DUTY}$   | Transmitter output clock duty cycle for both True and Emulated Differential I/O Standards | 45             | 50  | 55             | 45               | 50  | 55             | 45                | 50  | 55             | 45             | 50  | 55             | %    |
| $t_{RISE}$ & $t_{FALL}$                                    | True Differential I/O Standards   | —              | —   | 160            | —                | —   | 160            | —                 | —   | 200            | —              | —   | 200            | ps   |
|  | Emulated Differential I/O Standards with three external output resistor networks          | —              | —   | 250            | —                | —   | 250            | —                 | —   | 250            | —              | —   | 300            | ps   |
| TCCS   | True Differential I/O Standards   | —              | —   | 150            | —                | —   | 150            | —                 | —   | 150            | —              | —   | 150            | ps   |
|  | Emulated Differential I/O Standards   | —              | —   | 300            | —                | —   | 300            | —                 | —   | 300            | —              | —   | 300            | ps   |
| <b>Receiver</b>  |   |                |     |                |                  |     |                |                   |     |                |                |     |                |      |
| True Differential I/O Standards - $f_{HSDRDP}$ (data rate) | SERDES factor J = 3 to 10 <sup>(11), (12), (13), (14), (15), (16)</sup>                   | 150            | —   | 1434           | 150              | —   | 1434           | 150               | —   | 1250           | 150            | —   | 1050           | Mbps |
|  | SERDES factor J $\geq 4$  | 150            | —   | 1600           | 150              | —   | 1600           | 150               | —   | 1600           | 150            | —   | 1250           | Mbps |
|  | LVDS RX with DPA <sup>(12), (14), (15), (16)</sup>  | 150            | —   | 1600           | 150              | —   | 1600           | 150               | —   | 1600           | 150            | —   | 1250           | Mbps |
|  | SERDES factor J = 2, uses DDR Registers   | <sup>(6)</sup> | —   | <sup>(7)</sup> | <sup>(6)</sup>   | —   | <sup>(7)</sup> | <sup>(6)</sup>    | —   | <sup>(7)</sup> | <sup>(6)</sup> | —   | <sup>(7)</sup> | Mbps |
|  | SERDES factor J = 1, uses SDR Register  | <sup>(6)</sup> | —   | <sup>(7)</sup> | <sup>(6)</sup>   | —   | <sup>(7)</sup> | <sup>(6)</sup>    | —   | <sup>(7)</sup> | <sup>(6)</sup> | —   | <sup>(7)</sup> | Mbps |

Figure 7 shows the dynamic phase alignment (DPA) lock time specifications with the DPA PLL calibration option enabled.

**Figure 7. DPA Lock Time Specification with DPA PLL Calibration Enabled**



Table 37 lists the DPA lock time specifications for Stratix V devices.

**Table 37. DPA Lock Time Specifications for Stratix V GX Devices Only <sup>(1), (2), (3)</sup>**

| Standard           | Training Pattern     | Number of Data Transitions in One Repetition of the Training Pattern | Number of Repetitions per 256 Data Transitions <sup>(4)</sup> | Maximum              |
|--------------------|----------------------|--|---|----------------------|
| SPI-4              | 00000000001111111111 | 2  | 128   | 640 data transitions |
| Parallel Rapid I/O | 00001111             | 2  | 128   | 640 data transitions |
|                    | 10010000             | 4  | 64  | 640 data transitions |
| Miscellaneous      | 10101010             | 8  | 32  | 640 data transitions |
|                    | 01010101             | 8  | 32  | 640 data transitions |

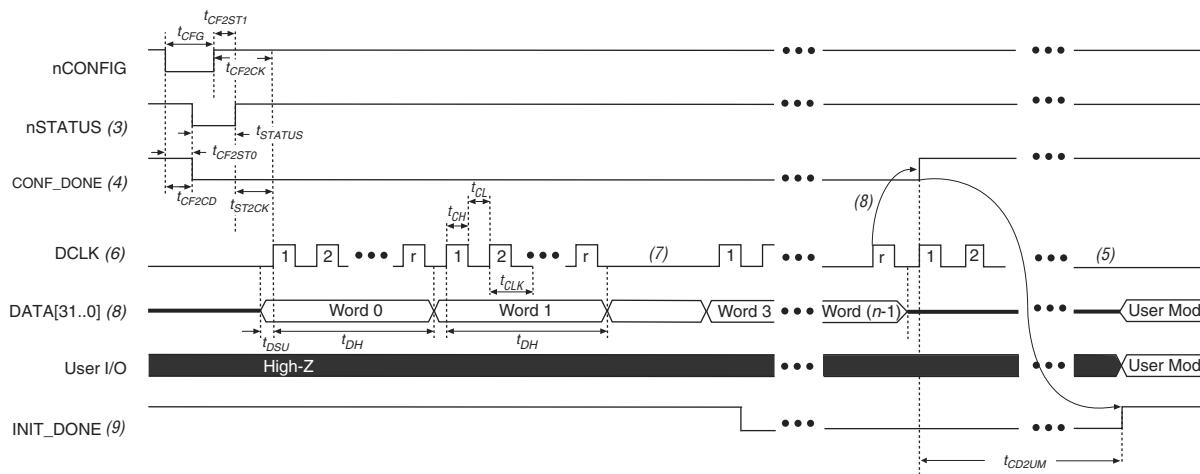
**Notes to Table 37:**

- (1) The DPA lock time is for one channel.
- (2) One data transition is defined as a 0-to-1 or 1-to-0 transition.
- (3) The DPA lock time stated in this table applies to both commercial and industrial grade.
- (4) This is the number of repetitions for the stated training pattern to achieve the 256 data transitions.

Figure 8 shows the LVDS soft-clock data recovery (CDR)/DPA sinusoidal jitter tolerance specification for a data rate  $\geq 1.25$  Gbps. Table 38 lists the LVDS soft-CDR/DPA sinusoidal jitter tolerance specification for a data rate  $\geq 1.25$  Gbps.

**Figure 8. LVDS Soft-CDR/DPA Sinusoidal Jitter Tolerance Specification for a Data Rate  $\geq 1.25$  Gbps**



**Figure 13. FPP Configuration Timing Waveform When the DCLK-to-DATA[] Ratio is >1 (1), (2)****Notes to Figure 13:**

- (1) Use this timing waveform and parameters when the DCLK-to-DATA[] ratio is >1. To find out the DCLK-to-DATA[] ratio for your system, refer to Table 49 on page 55.
- (2) The beginning of this waveform shows the device in user mode. In user mode, nCONFIG, nSTATUS, and CONF\_DONE are at logic high levels. When nCONFIG is pulled low, a reconfiguration cycle begins.
- (3) After power-up, the Stratix V device holds nSTATUS low for the time as specified by the POR delay.
- (4) After power-up, before and during configuration, CONF\_DONE is low.
- (5) Do not leave DCLK floating after configuration. You can drive it high or low, whichever is more convenient.
- (6) "r" denotes the DCLK-to-DATA[] ratio. For the DCLK-to-DATA[] ratio based on the decompression and the design security feature enable settings, refer to Table 49 on page 55.
- (7) If needed, pause DCLK by holding it low. When DCLK restarts, the external host must provide data on the DATA[31..0] pins prior to sending the first DCLK rising edge.
- (8) To ensure a successful configuration, send the entire configuration data to the Stratix V device. CONF\_DONE is released high after the Stratix V device receives all the configuration data successfully. After CONF\_DONE goes high, send two additional falling edges on DCLK to begin initialization and enter user mode.
- (9) After the option bit to enable the INIT\_DONE pin is configured into the device, the INIT\_DONE goes low.

## Active Serial Configuration Timing

Table 52 lists the DCLK frequency specification in the AS configuration scheme.

**Table 52. DCLK Frequency Specification in the AS Configuration Scheme <sup>(1), (2)</sup>**

| Minimum | Typical | Maximum | Unit |
|---------|---------|---------|------|
| 5.3     | 7.9     | 12.5    | MHz  |
| 10.6    | 15.7    | 25.0    | MHz  |
| 21.3    | 31.4    | 50.0    | MHz  |
| 42.6    | 62.9    | 100.0   | MHz  |

**Notes to Table 52:**

- (1) This applies to the DCLK frequency specification when using the internal oscillator as the configuration clock source.
- (2) The AS multi-device configuration scheme does not support DCLK frequency of 100 MHz.

Figure 14 shows the single-device configuration setup for an AS ×1 mode.

**Figure 14. AS Configuration Timing**



**Notes to Figure 14:**

- (1) If you are using AS ×4 mode, this signal represents the AS\_DATA [3 : 0] and EPCQ sends in 4-bits of data for each DCLK cycle.
- (2) The initialization clock can be from internal oscillator or CLKUSR pin.
- (3) After the option bit to enable the INIT\_DONE pin is configured into the device, the INIT\_DONE goes low.

Table 53 lists the timing parameters for AS ×1 and AS ×4 configurations in Stratix V devices.

**Table 53. AS Timing Parameters for AS ×1 and AS ×4 Configurations in Stratix V Devices <sup>(1), (2)</sup> (Part 1 of 2)**

| Symbol          | Parameter                                   | Minimum | Maximum | Units |
|-----------------|---|---------|---------|-------|
| t <sub>CO</sub> | DCLK falling edge to AS_DATA0/ASDO output   | —       | 2       | ns    |
| t <sub>SU</sub> | Data setup time before falling edge on DCLK | 1.5     | —       | ns    |
| t <sub>H</sub>  | Data hold time after falling edge on DCLK   | 0       | —       | ns    |



**Table 53. AS Timing Parameters for AS ×1 and AS ×4 Configurations in Stratix V Devices <sup>(1), (2)</sup> (Part 2 of 2)**

| Symbol       | Parameter   | Minimum  | Maximum | Units |
|--------------|---|--|---------|-------|
| $t_{CD2UM}$  | CONF_DONE high to user mode <sup>(3)</sup>        | 175  | 437     | μs    |
| $t_{CD2CU}$  | CONF_DONE high to CLKUSR enabled                  | 4 × maximum DCLK period                          | —       | —     |
| $t_{CD2UMC}$ | CONF_DONE high to user mode with CLKUSR option on | $t_{CD2CU} + (8576 \times \text{CLKUSR period})$ | —       | —     |

**Notes to Table 53:**

- (1) The minimum and maximum numbers apply only if you choose the internal oscillator as the clock source for initializing the device.
- (2)  $t_{CF2CD}$ ,  $t_{CF2ST0}$ ,  $t_{CFG}$ ,  $t_{STATUS}$ , and  $t_{CF2ST1}$  timing parameters are identical to the timing parameters for PS mode listed in Table 54 on page 63.
- (3) To enable the CLKUSR pin as the initialization clock source and to obtain the maximum frequency specification on this pin, refer to the Initialization section of the “Configuration, Design Security, and Remote System Upgrades in Stratix V Devices” chapter.

## Passive Serial Configuration Timing

Figure 15 shows the timing waveform for a passive serial (PS) configuration when using a MAX II device, MAX V device, or microprocessor as an external host.

**Figure 15. PS Configuration Timing Waveform <sup>(1)</sup>****Notes to Figure 15:**

- (1) The beginning of this waveform shows the device in user mode. In user mode, nCONFIG, nSTATUS, and CONF\_DONE are at logic high levels. When nCONFIG is pulled low, a reconfiguration cycle begins.
- (2) After power-up, the Stratix V device holds nSTATUS low for the time of the POR delay.
- (3) After power-up, before and during configuration, CONF\_DONE is low.
- (4) Do not leave DCLK floating after configuration. You can drive it high or low, whichever is more convenient.
- (5) DATA0 is available as a user I/O pin after configuration. The state of this pin depends on the dual-purpose pin settings in the **Device and Pins Option**.
- (6) To ensure a successful configuration, send the entire configuration data to the Stratix V device. CONF\_DONE is released high after the Stratix V device receives all the configuration data successfully. After CONF\_DONE goes high, send two additional falling edges on DCLK to begin initialization and enter user mode.
- (7) After the option bit to enable the INIT\_DONE pin is configured into the device, the INIT\_DONE goes low.

**Table 58. IOE Programmable Delay for Stratix V Devices (Part 2 of 2)**

| Parameter<br>(1) | Available<br>Settings | Min<br>Offset<br>(2) | Fast Model |            | Slow Model |       |       |       |       |             |       |      |
|------------------|-----------------------|----------------------|------------|------------|------------|-------|-------|-------|-------|-------------|-------|------|
|                  |                       |                      | Industrial | Commercial | C1         | C2    | C3    | C4    | I2    | I3,<br>I3YY | I4    | Unit |
| D3               | 8                     | 0                    | 1.587      | 1.699      | 2.793      | 2.793 | 2.992 | 3.192 | 2.811 | 3.047       | 3.257 | ns   |
| D4               | 64                    | 0                    | 0.464      | 0.492      | 0.838      | 0.838 | 0.924 | 1.011 | 0.843 | 0.920       | 1.006 | ns   |
| D5               | 64                    | 0                    | 0.464      | 0.493      | 0.838      | 0.838 | 0.924 | 1.011 | 0.844 | 0.921       | 1.006 | ns   |
| D6               | 32                    | 0                    | 0.229      | 0.244      | 0.415      | 0.415 | 0.458 | 0.503 | 0.418 | 0.456       | 0.499 | ns   |

**Notes to Table 58:**

- (1) You can set this value in the Quartus II software by selecting **D1**, **D2**, **D3**, **D5**, and **D6** in the **Assignment Name** column of **Assignment Editor**.
- (2) Minimum offset does not include the intrinsic delay.

## Programmable Output Buffer Delay

Table 59 lists the delay chain settings that control the rising and falling edge delays of the output buffer. The default delay is 0 ps.

**Table 59. Programmable Output Buffer Delay for Stratix V Devices (1)**

| Symbol              | Parameter                        | Typical     | Unit |
|---------------------|----------------------------------|-------------|------|
| D <sub>OUTBUF</sub> | Rising and/or falling edge delay | 0 (default) | ps   |
|                     |                                  | 25          | ps   |
|                     |                                  | 50          | ps   |
|                     |                                  | 75          | ps   |

**Note to Table 59:**

- (1) You can set the programmable output buffer delay in the Quartus II software by setting the **Output Buffer Delay Control** assignment to either positive, negative, or both edges, with the specific values stated here (in ps) for the **Output Buffer Delay** assignment.

## Glossary

Table 60 lists the glossary for this chapter.

**Table 60. Glossary (Part 1 of 4)**

| Letter | Subject              | Definitions   |
|--------|----------------------|---|
| A      | —                    | —   |
| B      |                      |   |
| C      |                      |   |
| D      | —                    | —   |
| E      | —                    | —   |
| F      | f <sub>HCLK</sub>    | Left and right PLL input clock frequency.   |
|        | f <sub>HSDR</sub>    | High-speed I/O block—Maximum and minimum <b>LVDS</b> data transfer rate (f <sub>HSDR</sub> = 1/TUI), non-DPA. |
|        | f <sub>HSDRDPA</sub> | High-speed I/O block—Maximum and minimum <b>LVDS</b> data transfer rate (f <sub>HSDRDPA</sub> = 1/TUI), DPA.  |

Table 60. Glossary (Part 3 of 4)

| Letter | Subject                                      | Definitions  |
|--------|--|--|
| S      | SW (sampling window)                         | <p>Timing Diagram—the period of time during which the data must be valid in order to capture it correctly. The setup and hold times determine the ideal strobe position within the sampling window, as shown:</p>    |
|        | Single-ended voltage referenced I/O standard | <p>The JEDEC standard for <b>SSTL</b> and <b>HSTL</b> I/O defines both the AC and DC input signal values. The AC values indicate the voltage levels at which the receiver must meet its timing specifications. The DC values indicate the voltage levels at which the final logic state of the receiver is unambiguously defined. After the receiver input has crossed the AC value, the receiver changes to the new logic state.</p> <p>The new logic state is then maintained as long as the input stays beyond the DC threshold. This approach is intended to provide predictable receiver timing in the presence of input waveform ringing:</p> <p><i>Single-Ended Voltage Referenced I/O Standard</i></p>  |
| T      | $t_c$  | High-speed receiver and transmitter input and output clock period.   |
|        | TCCS (channel-to-channel-skew)               | The timing difference between the fastest and slowest output edges, including $t_{CO}$ variation and clock skew, across channels driven by the same PLL. The clock is included in the TCCS measurement (refer to the <i>Timing Diagram</i> figure under <b>SW</b> in this table).  |
|        | $t_{DUTY}$                                   | <p>High-speed I/O block—Duty cycle on the high-speed transmitter output clock.</p> <p><b>Timing Unit Interval (TUI)</b></p> <p>The timing budget allowed for skew, propagation delays, and the data sampling window. (TUI = <math>1/(\text{receiver input clock frequency multiplication factor}) = t_c/w</math>)</p>  |
|        | $t_{FALL}$                                   | Signal high-to-low transition time (80-20%)  |
|        | $t_{INCCJ}$                                  | Cycle-to-cycle jitter tolerance on the PLL clock input.  |
|        | $t_{OUTPJ\_IO}$                              | Period jitter on the general purpose I/O driven by a PLL.  |
|        | $t_{OUTPJ\_DC}$                              | Period jitter on the dedicated clock output driven by a PLL.   |
|        | $t_{RISE}$                                   | Signal low-to-high transition time (20-80%)  |
| U      | —  | —  |

## Document Revision History

Table 61 lists the revision history for this chapter.

**Table 61. Document Revision History (Part 1 of 3)**

| Date          | Version | Changes   |
|---------------|---------|---|
| June 2018     | 3.9     | <ul style="list-style-type: none"> <li>Added the “Stratix V Device Overshoot Duration” figure.</li> </ul>   |
| April 2017    | 3.8     | <ul style="list-style-type: none"> <li>Added a footnote to the “High-Speed I/O Specifications for Stratix V Devices” table.</li> <li>Changed the minimum value for <math>t_{CD2UMC}</math> in the “PS Timing Parameters for Stratix V Devices” table.</li> <li>Changed the condition for <math>100\text{-}\Omega</math> <math>R_D</math> in the “OCT Without Calibration Resistance Tolerance Specifications for Stratix V Devices” table.</li> <li>Changed the minimum value for <math>t_{CD2UMC}</math> in the “AS Timing Parameters for AS ‘1 and AS ‘4 Configurations in Stratix V Devices” table</li> <li>Changed the minimum value for <math>t_{CD2UMC}</math> in the “FPP Timing Parameters for Stratix V Devices When the DCLK-to-DATA[] Ratio is &gt;1” table.</li> <li>Changed the minimum value for <math>t_{CD2UMC}</math> in the “FPP Timing Parameters for Stratix V Devices When the DCLK-to-DATA[] Ratio is &gt;1” table.</li> <li>Changed the minimum number of clock cycles value in the “Initialization Clock Source Option and the Maximum Frequency” table.</li> </ul> |
| June 2016     | 3.7     | <ul style="list-style-type: none"> <li>Added the <math>V_{ID}</math> minimum specification for LVPECL in the “Differential I/O Standard Specifications for Stratix V Devices” table</li> <li>Added the <math>I_{OUT}</math> specification to the “Absolute Maximum Ratings for Stratix V Devices” table.</li> </ul>   |
| December 2015 | 3.6     | <ul style="list-style-type: none"> <li>Added a footnote to the “High-Speed I/O Specifications for Stratix V Devices” table.</li> </ul>  |
| December 2015 | 3.5     | <ul style="list-style-type: none"> <li>Changed the transmitter, receiver, and ATX PLL data rate specifications in the “Transceiver Specifications for Stratix V GX and GS Devices” table.</li> <li>Changed the configuration .rbf sizes in the “Uncompressed .rbf Sizes for Stratix V Devices” table.</li> </ul>  |
| July 2015     | 3.4     | <ul style="list-style-type: none"> <li>Changed the data rate specification for transceiver speed grade 3 in the following tables:               <ul style="list-style-type: none"> <li>“Transceiver Specifications for Stratix V GX and GS Devices”</li> <li>“Stratix V Standard PCS Approximate Maximum Date Rate”</li> <li>“Stratix V 10G PCS Approximate Maximum Data Rate”</li> </ul> </li> <li>Changed the conditions for reference clock rise and fall time, and added a note to the “Transceiver Specifications for Stratix V GX and GS Devices” table.</li> <li>Added a note to the “Minimum differential eye opening at receiver serial input pins” specification in the “Transceiver Specifications for Stratix V GX and GS Devices” table.</li> <li>Changed the <math>t_{CO}</math> maximum value in the “AS Timing Parameters for AS ‘1 and AS ‘4 Configurations in Stratix V Devices” table.</li> <li>Removed the CDR ppm tolerance specification from the “Transceiver Specifications for Stratix V GX and GS Devices” table.</li> </ul>                                      |

