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Intel - 5SGXEBBR3H43I3N Datasheet



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Understanding <u>Embedded - FPGAs (Field</u> <u>Programmable Gate Array)</u>

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Obsolete
Number of LABs/CLBs	359200
Number of Logic Elements/Cells	952000
Total RAM Bits	53248000
Number of I/O	600
Number of Gates	-
Voltage - Supply	0.82V ~ 0.88V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	1760-BBGA, FCBGA
Supplier Device Package	1760-HBGA (45x45)
Purchase URL	https://www.e-xfl.com/product-detail/intel/5sgxebbr3h43i3n

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

								·	
Transceiver Speed		Core Speed Grade							
Grade	C1	C2, C2L	C3	C4	12, 12L	13, 13L	I 3YY	14	
3 GX channel—8.5 Gbps	_	Yes	Yes	Yes	_	Yes	Yes ⁽⁴⁾	Yes	

Table 1. Stratix V GX and GS Commercial and Industrial Speed Grade Offering ^{(1), (2), (3)} (Part 2 of 2)

Notes to Table 1:

(1) C = Commercial temperature grade; I = Industrial temperature grade.

(2) Lower number refers to faster speed grade.

(3) C2L, I2L, and I3L speed grades are for low-power devices.

(4) I3YY speed grades can achieve up to 10.3125 Gbps.

Table 2 lists the industrial and commercial speed grades for the Stratix V GT devices. **Table 2. Stratix V GT Commercial and Industrial Speed Grade Offering** ⁽¹⁾, ⁽²⁾

Transseiver Speed Grade	Core Speed Grade					
Transceiver Speeu draue	C1	C2	12	13		
2 GX channel—12.5 Gbps GT channel—28.05 Gbps	Yes	Yes	_	_		
3 GX channel—12.5 Gbps GT channel—25.78 Gbps	Yes	Yes	Yes	Yes		

Notes to Table 2:

(1) C = Commercial temperature grade; I = Industrial temperature grade.

(2) Lower number refers to faster speed grade.

Absolute Maximum Ratings

Absolute maximum ratings define the maximum operating conditions for Stratix V devices. The values are based on experiments conducted with the devices and theoretical modeling of breakdown and damage mechanisms. The functional operation of the device is not implied for these conditions.



Conditions other than those listed in Table 3 may cause permanent damage to the device. Additionally, device operation at the absolute maximum ratings for extended periods of time may have adverse effects on the device.

TANIC J. ANSULULC MAXIMUM NALINYS IVI SUALIX V DEVICES (FAIL I UI Z)	Table 3.	Absolute Maximum	Ratings	for Stratix \	/ Devices	(Part 1 of 2)
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Symbol	Description	Minimum	Maximum	Unit
V _{CC}	Power supply for core voltage and periphery circuitry	-0.5	1.35	V
V _{CCPT}	Power supply for programmable power technology	-0.5	1.8	V
V _{CCPGM}	Power supply for configuration pins	-0.5	3.9	V
V _{CC_AUX}	Auxiliary supply for the programmable power technology	-0.5	3.4	V
V _{CCBAT}	Battery back-up power supply for design security volatile key register	-0.5	3.9	V
V _{CCPD}	I/O pre-driver power supply	-0.5	3.9	V
V _{CCIO}	I/O power supply	-0.5	3.9	V

Table 5 lists the maximum allowed input overshoot voltage and the duration of the overshoot voltage as a percentage of device lifetime. The maximum allowed overshoot duration is specified as a percentage of high time over the lifetime of the device. A DC signal is equivalent to 100% of the duty cycle. For example, a signal that overshoots to 3.95 V can be at 3.95 V for only ~21% over the lifetime of the device; for a device lifetime of 10 years, the overshoot duration amounts to ~2 years.

Symbol	Description	Condition (V)	Overshoot Duration as % @ T _J = 100°C	Unit						
		3.8	100	%						
		3.85	64	%						
		3.9	36	%						
		3.95	21	%						
Vi (AC)	AC input voltage	4	12	%						
		4.05	7	%						
		4.1	4	%						
		4.15	2	%						
		4.2	1	%						

Table 5. Maximum Allowed Overshoot During Transitions

Figure 1. Stratix V Device Overshoot Duration



Symbol	Description	Condition	Min ⁽⁴⁾	Тур	Max ⁽⁴⁾	Unit
t _{RAMP}	Power supply ramp time	Standard POR	200 µs	_	100 ms	—
	Power supply ramp time	Fast POR	200 µs		4 ms	

Table 6. Recommended Operating Conditions for Stratix V Devices (Part 2 of 2)

Notes to Table 6:

(1) V_{CCPD} must be 2.5 V when V_{CCI0} is 2.5, 1.8, 1.5, 1.35, 1.25 or 1.2 V. V_{CCPD} must be 3.0 V when V_{CCI0} is 3.0 V.

(2) If you do not use the design security feature in Stratix V devices, connect V_{CCBAT} to a 1.2- to 3.0-V power supply. Stratix V power-on-reset (POR) circuitry monitors V_{CCBAT}. Stratix V devices will not exit POR if V_{CCBAT} stays at logic low.

(3) C2L and I2L can also be run at 0.90 V for legacy boards that were designed for the C2 and I2 speed grades.

(4) The power supply value describes the budget for the DC (static) power supply tolerance and does not include the dynamic tolerance requirements. Refer to the PDN tool for the additional budget for the dynamic tolerance requirements.

Table 7 lists the transceiver power supply recommended operating conditions for Stratix V GX, GS, and GT devices.

Table 7. Recommended Transceiver Power Supply Operating Conditions for Stratix V GX, GS, and GT Devices (Part 1 of 2)

Symbol	Description	Devices	Minimum ⁽⁴⁾	Typical	Maximum ⁽⁴⁾	Unit
V _{CCA GXBL}	Transceiver channel PLL power supply (left		2.85	3.0	3.15	V
(1), (3)	(1), (3) side)		2.375	2.5	2.625	v
V _{CCA_GXBR}	Transceiver channel PLL power supply (right	CV CS	2.85	3.0	3.15	V
(1), (3)	side)	ux, us	2.375	2.5	2.625	v
V _{CCA_GTBR}	Transceiver channel PLL power supply (right side)	GT	2.85	3.0	3.15	V
	Transceiver hard IP power supply (left side; C1, C2, I2, and I3YY speed grades)	GX, GS, GT	0.87	0.9	0.93	V
V _{CCHIP_L}	Transceiver hard IP power supply (left side; C2L, C3, C4, I2L, I3, I3L, and I4 speed grades)	GX, GS, GT	0.82	0.85	0.88	V
V _{CCHIP_R}	Transceiver hard IP power supply (right side; C1, C2, I2, and I3YY speed grades)	GX, GS, GT	0.87	0.9	0.93	V
	Transceiver hard IP power supply (right side; C2L, C3, C4, I2L, I3, I3L, and I4 speed grades)	GX, GS, GT	0.82	0.85	0.88	V
	Transceiver PCS power supply (left side; C1, C2, I2, and I3YY speed grades)	GX, GS, GT	0.87	0.9	0.93	V
V _{CCHSSI_L}	Transceiver PCS power supply (left side; C2L, C3, C4, I2L, I3, I3L, and I4 speed grades)	GX, GS, GT	0.82	0.85	0.88	V
	Transceiver PCS power supply (right side; C1, C2, I2, and I3YY speed grades)	GX, GS, GT	0.87	0.9	0.93	V
V _{CCHSSI_R}	Transceiver PCS power supply (right side; C2L, C3, C4, I2L, I3, I3L, and I4 speed grades)	GX, GS, GT	0.82	0.85	0.88	V
			0.82	0.85	0.88	
V _{CCR_GXBL}	Receiver analog nower supply (left side)		0.87	0.90	0.93	v
(2) _	Therefore analog power supply (left Slue)	un, uo, ui	0.97	1.0	1.03	v
			1.03	1.05	1.07	

Table 8 shows the transceiver power supply voltage requirements for various conditions.

Table 8. Transceiver Power Supply Voltage Requirements

Conditions	Core Speed Grade	VCCR_GXB & VCCT_GXB ⁽²⁾	VCCA_GXB	VCCH_GXB	Unit
If BOTH of the following conditions are true:	A11	1.05			
■ Data rate > 10.3 Gbps.	All	1.00			
 DFE is used. 					
If ANY of the following conditions are true ⁽¹⁾ :			3.0		
 ATX PLL is used. 					
■ Data rate > 6.5Gbps.	All	1.0			
■ DFE (data rate ≤ 10.3 Gbps), AEQ, or EyeQ feature is used.				1.5	V
If ALL of the following	C1, C2, I2, and I3YY	0.90	2.5		
 ATX PLL is not used. 					
■ Data rate \leq 6.5Gbps.	C2L, C3, C4, I2L, I3, I3L, and I4	0.85	2.5		
 DFE, AEQ, and EyeQ are not used. 					

Notes to Table 8:

(1) Choose this power supply voltage requirement option if you plan to upgrade your design later with any of the listed conditions.

(2) If the VCCR_GXB and VCCT_GXB supplies are set to 1.0 V or 1.05 V, they cannot be shared with the VCC core supply. If the VCCR_GXB and VCCT_GXB are set to either 0.90 V or 0.85 V, they can be shared with the VCC core supply.

DC Characteristics

This section lists the supply current, I/O pin leakage current, input pin capacitance, on-chip termination tolerance, and hot socketing specifications.

Supply Current

Supply current is the current drawn from the respective power rails used for power budgeting. Use the Excel-based Early Power Estimator (EPE) to get supply current estimates for your design because these currents vary greatly with the resources you use.

For more information about power estimation tools, refer to the *PowerPlay Early Power Estimator User Guide* and the *PowerPlay Power Analysis* chapter in the *Quartus II Handbook*.

1/0 Standard	V _{CCIO} (V)			V _{REF} (V)			V _π (V)		
i/O Stailualu	Min	Тур	Max	Min	Тур	Max	Min	Тур	Max
SSTL-2 Class I, II	2.375	2.5	2.625	0.49 * V _{CCIO}	0.5 * V _{CCIO}	0.51 * V _{CCIO}	V _{REF} – 0.04	V _{REF}	V _{REF} + 0.04
SSTL-18 Class I, II	1.71	1.8	1.89	0.833	0.9	0.969	V _{REF} – 0.04	V _{REF}	V _{REF} + 0.04
SSTL-15 Class I, II	1.425	1.5	1.575	0.49 * V _{CCIO}	0.5 * V _{CCIO}	0.51 * V _{CCIO}	0.49 * V _{CCIO}	0.5 * VCCIO	0.51 * V _{CCIO}
SSTL-135 Class I, II	1.283	1.35	1.418	0.49 * V _{CCIO}	0.5 * V _{CCIO}	0.51 * V _{CCIO}	0.49 * V _{CCIO}	0.5 * V _{CCIO}	0.51 * V _{CCIO}
SSTL-125 Class I, II	1.19	1.25	1.26	0.49 * V _{CCIO}	0.5 * V _{CCIO}	0.51 * V _{CCIO}	0.49 * V _{CCIO}	0.5 * VCCIO	0.51 * V _{CCIO}
SSTL-12 Class I, II	1.14	1.20	1.26	0.49 * V _{CCIO}	0.5 * V _{CCIO}	0.51 * V _{CCIO}	0.49 * V _{CCIO}	0.5 * VCCIO	0.51 * V _{CCIO}
HSTL-18 Class I, II	1.71	1.8	1.89	0.85	0.9	0.95	_	V _{CCI0} /2	_
HSTL-15 Class I, II	1.425	1.5	1.575	0.68	0.75	0.9	_	V _{CCI0} /2	_
HSTL-12 Class I, II	1.14	1.2	1.26	0.47 * V _{CCIO}	0.5 * V _{CCIO}	0.53 * V _{CCIO}	_	V _{CCI0} /2	_
HSUL-12	1.14	1.2	1.3	0.49 * V _{CCIO}	0.5 * V _{CCIO}	0.51 * V _{CCIO}	_	_	

Table 18. Single-Ended SSTL, HSTL, and HSUL I/O Reference Voltage Specifications for Stratix V Devi	ces
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Table 19.	Single-Ended SSTL	, HSTL, and HSUL I/	/O Standards Signal S	Specifications for	Stratix V Devices	(Part 1 of 2)
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1/0 Standard	V _{IL(DC)} (V)		V _{IH(DC)} (V)		V _{IL(AC)} (V)	V _{IH(AC)} (V)	V _{ol} (V)	V _{oh} (V)	I (mA)	I _{oh}
i/o Stanuaru	Min	Max	Min	Max	Max	Min	Max	Min	I _{ol} (IIIA)	(mÄ)
SSTL-2 Class I	-0.3	V _{REF} – 0.15	V _{REF} + 0.15	V _{CCI0} + 0.3	V _{REF} – 0.31	V _{REF} + 0.31	V _{TT} – 0.608	V _{TT} + 0.608	8.1	-8.1
SSTL-2 Class II	-0.3	V _{REF} – 0.15	V _{REF} + 0.15	V _{CCI0} + 0.3	V _{REF} – 0.31	V _{REF} + 0.31	V _{TT} – 0.81	V _{TT} + 0.81	16.2	-16.2
SSTL-18 Class I	-0.3	V _{REF} – 0.125	V _{REF} + 0.125	V _{CCI0} + 0.3	V _{REF} – 0.25	V _{REF} + 0.25	V _{TT} – 0.603	V _{TT} + 0.603	6.7	-6.7
SSTL-18 Class II	-0.3	V _{REF} – 0.125	V _{REF} + 0.125	V _{CCI0} + 0.3	V _{REF} – 0.25	V _{REF} + 0.25	0.28	V _{CCI0} – 0.28	13.4	-13.4
SSTL-15 Class I	_	V _{REF} – 0.1	V _{REF} + 0.1	_	V _{REF} – 0.175	V _{REF} + 0.175	0.2 * V _{CCI0}	0.8 * V _{CCI0}	8	-8
SSTL-15 Class II	_	V _{REF} – 0.1	V _{REF} + 0.1	_	V _{REF} – 0.175	V _{REF} + 0.175	0.2 * V _{CCI0}	0.8 * V _{CCI0}	16	-16
SSTL-135 Class I, II	_	V _{REF} – 0.09	V _{REF} + 0.09	—	V _{REF} – 0.16	V _{REF} + 0.16	0.2 * V _{CCI0}	0.8 * V _{CCI0}	—	_
SSTL-125 Class I, II		V _{REF} – 0.85	V _{REF} + 0.85	_	V _{REF} – 0.15	V _{REF} + 0.15	0.2 * V _{CCI0}	0.8 * V _{CCI0}		
SSTL-12 Class I, II	_	V _{REF} – 0.1	V _{REF} + 0.1	_	V _{REF} – 0.15	V _{REF} + 0.15	0.2 * V _{CCI0}	0.8 * V _{CCI0}	_	

Table 26 shows the approximate maximum data rate using the 10G PCS.

Mode (2) Transceiver		PMA Width	64	40	40	40	32	32		
mode ""	Speed Grade	PCS Width	64	66/67	50	40	64/66/67	32		
	1	C1, C2, C2L, I2, I2L core speed grade	14.1	14.1	10.69	14.1	13.6	13.6		
	2	C1, C2, C2L, I2, I2L core speed grade	12.5	12.5	10.69	12.5	12.5	12.5		
FIFO or Register 3	Z	C3, I3, I3L core speed grade	12.5	12.5	10.69	12.5	10.88	10.88		
		C1, C2, C2L, I2, I2L core speed grade								
	3	C3, I3, I3L core speed grade	8.5 Gbps							
	5	C4, I4 core speed grade								
		I3YY core speed grade	10.3125 Gbps							

Notes to Table 26:

(1) The maximum data rate is in Gbps.

(2) The Phase Compensation FIFO can be configured in FIFO mode or register mode. In the FIFO mode, the pointers are not fixed, and the latency can vary. In the register mode the pointers are fixed for low latency.





Figure 3 shows the Stratix V AC gain curves for GX channels.

Figure 3. AC Gain Curves for GX Channels (full bandwidth)

Stratix V GT devices contain both GX and GT channels. All transceiver specifications for the GX channels not listed in Table 28 are the same as those listed in Table 23.

Table 28 lists the Stratix V GT transceiver specifications.

Symbol/ Description	Conditions	s	Transceive peed Grade	r 2	S	Transceive peed Grade	r 3	Unit			
Description		Min	Тур	Max	Min	Тур	Max				
Reference Clock								1			
Supported I/O Standards	Dedicated reference clock pin	1.2-V PCN	IL, 1.4-V PC	ML, 1.5-V P(CML, 2.5-V I and HCSL	PCML, Diffe	rential LVPE	ECL, LVDS,			
otanuarus	RX reference clock pin		1.4-V PCML, 1.5-V PCML, 2.5-V PCML, LVPECL, and LVDS								
Input Reference Clock Frequency (CMU PLL) ⁽⁶⁾	_	40	_	710	40	_	710	MHz			
Input Reference Clock Frequency (ATX PLL) ⁽⁶⁾	_	100	_	710	100	_	710	MHz			
Rise time	20% to 80%	_		400	_	_	400				
Fall time	80% to 20%			400	—	_	400	ps			
Duty cycle	—	45	_	55	45	_	55	%			
Spread-spectrum modulating clock frequency	PCI Express (PCIe)	30	_	33	30	_	33	kHz			
Spread-spectrum downspread	PCle	_	0 to -0.5	_	_	0 to -0.5	_	%			
On-chip termination resistors ⁽¹⁹⁾	_	_	100	_	_	100	_	Ω			
Absolute V _{MAX} ⁽³⁾	Dedicated reference clock pin	_	_	1.6	_	_	1.6	V			
	RX reference clock pin	_	_	1.2	_	_	1.2				
Absolute V _{MIN}	—	-0.4		—	-0.4	—		V			
Peak-to-peak differential input voltage	_	200	_	1600	200	_	1600	mV			
V _{ICM} (AC coupled)	Dedicated reference clock pin		1050/1000 ^{(,}	2)	1	050/1000 (2)	mV			
	RX reference clock pin	1	.0/0.9/0.85 (22)	1.	V					
V _{ICM} (DC coupled)	HCSL I/O standard for PCIe reference clock	250	_	550	250	_	550	mV			

Table 28. Transceiver Specifications for Stratix V GT Devices (Part 1 of 5)⁽¹⁾

Symbol/	Conditions	S	Transceive peed Grade	2	S	Fransceive Deed Grade	r 3	Unit
Description		Min	Тур	Max	Min	Тур	Max	
Differential on-chip termination resistors ⁽⁷⁾	GT channels		100	_	_	100	_	Ω
	85- Ω setting	_	85 ± 30%	_	_	85 ± 30%	_	Ω
Differential on-chip	100-Ω setting	_	100 ± 30%	_	_	100 ± 30%	_	Ω
for GX channels ⁽¹⁹⁾	120-Ω setting	_	120 ± 30%	_	—	120 ± 30%	—	Ω
	150-Ω setting		150 ± 30%	_	_	150 ± 30%	_	Ω
V _{ICM} (AC coupled)	GT channels	_	650	_	—	650	—	mV
	VCCR_GXB = 0.85 V or 0.9 V	_	600	_	_	600	_	mV
VICM (AC and DC coupled) for GX Channels	VCCR_GXB = 1.0 V full bandwidth	_	700		_	700	_	mV
	VCCR_GXB = 1.0 V half bandwidth	_	750	_	_	750	_	mV
t _{LTR} ⁽⁹⁾	—	_	—	10	—	—	10	μs
t _{LTD} ⁽¹⁰⁾		4			4	_	_	μs
t _{LTD_manual} ⁽¹¹⁾		4	_		4	_	_	μs
t _{LTR_LTD_manual} ⁽¹²⁾	—	15	—	_	15	—	—	μs
Run Lenath	GT channels		—	72	—	—	72	CID
	GX channels				(8)			
CDR PPM	GT channels	_	—	1000	—	—	1000	± PPM
	GX channels				(8)			
Programmable	GT channels			14		—	14	dB
(AC Gain) ⁽⁵⁾	GX channels				(8)			
Programmable	GT channels	_		7.5	_		7.5	dB
DC gain ⁽⁶⁾	GX channels				(8)			
Differential on-chip termination resistors ⁽⁷⁾	GT channels	_	100	—	_	100	_	Ω
Transmitter								
Supported I/O Standards	_			1.4-V	and 1.5-V P	CML		
Data rate (Standard PCS)	GX channels	600	_	8500	600		8500	Mbps
Data rate (10G PCS)	GX channels	600		12,500	600		12,500	Mbps

Table 28. Transceiver Specifications for Stratix V GT Devices (Part 3 of 5)⁽¹⁾

	Table 28.	Transceiver S	pecifications	for Stratix V	GT Devices	(Part 4 of 5) (1)
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Symbol/ Description	Conditions	s	Transceive peed Grade	r 2	ר Sp	Fransceive Deed Grade	r 3	Unit		
Description		Min	Тур	Max	Min	Тур	Max			
Data rate	GT channels	19,600	_	28,050	19,600		25,780	Mbps		
Differential on-chip	GT channels	_	100	—		100	_	Ω		
termination resistors	GX channels				(8)					
	GT channels	_	500	_		500	_	mV		
V _{OCM} (AC Coupled)	GX channels	(8)								
Dice/Fell time	GT channels	_	15	—	—	15	—	ps		
Rise/Fail lime	GX channels				(8)					
Intra-differential pair skew	GX channels				(8)					
Intra-transceiver block transmitter channel-to- channel skew	GX channels		(8)							
Inter-transceiver block transmitter channel-to- channel skew	GX channels		(8)							
CMU PLL										
Supported Data Range	—	600		12500	600		8500	Mbps		
t _{pll_powerdown} ⁽¹³⁾	—	1	—	—	1	_	—	μs		
t _{pll_lock} ⁽¹⁴⁾	—	_	—	10	_	_	10	μs		
ATX PLL										
	VCO post- divider L=2	8000	_	12500	8000	_	8500	Mbps		
	L=4	4000	—	6600	4000	_	6600	Mbps		
Supported Data Rate	L=8	2000	—	3300	2000	_	3300	Mbps		
Range for GX Channels	L=8, Local/Central Clock Divider =2	1000	_	1762.5	1000	_	1762.5	Mbps		
Supported Data Rate Range for GT Channels	VCO post- divider L=2	9800	_	14025	9800	_	12890	Mbps		
t _{pll_powerdown} ⁽¹³⁾	—	1	—	—	1	_	—	μs		
t _{pll_lock} ⁽¹⁴⁾	—	_	—	10	_	_	10	μs		
fPLL										
Supported Data Range		600		3250/ 3.125 ⁽²³⁾	600		3250/ 3.125 ⁽²³⁾	Mbps		
t _{pll_powerdown} ⁽¹³⁾	—	1	—	—	1	—	—	μs		

Figure 4 shows the differential transmitter output waveform.





Figure 5 shows the Stratix V AC gain curves for GT channels.

Figure 5. AC Gain Curves for GT Channels

Figure 6 shows the Stratix V DC gain curves for GT channels.

Figure 6. DC Gain Curves for GT Channels

Transceiver Characterization

This section summarizes the Stratix V transceiver characterization results for compliance with the following protocols:

- Interlaken
- 40G (XLAUI)/100G (CAUI)
- 10GBase-KR
- QSGMII
- XAUI
- SFI
- Gigabit Ethernet (Gbe / GIGE)
- SPAUI
- Serial Rapid IO (SRIO)
- CPRI
- OBSAI
- Hyper Transport (HT)
- SATA
- SAS
- CEI

- XFI
- ASI
- HiGig/HiGig+
- HiGig2/HiGig2+
- Serial Data Converter (SDC)
- GPON
- SDI
- SONET
- Fibre Channel (FC)
- PCIe
- QPI
- SFF-8431

Download the Stratix V Characterization Report Tool to view the characterization report summary for these protocols.

Core Performance Specifications

This section describes the clock tree, phase-locked loop (PLL), digital signal processing (DSP), memory blocks, configuration, and JTAG specifications.

Clock Tree Specifications

Table 30 lists the clock tree specifications for Stratix V devices.

Table 30. Clock Tree Performance for Stratix V Devices (1)

	Performance						
Symbol	C1, C2, C2L, I2, and I2L	C3, I3, I3L, and I3YY	C4, I4	Unit			
Global and Regional Clock	717	650	580	MHz			
Periphery Clock	550	500	500	MHz			

Note to Table 30:

(1) The Stratix V ES devices are limited to 600 MHz core clock tree performance.

PLL Specifications

Table 31 lists the Stratix V PLL specifications when operating in both the commercial junction temperature range (0° to 85° C) and the industrial junction temperature range (-40° to 100° C).

Table 31. PLL Specifications for Stratix V Devices (Part 1 of 3)

Symbol	Parameter	Min	Тур	Max	Unit
	Input clock frequency (C1, C2, C2L, I2, and I2L speed grades)	5		800 (1)	MHz
f _{IN}	Input clock frequency (C3, I3, I3L, and I3YY speed grades)	5		800 (1)	MHz
	Input clock frequency (C4, I4 speed grades)	5	—	650 ⁽¹⁾	MHz
f _{INPFD}	Input frequency to the PFD	5	—	325	MHz
f _{FINPFD}	Fractional Input clock frequency to the PFD	50	—	160	MHz
	PLL VCO operating range (C1, C2, C2L, I2, I2L speed grades)	600	_	1600	MHz
f _{VCO} (9)	PLL VCO operating range (C3, I3, I3L, I3YY speed grades)	600		1600	MHz
	PLL VCO operating range (C4, I4 speed grades)	600	—	1300	MHz
t _{einduty}	Input clock or external feedback clock input duty cycle	40	—	60	%
	Output frequency for an internal global or regional clock (C1, C2, C2L, I2, I2L speed grades)	_	_	717 ⁽²⁾	MHz
f _{OUT}	Output frequency for an internal global or regional clock (C3, I3, I3L speed grades)			650 ⁽²⁾	MHz
	Output frequency for an internal global or regional clock (C4, I4 speed grades)			580 ⁽²⁾	MHz
	Output frequency for an external clock output (C1, C2, C2L, I2, I2L speed grades)			800 ⁽²⁾	MHz
f _{OUT_EXT}	Output frequency for an external clock output (C3, I3, I3L speed grades)			667 ⁽²⁾	MHz
	Output frequency for an external clock output (C4, I4 speed grades)			553 ⁽²⁾	MHz
t _{outduty}	Duty cycle for a dedicated external clock output (when set to 50%)	45	50	55	%
t _{FCOMP}	External feedback clock compensation time	_		10	ns
f _{dyconfigclk}	Dynamic Configuration Clock used for mgmt_clk and scanclk		_	100	MHz
t _{LOCK}	Time required to lock from the end-of-device configuration or deassertion of areset			1	ms
t _{DLOCK}	Time required to lock dynamically (after switchover or reconfiguring any non-post-scale counters/delays)			1	ms
	PLL closed-loop low bandwidth	—	0.3	—	MHz
f _{CLBW}	PLL closed-loop medium bandwidth	—	1.5	—	MHz
	PLL closed-loop high bandwidth (7)	—	4	-	MHz
t _{PLL_PSERR}	Accuracy of PLL phase shift	—	—	±50	ps
t _{ARESET}	Minimum pulse width on the areset signal	10	—	_	ns

	Mode	Resources Used		Performance							
Memory		ALUTS	Memory	C1	C2, C2L	C3	C4	12, 12L	13, 13L, 13YY	14	Unit
	Single-port, all supported widths	0	1	700	700	650	550	700	500	450	MHz
	Simple dual-port, all supported widths	0	1	700	700	650	550	700	500	450	MHz
	Simple dual-port with the read-during-write option set to Old Data , all supported widths	0	1	525	525	455	400	525	455	400	MHz
M20K Block	Simple dual-port with ECC enabled, 512 × 32	0	1	450	450	400	350	450	400	350	MHz
	Simple dual-port with ECC and optional pipeline registers enabled, 512 × 32	0	1	600	600	500	450	600	500	450	MHz
	True dual port, all supported widths	0	1	700	700	650	550	700	500	450	MHz
	ROM, all supported widths	0	1	700	700	650	550	700	500	450	MHz

Table 33. Memory Block Performance Specifications for Stratix V Devices ^{(1), (2)} (Part 2 of 2)

Notes to Table 33:

(1) To achieve the maximum memory block performance, use a memory block clock that comes through global clock routing from an on-chip PLL set to **50**% output duty cycle. Use the Quartus II software to report timing for this and other memory block clocking schemes.

(2) When you use the error detection cyclical redundancy check (CRC) feature, there is no degradation in F_{MAX}.

(3) The F_{MAX} specification is only achievable with Fitter options, MLAB Implementation In 16-Bit Deep Mode enabled.

Temperature Sensing Diode Specifications

Table 34 lists the internal TSD specification.

Table 34. Internal Temperature Sensing Diode Specification

Temperature Range	Accuracy	Offset Calibrated Option	Sampling Rate	Conversion Time	Resolution	Minimum Resolution with no Missing Codes
-40°C to 100°C	±8°C	No	1 MHz, 500 KHz	< 100 ms	8 bits	8 bits

Table 35 lists the specifications for the Stratix V external temperature sensing diode.

Table 35.	External	Temperature	Sensing Dic	de Specifica	ations for Stratix	V Devices
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Description	Min	Тур	Max	Unit
I _{bias} , diode source current	8	—	200	μA
V _{bias,} voltage across diode	0.3	—	0.9	V
Series resistance	—	_	< 1	Ω
Diode ideality factor	1.006	1.008	1.010	_

Symbol	Conditiono	C1		C2, C2L, I2, I2L		C3, I3, I3L, I3YY		C4,14						
Symbol	Conditions	Min	Тур	Max	Min	Тур	Max	Min	Тур	Max	Min	Тур	Max	UIIIL
Transmitter														
	SERDES factor J = 3 to 10 ⁽⁹⁾ , ⁽¹¹⁾ , ⁽¹²⁾ , ⁽¹³⁾ , ⁽¹⁴⁾ , ⁽¹⁵⁾ , ⁽¹⁶⁾	(6)	_	1600	(6)	_	1434	(6)	_	1250	(6)	_	1050	Mbps
True Differential I/O Standards - f _{HSDR} (data rate)	SERDES factor J ≥ 4 LVDS TX with DPA (12), (14), (15), (16)	(6)		1600	(6)		1600	(6)		1600	(6)	_	1250	Mbps
	SERDES factor J = 2, uses DDR Registers	(6)	_	(7)	(6)	_	(7)	(6)	_	(7)	(6)		(7)	Mbps
	SERDES factor J = 1, uses SDR Register	(6)	_	(7)	(6)	_	(7)	(6)	_	(7)	(6)	_	(7)	Mbps
Emulated Differential I/O Standards with Three External Output Resistor Networks - f _{HSDR} (data rate) ⁽¹⁰⁾	SERDES factor J = 4 to 10 $(^{17})$	(6)		1100	(6)		1100	(6)		840	(6)		840	Mbps
t _{x Jitter} - True Differential	Total Jitter for Data Rate 600 Mbps - 1.25 Gbps		_	160		_	160		_	160			160	ps
I/O Standards	Total Jitter for Data Rate < 600 Mbps		_	0.1			0.1			0.1		_	0.1	UI
t _{x Jitter} - Emulated Differential I/O Standards	Total Jitter for Data Rate 600 Mbps - 1.25 Gbps	_	_	300	_		300	_	_	300	_		325	ps
with Three External Output Resistor Network	Total Jitter for Data Rate < 600 Mbps	_	_	0.2	_	_	0.2	_	_	0.2	_	_	0.25	UI

Table 36. High-Speed I/O Specifications for Stratix V Devices (1), (2) (Part 2 of 4)

Symbol	Description	Min	Max	Unit
t _{JPH}	JTAG port hold time	5	—	ns
t _{JPCO}	JTAG port clock to output	—	11 ⁽¹⁾	ns
t _{JPZX}	JTAG port high impedance to valid output	—	14 ⁽¹⁾	ns
t _{JPXZ}	JTAG port valid output to high impedance	—	14 ⁽¹⁾	ns

Table 46. JTAG Timing Parameters and Values for Stratix V Devices

Notes to Table 46:

(1) A 1 ns adder is required for each V_{CCI0} voltage step down from 3.0 V. For example, $t_{JPC0} = 12$ ns if V_{CCI0} of the TDO I/O bank = 2.5 V, or 13 ns if it equals 1.8 V.

(2) The minimum TCK clock period is 167 ns if VCCBAT is within the range 1.2V-1.5V when you perform the volatile key programming.

Raw Binary File Size

For the POR delay specification, refer to the "POR Delay Specification" section of the "Configuration, Design Security, and Remote System Upgrades in Stratix V Devices".

Table 47 lists the uncompressed raw binary file (.rbf) sizes for Stratix V devices.

Family	Device	Package	Configuration .rbf Size (bits)	IOCSR .rbf Size (bits) ^{(4), (5)}
	500742	H35, F40, F35 ⁽²⁾	213,798,880	562,392
	JOUNAS	H29, F35 ⁽³⁾	137,598,880	564,504
	5SGXA4	—	213,798,880	563,672
	5SGXA5	—	269,979,008	562,392
	5SGXA7	—	269,979,008	562,392
Stratix V GX	5SGXA9	—	342,742,976	700,888
	5SGXAB	—	342,742,976	700,888
	5SGXB5	—	270,528,640	584,344
	5SGXB6	—	270,528,640	584,344
	5SGXB9	—	342,742,976	700,888
	5SGXBB	—	342,742,976	700,888
Stratix V CT	5SGTC5	—	269,979,008	562,392
	5SGTC7	—	269,979,008	562,392
	5SGSD3	—	137,598,880	564,504
	590904	F1517	213,798,880	563,672
Stratix V GS	J303D4	_	137,598,880	564,504
	5SGSD5		213,798,880	563,672
	5SGSD6		293,441,888	565,528
	5SGSD8	—	293,441,888	565,528

Table 47. Uncompressed .rbf Sizes for Stratix V Devices

Baramatar Available Min		Min	Fast Model		Slow Model							
(1)	Settings	Offset (2)	Industrial	Commercial	C1	C2	C3	C4	12	13, 13YY	14	Unit
D3	8	0	1.587	1.699	2.793	2.793	2.992	3.192	2.811	3.047	3.257	ns
D4	64	0	0.464	0.492	0.838	0.838	0.924	1.011	0.843	0.920	1.006	ns
D5	64	0	0.464	0.493	0.838	0.838	0.924	1.011	0.844	0.921	1.006	ns
D6	32	0	0.229	0.244	0.415	0.415	0.458	0.503	0.418	0.456	0.499	ns

Table 58.	IOE Pro	grammable De	lay for	Stratix V	V Devices	(Part 2 of 2)
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Notes to Table 58:

(1) You can set this value in the Quartus II software by selecting D1, D2, D3, D5, and D6 in the Assignment Name column of Assignment Editor.

(2) Minimum offset does not include the intrinsic delay.

Programmable Output Buffer Delay

Table 59 lists the delay chain settings that control the rising and falling edge delays of the output buffer. The default delay is 0 ps.

Symbol	Parameter	Typical	Unit
		0 (default)	ps
Dauman	Rising and/or falling edge	25	ps
DOUTBUF	delay	50	ps
		75	ps

Note to Table 59:

(1) You can set the programmable output buffer delay in the Quartus II software by setting the Output Buffer Delay Control assignment to either positive, negative, or both edges, with the specific values stated here (in ps) for the Output Buffer Delay assignment.

Glossary

Table 60 lists the glossary for this chapter.

Table 60. Glossary (Part 1 of 4)

Letter	r Subject Definitions		
Α			
В	—	—	
С			
D	—	_	
E	—	_	
	f _{HSCLK}	Left and right PLL input clock frequency.	
F	f _{HSDR}	High-speed I/O block—Maximum and minimum LVDS data transfer rate (f _{HSDR} = 1/TUI), non-DPA.	
	f _{hsdrdpa}	High-speed I/O block—Maximum and minimum LVDS data transfer rate (f _{HSDRDPA} = 1/TUI), DPA.	

Table 60. Glossary (Part 2 of 4)

Letter	Subject	Definitions
G H I	JTAG Timing Specifications	High-speed I/O block—Deserialization factor (width of parallel data bus). JTAG Timing Specifications: TMS
K L M N O		
Ρ	PLL Specifications	Diagram of PLL Specifications ⁽¹⁾
Q	—	—
R	RL	Receiver differential input discrete resistor (external to the Stratix V device).

Table 60.	Glossary	(Part 3 of 4)
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Letter	Subject	Definitions					
	SW (sampling window)	Timing Diagram—the period of time during which the data must be valid in order to capture it correctly. The setup and hold times determine the ideal strobe position within the sampling window, as shown: Bit Time 0.5 x TCCS RSKM Sampling Window RSKM 0.5 x TCCS RSKM					
S	Single-ended voltage referenced I/O standard	The JEDEC standard for SSTL and HSTL I/O defines both the AC and DC input signal values. The AC values indicate the voltage levels at which the receiver must meet its timing specifications. The DC values indicate the voltage levels at which the final logic state of the receiver is unambiguously defined. After the receiver input has crossed the AC value, the receiver changes to the new logic state. The new logic state is then maintained as long as the input stays beyond the DC threshold. This approach is intended to provide predictable receiver timing in the presence of input waveform ringing: Single-Ended Voltage Referenced I/O Standard					
	t _C	High-speed receiver and transmitter input and output clock period.					
	TCCS (channel- to-channel-skew)	The timing difference between the fastest and slowest output edges, including t_{CO} variation and clock skew, across channels driven by the same PLL. The clock is included in the TCCS measurement (refer to the <i>Timing Diagram</i> figure under SW in this table).					
		High-speed I/O block—Duty cycle on the high-speed transmitter output clock.					
т	t _{DUTY}	Timing Unit Interval (TUI) The timing budget allowed for skew, propagation delays, and the data sampling window.					
		$(TUI = 1/(receiver input clock frequency multiplication factor) = t_c/w)$					
	t _{FALL}	Signal high-to-low transition time (80-20%)					
	t _{INCCJ}	Cycle-to-cycle jitter tolerance on the PLL clock input.					
	t _{outpj_i0}	Period jitter on the general purpose I/O driven by a PLL.					
	t _{outpj_dc}	Period jitter on the dedicated clock output driven by a PLL.					
	t _{RISE}	Signal low-to-high transition time (20-80%)					
U	—	—					