#### Intel - <u>5SGXMA3E1H29C2L Datasheet</u>





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#### Understanding <u>Embedded - FPGAs (Field</u> <u>Programmable Gate Array)</u>

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

#### **Applications of Embedded - FPGAs**

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

#### Details

Product Status	Obsolete
Number of LABs/CLBs	128300
Number of Logic Elements/Cells	340000
Total RAM Bits	19456000
Number of I/O	600
Number of Gates	-
Voltage - Supply	0.82V ~ 0.88V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	780-BBGA, FCBGA
Supplier Device Package	780-HBGA (33x33)
Purchase URL	https://www.e-xfl.com/product-detail/intel/5sgxma3e1h29c2l

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

Symbol	Description	Minimum	Maximum	Unit
V <sub>CCD_FPLL</sub>	PLL digital power supply	-0.5	1.8	V
V <sub>CCA_FPLL</sub>	PLL analog power supply	-0.5	3.4	V
VI	DC input voltage	-0.5	3.8	V
TJ	Operating junction temperature	-55	125	°C
T <sub>STG</sub>	Storage temperature (No bias)	-65	150	°C
I <sub>OUT</sub>	DC output current per pin	-25	40	mA

Table 3. Absolute Maximum Ratings for Stratix V Devices (Part 2 of 2)

Table 4 lists the absolute conditions for the transceiver power supply for Stratix V GX, GS, and GT devices.

Table 4. Transceiver Power Supply Absolute Conditions for Stratix V GX, GS, and GT Devices

Symbol	Description	Devices	Minimum	Maximum	Unit
V <sub>CCA_GXBL</sub>	Transceiver channel PLL power supply (left side)	GX, GS, GT	-0.5	3.75	V
V <sub>CCA_GXBR</sub>	Transceiver channel PLL power supply (right side)	GX, GS	-0.5	3.75	V
V <sub>CCA_GTBR</sub>	Transceiver channel PLL power supply (right side)	GT	-0.5	3.75	V
V <sub>CCHIP_L</sub>	Transceiver hard IP power supply (left side)	GX, GS, GT	-0.5	1.35	V
V <sub>CCHIP_R</sub>	Transceiver hard IP power supply (right side)	GX, GS, GT	-0.5	1.35	V
V <sub>CCHSSI_L</sub>	Transceiver PCS power supply (left side)	GX, GS, GT	-0.5	1.35	V
V <sub>CCHSSI_R</sub>	Transceiver PCS power supply (right side)	GX, GS, GT	-0.5	1.35	V
V <sub>CCR_GXBL</sub>	Receiver analog power supply (left side)	GX, GS, GT	-0.5	1.35	V
V <sub>CCR_GXBR</sub>	Receiver analog power supply (right side)	GX, GS, GT	-0.5	1.35	V
V <sub>CCR_GTBR</sub>	Receiver analog power supply for GT channels (right side)	GT	-0.5	1.35	V
V <sub>CCT_GXBL</sub>	Transmitter analog power supply (left side)	GX, GS, GT	-0.5	1.35	V
V <sub>CCT_GXBR</sub>	Transmitter analog power supply (right side)	GX, GS, GT	-0.5	1.35	V
V <sub>CCT_GTBR</sub>	Transmitter analog power supply for GT channels (right side)	GT	-0.5	1.35	V
V <sub>CCL_GTBR</sub>	Transmitter clock network power supply (right side)	GT	-0.5	1.35	V
V <sub>CCH_GXBL</sub>	Transmitter output buffer power supply (left side)	GX, GS, GT	-0.5	1.8	V
V <sub>CCH_GXBR</sub>	Transmitter output buffer power supply (right side)	GX, GS, GT	-0.5	1.8	V

#### **Maximum Allowed Overshoot and Undershoot Voltage**

During transitions, input signals may overshoot to the voltage shown in Table 5 and undershoot to -2.0 V for input currents less than 100 mA and periods shorter than 20 ns.

Symbol	Description	Condition	Min <sup>(4)</sup>	Тур	Max <sup>(4)</sup>	Unit
t <sub>RAMP</sub>	Power supply ramp time	Standard POR	200 µs	_	100 ms	—
		Fast POR	200 µs		4 ms	

#### Table 6. Recommended Operating Conditions for Stratix V Devices (Part 2 of 2)

#### Notes to Table 6:

(1)  $V_{CCPD}$  must be 2.5 V when  $V_{CCI0}$  is 2.5, 1.8, 1.5, 1.35, 1.25 or 1.2 V.  $V_{CCPD}$  must be 3.0 V when  $V_{CCI0}$  is 3.0 V.

(2) If you do not use the design security feature in Stratix V devices, connect V<sub>CCBAT</sub> to a 1.2- to 3.0-V power supply. Stratix V power-on-reset (POR) circuitry monitors V<sub>CCBAT</sub>. Stratix V devices will not exit POR if V<sub>CCBAT</sub> stays at logic low.

(3) C2L and I2L can also be run at 0.90 V for legacy boards that were designed for the C2 and I2 speed grades.

(4) The power supply value describes the budget for the DC (static) power supply tolerance and does not include the dynamic tolerance requirements. Refer to the PDN tool for the additional budget for the dynamic tolerance requirements.

Table 7 lists the transceiver power supply recommended operating conditions for Stratix V GX, GS, and GT devices.

# Table 7. Recommended Transceiver Power Supply Operating Conditions for Stratix V GX, GS, and GT Devices (Part 1 of 2)

Symbol	Description	Devices	Minimum <sup>(4)</sup>	Typical	Maximum <sup>(4)</sup>	Unit
V <sub>CCA GXBL</sub>	Transceiver channel PLL power supply (left		2.85	3.0	3.15	V
(1), (3)	side)	un, us, ui	2.375	2.5	2.625	v
V <sub>CCA_GXBR</sub>	Transceiver channel PLL power supply (right	CV CS	2.85	3.0	3.15	V
(1), (3)	side)	ux, us	2.375	2.5	2.625	v
V <sub>CCA_GTBR</sub>	Transceiver channel PLL power supply (right side)	GT	2.85	3.0	3.15	V
	Transceiver hard IP power supply (left side; C1, C2, I2, and I3YY speed grades)	GX, GS, GT	0.87	0.9	0.93	V
V <sub>CCHIP_L</sub>	Transceiver hard IP power supply (left side; C2L, C3, C4, I2L, I3, I3L, and I4 speed grades)	GX, GS, GT	0.82	0.85	0.88	V
V <sub>CCHIP_R</sub>	Transceiver hard IP power supply (right side; C1, C2, I2, and I3YY speed grades)	GX, GS, GT	0.87	0.9	0.93	V
	Transceiver hard IP power supply (right side; C2L, C3, C4, I2L, I3, I3L, and I4 speed grades)	GX, GS, GT	0.82	0.85	0.88	V
	Transceiver PCS power supply (left side; C1, C2, I2, and I3YY speed grades)	GX, GS, GT	0.87	0.9	0.93	V
V <sub>CCHSSI_L</sub>	Transceiver PCS power supply (left side; C2L, C3, C4, I2L, I3, I3L, and I4 speed grades)	GX, GS, GT	0.82	0.85	0.88	V
	Transceiver PCS power supply (right side; C1, C2, I2, and I3YY speed grades)	GX, GS, GT	0.87	0.9	0.93	V
V <sub>CCHSSI_R</sub>	Transceiver PCS power supply (right side; C2L, C3, C4, I2L, I3, I3L, and I4 speed grades)	GX, GS, GT	0.82	0.85	0.88	V
			0.82	0.85	0.88	
V <sub>CCR_GXBL</sub>	Receiver analog nower supply (left side)	GX, GS, GT	0.87	0.90	0.93	V
(2) _	Therefore analog power supply (left Slue)		0.97	1.0	1.03	
			1.03	1.05	1.07	

			Calibration Accuracy				
Symbol	Description	Conditions	C1	C2,I2	C3,I3, I3YY	C4,14	Unit
50-Ω R <sub>S</sub>	Internal series termination with calibration (50- $\Omega$ setting)	V <sub>CCI0</sub> = 3.0, 2.5, 1.8, 1.5, 1.2 V	±15	±15	±15	±15	%
34- $\Omega$ and 40- $\Omega$ R <sub>S</sub>	Internal series termination with calibration (34- $\Omega$ and 40- $\Omega$ setting)	V <sub>CCI0</sub> = 1.5, 1.35, 1.25, 1.2 V	±15	±15	±15	±15	%
48-Ω, 60-Ω, 80-Ω, and 240-Ω R <sub>S</sub>	Internal series termination with calibration (48- $\Omega$ , 60- $\Omega$ , 80- $\Omega$ , and 240- $\Omega$ setting)	V <sub>CCI0</sub> = 1.2 V	±15	±15	±15	±15	%
50-Ω R <sub>T</sub>	Internal parallel termination with calibration (50-Ω setting)	V <sub>CCI0</sub> = 2.5, 1.8, 1.5, 1.2 V	-10 to +40	-10 to +40	-10 to +40	-10 to +40	%
20-Ω, 30-Ω, 40-Ω,60-Ω, and 120-Ω R <sub>T</sub>	Internal parallel termination with calibration ( $20 - \Omega$ , $30 - \Omega$ , $40 - \Omega$ , $60 - \Omega$ , and $120 - \Omega$ setting)	V <sub>CCI0</sub> = 1.5, 1.35, 1.25 V	-10 to +40	-10 to +40	-10 to +40	-10 to +40	%
60- $Ω$ and 120- $Ω$ R <sub>T</sub>	Internal parallel termination with calibration (60-Ω and 120-Ω setting)	V <sub>CCI0</sub> = 1.2	-10 to +40	-10 to +40	-10 to +40	-10 to +40	%
$25-\Omega \\ R_{S\_left\_shift}$	Internal left shift series termination with calibration ( $25-\Omega$ R <sub>S_left_shift</sub> setting)	V <sub>CCI0</sub> = 3.0, 2.5, 1.8, 1.5, 1.2 V	±15	±15	±15	±15	%

Table II. OUI Valiblation Accuracy specifications for Stratix V Devices' / (I all 2 of	Table 11.	<b>OCT Calibration A</b>	ccuracy Specificati	ons for Stratix V D	Devices <sup>(1)</sup> (	Part 2 of
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#### Note to Table 11:

(1) OCT calibration accuracy is valid at the time of calibration only.

Table 12 lists the Stratix V OCT without calibration resistance to PVT changes.

Table 12.	OCT Without Calibration	<b>Resistance</b> 1	<b>Tolerance</b>	<b>Specifications</b>	for Stratix	V Devices	(Part 1	of 2)
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			<b>Resistance Tolerance</b>				
Symbol	Description	Conditions	C1	C2,I2	C3, I3, I3YY	C4, I4	Unit
25-Ω R, 50-Ω R <sub>S</sub>	Internal series termination without calibration (25-Ω setting)	$V_{CCIO} = 3.0$ and 2.5 V	±30	±30	±40	±40	%
25-Ω R <sub>S</sub>	Internal series termination without calibration (25-Ω setting)	V <sub>CCIO</sub> = 1.8 and 1.5 V	±30	±30	±40	±40	%
25-Ω R <sub>S</sub>	Internal series termination without calibration (25-Ω setting)	V <sub>CCI0</sub> = 1.2 V	±35	±35	±50	±50	%

#### **Internal Weak Pull-Up Resistor**

Table 16 lists the weak pull-up resistor values for Stratix V devices.

Symbol	Description	V <sub>CCIO</sub> Conditions (V) <sup>(3)</sup>	Value <sup>(4)</sup>	Unit		
		3.0 ±5%	25	kΩ		
		2.5 ±5% 25				
	Value of the I/O pin pull-up resistor before	1.8 ±5%	25	kΩ		
R <sub>PU</sub>	and during configuration, as well as user mode if you enable the programmable	1.5 ±5%	25	kΩ		
	pull-up resistor option.	1.35 ±5%	25	kΩ		
		1.25 ±5%	25	kΩ		
		1.2 ±5%	25	kΩ		

Table 16. Internal Weak Pull-Up Resistor for Stratix V Devices (1), (2)

Notes to Table 16:

(1) All I/O pins have an option to enable the weak pull-up resistor except the configuration, test, and JTAG pins.

(2) The internal weak pull-down feature is only available for the JTAG TCK pin. The typical value for this internal weak pull-down resistor is approximately 25 k $\Omega$ .

- (3) The pin pull-up resistance values may be lower if an external source drives the pin higher than V<sub>CCIO</sub>.
- (4) These specifications are valid with a  $\pm 10\%$  tolerance to cover changes over PVT.

### I/O Standard Specifications

Table 17 through Table 22 list the input voltage (V<sub>IH</sub> and V<sub>IL</sub>), output voltage (V<sub>OH</sub> and V<sub>OL</sub>), and current drive characteristics (I<sub>OH</sub> and I<sub>OL</sub>) for various I/O standards supported by Stratix V devices. These tables also show the Stratix V device family I/O standard specifications. The V<sub>OL</sub> and V<sub>OH</sub> values are valid at the corresponding I<sub>OH</sub> and I<sub>OL</sub>, respectively.

For an explanation of the terms used in Table 17 through Table 22, refer to "Glossary" on page 65. For tolerance calculations across all SSTL and HSTL I/O standards, refer to Altera knowledge base solution rd07262012\_486.

I/O	V <sub>CCIO</sub> (V)			V <sub>IL</sub> (V)		VIH	(V)	V <sub>OL</sub> (V)	V <sub>OH</sub> (V)	I <sub>OL</sub>	I <sub>oh</sub>
Standard	Min	Тур	Max	Min	Max	Min	Max	Max	Min	(mA)	(mA)
LVTTL	2.85	3	3.15	-0.3	0.8	1.7	3.6	0.4	2.4	2	-2
LVCMOS	2.85	3	3.15	-0.3	0.8	1.7	3.6	0.2	$V_{CCIO} - 0.2$	0.1	-0.1
2.5 V	2.375	2.5	2.625	-0.3	0.7	1.7	3.6	0.4	2	1	-1
1.8 V	1.71	1.8	1.89	-0.3	0.35 * V <sub>CCIO</sub>	0.65 * V <sub>CCIO</sub>	V <sub>CCI0</sub> + 0.3	0.45	V <sub>CCI0</sub> – 0.45	2	-2
1.5 V	1.425	1.5	1.575	-0.3	0.35 * V <sub>CCI0</sub>	0.65 * V <sub>CCI0</sub>	V <sub>CCI0</sub> + 0.3	0.25 * V <sub>CCIO</sub>	0.75 * V <sub>CCIO</sub>	2	-2
1.2 V	1.14	1.2	1.26	-0.3	0.35 * V <sub>CCI0</sub>	0.65 * V <sub>CCI0</sub>	V <sub>CCI0</sub> + 0.3	0.25 * V <sub>CCIO</sub>	0.75 * V <sub>CCIO</sub>	2	-2

Table 17. Single-Ended I/O Standards for Stratix V Devices

1/0 Standard		V <sub>ccio</sub> (V)			V <sub>REF</sub> (V)		ν <sub>π</sub> (ν)			
i/O Stanuaru	Min	Тур	Max	Min	Тур	Max	Min	Тур	Max	
SSTL-2 Class I, II	2.375	2.5	2.625	0.49 * V <sub>CCIO</sub>	0.5 * V <sub>CCIO</sub>	0.51 * V <sub>CCIO</sub>	V <sub>REF</sub> – 0.04	V <sub>REF</sub>	V <sub>REF</sub> + 0.04	
SSTL-18 Class I, II	1.71	1.8	1.89	0.833	0.9	0.969	V <sub>REF</sub> – 0.04	V <sub>REF</sub>	V <sub>REF</sub> + 0.04	
SSTL-15 Class I, II	1.425	1.5	1.575	0.49 * V <sub>CCIO</sub>	0.5 * V <sub>CCIO</sub>	0.51 * V <sub>CCIO</sub>	0.49 * V <sub>CCIO</sub>	0.5 * VCCIO	0.51 * V <sub>CCIO</sub>	
SSTL-135 Class I, II	1.283	1.35	1.418	0.49 * V <sub>CCIO</sub>	0.5 * V <sub>CCIO</sub>	0.51 * V <sub>CCIO</sub>	0.49 * V <sub>CCIO</sub>	0.5 * V <sub>CCIO</sub>	0.51 * V <sub>CCIO</sub>	
SSTL-125 Class I, II	1.19	1.25	1.26	0.49 * V <sub>CCIO</sub>	0.5 * V <sub>CCIO</sub>	0.51 * V <sub>CCIO</sub>	0.49 * V <sub>CCIO</sub>	0.5 * VCCIO	0.51 * V <sub>CCIO</sub>	
SSTL-12 Class I, II	1.14	1.20	1.26	0.49 * V <sub>CCIO</sub>	0.5 * V <sub>CCIO</sub>	0.51 * V <sub>CCIO</sub>	0.49 * V <sub>CCIO</sub>	0.5 * VCCIO	0.51 * V <sub>CCIO</sub>	
HSTL-18 Class I, II	1.71	1.8	1.89	0.85	0.9	0.95	_	V <sub>CCI0</sub> /2	_	
HSTL-15 Class I, II	1.425	1.5	1.575	0.68	0.75	0.9	_	V <sub>CCI0</sub> /2	_	
HSTL-12 Class I, II	1.14	1.2	1.26	0.47 * V <sub>CCIO</sub>	0.5 * V <sub>CCIO</sub>	0.53 * V <sub>CCIO</sub>	_	V <sub>CCI0</sub> /2	_	
HSUL-12	1.14	1.2	1.3	0.49 * V <sub>CCIO</sub>	0.5 * V <sub>CCIO</sub>	0.51 * V <sub>CCIO</sub>	_			

Table 18. Single-Ended SSTL, HSTL, and HSUL I/O Reference Voltage Specifications for Stratix V Devi	ces
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Table 19.	Single-Ended SSTL	, HSTL, and HSUL I/	/O Standards Signal S	<b>Specifications for</b>	Stratix V Devices	(Part 1 of 2)
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1/0 Standard	$V_{IL(DC)}(V) \qquad V_{IH(DC)}(V) \qquad V_{IL(AC)}(V) \qquad V_{IH(AC)}(V)$		V <sub>IH(AC)</sub> (V)	V <sub>ol</sub> (V)	V <sub>oh</sub> (V)	I (mA)	I <sub>oh</sub>			
i/o Stanuaru	Min	Max	Min	Max	Max	Min	Max	Min	I <sub>ol</sub> (IIIA)	(mÄ)
SSTL-2 Class I	-0.3	V <sub>REF</sub> – 0.15	V <sub>REF</sub> + 0.15	V <sub>CCI0</sub> + 0.3	V <sub>REF</sub> – 0.31	V <sub>REF</sub> + 0.31	V <sub>TT</sub> – 0.608	V <sub>TT</sub> + 0.608	8.1	-8.1
SSTL-2 Class II	-0.3	V <sub>REF</sub> – 0.15	V <sub>REF</sub> + 0.15	V <sub>CCI0</sub> + 0.3	V <sub>REF</sub> – 0.31	V <sub>REF</sub> + 0.31	V <sub>TT</sub> – 0.81	V <sub>TT</sub> + 0.81	16.2	-16.2
SSTL-18 Class I	-0.3	V <sub>REF</sub> – 0.125	V <sub>REF</sub> + 0.125	V <sub>CCI0</sub> + 0.3	V <sub>REF</sub> – 0.25	V <sub>REF</sub> + 0.25	V <sub>TT</sub> – 0.603	V <sub>TT</sub> + 0.603	6.7	-6.7
SSTL-18 Class II	-0.3	V <sub>REF</sub> – 0.125	V <sub>REF</sub> + 0.125	V <sub>CCI0</sub> + 0.3	V <sub>REF</sub> – 0.25	V <sub>REF</sub> + 0.25	0.28	V <sub>CCI0</sub> – 0.28	13.4	-13.4
SSTL-15 Class I	_	V <sub>REF</sub> – 0.1	V <sub>REF</sub> + 0.1	_	V <sub>REF</sub> – 0.175	V <sub>REF</sub> + 0.175	0.2 * V <sub>CCI0</sub>	0.8 * V <sub>CCI0</sub>	8	-8
SSTL-15 Class II	_	V <sub>REF</sub> – 0.1	V <sub>REF</sub> + 0.1	_	V <sub>REF</sub> – 0.175	V <sub>REF</sub> + 0.175	0.2 * V <sub>CCI0</sub>	0.8 * V <sub>CCI0</sub>	16	-16
SSTL-135 Class I, II	_	V <sub>REF</sub> – 0.09	V <sub>REF</sub> + 0.09	—	V <sub>REF</sub> – 0.16	V <sub>REF</sub> + 0.16	0.2 * V <sub>CCI0</sub>	0.8 * V <sub>CCI0</sub>	—	_
SSTL-125 Class I, II		V <sub>REF</sub> – 0.85	V <sub>REF</sub> + 0.85	_	V <sub>REF</sub> – 0.15	V <sub>REF</sub> + 0.15	0.2 * V <sub>CCI0</sub>	0.8 * V <sub>CCI0</sub>		
SSTL-12 Class I, II	_	V <sub>REF</sub> – 0.1	V <sub>REF</sub> + 0.1	_	V <sub>REF</sub> – 0.15	V <sub>REF</sub> + 0.15	0.2 * V <sub>CCI0</sub>	0.8 * V <sub>CCI0</sub>	_	

- You typically use the interactive Excel-based Early Power Estimator before designing the FPGA to get a magnitude estimate of the device power. The Quartus II PowerPlay Power Analyzer provides better quality estimates based on the specifics of the design after you complete place-and-route. The PowerPlay Power Analyzer can apply a combination of user-entered, simulation-derived, and estimated signal activities that, when combined with detailed circuit models, yields very accurate power estimates.
- **\*** For more information about power estimation tools, refer to the *PowerPlay Early Power Estimator User Guide* and the *PowerPlay Power Analysis* chapter in the *Quartus II Handbook*.

Table 24 shows the maximum transmitter data rate for the clock network.

Table 24. Clock Network Maximum Data Rate Transmitter Specifications (1)

		ATX PLL			CMU PLL <sup>(2)</sup>	)	fPLL			
Clock Network	Non- bonded Mode (Gbps)	Bonded Mode (Gbps)	Channel Span	Non- bonded Mode (Gbps)	Bonded Mode (Gbps)	Channel Span	Non- bonded Mode (Gbps)	Bonded Mode (Gbps)	Channel Span	
x1 <sup>(3)</sup>	14.1	_	6	12.5	_	6	3.125	—	3	
x6 <sup>(3)</sup>	_	14.1	6	—	12.5	6	—	3.125	6	
x6 PLL Feedback <sup>(4)</sup>	_	14.1	Side- wide	_	12.5	Side- wide	_	_	_	
xN (PCIe)	_	8.0	8	—	5.0	8	—	—	—	
VNI (Native DHV ID)	8.0	8.0	Up to 13 channels above and below PLL	7 00	7 00	Up to 13 channels above	3 125	3 125	Up to 13 channels above	
	_	8.01 to 9.8304	Up to 7 channels above and below PLL	7.99	7.99	and below PLL	0.120	0.120	and below PLL	

Notes to Table 24:

(1) Valid data rates below the maximum specified in this table depend on the reference clock frequency and the PLL counter settings. Check the MegaWizard message during the PHY IP instantiation.

(2) ATX PLL is recommended at 8 Gbps and above data rates for improved jitter performance.

(3) Channel span is within a transceiver bank.

(4) Side-wide channel bonding is allowed up to the maximum supported by the PHY IP.

Mada (2)	Transceiver	PMA Width	20	20	16	16	10	10	8	8
	Speed Grade	PCS/Core Width	40	20	32	16	20	10	16	8
	1	C1, C2, C2L, I2, I2L core speed grade	12.2	11.4	9.76	9.12	6.5	5.8	5.2	4.72
	ŋ	C1, C2, C2L, I2, I2L core speed grade	12.2	11.4	9.76	9.12	6.5	5.8	5.2	4.72
	۷	C3, I3, I3L core speed grade	9.8	9.0	7.84	7.2	5.3	4.7	4.24	3.76
FIFO		C1, C2, C2L, I2, I2L core speed grade	8.5	8.5	8.5	8.5	6.5	5.8	5.2	4.72
	3	I3YY core speed grade	10.3125	10.3125	7.84	7.2	5.3	4.7	4.24	3.76
		C3, I3, I3L core speed grade	8.5	8.5	7.84	7.2	5.3	4.7	4.24	3.76
		C4, I4 core speed grade	8.5	8.2	7.04	6.56	4.8	4.2	3.84	3.44
	1	C1, C2, C2L, I2, I2L core speed grade	12.2	11.4	9.76	9.12	6.1	5.7	4.88	4.56
	ŋ	C1, C2, C2L, I2, I2L core speed grade	12.2	11.4	9.76	9.12	6.1	5.7	4.88	4.56
	۷	C3, I3, I3L core speed grade	9.8	9.0	7.92	7.2	4.9	4.5	3.96	3.6
Register		C1, C2, C2L, I2, I2L core speed grade	10.3125	10.3125	10.3125	10.3125	6.1	5.7	4.88	4.56
	3	I3YY core speed grade	10.3125	10.3125	7.92	7.2	4.9	4.5	3.96	3.6
	J	C3, I3, I3L core speed grade	8.5	8.5	7.92	7.2	4.9	4.5	3.96	3.6
	-	C4, I4 core speed grade	8.5	8.2	7.04	6.56	4.4	4.1	3.52	3.28

Table 25 shows the approximate maximum data rate using the standard PCS.

Table 25. Stratix V Standard PCS Approximate Maximum Date Rate (1), (3)

Notes to Table 25:

(1) The maximum data rate is in Gbps.

(2) The Phase Compensation FIFO can be configured in FIFO mode or register mode. In the FIFO mode, the pointers are not fixed, and the latency can vary. In the register mode the pointers are fixed for low latency.

(3) The maximum data rate is also constrained by the transceiver speed grade. Refer to Table 1 for the transceiver speed grade.

Table 27 shows the  $V_{\text{OD}}$  settings for the GX channel.

Symbol	V <sub>op</sub> Setting	V <sub>od</sub> Value (mV)	V <sub>op</sub> Setting	V <sub>op</sub> Value (mV)
	0 (1)	0	32	640
	1 (1)	20	33	660
	2 (1)	40	34	680
	3 (1)	60	35	700
	4 (1)	80	36	720
	5 <sup>(1)</sup>	100	37	740
	6	120	38	760
	7	140	39	780
	8	160	40	800
	9	180	41	820
	10	200	42	840
	11	220	43	860
	12	240	44	880
	13	260	45	900
	14	280	46	920
$V_{0D}$ differential peak to peak	15	300	47	940
typical <sup>(3)</sup>	16	320	48	960
	17	340	49	980
	18	360	50	1000
	19	380	51	1020
	20	400	52	1040
	21	420	53	1060
	22	440	54	1080
	23	460	55	1100
	24	480	56	1120
	25	500	57	1140
	26	520	58	1160
	27	540	59	1180
	28	560	60	1200
	29	580	61	1220
	30	600	62	1240
	31	620	63	1260

Table 27. Typical V\_{0D} Setting for GX Channel, TX Termination = 100  $\Omega^{\left(2\right)}$ 

#### Note to Table 27:

(1) If TX termination resistance =  $100\Omega$ , this VOD setting is illegal.

(2) The tolerance is +/-20% for all VOD settings except for settings 2 and below.

(3) Refer to Figure 2.

	Table 28.	<b>Transceiver S</b>	pecifications	for Stratix V	GT Devices	(Part 4 of 5) (1)
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Symbol/	Conditions	s	Transceive peed Grade	r 2	ר Sp	Fransceive Deed Grade	r 3	Unit	
Description		Min	Тур	Max	Min	Тур	Max		
Data rate	GT channels	19,600	_	28,050	19,600		25,780	Mbps	
Differential on-chip	GT channels	_	100	—		100	_	Ω	
termination resistors	GX channels				(8)				
	GT channels	_	500	_		500	_	mV	
V <sub>OCM</sub> (AC Coupled)	GX channels		•	•	(8)		•		
Dice/Fell time	GT channels	_	15	—	—	—	ps		
Rise/Fail lime	GX channels				(8)				
Intra-differential pair skew	GX channels				(8)				
Intra-transceiver block transmitter channel-to- channel skew	GX channels				(8)				
Inter-transceiver block transmitter channel-to- channel skew	GX channels				(8)				
CMU PLL									
Supported Data Range	—	600		12500	600		8500	Mbps	
t <sub>pll_powerdown</sub> <sup>(13)</sup>	—	1	—	—	1	_	—	μs	
t <sub>pll_lock</sub> <sup>(14)</sup>	—	_	—	10	_	_	10	μs	
ATX PLL									
	VCO post- divider L=2	8000	_	12500	8000	_	8500	Mbps	
	L=4	4000	—	6600	4000	_	6600	Mbps	
Supported Data Rate	L=8	2000	—	3300	2000	_	3300	Mbps	
Range for GX Channels	L=8, Local/Central Clock Divider =2	1000	_	1762.5	1000	_	1762.5	Mbps	
Supported Data Rate Range for GT Channels	VCO post- divider L=2	9800	_	14025	9800	_	12890	Mbps	
t <sub>pll_powerdown</sub> <sup>(13)</sup>	—	1	—	—	1	_	—	μs	
t <sub>pll_lock</sub> <sup>(14)</sup>	—	_	—	10	_	_	10	μs	
fPLL									
Supported Data Range		600		3250/ 3.125 <sup>(23)</sup>	600		3250/ 3.125 <sup>(23)</sup>	Mbps	
t <sub>pll_powerdown</sub> <sup>(13)</sup>	—	1	—	—	1	—	—	μs	

- XFI
- ASI
- HiGig/HiGig+
- HiGig2/HiGig2+
- Serial Data Converter (SDC)
- GPON
- SDI
- SONET
- Fibre Channel (FC)
- PCIe
- QPI
- SFF-8431

Download the Stratix V Characterization Report Tool to view the characterization report summary for these protocols.

### **Core Performance Specifications**

This section describes the clock tree, phase-locked loop (PLL), digital signal processing (DSP), memory blocks, configuration, and JTAG specifications.

### **Clock Tree Specifications**

Table 30 lists the clock tree specifications for Stratix V devices.

Table 30. Clock Tree Performance for Stratix V Devices (1)

	Performance								
Symbol	C1, C2, C2L, I2, and I2L	C3, I3, I3L, and I3YY	C4, I4	Unit					
Global and Regional Clock	717	650	580	MHz					
Periphery Clock	550	500	500	MHz					

#### Note to Table 30:

(1) The Stratix V ES devices are limited to 600 MHz core clock tree performance.

Symbol	Parameter	Min	Тур	Max	Unit
+ (3) (4)	Input clock cycle-to-cycle jitter ( $f_{REF} \ge 100 \text{ MHz}$ )			0.15	UI (p-p)
LINCCJ (0), (1)	Input clock cycle-to-cycle jitter (f <sub>REF</sub> < 100 MHz)	-750		+750	ps (p-p)
+ (5)	Period Jitter for dedicated clock output (f_{OUT} $\geq$ 100 MHz)	_	_	175 <sup>(1)</sup>	ps (p-p)
CUTPJ_DC	Period Jitter for dedicated clock output (f <sub>OUT</sub> < 100 MHz)	_	_	17.5 <sup>(1)</sup>	mUI (p-p)
+ (5)	Period Jitter for dedicated clock output in fractional PLL ( $f_{OUT} \ge 100 \text{ MHz}$ )	_	_	250 <sup>(11)</sup> , 175 <sup>(12)</sup>	ps (p-p)
<sup>L</sup> FOUTPJ_DC	Period Jitter for dedicated clock output in fractional PLL (f <sub>OUT</sub> < 100 MHz)	_	_	25 <sup>(11)</sup> , 17.5 <sup>(12)</sup>	mUI (p-p)
+ (5)	Cycle-to-Cycle Jitter for a dedicated clock output ( $f_{\text{OUT}} \geq 100 \text{ MHz})$		_	175	ps (p-p)
COUTCCJ_DC	Cycle-to-Cycle Jitter for a dedicated clock output $(f_{OUT} < 100 \text{ MHz})$		_	17.5	mUI (p-p)
+ (5)	Cycle-to-cycle Jitter for a dedicated clock output in fractional PLL ( $f_{OUT} \ge 100 \text{ MHz}$ )		_	250 <sup>(11)</sup> , 175 <sup>(12)</sup>	ps (p-p)
FOUTCCJ_DC	Cycle-to-cycle Jitter for a dedicated clock output in fractional PLL ( $f_{OUT} < 100 \text{ MHz}$ )+		_	25 <sup>(11)</sup> , 17.5 <sup>(12)</sup>	mUI (p-p)
t <sub>outpj 10</sub> (5),	Period Jitter for a clock output on a regular I/O in integer PLL ( $f_{OUT} \ge 100 \text{ MHz}$ )		_	600	ps (p-p)
(8)	Period Jitter for a clock output on a regular I/O $(f_{OUT} < 100 \text{ MHz})$		_	60	mUI (p-p)
t <sub>foutpj 10</sub> <sup>(5),</sup>	Period Jitter for a clock output on a regular I/O in fractional PLL ( $f_{OUT} \ge 100 \text{ MHz}$ )	_	_	600 <sup>(10)</sup>	ps (p-p)
(8), (11)	Period Jitter for a clock output on a regular I/O in fractional PLL (f <sub>OUT</sub> < 100 MHz)	_	_	60 <sup>(10)</sup>	mUI (p-p)
t <sub>outccj_io</sub> (5),	Cycle-to-cycle Jitter for a clock output on a regular I/O in integer PLL ( $f_{OUT} \geq 100 \mbox{ MHz})$	_	_	600	ps (p-p)
(8)	Cycle-to-cycle Jitter for a clock output on a regular I/O in integer PLL (f <sub>OUT</sub> < 100 MHz)	_	_	60 <sup>(10)</sup>	mUI (p-p)
t <sub>FOUTCCJ 10</sub> (5),	Cycle-to-cycle Jitter for a clock output on a regular I/O in fractional PLL ( $f_{OUT} \ge 100$ MHz)		_	600 <sup>(10)</sup>	ps (p-p)
(8), (11)	Cycle-to-cycle Jitter for a clock output on a regular I/O in fractional PLL (f <sub>OUT</sub> < 100 MHz)	_	_	60	mUI (p-p)
t <sub>CASC OUTPJ DC</sub>	Period Jitter for a dedicated clock output in cascaded PLLs ( $f_{OUT} \ge 100 \text{ MHz}$ )	_	_	175	ps (p-p)
(5), (6)	Period Jitter for a dedicated clock output in cascaded PLLs ( $f_{OUT}$ < 100 MHz)	_	_	17.5	mUI (p-p)
f <sub>DRIFT</sub>	Frequency drift after PFDENA is disabled for a duration of 100 $\mu s$		_	±10	%
dK <sub>BIT</sub>	Bit number of Delta Sigma Modulator (DSM)	8	24	32	Bits
k <sub>VALUE</sub>	Numerator of Fraction	128	8388608	2147483648	—

Table 31. PLL Specifications for Stratix V Devices (Part 2 of 3)

	0		C1		C2, C2L, I2, I2L			C3, I3, I3L, I3YY			C4,14			
Symbol	Conditions	Min	Тур	Max	Min	Тур	Max	Min	Тур	Max	Min	Тур	Max	Unit
t <sub>duty</sub>	Transmitter output clock duty cycle for both True and Emulated Differential I/O Standards	45	50	55	45	50	55	45	50	55	45	50	55	%
	True Differential I/O Standards	_	_	160	_	_	160	_	_	200	_	_	200	ps
t <sub>rise</sub> & t <sub>fall</sub>	Emulated Differential I/O Standards with three external output resistor networks			250			250			250			300	ps
	True Differential I/O Standards	_	_	150	_	_	150	_	_	150	_	_	150	ps
TCCS	Emulated Differential I/O Standards			300			300	_		300			300	ps
Receiver														
	SERDES factor J = 3 to 10 (11), (12), (13), (14), (15), (16)	150		1434	150	_	1434	150	_	1250	150	_	1050	Mbps
True Differential I/O Standards - f <sub>HSDRDPA</sub> (data rate)	SERDES factor J ≥ 4 LVDS RX with DPA (12), (14), (15), (16)	150	_	1600	150	_	1600	150	_	1600	150	_	1250	Mbps
	SERDES factor J = 2, uses DDR Registers	(6)		(7)	(6)	_	(7)	(6)	_	(7)	(6)	_	(7)	Mbps
	SERDES factor J = 1, uses SDR Register	(6)	_	(7)	(6)	_	(7)	(6)	_	(7)	(6)		(7)	Mbps

### Table 36. High-Speed I/O Specifications for Stratix V Devices (1), (2) (Part 3 of 4)

Speed Grade	Min	Max	Unit
C4,I4	8	16	ps

#### Table 40. DQS Phase Offset Delay Per Setting for Stratix V Devices <sup>(1), (2)</sup> (Part 2 of 2)

#### Notes to Table 40:

(1) The typical value equals the average of the minimum and maximum values.

(2) The delay settings are linear with a cumulative delay variation of 40 ps for all speed grades. For example, when using a -2 speed grade and applying a 10-phase offset setting to a 90° phase shift at 400 MHz, the expected average cumulative delay is [625 ps + (10 × 10 ps) ± 20 ps] = 725 ps ± 20 ps.

Table 41 lists the DQS phase shift error for Stratix V devices.

Table 41. DQS Phase Shift Error Specification for DLL-Delayed Clock (t<sub>DQS\_PSERR</sub>) for Stratix V Devices <sup>(1)</sup>

Number of DQS Delay Buffers	C1	C2, C2L, I2, I2L	C3, I3, I3L, I3YY	C4,14	Unit
1	28	28	30	32	ps
2	56	56	60	64	ps
3	84	84	90	96	ps
4	112	112	120	128	ps

Notes to Table 41:

(1) This error specification is the absolute maximum and minimum error. For example, skew on three DQS delay buffers in a -2 speed grade is  $\pm 78$  ps or  $\pm 39$  ps.

Table 42 lists the memory output clock jitter specifications for Stratix V devices.

Table 42. Memory Output Clock Jitter Specification for Stratix V Devices (1	<sup>),</sup> (Part 1 of 2) <sup>(2), (3)</sup>
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Clock	Parameter Symbol		C1 C2, C2L, I2,		, 12, 12L	C3, I3, I3L, I3YY		C4,14		Unit	
NELWURK		-	Min	Max	Min	Max	Min	Max	Min	Max	
	Clock period jitter	$t_{JIT(per)}$	-50	50	-50	50	-55	55	-55	55	ps
Regional	Cycle-to-cycle period jitter	$t_{\text{JIT(cc)}}$	-100	100	-100	100	-110	110	-110	110	ps
	Duty cycle jitter	$t_{JIT(duty)}$	-50	50	-50	50	-82.5	82.5	-82.5	82.5	ps
	Clock period jitter	$t_{JIT(per)}$	-75	75	-75	75	-82.5	82.5	-82.5	82.5	ps
Global	Cycle-to-cycle period jitter	$t_{\text{JIT(cc)}}$	-150	150	-150	150	-165	165	-165	165	ps
	Duty cycle jitter	$t_{JIT(duty)}$	-75	75	-75	75	-90	90	-90	90	ps

Clock	Parameter Symbol		C	C1 C2, C2L, I2, I2L		C3, I3, I3L, I3YY		C4,14		Unit	
NELWUIK		-	Min	Max	Min	Max	Min	Max	Min	Max	
	Clock period jitter	$t_{JIT(per)}$	-25	25	-25	25	-30	30	-35	35	ps
PHY Clock	Cycle-to-cycle period jitter	$t_{\rm JIT(cc)}$	-50	50	-50	50	-60	60	-70	70	ps
	Duty cycle jitter	$t_{JIT(duty)}$	-37.5	37.5	-37.5	37.5	-45	45	-56	56	ps

#### Table 42. Memory Output Clock Jitter Specification for Stratix V Devices (1), (Part 2 of 2) (2), (3)

#### Notes to Table 42:

(1) The clock jitter specification applies to the memory output clock pins generated using differential signal-splitter and DDIO circuits clocked by a PLL output routed on a PHY, regional, or global clock network as specified. Altera recommends using PHY clock networks whenever possible.

(2) The clock jitter specification applies to the memory output clock pins clocked by an integer PLL.

(3) The memory output clock jitter is applicable when an input jitter of 30 ps peak-to-peak is applied with bit error rate (BER) -12, equivalent to 14 sigma.

### **OCT Calibration Block Specifications**

Table 43 lists the OCT calibration block specifications for Stratix V devices.

#### Table 43. OCT Calibration Block Specifications for Stratix V Devices

Symbol	Description	Min	Тур	Max	Unit
OCTUSRCLK	Clock required by the OCT calibration blocks	—	_	20	MHz
T <sub>OCTCAL</sub>	Number of OCTUSRCLK clock cycles required for OCT $\rm R_S/R_T$ calibration		1000	_	Cycles
T <sub>OCTSHIFT</sub>	Number of OCTUSRCLK clock cycles required for the OCT code to shift out	_	32	_	Cycles
T <sub>RS_RT</sub>	Time required between the dyn_term_ctrl and oe signal transitions in a bidirectional I/O buffer to dynamically switch between OCT $R_S$ and $R_T$ (Figure 10)		2.5		ns

Figure 10 shows the timing diagram for the oe and dyn\_term\_ctrl signals.

#### Figure 10. Timing Diagram for oe and dyn\_term\_ctrl Signals



Mombor			Active Serial <sup>(1)</sup>	)	Fast Passive Parallel <sup>(2)</sup>			
Variant	Code	Width	DCLK (MHz)	Min Config Time (s)	Width	DCLK (MHz)	Min Config Time (s)	
	D3	4	100	0.344	32	100	0.043	
	D4	4	100	0.534	32	100	0.067	
68	04	4	100	0.344	32	100	0.043	
03	D5	4	100	0.534	32	100	0.067	
	D6	4	100	0.741	32	100	0.093	
	D8	4	100	0.741	32	100	0.093	
E	E9	4	100	0.857	32	100	0.107	
Ľ	EB	4	100	0.857	32	100	0.107	

Table 48. Minimum Configuration Time Estimation for Stratix V Devices

#### Notes to Table 48:

(1) DCLK frequency of 100 MHz using external CLKUSR.

(2) Max FPGA FPP bandwidth may exceed bandwidth available from some external storage or control logic.

# **Fast Passive Parallel Configuration Timing**

This section describes the fast passive parallel (FPP) configuration timing parameters for Stratix V devices.

### DCLK-to-DATA[] Ratio for FPP Configuration

FPP configuration requires a different DCLK-to-DATA[]ratio when you enable the design security, decompression, or both features. Table 49 lists the DCLK-to-DATA[]ratio for each combination.

Configuration Scheme	Decompression	Design Security	DCLK-to-DATA[] Ratio
	Disabled	Disabled	1
	Disabled	Enabled	1
111 ×0	Enabled	Disabled	2
	Enabled	Enabled	2
	Disabled	Disabled	1
	Disabled	Enabled	2
	Enabled	Disabled	4
	Enabled	Enabled	4

 Table 49. DCLK-to-DATA[] Ratio <sup>(1)</sup> (Part 1 of 2)

### FPP Configuration Timing when DCLK-to-DATA [] = 1

Figure 12 shows the timing waveform for FPP configuration when using a MAX II or MAX V device as an external host. This waveform shows timing when the DCLK-to-DATA[] ratio is 1.





#### Notes to Figure 12:

- (1) Use this timing waveform when the DCLK-to-DATA [] ratio is 1.
- (2) The beginning of this waveform shows the device in user mode. In user mode, nCONFIG, nSTATUS, and CONF\_DONE are at logic-high levels. When nCONFIG is pulled low, a reconfiguration cycle begins.
- (3) After power-up, the Stratix V device holds nstatus low for the time of the POR delay.
- (4) After power-up, before and during configuration, CONF\_DONE is low.
- (5) Do not leave DCLK floating after configuration. DCLK is ignored after configuration is complete. It can toggle high or low if required.
- (6) For FPP ×16, use DATA [15..0]. For FPP ×8, use DATA [7..0]. DATA [31..0] are available as a user I/O pin after configuration. The state of this pin depends on the dual-purpose pin settings.
- (7) To ensure a successful configuration, send the entire configuration data to the Stratix V device. CONF\_DONE is released high when the Stratix V device receives all the configuration data successfully. After CONF\_DONE goes high, send two additional falling edges on DCLK to begin initialization and enter user mode.
- (8) After the option bit to enable the INIT\_DONE pin is configured into the device, the INIT DONE goes low.

Table 50 lists the timing parameters for Stratix V devices for FPP configuration when the DCLK-to-DATA[] ratio is 1.

Table 50. FPP Timing Parameters for Stratix V Devices (1)

Symbol	Parameter	Minimum	Maximum	Units
t <sub>CF2CD</sub>	nCONFIG low to CONF_DONE low	—	600	ns
t <sub>CF2ST0</sub>	nCONFIG low to nSTATUS low		600	ns
t <sub>CFG</sub>	nCONFIG low pulse width	2		μS
t <sub>status</sub>	nSTATUS low pulse width	268	1,506 <sup>(2)</sup>	μS
t <sub>CF2ST1</sub>	nCONFIG high to nSTATUS high	—	1,506 <sup>(3)</sup>	μS
t <sub>CF2CK</sub> (6)	nCONFIG high to first rising edge on DCLK	1,506		μS
t <sub>ST2CK</sub> (6)	nSTATUS high to first rising edge of DCLK	2		μS
t <sub>DSU</sub>	DATA [] setup time before rising edge on DCLK	5.5	_	ns
t <sub>DH</sub>	DATA [] hold time after rising edge on DCLK	0	_	ns
t <sub>CH</sub>	DCLK high time	$0.45\times1/f_{MAX}$		S
t <sub>CL</sub>	DCLK low time	$0.45\times1/f_{MAX}$	_	S
t <sub>CLK</sub>	DCLK period	1/f <sub>MAX</sub>		S
4	DCLK frequency (FPP ×8/×16)	—	125	MHz
IMAX	DCLK frequency (FPP ×32)	—	100	MHz
t <sub>CD2UM</sub>	CONF_DONE high to user mode <sup>(4)</sup>	175	437	μS
+	CONTR DOWN high to CT WARD analysis	4 × maximum		
LCD2CU	CONF_DONE HIGH to CLEOSE enabled	DCLK period	—	_
t <sub>cD2UMC</sub>	CONF_DONE high to user mode with CLKUSR option on	$\begin{array}{c} t_{\text{CD2CU}} + \\ (8576 \times \text{CLKUSR} \\ \text{period}) \ ^{(5)} \end{array}$		_

#### Notes to Table 50:

(1) Use these timing parameters when the decompression and design security features are disabled.

(2) This value is applicable if you do not delay configuration by extending the nCONFIG or nSTATUS low pulse width.

(3) This value is applicable if you do not delay configuration by externally holding the nSTATUS low.

- (4) The minimum and maximum numbers apply only if you chose the internal oscillator as the clock source for initializing the device.
- (5) To enable the CLKUSR pin as the initialization clock source and to obtain the maximum frequency specification on these pins, refer to the Initialization section of the "Configuration, Design Security, and Remote System Upgrades in Stratix V Devices" chapter.
- (6) If nSTATUS is monitored, follow the t<sub>ST2CK</sub> specification. If nSTATUS is not monitored, follow the t<sub>CF2CK</sub> specification.

### FPP Configuration Timing when DCLK-to-DATA [] > 1

Figure 13 shows the timing waveform for FPP configuration when using a MAX II device, MAX V device, or microprocessor as an external host. This waveform shows timing when the DCLK-to-DATA [] ratio is more than 1.

Symbol	Parameter	Minimum	Maximum	Units
t <sub>CD2UM</sub>	CONF_DONE high to user mode $(3)$	175	437	μS
t <sub>CD2CU</sub>	CONF_DONE high to CLKUSR enabled	4 × maximum DCLK period	_	—
t <sub>CD2UMC</sub>	CONF_DONE high to user mode with CLKUSR option on	t <sub>cd2cu</sub> + (8576 × clkusr period)	_	—

Table 53. AS Timing Parameters for AS  $\times$ 1 and AS  $\times$ 4 Configurations in Stratix V Devices <sup>(1), (2)</sup> (Part 2 of 2)

#### Notes to Table 53:

(1) The minimum and maximum numbers apply only if you choose the internal oscillator as the clock source for initializing the device.

(2) t<sub>CF2CD</sub>, t<sub>CF2ST0</sub>, t<sub>CF2ST0</sub>, t<sub>CF6</sub>, t<sub>STATUS</sub>, and t<sub>CF2ST1</sub> timing parameters are identical to the timing parameters for PS mode listed in Table 54 on page 63.

(3) To enable the CLKUSR pin as the initialization clock source and to obtain the maximum frequency specification on this pin, refer to the Initialization section of the "Configuration, Design Security, and Remote System Upgrades in Stratix V Devices" chapter.

## **Passive Serial Configuration Timing**

Figure 15 shows the timing waveform for a passive serial (PS) configuration when using a MAX II device, MAX V device, or microprocessor as an external host.

Figure 15. PS Configuration Timing Waveform <sup>(1)</sup>



#### Notes to Figure 15:

- (1) The beginning of this waveform shows the device in user mode. In user mode, nCONFIG, nSTATUS, and CONF\_DONE are at logic high levels. When nCONFIG is pulled low, a reconfiguration cycle begins.
- (2) After power-up, the Stratix V device holds nSTATUS low for the time of the POR delay.
- (3) After power-up, before and during configuration, CONF DONE is low.
- (4) Do not leave DCLK floating after configuration. You can drive it high or low, whichever is more convenient.
- (5) DATAO is available as a user I/O pin after configuration. The state of this pin depends on the dual-purpose pin settings in the **Device and Pins Option**.
- (6) To ensure a successful configuration, send the entire configuration data to the Stratix V device. CONF\_DONE is released high after the Stratix V device receives all the configuration data successfully. After CONF\_DONE goes high, send two additional falling edges on DCLK to begin initialization and enter user mode.
- (7) After the option bit to enable the INIT DONE pin is configured into the device, the INIT DONE goes low.

Table 54 lists the PS configuration timing parameters for Stratix V devices.

Table 54. PS Timing Parameters for Stratix V Devices

Symbol	Parameter	Minimum	Maximum	Units
t <sub>CF2CD</sub>	nCONFIG low to CONF_DONE low	—	600	ns
t <sub>CF2ST0</sub>	nCONFIG low to nSTATUS low	—	600	ns
t <sub>CFG</sub>	nCONFIG low pulse width	2	—	μS
t <sub>status</sub>	nSTATUS low pulse width	268	1,506 <sup>(1)</sup>	μS
t <sub>CF2ST1</sub>	nCONFIG high to nSTATUS high	—	1,506 <sup>(2)</sup>	μS
t <sub>CF2CK</sub> (5)	nCONFIG high to first rising edge on DCLK	1,506	—	μS
t <sub>ST2CK</sub> (5)	nSTATUS high to first rising edge of DCLK	2	—	μS
t <sub>DSU</sub>	DATA[] setup time before rising edge on DCLK	5.5	—	ns
t <sub>DH</sub>	DATA [] hold time after rising edge on DCLK	0	—	ns
t <sub>CH</sub>	DCLK high time	$0.45\times 1/f_{MAX}$	—	S
t <sub>CL</sub>	DCLK low time	$0.45\times 1/f_{MAX}$	—	S
t <sub>CLK</sub>	DCLK period	1/f <sub>MAX</sub>	—	S
f <sub>MAX</sub>	DCLK frequency	—	125	MHz
t <sub>CD2UM</sub>	CONF_DONE high to user mode <sup>(3)</sup>	175	437	μS
t <sub>CD2CU</sub>	CONF_DONE high to CLKUSR enabled	4 × maximum DCLK period	_	_
t <sub>cd2UMC</sub>	CONF_DONE high to user mode with CLKUSR option on	$t_{CD2CU}$ + (8576 × CLKUSR period) <sup>(4)</sup>	_	_

#### Notes to Table 54:

(1) This value is applicable if you do not delay configuration by extending the nCONFIG or nSTATUS low pulse width.

(2) This value is applicable if you do not delay configuration by externally holding the nSTATUS low.

(3) The minimum and maximum numbers apply only if you choose the internal oscillator as the clock source for initializing the device.

(4) To enable the CLKUSR pin as the initialization clock source and to obtain the maximum frequency specification on these pins, refer to the "Initialization" section.

(5) If nSTATUS is monitored, follow the t<sub>ST2CK</sub> specification. If nSTATUS is not monitored, follow the t<sub>CF2CK</sub> specification.

### Initialization

Table 55 lists the initialization clock source option, the applicable configuration schemes, and the maximum frequency.

Table 55.	Initialization	<b>Clock Source</b>	e Option	and the	Maximum	Frequency

Initialization Clock Source	Configuration Schemes	Maximum Frequency	Minimum Number of Clock Cycles <sup>(1)</sup>
Internal Oscillator	AS, PS, FPP	12.5 MHz	
CLKUSR	AS, PS, FPP <sup>(2)</sup>	125 MHz	8576
DCLK	PS, FPP	125 MHz	

#### Notes to Table 55:

(1) The minimum number of clock cycles required for device initialization.

(2) To enable CLKUSR as the initialization clock source, turn on the Enable user-supplied start-up clock (CLKUSR) option in the Quartus II software from the General panel of the Device and Pin Options dialog box.