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### Intel - 5SGXMA3H1F35C2LN Datasheet



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#### Understanding <u>Embedded - FPGAs (Field</u> <u>Programmable Gate Array)</u>

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

#### **Applications of Embedded - FPGAs**

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

#### Details

Product Status	Obsolete
Number of LABs/CLBs	128300
Number of Logic Elements/Cells	340000
Total RAM Bits	19456000
Number of I/O	600
Number of Gates	-
Voltage - Supply	0.82V ~ 0.88V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	1152-BBGA, FCBGA
Supplier Device Package	1152-FBGA (35x35)
Purchase URL	https://www.e-xfl.com/product-detail/intel/5sgxma3h1f35c2In

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This section lists the functional operating limits for the AC and DC parameters for Stratix V devices. Table 6 lists the steady-state voltage and current values expected from Stratix V devices. Power supply ramps must all be strictly monotonic, without plateaus.

Table 6. Recommended Operating Conditions for Stratix V Devices (Part 1 of 2)

Symbol	Description	Condition	Min <sup>(4)</sup>	Тур	Max <sup>(4)</sup>	Unit
	Core voltage and periphery circuitry power supply (C1, C2, I2, and I3YY speed grades)	_	0.87	0.9	0.93	V
V <sub>CC</sub>	Core voltage and periphery circuitry power supply (C2L, C3, C4, I2L, I3, I3L, and I4 speed grades) <sup>(3)</sup>		0.82	0.85	0.88	V
V <sub>CCPT</sub>	Power supply for programmable power technology	_	1.45	1.50	1.55	V
V <sub>CC_AUX</sub>	Auxiliary supply for the programmable power technology		2.375	2.5	2.625	V
VI (1)	I/O pre-driver (3.0 V) power supply	_	2.85	3.0	3.15	V
VCCPD	I/O pre-driver (2.5 V) power supply		2.375	2.5	2.625	V
	I/O buffers (3.0 V) power supply	_	2.85	3.0	3.15	V
	I/O buffers (2.5 V) power supply		2.375	2.5	2.625	V
V <sub>CCIO</sub>	I/O buffers (1.8 V) power supply	_	1.71	1.8	1.89	V
	I/O buffers (1.5 V) power supply	_	1.425	1.5	1.575	V
	I/O buffers (1.35 V) power supply		1.283	1.35	1.45	V
	I/O buffers (1.25 V) power supply	_	1.19	1.25	1.31	V
	I/O buffers (1.2 V) power supply	_	1.14	1.2	1.26	V
	Configuration pins (3.0 V) power supply		2.85	3.0	3.15	V
V <sub>CCPGM</sub>	Configuration pins (2.5 V) power supply	_	2.375	2.5	2.625	V
	Configuration pins (1.8 V) power supply	-	1.71	1.8	1.89	V
V <sub>CCA_FPLL</sub>	PLL analog voltage regulator power supply		2.375	2.5	2.625	V
V <sub>CCD_FPLL</sub>	PLL digital voltage regulator power supply	-	1.45	1.5	1.55	V
V <sub>CCBAT</sub> (2)	Battery back-up power supply (For design security volatile key register)	_	1.2	_	3.0	V
VI	DC input voltage	_	-0.5	—	3.6	V
V <sub>0</sub>	Output voltage		0	_	V <sub>CCIO</sub>	V
т	Operating junction temperature	Commercial	0	—	85	°C
IJ		Industrial	-40	_	100	°C

				Calibration Accuracy						
Symbol	Description	Conditions	C1	C2,I2	C3,I3, I3YY	C4,14	Unit			
50-Ω R <sub>S</sub>	Internal series termination with calibration (50- $\Omega$ setting)	V <sub>CCI0</sub> = 3.0, 2.5, 1.8, 1.5, 1.2 V	±15	±15	±15	±15	%			
34- $\Omega$ and 40- $\Omega$ R <sub>S</sub>	Internal series termination with calibration (34- $\Omega$ and 40- $\Omega$ setting)	V <sub>CCI0</sub> = 1.5, 1.35, 1.25, 1.2 V	±15	±15	±15	±15	%			
48-Ω, 60-Ω, 80-Ω, and 240-Ω R <sub>S</sub>	Internal series termination with calibration (48- $\Omega$ , 60- $\Omega$ , 80- $\Omega$ , and 240- $\Omega$ setting)	V <sub>CCI0</sub> = 1.2 V	±15	±15	±15	±15	%			
50-Ω R <sub>T</sub>	Internal parallel termination with calibration (50-Ω setting)	V <sub>CCI0</sub> = 2.5, 1.8, 1.5, 1.2 V	-10 to +40	-10 to +40	-10 to +40	-10 to +40	%			
20-Ω, 30-Ω, 40-Ω,60-Ω, and 120-Ω R <sub>T</sub>	Internal parallel termination with calibration ( $20 - \Omega$ , $30 - \Omega$ , $40 - \Omega$ , $60 - \Omega$ , and $120 - \Omega$ setting)	V <sub>CCI0</sub> = 1.5, 1.35, 1.25 V	-10 to +40	-10 to +40	-10 to +40	-10 to +40	%			
60- $Ω$ and 120- $Ω$ R <sub>T</sub>	Internal parallel termination with calibration (60-Ω and 120-Ω setting)	V <sub>CCI0</sub> = 1.2	-10 to +40	-10 to +40	-10 to +40	-10 to +40	%			
$25-\Omega \\ R_{S\_left\_shift}$	Internal left shift series termination with calibration ( $25-\Omega$ R <sub>S_left_shift</sub> setting)	V <sub>CCI0</sub> = 3.0, 2.5, 1.8, 1.5, 1.2 V	±15	±15	±15	±15	%			

Table II. OUI Valiblation Accuracy specifications for Stratix V Devices' / (Latt 2 OF	Table 11.	<b>OCT Calibration A</b>	ccuracy Specificati	ons for Stratix V D	Devices <sup>(1)</sup> (	Part 2 of
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#### Note to Table 11:

(1) OCT calibration accuracy is valid at the time of calibration only.

Table 12 lists the Stratix V OCT without calibration resistance to PVT changes.

Table 12.	OCT Without Calibration	<b>Resistance</b> 1	<b>Tolerance</b>	<b>Specifications</b>	for Stratix	<b>V</b> Devices	(Part 1	of 2)
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			<b>Resistance Tolerance</b>					
Symbol	Description	Conditions	C1	C2,I2	C3, I3, I3YY	C4, I4	Unit	
25-Ω R, 50-Ω R <sub>S</sub>	Internal series termination without calibration (25-Ω setting)	$V_{CCIO} = 3.0$ and 2.5 V	±30	±30	±40	±40	%	
25-Ω R <sub>S</sub>	Internal series termination without calibration (25-Ω setting)	V <sub>CCI0</sub> = 1.8 and 1.5 V	±30	±30	±40	±40	%	
25-Ω R <sub>S</sub>	Internal series termination without calibration (25-Ω setting)	V <sub>CCI0</sub> = 1.2 V	±35	±35	±50	±50	%	

#### **Internal Weak Pull-Up Resistor**

Table 16 lists the weak pull-up resistor values for Stratix V devices.

Symbol	Description	V <sub>CCIO</sub> Conditions (V) <sup>(3)</sup>	Value <sup>(4)</sup>	Unit		
		3.0 ±5%	25	kΩ		
Vali		2.5 ±5% 25				
	Value of the I/O pin pull-up resistor before	1.8 ±5%	25	kΩ		
R <sub>PU</sub>	and during configuration, as well as user mode if you enable the programmable	1.5 ±5%	25	kΩ		
	pull-up resistor option.	1.35 ±5%	25	kΩ		
		1.25 ±5%	25	kΩ		
		1.2 ±5%	25	kΩ		

Table 16. Internal Weak Pull-Up Resistor for Stratix V Devices (1), (2)

Notes to Table 16:

(1) All I/O pins have an option to enable the weak pull-up resistor except the configuration, test, and JTAG pins.

(2) The internal weak pull-down feature is only available for the JTAG TCK pin. The typical value for this internal weak pull-down resistor is approximately 25 k $\Omega$ .

- (3) The pin pull-up resistance values may be lower if an external source drives the pin higher than V<sub>CCIO</sub>.
- (4) These specifications are valid with a  $\pm 10\%$  tolerance to cover changes over PVT.

### I/O Standard Specifications

Table 17 through Table 22 list the input voltage (V<sub>IH</sub> and V<sub>IL</sub>), output voltage (V<sub>OH</sub> and V<sub>OL</sub>), and current drive characteristics (I<sub>OH</sub> and I<sub>OL</sub>) for various I/O standards supported by Stratix V devices. These tables also show the Stratix V device family I/O standard specifications. The V<sub>OL</sub> and V<sub>OH</sub> values are valid at the corresponding I<sub>OH</sub> and I<sub>OL</sub>, respectively.

For an explanation of the terms used in Table 17 through Table 22, refer to "Glossary" on page 65. For tolerance calculations across all SSTL and HSTL I/O standards, refer to Altera knowledge base solution rd07262012\_486.

I/O		V <sub>ccio</sub> (V)		VII	V <sub>IL</sub> (V)         V <sub>IH</sub> (V)         V <sub>OL</sub> (V)		V <sub>OH</sub> (V)	I <sub>OL</sub>	I <sub>oh</sub>		
Standard	Min	Тур	Max	Min	Max	Min	Max	Max	Min	(mA)	(mA)
LVTTL	2.85	3	3.15	-0.3	0.8	1.7	3.6	0.4	2.4	2	-2
LVCMOS	2.85	3	3.15	-0.3	0.8	1.7	3.6	0.2	$V_{CCIO} - 0.2$	0.1	-0.1
2.5 V	2.375	2.5	2.625	-0.3	0.7	1.7	3.6	0.4	2	1	-1
1.8 V	1.71	1.8	1.89	-0.3	0.35 * V <sub>CCIO</sub>	0.65 * V <sub>CCIO</sub>	V <sub>CCI0</sub> + 0.3	0.45	V <sub>CCI0</sub> – 0.45	2	-2
1.5 V	1.425	1.5	1.575	-0.3	0.35 * V <sub>CCI0</sub>	0.65 * V <sub>CCI0</sub>	V <sub>CCI0</sub> + 0.3	0.25 * V <sub>CCIO</sub>	0.75 * V <sub>CCIO</sub>	2	-2
1.2 V	1.14	1.2	1.26	-0.3	0.35 * V <sub>CCI0</sub>	0.65 * V <sub>CCI0</sub>	V <sub>CCI0</sub> + 0.3	0.25 * V <sub>CCIO</sub>	0.75 * V <sub>CCIO</sub>	2	-2

Table 17. Single-Ended I/O Standards for Stratix V Devices

I/O Standard	V <sub>IL(DI</sub>	<sub>c)</sub> (V)	V <sub>IH(D</sub>	<sub>C)</sub> (V)	V <sub>IL(AC)</sub> (V)	V <sub>IH(AC)</sub> (V)	V <sub>ol</sub> (V)	V <sub>oh</sub> (V)	I (mA)	l <sub>oh</sub>
i/U Stanuaru	Min	Max	Min	Max	Max	Min	Max	Min	i <sub>ol</sub> (IIIA)	(mA)
HSTL-18 Class I	—	V <sub>REF</sub> – 0.1	V <sub>REF</sub> + 0.1	_	$V_{REF} - 0.2$	V <sub>REF</sub> + 0.2	0.4	V <sub>CCI0</sub> – 0.4	8	-8
HSTL-18 Class II	_	V <sub>REF</sub> – 0.1	V <sub>REF</sub> + 0.1	_	V <sub>REF</sub> - 0.2	V <sub>REF</sub> + 0.2	0.4	V <sub>CCI0</sub> – 0.4	16	-16
HSTL-15 Class I	_	V <sub>REF</sub> – 0.1	V <sub>REF</sub> + 0.1	_	V <sub>REF</sub> - 0.2	V <sub>REF</sub> + 0.2	0.4	V <sub>CCI0</sub> – 0.4	8	-8
HSTL-15 Class II	_	V <sub>REF</sub> – 0.1	V <sub>REF</sub> + 0.1	_	V <sub>REF</sub> - 0.2	V <sub>REF</sub> + 0.2	0.4	V <sub>CCI0</sub> – 0.4	16	-16
HSTL-12 Class I	-0.15	V <sub>REF</sub> - 0.08	V <sub>REF</sub> + 0.08	V <sub>CCIO</sub> + 0.15	V <sub>REF</sub> – 0.15	V <sub>REF</sub> + 0.15	0.25* V <sub>CCI0</sub>	0.75* V <sub>CCI0</sub>	8	-8
HSTL-12 Class II	-0.15	V <sub>REF</sub> - 0.08	V <sub>REF</sub> + 0.08	V <sub>CCIO</sub> + 0.15	V <sub>REF</sub> – 0.15	V <sub>REF</sub> + 0.15	0.25* V <sub>CCI0</sub>	0.75* V <sub>CCI0</sub>	16	-16
HSUL-12	—	V <sub>REF</sub> - 0.13	V <sub>REF</sub> + 0.13	_	V <sub>REF</sub> – 0.22	V <sub>REF</sub> + 0.22	0.1* V <sub>CCIO</sub>	0.9* V <sub>CCI0</sub>	_	

#### Table 19. Single-Ended SSTL, HSTL, and HSUL I/O Standards Signal Specifications for Stratix V Devices (Part 2 of 2)

Table 20. Differential SSTL I/O Standards for Stratix V Devices

1/0 Standard		V <sub>ccio</sub> (V)		V <sub>SWIN</sub>	V <sub>SWING(DC)</sub> (V)		V <sub>X(AC)</sub> (V)		V <sub>SWING(</sub>	<sub>AC)</sub> (V)
ijo Stanuaru	Min	Тур	Max	Min	Max	Min	Тур	Max	Min	Max
SSTL-2 Class I, II	2.375	2.5	2.625	0.3	V <sub>CCI0</sub> + 0.6	V <sub>CCI0</sub> /2- 0.2	_	V <sub>CCI0</sub> /2 + 0.2	0.62	V <sub>CCI0</sub> + 0.6
SSTL-18 Class I, II	1.71	1.8	1.89	0.25	V <sub>CCIO</sub> + 0.6	V <sub>CCI0</sub> /2- 0.175	_	V <sub>CCI0</sub> /2 + 0.175	0.5	V <sub>CCI0</sub> + 0.6
SSTL-15 Class I, II	1.425	1.5	1.575	0.2	(1)	V <sub>CCI0</sub> /2- 0.15	_	V <sub>CCI0</sub> /2 + 0.15	0.35	_
SSTL-135 Class I, II	1.283	1.35	1.45	0.2	(1)	V <sub>CCI0</sub> /2- 0.15	V <sub>CCI0</sub> /2	V <sub>CCI0</sub> /2 + 0.15	2(V <sub>IH(AC)</sub> - V <sub>REF</sub> )	2(V <sub>IL(AC)</sub> - V <sub>REF</sub> )
SSTL-125 Class I, II	1.19	1.25	1.31	0.18	(1)	V <sub>CCI0</sub> /2- 0.15	V <sub>CCI0</sub> /2	V <sub>CCI0</sub> /2 + 0.15	2(V <sub>IH(AC)</sub> - V <sub>REF</sub> )	_
SSTL-12 Class I, II	1.14	1.2	1.26	0.18	_	V <sub>REF</sub> 0.15	V <sub>CCI0</sub> /2	V <sub>REF</sub> + 0.15	-0.30	0.30

Note to Table 20:

(1) The maximum value for  $V_{SWING(DC)}$  is not defined. However, each single-ended signal needs to be within the respective single-ended limits  $(V_{IH(DC)} \text{ and } V_{IL(DC)})$ .

							· · · · ·						
I/O	V <sub>CCIO</sub> (V)			V <sub>DIF(DC)</sub> (V)		V <sub>X(AC)</sub> (V)				V <sub>CM(DC)</sub> (V	V <sub>DIF(AC)</sub> (V)		
Standard	Min	Тур	Max	Min	Max	Min	Тур	Max	Min	Тур	Max	Min	Max
HSTL-18 Class I, II	1.71	1.8	1.89	0.2	_	0.78	_	1.12	0.78	_	1.12	0.4	_
HSTL-15 Class I, II	1.425	1.5	1.575	0.2	_	0.68	_	0.9	0.68		0.9	0.4	_

# **Switching Characteristics**

This section provides performance characteristics of the Stratix V core and periphery blocks.

These characteristics can be designated as Preliminary or Final.

- Preliminary characteristics are created using simulation results, process data, and other known parameters. The title of these tables show the designation as "Preliminary."
- Final numbers are based on actual silicon characterization and testing. The numbers reflect the actual performance of the device under worst-case silicon process, voltage, and junction temperature conditions. There are no designations on finalized tables.

# **Transceiver Performance Specifications**

This section describes transceiver performance specifications.

Table 23 lists the Stratix V GX and GS transceiver specifications.

Table 23.	Transceiver 3	Specifications	for Stratix	V GX	and GS	Devices	(1)	(Part 1	nf 7	۱
Table 20.	TIANSUCIACI	opeonitionationa	IUI UIIAIIA	I UA	anu uu	DEVICES	• •	(1 61 6 1		

Symbol/	Conditions	Transceiver Speed Grade 1		Transceiver Speed Grade 2			Trai	Unit				
Description		Min	Тур	Max	Min	Тур	Max	Min	Тур	Max		
Reference Clock												
Supported I/O	Dedicated reference clock pin	1.2-V	PCML,	1.4-V PCM	IL, 1.5-∖	/ PCML	, 2.5-V PCN HCSL	1L, Diffe	rential	LVPECL, L\	/DS, and	
Standards	RX reference clock pin		1.4-V PCML, 1.5-V PCML, 2.5-V PCML, LVPECL, and LVDS									
Input Reference Clock Frequency (CMU PLL) <sup>(8)</sup>	_	40		710	40	_	710	40	_	710	MHz	
Input Reference Clock Frequency (ATX PLL) <sup>(8)</sup>		100		710	100		710	100		710	MHz	
Rise time	Measure at ±60 mV of differential signal <sup>(26)</sup>			400	_		400			400	- ps	
Fall time	Measure at ±60 mV of differential signal <sup>(26)</sup>		_	400	_		400			400		
Duty cycle		45		55	45		55	45	—	55	%	
Spread-spectrum modulating clock frequency	PCI Express® (PCIe <sup>®</sup> )	30		33	30		33	30	_	33	kHz	

Symbol/	Conditions	s	Transceive peed Grade	r 2	S	Transceive peed Grade	r 3	Unit			
Description		Min	Тур	Max	Min	Тур	Max				
Reference Clock								1			
Supported I/O Standards	Dedicated reference clock pin	1.2-V PCN	IL, 1.4-V PC	ML, 1.5-V P(	CML, 2.5-V I and HCSL	PCML, Diffe	rential LVPE	ECL, LVDS,			
otanuarus	RX reference clock pin		1.4-V PCML, 1.5-V PCML, 2.5-V PCML, LVPECL, and LVDS								
Input Reference Clock Frequency (CMU PLL) <sup>(6)</sup>	_	40	_	710	40	_	710	MHz			
Input Reference Clock Frequency (ATX PLL) <sup>(6)</sup>	_	100	_	710	100	_	710	MHz			
Rise time	20% to 80%	_		400	_	_	400				
Fall time	80% to 20%			400	—	_	400	ps			
Duty cycle	—	45	_	55	45	_	55	%			
Spread-spectrum modulating clock frequency	PCI Express (PCIe)	30	_	33	30	_	33	kHz			
Spread-spectrum downspread	PCle	_	0 to -0.5	_	_	0 to -0.5	_	%			
On-chip termination resistors <sup>(19)</sup>	_	_	100	_	_	100	_	Ω			
Absolute V <sub>MAX</sub> <sup>(3)</sup>	Dedicated reference clock pin	_	_	1.6	_	_	1.6	V			
	RX reference clock pin	_	_	1.2	_	_	1.2				
Absolute V <sub>MIN</sub>	—	-0.4		—	-0.4	—		V			
Peak-to-peak differential input voltage	_	200	_	1600	200	_	1600	mV			
V <sub>ICM</sub> (AC coupled)	Dedicated reference clock pin		1050/1000 <sup>(,</sup>	2)	1	050/1000 (	2)	mV			
	RX reference clock pin	1	.0/0.9/0.85 (	22)	1.	V					
V <sub>ICM</sub> (DC coupled)	HCSL I/O standard for PCIe reference clock	250	_	550	250		550	mV			

#### Table 28. Transceiver Specifications for Stratix V GT Devices (Part 1 of 5)<sup>(1)</sup>

Table 29 shows the  $V_{\text{OD}}$  settings for the GT channel.

Symbol	V <sub>OD</sub> Setting	V <sub>od</sub> Value (mV)
	0	0
	1	200
V., differential neak to neak typical $(1)$	2	400
The american hear to hear thicat to	3	600
	4	800
	5	1000

#### Note:

(1) Refer to Figure 4.

#### Table 31. PLL Specifications for Stratix V Devices (Part 3 of 3)

Symbol	Parameter	Min	Тур	Max	Unit
f <sub>RES</sub>	Resolution of VCO frequency ( $f_{INPFD} = 100 \text{ MHz}$ )	390625	5.96	0.023	Hz

#### Notes to Table 31:

(1) This specification is limited in the Quartus II software by the I/O maximum frequency. The maximum I/O frequency is different for each I/O standard.

(2) This specification is limited by the lower of the two: I/O  $f_{MAX}$  or  $f_{OUT}$  of the PLL.

- (3) A high input jitter directly affects the PLL output jitter. To have low PLL output clock jitter, you must provide a clean clock source < 120 ps.
- (4)  $f_{REF}$  is fIN/N when N = 1.
- (5) Peak-to-peak jitter with a probability level of 10<sup>-12</sup> (14 sigma, 99.9999999974404% confidence level). The output jitter specification applies to the intrinsic jitter of the PLL, when an input jitter of 30 ps is applied. The external memory interface clock output jitter specifications use a different measurement method and are available in Table 44 on page 52.
- (6) The cascaded PLL specification is only applicable with the following condition: a. Upstream PLL: 0.59Mhz ≤ Upstream PLL BW < 1 MHz b. Downstream PLL: Downstream PLL BW > 2 MHz
- (7) High bandwidth PLL settings are not supported in external feedback mode.
- (8) The external memory interface clock output jitter specifications use a different measurement method, which is available in Table 42 on page 50.
- (9) The VCO frequency reported by the Quartus II software in the PLL Usage Summary section of the compilation report takes into consideration the VCO post-scale counter K value. Therefore, if the counter K has a value of 2, the frequency reported can be lower than the f<sub>VCO</sub> specification.
- (10) This specification only covers fractional PLL for low bandwidth. The  $f_{VCO}$  for fractional value range 0.05 0.95 must be  $\geq$  1000 MHz, while  $f_{VCO}$  for fractional value range 0.20 0.80 must be  $\geq$  1200 MHz.
- (11) This specification only covered fractional PLL for low bandwidth. The  $f_{VC0}$  for fractional value range 0.05-0.95 must be  $\geq$  1000 MHz.
- (12) This specification only covered fractional PLL for low bandwidth. The  $f_{VC0}$  for fractional value range 0.20-0.80 must be  $\geq$  1200 MHz.

### **DSP Block Specifications**

Table 32 lists the Stratix V DSP block performance specifications.

			F	Peformanc	e			
Mode	C1	C2, C2L	12, 12L	C3	13, 13L, 13YY	C4	14	Unit
		Modes ı	using one	DSP				
Three 9 x 9	600	600	600	480	480	420	420	MHz
One 18 x 18	600	600	600	480	480	420	400	MHz
Two partial 18 x 18 (or 16 x 16)	600	600	600	480	480	420	400	MHz
One 27 x 27	500	500	500	400	400	350	350	MHz
One 36 x 18	500	500	500	400	400	350	350	MHz
One sum of two 18 x 18(One sum of 2 16 x 16)	500	500	500	400	400	350	350	MHz
One sum of square	500	500	500	400	400	350	350	MHz
One 18 x 18 plus 36 (a x b) + c	500	500	500	400	400	350	350	MHz
		Modes u	sing two l	DSPs				·
Three 18 x 18	500	500	500	400	400	350	350	MHz
One sum of four 18 x 18	475	475	475	380	380	300	300	MHz
One sum of two 27 x 27	465	465	450	380	380	300	290	MHz
One sum of two 36 x 18	475	475	475	380	380	300	300	MHz
One complex 18 x 18	500	500	500	400	400	350	350	MHz
One 36 x 36	475	475	475	380	380	300	300	MHz

#### Table 32. Block Performance Specifications for Stratix V DSP Devices (Part 1 of 2)

Speed Grade	Min	Max	Unit
C4,I4	8	16	ps

#### Table 40. DQS Phase Offset Delay Per Setting for Stratix V Devices <sup>(1), (2)</sup> (Part 2 of 2)

#### Notes to Table 40:

(1) The typical value equals the average of the minimum and maximum values.

(2) The delay settings are linear with a cumulative delay variation of 40 ps for all speed grades. For example, when using a -2 speed grade and applying a 10-phase offset setting to a 90° phase shift at 400 MHz, the expected average cumulative delay is [625 ps + (10 × 10 ps) ± 20 ps] = 725 ps ± 20 ps.

Table 41 lists the DQS phase shift error for Stratix V devices.

Table 41. DQS Phase Shift Error Specification for DLL-Delayed Clock (t<sub>DQS\_PSERR</sub>) for Stratix V Devices <sup>(1)</sup>

Number of DQS Delay Buffers	C1	C2, C2L, I2, I2L	C3, I3, I3L, I3YY	C4,14	Unit
1	28	28	30	32	ps
2	56	56	60	64	ps
3	84	84	90	96	ps
4	112	112	120	128	ps

Notes to Table 41:

(1) This error specification is the absolute maximum and minimum error. For example, skew on three DQS delay buffers in a -2 speed grade is  $\pm 78$  ps or  $\pm 39$  ps.

Table 42 lists the memory output clock jitter specifications for Stratix V devices.

Table 42. Memory Output Clock Jitter Specification for Stratix V Devices (1	<sup>),</sup> (Part 1 of 2) <sup>(2), (3)</sup>
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Clock Network	Parameter	Symbol	C1		C2, C2L, I2, I2L		C3, I3, I3L, I3YY		C4,14		Unit
			Min	Max	Min	Max	Min	Max	Min	Max	
Regional	Clock period jitter	$t_{JIT(per)}$	-50	50	-50	50	-55	55	-55	55	ps
	Cycle-to-cycle period jitter	$t_{\text{JIT(cc)}}$	-100	100	-100	100	-110	110	-110	110	ps
	Duty cycle jitter	t <sub>JIT(duty)</sub>	-50	50	-50	50	-82.5	82.5	-82.5	82.5	ps
	Clock period jitter	$t_{JIT(per)}$	-75	75	-75	75	-82.5	82.5	-82.5	82.5	ps
Global	Cycle-to-cycle period jitter	t <sub>JIT(cc)</sub>	-150	150	-150	150	-165	165	-165	165	ps
	Duty cycle jitter	$t_{\text{JIT}(\text{duty})}$	-75	75	-75	75	-90	90	-90	90	ps

Clock Network	Parameter	Symbol	C1		C2, C2L, I2, I2L		C3, I3, I3L, I3YY		C4,14		Unit
			Min	Max	Min	Max	Min	Max	Min	Max	
	Clock period jitter	$t_{\text{JIT}(\text{per})}$	-25	25	-25	25	-30	30	-35	35	ps
PHY Clock	Cycle-to-cycle period jitter	$t_{\rm JIT(cc)}$	-50	50	-50	50	-60	60	-70	70	ps
	Duty cycle jitter	$t_{JIT(duty)}$	-37.5	37.5	-37.5	37.5	-45	45	-56	56	ps

#### Table 42. Memory Output Clock Jitter Specification for Stratix V Devices (1), (Part 2 of 2) (2), (3)

#### Notes to Table 42:

(1) The clock jitter specification applies to the memory output clock pins generated using differential signal-splitter and DDIO circuits clocked by a PLL output routed on a PHY, regional, or global clock network as specified. Altera recommends using PHY clock networks whenever possible.

(2) The clock jitter specification applies to the memory output clock pins clocked by an integer PLL.

(3) The memory output clock jitter is applicable when an input jitter of 30 ps peak-to-peak is applied with bit error rate (BER) -12, equivalent to 14 sigma.

### **OCT Calibration Block Specifications**

Table 43 lists the OCT calibration block specifications for Stratix V devices.

#### Table 43. OCT Calibration Block Specifications for Stratix V Devices

Symbol	Description	Min	Тур	Max	Unit
OCTUSRCLK	Clock required by the OCT calibration blocks	—	—	20	MHz
T <sub>OCTCAL</sub>	Number of OCTUSRCLK clock cycles required for OCT $\rm R_S/R_T$ calibration		1000	_	Cycles
T <sub>OCTSHIFT</sub>	Number of OCTUSRCLK clock cycles required for the OCT code to shift out	_	32	_	Cycles
T <sub>RS_RT</sub>	Time required between the dyn_term_ctrl and oe signal transitions in a bidirectional I/O buffer to dynamically switch between OCT $R_S$ and $R_T$ (Figure 10)		2.5		ns

Figure 10 shows the timing diagram for the oe and dyn\_term\_ctrl signals.

#### Figure 10. Timing Diagram for oe and dyn\_term\_ctrl Signals



	Mombor		Active Serial <sup>(1)</sup>	)	Fast	t Passive Parall	el <sup>(2)</sup>
Variant	Code	Width	DCLK (MHz)	Min Config Time (s)	Width	DCLK (MHz)	Min Config Time (s)
	D3	4	100	0.344	32	100	0.043
	D4	4	100	0.534	32	100	0.067
68	D4	4	100	0.344	32	100	0.043
03	D5	4	100	0.534	32	100	0.067
	D6	4	100	0.741	32	100	0.093
	D8	4	100	0.741	32	100	0.093
F	E9	4	100	0.857	32	100	0.107
L	EB	4	100	0.857	32	100	0.107

Table 48. Minimum Configuration Time Estimation for Stratix V Devices

#### Notes to Table 48:

(1) DCLK frequency of 100 MHz using external CLKUSR.

(2) Max FPGA FPP bandwidth may exceed bandwidth available from some external storage or control logic.

# **Fast Passive Parallel Configuration Timing**

This section describes the fast passive parallel (FPP) configuration timing parameters for Stratix V devices.

### DCLK-to-DATA[] Ratio for FPP Configuration

FPP configuration requires a different DCLK-to-DATA[]ratio when you enable the design security, decompression, or both features. Table 49 lists the DCLK-to-DATA[]ratio for each combination.

Configuration Scheme	Decompression	Design Security	DCLK-to-DATA[] Ratio
	Disabled	Disabled	1
	Disabled	Enabled	1
IFF ×0	Enabled	Disabled	2
	Enabled	Enabled	2
	Disabled	Disabled	1
	Disabled	Enabled	2
IFF ×10	Enabled	Disabled	4
	Enabled	Enabled	4

 Table 49. DCLK-to-DATA[] Ratio <sup>(1)</sup> (Part 1 of 2)

Configuration Scheme	Decompression	Design Security	DCLK-to-DATA[] Ratio
	Disabled	Disabled	1
	Disabled	Enabled	4
IFF XJZ	Enabled	Disabled	8
	Enabled	Enabled	8

Table 49.	DCLK-to-DATA[]	Ratio <sup>(1)</sup>	(Part 2 of 2)
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Note to Table 49:

(1) Depending on the DCLK-to-DATA [] ratio, the host must send a DCLK frequency that is r times the data rate in bytes per second (Bps), or words per second (Wps). For example, in FPP ×16 when the DCLK-to-DATA [] ratio is 2, the DCLK frequency must be 2 times the data rate in Wps. Stratix V devices use the additional clock cycles to decrypt and decompress the configuration data.

Figure 11 shows the configuration interface connections between the Stratix V device and a MAX II or MAX V device for single device configuration.

#### Figure 11. Single Device FPP Configuration Using an External Host



#### Notes to Figure 11:

- (1) Connect the resistor to a supply that provides an acceptable input signal for the Stratix V device.  $V_{CCPGM}$  must be high enough to meet the  $V_{IH}$  specification of the I/O on the device and the external host. Altera recommends powering up all configuration system I/Os with  $V_{CCPGM}$ .
- (2) You can leave the nCEO pin unconnected or use it as a user I/O pin when it does not feed another device's nCE pin.
- (3) The MSEL pin settings vary for different data width, configuration voltage standards, and POR delay. To connect MSEL, refer to the MSEL Pin Settings section of the "Configuration, Design Security, and Remote System Upgrades in Stratix V Devices" chapter.
- (4) If you use FPP ×8, use DATA [7..0]. If you use FPP ×16, use DATA [15..0].

IF the DCLK-to-DATA[] ratio is greater than 1, at the end of configuration, you can only stop the DCLK (DCLK-to-DATA[] ratio – 1) clock cycles after the last data is latched into the Stratix V device.

### FPP Configuration Timing when DCLK-to-DATA [] = 1

Figure 12 shows the timing waveform for FPP configuration when using a MAX II or MAX V device as an external host. This waveform shows timing when the DCLK-to-DATA[] ratio is 1.





#### Notes to Figure 12:

- (1) Use this timing waveform when the DCLK-to-DATA [] ratio is 1.
- (2) The beginning of this waveform shows the device in user mode. In user mode, nCONFIG, nSTATUS, and CONF\_DONE are at logic-high levels. When nCONFIG is pulled low, a reconfiguration cycle begins.
- (3) After power-up, the Stratix V device holds nstatus low for the time of the POR delay.
- (4) After power-up, before and during configuration, CONF\_DONE is low.
- (5) Do not leave DCLK floating after configuration. DCLK is ignored after configuration is complete. It can toggle high or low if required.
- (6) For FPP ×16, use DATA [15..0]. For FPP ×8, use DATA [7..0]. DATA [31..0] are available as a user I/O pin after configuration. The state of this pin depends on the dual-purpose pin settings.
- (7) To ensure a successful configuration, send the entire configuration data to the Stratix V device. CONF\_DONE is released high when the Stratix V device receives all the configuration data successfully. After CONF\_DONE goes high, send two additional falling edges on DCLK to begin initialization and enter user mode.
- (8) After the option bit to enable the INIT\_DONE pin is configured into the device, the INIT DONE goes low.

Table 51 lists the timing parameters for Stratix V devices for FPP configuration when the DCLK-to-DATA [] ratio is more than 1.

Table 51.	<b>FPP</b> Timing	Parameters f	or Stratix V	<b>Devices</b> When	the DCLK-te	o-DATA[] Ratio	is >1 (	1)
			•••••••••••••••••••••••••••••••••••••••			• • • • • • • • • • • • • • • • • • •		

Symbol	Parameter	Minimum	Maximum	Units
t <sub>CF2CD</sub>	nCONFIG low to CONF_DONE low	—	600	ns
t <sub>CF2ST0</sub>	nCONFIG low to nSTATUS low	—	600	ns
t <sub>CFG</sub>	nCONFIG low pulse width	2		μS
t <sub>STATUS</sub>	nSTATUS low pulse width	268	1,506 <sup>(2)</sup>	μS
t <sub>CF2ST1</sub>	nCONFIG high to nSTATUS high	—	1,506 <sup>(2)</sup>	μS
t <sub>CF2CK</sub> (5)	nCONFIG high to first rising edge on DCLK	1,506		μS
t <sub>ST2CK</sub> (5)	nSTATUS high to first rising edge of DCLK	2		μS
t <sub>DSU</sub>	DATA [] setup time before rising edge on DCLK	5.5		ns
t <sub>DH</sub>	DATA [] hold time after rising edge on DCLK	N-1/f <sub>DCLK</sub> (5)		S
t <sub>CH</sub>	DCLK high time	$0.45\times 1/f_{MAX}$		S
t <sub>CL</sub>	DCLK low time	$0.45\times 1/f_{MAX}$		S
t <sub>CLK</sub>	DCLK period	1/f <sub>MAX</sub>		S
f	DCLK frequency (FPP ×8/×16)	—	125	MHz
IMAX	DCLK frequency (FPP ×32)	—	100	MHz
t <sub>R</sub>	Input rise time	—	40	ns
t <sub>F</sub>	Input fall time	—	40	ns
t <sub>CD2UM</sub>	CONF_DONE high to user mode <sup>(3)</sup>	175	437	μS
t <sub>CD2CU</sub>	CONF_DONE high to CLKUSR enabled	4 × maximum DCLK period	_	_
t <sub>CD2UMC</sub>	CONF_DONE high to user mode with CLKUSR option on	t <sub>CD2CU</sub> + (8576 × CLKUSR period) <sup>(4)</sup>	_	_

#### Notes to Table 51:

- (1) Use these timing parameters when you use the decompression and design security features.
- (2) You can obtain this value if you do not delay configuration by extending the nCONFIG or nSTATUS low pulse width.
- (3) The minimum and maximum numbers apply only if you use the internal oscillator as the clock source for initializing the device.
- (4) To enable the CLKUSR pin as the initialization clock source and to obtain the maximum frequency specification on these pins, refer to the Initialization section of the "Configuration, Design Security, and Remote System Upgrades in Stratix V Devices" chapter.
- (5) N is the DCLK-to-DATA ratio and  $f_{\text{DCLK}}$  is the DCLK frequency the system is operating.
- (6) If nSTATUS is monitored, follow the t<sub>ST2CK</sub> specification. If nSTATUS is not monitored, follow the t<sub>CF2CK</sub> specification.

# **Active Serial Configuration Timing**

Table 52 lists the DCLK frequency specification in the AS configuration scheme.

Fable 52.	DCLK Frequency	Specification in th	e AS Configuration	Scheme <sup>(1),</sup>	(2)
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Minimum	Typical	Maximum	Unit
5.3	7.9	12.5	MHz
10.6	15.7	25.0	MHz
21.3	31.4	50.0	MHz
42.6	62.9	100.0	MHz

#### Notes to Table 52:

(1) This applies to the DCLK frequency specification when using the internal oscillator as the configuration clock source.

(2) The AS multi-device configuration scheme does not support DCLK frequency of 100 MHz.

Figure 14 shows the single-device configuration setup for an AS ×1 mode.





#### Notes to Figure 14:

- (1) If you are using AS  $\times 4$  mode, this signal represents the AS\_DATA[3..0] and EPCQ sends in 4-bits of data for each DCLK cycle.
- (2) The initialization clock can be from internal oscillator or CLKUSR pin.
- (3) After the option bit to enable the INIT\_DONE pin is configured into the device, the INIT\_DONE goes low.

Table 53 lists the timing parameters for AS  $\times 1$  and AS  $\times 4$  configurations in Stratix V devices.

Table JS. As fining falancees for as $\times 1$ and as $\times 4$ configurations in straits V devices $(2, 2, 2, 3, 3, 3, 3, 3, 3, 3, 3, 3, 3, 3, 3, 3,$	Table 53.	AS Timing	<b>Parameters for AS</b>	$\times$ 1 and AS $\times$ 4 Confi	gurations in Stratix V	/ Devices <sup>(1), (2)</sup>	(Part 1 of 2)
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Symbol	Parameter	Minimum	Maximum	Units
t <sub>CO</sub>	DCLK falling edge to AS_DATA0/ASDO output	—	2	ns
t <sub>SU</sub>	Data setup time before falling edge on DCLK	1.5	_	ns
t <sub>H</sub>	Data hold time after falling edge on DCLK	0	_	ns

# **Remote System Upgrades**

Table 56 lists the timing parameter specifications for the remote system upgrade circuitry.

Table 56. Remote System Upgrade Circuitry Timing Specificatio
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Parameter	Minimum	Maximum	Unit
t <sub>RU_nCONFIG</sub> <sup>(1)</sup>	250	—	ns
t <sub>RU_nRSTIMER</sub> <sup>(2)</sup>	250	_	ns

#### Notes to Table 56:

- (1) This is equivalent to strobing the reconfiguration input of the ALTREMOTE\_UPDATE megafunction high for the minimum timing specification. For more information, refer to the Remote System Upgrade State Machine section of the "Configuration, Design Security, and Remote System Upgrades in Stratix V Devices" chapter.
- (2) This is equivalent to strobing the reset\_timer input of the ALTREMOTE\_UPDATE megafunction high for the minimum timing specification. For more information, refer to the User Watchdog Timer section of the "Configuration, Design Security, and Remote System Upgrades in Stratix V Devices" chapter.

# **User Watchdog Internal Circuitry Timing Specification**

Table 57 lists the operating range of the 12.5-MHz internal oscillator.

#### Table 57. 12.5-MHz Internal Oscillator Specifications

Minimum	Typical	Maximum	Units
5.3	7.9	12.5	MHz

# I/O Timing

Altera offers two ways to determine I/O timing—the Excel-based I/O Timing and the Quartus II Timing Analyzer.

Excel-based I/O timing provides pin timing performance for each device density and speed grade. The data is typically used prior to designing the FPGA to get an estimate of the timing budget as part of the link timing analysis. The Quartus II Timing Analyzer provides a more accurate and precise I/O timing data based on the specifics of the design after you complete place-and-route.

 You can download the Excel-based I/O Timing spreadsheet from the Stratix V Devices Documentation web page.

## **Programmable IOE Delay**

Table 58 lists the Stratix V IOE programmable delay settings.

Table 58. IOE Programmable Delay for Stratix V Devices (Part 1 of 2)

Deremeter	Min		Fast	Model				Slow N	lodel			
(1)	Settings	<b>Offset</b> (2)	Industrial	Commercial	C1	C2	C3	C4	12	13, 13YY	14	Unit
D1	64	0	0.464	0.493	0.838	0.838	0.924	1.011	0.844	0.921	1.006	ns
D2	32	0	0.230	0.244	0.415	0.415	0.459	0.503	0.417	0.456	0.500	ns

Paramotor	otor Available Min		Fast Model		Slow Model							
(1)	Settings	Offset (2)	Industrial	Commercial	C1	C2	C3	C4	12	13, 13YY	14	Unit
D3	8	0	1.587	1.699	2.793	2.793	2.992	3.192	2.811	3.047	3.257	ns
D4	64	0	0.464	0.492	0.838	0.838	0.924	1.011	0.843	0.920	1.006	ns
D5	64	0	0.464	0.493	0.838	0.838	0.924	1.011	0.844	0.921	1.006	ns
D6	32	0	0.229	0.244	0.415	0.415	0.458	0.503	0.418	0.456	0.499	ns

Table 58.	IOE Pro	grammable De	ay for	Stratix V	V Devices	(Part 2 of 2	)
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#### Notes to Table 58:

(1) You can set this value in the Quartus II software by selecting D1, D2, D3, D5, and D6 in the Assignment Name column of Assignment Editor.

(2) Minimum offset does not include the intrinsic delay.

## **Programmable Output Buffer Delay**

Table 59 lists the delay chain settings that control the rising and falling edge delays of the output buffer. The default delay is 0 ps.

Symbol	Parameter	Typical	Unit
		0 (default)	ps
Dauman	Rising and/or falling edge	25	ps
DOUTBUF	delay	50	ps
		75	ps

Note to Table 59:

(1) You can set the programmable output buffer delay in the Quartus II software by setting the Output Buffer Delay Control assignment to either positive, negative, or both edges, with the specific values stated here (in ps) for the Output Buffer Delay assignment.

# Glossary

Table 60 lists the glossary for this chapter.

Table 60. Glossary (Part 1 of 4)

Letter	Subject	Definitions
Α		
В	—	—
С		
D	—	_
E	—	_
	f <sub>HSCLK</sub>	Left and right PLL input clock frequency.
F	f <sub>HSDR</sub>	High-speed I/O block—Maximum and minimum <b>LVDS</b> data transfer rate (f <sub>HSDR</sub> = 1/TUI), non-DPA.
	f <sub>hsdrdpa</sub>	High-speed I/O block—Maximum and minimum <b>LVDS</b> data transfer rate (f <sub>HSDRDPA</sub> = 1/TUI), DPA.

Letter	Subject	Definitions
	V <sub>CM(DC)</sub>	DC common mode input voltage.
	V <sub>ICM</sub>	Input common mode voltage—The common mode of the differential signal at the receiver.
	V <sub>ID</sub>	Input differential voltage swing—The difference in voltage between the positive and complementary conductors of a differential transmission at the receiver.
	V <sub>DIF(AC)</sub>	AC differential input voltage—Minimum AC input differential voltage required for switching.
	V <sub>DIF(DC)</sub>	DC differential input voltage— Minimum DC input differential voltage required for switching.
	V <sub>IH</sub>	Voltage input high—The minimum positive voltage applied to the input which is accepted by the device as a logic high.
	V <sub>IH(AC)</sub>	High-level AC input voltage
	V <sub>IH(DC)</sub>	High-level DC input voltage
V	V <sub>IL</sub>	Voltage input low—The maximum positive voltage applied to the input which is accepted by the device as a logic low.
	V <sub>IL(AC)</sub>	Low-level AC input voltage
	V <sub>IL(DC)</sub>	Low-level DC input voltage
	V <sub>OCM</sub>	Output common mode voltage—The common mode of the differential signal at the transmitter.
	V <sub>OD</sub>	Output differential voltage swing—The difference in voltage between the positive and complementary conductors of a differential transmission at the transmitter.
	V <sub>SWING</sub>	Differential input voltage
	V <sub>X</sub>	Input differential cross point voltage
	V <sub>OX</sub>	Output differential cross point voltage
W	W	High-speed I/O block—clock boost factor
X		
Y	—	—
Z		

#### Table 60. Glossary (Part 4 of 4)

 Table 61. Document Revision History (Part 3 of 3)

Date	Version	Changes
		■ Updated Table 2, Table 6, Table 7, Table 20, Table 23, Table 27, Table 47, Table 60
May 2013	2.7	Added Table 24, Table 48
		<ul> <li>Updated Figure 9, Figure 10, Figure 11, Figure 12</li> </ul>
February 2013	2.6	<ul> <li>Updated Table 7, Table 9, Table 20, Table 23, Table 27, Table 30, Table 31, Table 35, Table 46</li> </ul>
		Updated "Maximum Allowed Overshoot and Undershoot Voltage"
		<ul> <li>Updated Table 3, Table 6, Table 7, Table 8, Table 23, Table 24, Table 25, Table 27, Table 30, Table 32, Table 35</li> </ul>
		Added Table 33
		<ul> <li>Added "Fast Passive Parallel Configuration Timing"</li> </ul>
		<ul> <li>Added "Active Serial Configuration Timing"</li> </ul>
December 2012	2.5	<ul> <li>Added "Passive Serial Configuration Timing"</li> </ul>
		<ul> <li>Added "Remote System Upgrades"</li> </ul>
		<ul> <li>Added "User Watchdog Internal Circuitry Timing Specification"</li> </ul>
		Added "Initialization"
		Added "Raw Binary File Size"
lune 2012	2.4	<ul> <li>Added Figure 1, Figure 2, and Figure 3.</li> </ul>
		<ul> <li>Updated Table 1, Table 2, Table 3, Table 6, Table 11, Table 22, Table 23, Table 27, Table 29, Table 30, Table 31, Table 32, Table 35, Table 38, Table 39, Table 40, Table 41, Table 43, Table 56, and Table 59.</li> </ul>
		<ul> <li>Various edits throughout to fix bugs.</li> </ul>
		Changed title of document to <i>Stratix V Device Datasheet</i> .
		<ul> <li>Removed document from the Stratix V handbook and made it a separate document.</li> </ul>
February 2012	2.3	■ Updated Table 1–22, Table 1–29, Table 1–31, and Table 1–31.
December 2011	22	■ Added Table 2–31.
December 2011	2.2	■ Updated Table 2–28 and Table 2–34.
		<ul> <li>Added Table 2–2 and Table 2–21 and updated Table 2–5 with information about Stratix V GT devices.</li> </ul>
November 2011	2.1	<ul> <li>Updated Table 2–11, Table 2–13, Table 2–20, and Table 2–25.</li> </ul>
		<ul> <li>Various edits throughout to fix SPRs.</li> </ul>
		■ Updated Table 2–4, Table 2–18, Table 2–19, Table 2–21, Table 2–22, Table 2–23, and Table 2–24.
May 2011	2.0	<ul> <li>Updated the "DQ Logic Block and Memory Output Clock Jitter Specifications" title.</li> </ul>
		Chapter moved to Volume 1.
		<ul> <li>Minor text edits.</li> </ul>
		■ Updated Table 1–2, Table 1–4, Table 1–19, and Table 1–23.
December 2010	1.1	<ul> <li>Converted chapter to the new template.</li> </ul>
		<ul> <li>Minor text edits.</li> </ul>
July 2010	1.0	Initial release.