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Understanding **Embedded - FPGAs (Field Programmable Gate Array)**

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

| | |
|--------------------------------|---|
| Product Status | Obsolete |
| Number of LABs/CLBs | 128300 |
| Number of Logic Elements/Cells | 340000 |
| Total RAM Bits | 19456000 |
| Number of I/O | 600 |
| Number of Gates | - |
| Voltage - Supply | 0.82V ~ 0.88V |
| Mounting Type | Surface Mount |
| Operating Temperature | -40°C ~ 100°C (TJ) |
| Package / Case | 1152-BBGA, FCBGA |
| Supplier Device Package | 1152-FBGA (35x35) |
| Purchase URL | https://www.e-xfl.com/product-detail/intel/5sgxma3h2f35i3ln |

Table 7. Recommended Transceiver Power Supply Operating Conditions for Stratix V GX, GS, and GT Devices (Part 2 of 2)

| Symbol | Description | Devices | Minimum ⁽⁴⁾ | Typical | Maximum ⁽⁴⁾ | Unit |
|------------------------|--|------------|------------------------|---------|------------------------|------|
| V_{CCR_GXBR} (2) | Receiver analog power supply (right side) | GX, GS, GT | 0.82 | 0.85 | 0.88 | V |
| | | | 0.87 | 0.90 | 0.93 | |
| | | | 0.97 | 1.0 | 1.03 | |
| | | | 1.03 | 1.05 | 1.07 | |
| V_{CCR_GTBR} | Receiver analog power supply for GT channels (right side) | GT | 1.02 | 1.05 | 1.08 | V |
| V_{CCT_GXBL} (2) | Transmitter analog power supply (left side) | GX, GS, GT | 0.82 | 0.85 | 0.88 | V |
| | | | 0.87 | 0.90 | 0.93 | |
| | | | 0.97 | 1.0 | 1.03 | |
| | | | 1.03 | 1.05 | 1.07 | |
| V_{CCT_GXBR} (2) | Transmitter analog power supply (right side) | GX, GS, GT | 0.82 | 0.85 | 0.88 | V |
| | | | 0.87 | 0.90 | 0.93 | |
| | | | 0.97 | 1.0 | 1.03 | |
| | | | 1.03 | 1.05 | 1.07 | |
| V_{CCT_GTBR} | Transmitter analog power supply for GT channels (right side) | GT | 1.02 | 1.05 | 1.08 | V |
| V_{CCL_GTBR} | Transmitter clock network power supply | GT | 1.02 | 1.05 | 1.08 | V |
| V_{CCH_GXBL} | Transmitter output buffer power supply (left side) | GX, GS, GT | 1.425 | 1.5 | 1.575 | V |
| V_{CCH_GXBR} | Transmitter output buffer power supply (right side) | GX, GS, GT | 1.425 | 1.5 | 1.575 | V |

Notes to Table 7:

- (1) This supply must be connected to 3.0 V if the CMU PLL, receiver CDR, or both, are configured at a base data rate > 6.5 Gbps. Up to 6.5 Gbps, you can connect this supply to either 3.0 V or 2.5 V.
- (2) Refer to Table 8 to select the correct power supply level for your design.
- (3) When using ATX PLLs, the supply must be 3.0 V.
- (4) This value describes the budget for the DC (static) power supply tolerance and does not include the dynamic tolerance requirements. Refer to the PDN tool for the additional budget for the dynamic tolerance requirements.

Table 11. OCT Calibration Accuracy Specifications for Stratix V Devices ⁽¹⁾ (Part 2 of 2)

| Symbol | Description | Conditions | Calibration Accuracy | | | | Unit |
|--|--|---|----------------------|------------|----------------|------------|------|
| | | | C1 | C2,I2 | C3,I3, I3YY | C4,I4 | |
| 50-Ω R _S | Internal series termination with calibration (50-Ω setting) | V _{CCIO} = 3.0, 2.5, 1.8, 1.5, 1.2 V | ±15 | ±15 | ±15 | ±15 | % |
| 34-Ω and 40-Ω R _S | Internal series termination with calibration (34-Ω and 40-Ω setting) | V _{CCIO} = 1.5, 1.35, 1.25, 1.2 V | ±15 | ±15 | ±15 | ±15 | % |
| 48-Ω, 60-Ω, 80-Ω, and 240-Ω R _S | Internal series termination with calibration (48-Ω, 60-Ω, 80-Ω, and 240-Ω setting) | V _{CCIO} = 1.2 V | ±15 | ±15 | ±15 | ±15 | % |
| 50-Ω R _T | Internal parallel termination with calibration (50-Ω setting) | V _{CCIO} = 2.5, 1.8, 1.5, 1.2 V | -10 to +40 | -10 to +40 | -10 to +40 | -10 to +40 | % |
| 20-Ω, 30-Ω, 40-Ω, 60-Ω, and 120-Ω R _T | Internal parallel termination with calibration (20-Ω, 30-Ω, 40-Ω, 60-Ω, and 120-Ω setting) | V _{CCIO} = 1.5, 1.35, 1.25 V | -10 to +40 | -10 to +40 | -10 to +40 | -10 to +40 | % |
| 60-Ω and 120-Ω R _T | Internal parallel termination with calibration (60-Ω and 120-Ω setting) | V _{CCIO} = 1.2 | -10 to +40 | -10 to +40 | -10 to +40 | -10 to +40 | % |
| 25-Ω R _{S_left_shift} | Internal left shift series termination with calibration (25-Ω R _{S_left_shift} setting) | V _{CCIO} = 3.0, 2.5, 1.8, 1.5, 1.2 V | ±15 | ±15 | ±15 | ±15 | % |

Note to Table 11:

(1) OCT calibration accuracy is valid at the time of calibration only.

Table 12 lists the Stratix V OCT without calibration resistance tolerance to PVT changes.

Table 12. OCT Without Calibration Resistance Tolerance Specifications for Stratix V Devices (Part 1 of 2)

| Symbol | Description | Conditions | Resistance Tolerance | | | | Unit |
|-----------------------------|--|-----------------------------------|----------------------|-------|-----------------|--------|------|
| | | | C1 | C2,I2 | C3, I3, I3YY | C4, I4 | |
| 25-Ω R, 50-Ω R _S | Internal series termination without calibration (25-Ω setting) | V _{CCIO} = 3.0 and 2.5 V | ±30 | ±30 | ±40 | ±40 | % |
| 25-Ω R _S | Internal series termination without calibration (25-Ω setting) | V _{CCIO} = 1.8 and 1.5 V | ±30 | ±30 | ±40 | ±40 | % |
| 25-Ω R _S | Internal series termination without calibration (25-Ω setting) | V _{CCIO} = 1.2 V | ±35 | ±35 | ±50 | ±50 | % |

Table 13. OCT Variation after Power-Up Calibration for Stratix V Devices (Part 2 of 2) ⁽¹⁾

| Symbol | Description | V _{CCIO} (V) | Typical | Unit |
|--------|--|-----------------------|---------|-------------------|
| dR/dT | OCT variation with temperature without recalibration | 3.0 | 0.189 | %/ ^o C |
| | | 2.5 | 0.208 | |
| | | 1.8 | 0.266 | |
| | | 1.5 | 0.273 | |
| | | 1.2 | 0.317 | |

Note to Table 13:

(1) Valid for a V_{CCIO} range of $\pm 5\%$ and a temperature range of 0° to 85°C.

Pin Capacitance

Table 14 lists the Stratix V device family pin capacitance.

Table 14. Pin Capacitance for Stratix V Devices

| Symbol | Description | Value | Unit |
|--------------------|--|-------|------|
| C _{IOTB} | Input capacitance on the top and bottom I/O pins | 6 | pF |
| C _{IOLR} | Input capacitance on the left and right I/O pins | 6 | pF |
| C _{OUTFB} | Input capacitance on dual-purpose clock output and feedback pins | 6 | pF |

Hot Socketing

Table 15 lists the hot socketing specifications for Stratix V devices.

Table 15. Hot Socketing Specifications for Stratix V Devices

| Symbol | Description | Maximum |
|---------------------------|--|---------------------|
| I _{IOPIN} (DC) | DC current per I/O pin | 300 μ A |
| I _{IOPIN} (AC) | AC current per I/O pin | 8 mA ⁽¹⁾ |
| I _{XCVR-TX} (DC) | DC current per transceiver transmitter pin | 100 mA |
| I _{XCVR-RX} (DC) | DC current per transceiver receiver pin | 50 mA |

Note to Table 15:

(1) The I/O ramp rate is 10 ns or more. For ramp rates faster than 10 ns, $|I_{IOPIN}| = C \, dv/dt$, in which C is the I/O pin capacitance and dv/dt is the slew rate.

Table 19. Single-Ended SSTL, HSTL, and HSUL I/O Standards Signal Specifications for Stratix V Devices (Part 2 of 2)

| I/O Standard | $V_{IL(DC)}$ (V) | | $V_{IH(DC)}$ (V) | | $V_{IL(AC)}$ (V) | $V_{IH(AC)}$ (V) | V_{OL} (V) | V_{OH} (V) | I_{ol} (mA) | I_{oh} (mA) |
|------------------|------------------|------------------|------------------|-------------------|------------------|------------------|-------------------|-------------------|---------------|---------------|
| | Min | Max | Min | Max | Max | Min | Max | Min | | |
| HSTL-18 Class I | — | $V_{REF} - 0.1$ | $V_{REF} + 0.1$ | — | $V_{REF} - 0.2$ | $V_{REF} + 0.2$ | 0.4 | $V_{CCIO} - 0.4$ | 8 | -8 |
| HSTL-18 Class II | — | $V_{REF} - 0.1$ | $V_{REF} + 0.1$ | — | $V_{REF} - 0.2$ | $V_{REF} + 0.2$ | 0.4 | $V_{CCIO} - 0.4$ | 16 | -16 |
| HSTL-15 Class I | — | $V_{REF} - 0.1$ | $V_{REF} + 0.1$ | — | $V_{REF} - 0.2$ | $V_{REF} + 0.2$ | 0.4 | $V_{CCIO} - 0.4$ | 8 | -8 |
| HSTL-15 Class II | — | $V_{REF} - 0.1$ | $V_{REF} + 0.1$ | — | $V_{REF} - 0.2$ | $V_{REF} + 0.2$ | 0.4 | $V_{CCIO} - 0.4$ | 16 | -16 |
| HSTL-12 Class I | -0.15 | $V_{REF} - 0.08$ | $V_{REF} + 0.08$ | $V_{CCIO} + 0.15$ | $V_{REF} - 0.15$ | $V_{REF} + 0.15$ | $0.25^* V_{CCIO}$ | $0.75^* V_{CCIO}$ | 8 | -8 |
| HSTL-12 Class II | -0.15 | $V_{REF} - 0.08$ | $V_{REF} + 0.08$ | $V_{CCIO} + 0.15$ | $V_{REF} - 0.15$ | $V_{REF} + 0.15$ | $0.25^* V_{CCIO}$ | $0.75^* V_{CCIO}$ | 16 | -16 |
| HSUL-12 | — | $V_{REF} - 0.13$ | $V_{REF} + 0.13$ | — | $V_{REF} - 0.22$ | $V_{REF} + 0.22$ | $0.1^* V_{CCIO}$ | $0.9^* V_{CCIO}$ | — | — |

Table 20. Differential SSTL I/O Standards for Stratix V Devices

| I/O Standard | V_{CCIO} (V) | | | $V_{SWING(DC)}$ (V) | | $V_{X(AC)}$ (V) | | | $V_{SWING(AC)}$ (V) | |
|----------------------|----------------|------|-------|---------------------|------------------|----------------------|--------------|----------------------|---------------------------|---------------------------|
| | Min | Typ | Max | Min | Max | Min | Typ | Max | Min | Max |
| SSTL-2 Class I, II | 2.375 | 2.5 | 2.625 | 0.3 | $V_{CCIO} + 0.6$ | $V_{CCIO}/2 - 0.2$ | — | $V_{CCIO}/2 + 0.2$ | 0.62 | $V_{CCIO} + 0.6$ |
| SSTL-18 Class I, II | 1.71 | 1.8 | 1.89 | 0.25 | $V_{CCIO} + 0.6$ | $V_{CCIO}/2 - 0.175$ | — | $V_{CCIO}/2 + 0.175$ | 0.5 | $V_{CCIO} + 0.6$ |
| SSTL-15 Class I, II | 1.425 | 1.5 | 1.575 | 0.2 | (1) | $V_{CCIO}/2 - 0.15$ | — | $V_{CCIO}/2 + 0.15$ | 0.35 | — |
| SSTL-135 Class I, II | 1.283 | 1.35 | 1.45 | 0.2 | (1) | $V_{CCIO}/2 - 0.15$ | $V_{CCIO}/2$ | $V_{CCIO}/2 + 0.15$ | $2(V_{IH(AC)} - V_{REF})$ | $2(V_{IL(AC)} - V_{REF})$ |
| SSTL-125 Class I, II | 1.19 | 1.25 | 1.31 | 0.18 | (1) | $V_{CCIO}/2 - 0.15$ | $V_{CCIO}/2$ | $V_{CCIO}/2 + 0.15$ | $2(V_{IH(AC)} - V_{REF})$ | — |
| SSTL-12 Class I, II | 1.14 | 1.2 | 1.26 | 0.18 | — | $V_{REF} - 0.15$ | $V_{CCIO}/2$ | $V_{REF} + 0.15$ | -0.30 | 0.30 |

Note to Table 20:

(1) The maximum value for $V_{SWING(DC)}$ is not defined. However, each single-ended signal needs to be within the respective single-ended limits ($V_{IH(DC)}$ and $V_{IL(DC)}$).

Table 21. Differential HSTL and HSUL I/O Standards for Stratix V Devices (Part 1 of 2)

| I/O Standard | V_{CCIO} (V) | | | $V_{DIF(DC)}$ (V) | | $V_{X(AC)}$ (V) | | | $V_{CM(DC)}$ (V) | | | $V_{DIF(AC)}$ (V) | |
|---------------------|----------------|-----|-------|-------------------|-----|-----------------|-----|------|------------------|-----|------|-------------------|-----|
| | Min | Typ | Max | Min | Max | Min | Typ | Max | Min | Typ | Max | Min | Max |
| HSTL-18 Class I, II | 1.71 | 1.8 | 1.89 | 0.2 | — | 0.78 | — | 1.12 | 0.78 | — | 1.12 | 0.4 | — |
| HSTL-15 Class I, II | 1.425 | 1.5 | 1.575 | 0.2 | — | 0.68 | — | 0.9 | 0.68 | — | 0.9 | 0.4 | — |

Switching Characteristics

This section provides performance characteristics of the Stratix V core and periphery blocks.

These characteristics can be designated as Preliminary or Final.

- Preliminary characteristics are created using simulation results, process data, and other known parameters. The title of these tables show the designation as “Preliminary.”
- Final numbers are based on actual silicon characterization and testing. The numbers reflect the actual performance of the device under worst-case silicon process, voltage, and junction temperature conditions. There are no designations on finalized tables.

Transceiver Performance Specifications

This section describes transceiver performance specifications.

Table 23 lists the Stratix V GX and GS transceiver specifications.

Table 23. Transceiver Specifications for Stratix V GX and GS Devices ⁽¹⁾ (Part 1 of 7)

| Symbol/ Description | Conditions | Transceiver Speed Grade 1 | | | Transceiver Speed Grade 2 | | | Transceiver Speed Grade 3 | | | Unit |
|--|---|---|-----|-----|------------------------------|-----|-----|------------------------------|-----|-----|------|
| | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| Reference Clock | | | | | | | | | | | |
| Supported I/O Standards | Dedicated reference clock pin | 1.2-V PCML, 1.4-V PCML, 1.5-V PCML, 2.5-V PCML, Differential LVPECL, LVDS, and HCSL | | | | | | | | | |
| | RX reference clock pin | 1.4-V PCML, 1.5-V PCML, 2.5-V PCML, LVPECL, and LVDS | | | | | | | | | |
| Input Reference Clock Frequency (CMU PLL) ⁽⁸⁾ | — | 40 | — | 710 | 40 | — | 710 | 40 | — | 710 | MHz |
| Input Reference Clock Frequency (ATX PLL) ⁽⁸⁾ | — | 100 | — | 710 | 100 | — | 710 | 100 | — | 710 | MHz |
| Rise time | Measure at ±60 mV of differential signal ⁽²⁶⁾ | — | — | 400 | — | — | 400 | — | — | 400 | ps |
| Fall time | Measure at ±60 mV of differential signal ⁽²⁶⁾ | — | — | 400 | — | — | 400 | — | — | 400 | |
| Duty cycle | — | 45 | — | 55 | 45 | — | 55 | 45 | — | 55 | % |
| Spread-spectrum modulating clock frequency | PCI Express® (PCIe®) | 30 | — | 33 | 30 | — | 33 | 30 | — | 33 | kHz |

Table 23. Transceiver Specifications for Stratix V GX and GS Devices ⁽¹⁾ (Part 3 of 7)

| Symbol/ Description | Conditions | Transceiver Speed Grade 1 | | | Transceiver Speed Grade 2 | | | Transceiver Speed Grade 3 | | | Unit |
|---|--|--|-----|-------|------------------------------|-----|-------|------------------------------|-----|--------------------------|------|
| | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| Reconfiguration clock (<code>mgmt_clk_clk</code>) frequency | — | 100 | — | 125 | 100 | — | 125 | 100 | — | 125 | MHz |
| Receiver | | | | | | | | | | | |
| Supported I/O Standards | — | 1.4-V PCML, 1.5-V PCML, 2.5-V PCML, LVPECL, and LVDS | | | | | | | | | |
| Data rate (Standard PCS) (9), (23) | — | 600 | — | 12200 | 600 | — | 12200 | 600 | — | 8500/ 10312.5 (24) | Mbps |
| Data rate (10G PCS) (9), (23) | — | 600 | — | 14100 | 600 | — | 12500 | 600 | — | 8500/ 10312.5 (24) | Mbps |
| Absolute V_{MAX} for a receiver pin ⁽⁵⁾ | — | — | — | 1.2 | — | — | 1.2 | — | — | 1.2 | V |
| Absolute V_{MIN} for a receiver pin | — | −0.4 | — | — | −0.4 | — | — | −0.4 | — | — | V |
| Maximum peak- to-peak differential input voltage V_{ID} (diff p- p) before device configuration ⁽²²⁾ | — | — | — | 1.6 | — | — | 1.6 | — | — | 1.6 | V |
| Maximum peak- to-peak differential input voltage V_{ID} (diff p- p) after device configuration ⁽¹⁸⁾ , (22) | $V_{CCR_GXB} =$ 1.0 V/1.05 V ($V_{ICM} =$ 0.70 V) | — | — | 2.0 | — | — | 2.0 | — | — | 2.0 | V |
| | $V_{CCR_GXB} =$ 0.90 V ($V_{ICM} = 0.6$ V) | — | — | 2.4 | — | — | 2.4 | — | — | 2.4 | V |
| | $V_{CCR_GXB} =$ 0.85 V ($V_{ICM} = 0.6$ V) | — | — | 2.4 | — | — | 2.4 | — | — | 2.4 | V |
| Minimum differential eye opening at receiver serial input pins ⁽⁶⁾ , (22), (27) | — | 85 | — | — | 85 | — | — | 85 | — | — | mV |

Table 23. Transceiver Specifications for Stratix V GX and GS Devices ⁽¹⁾ (Part 4 of 7)

| Symbol/ Description | Conditions | Transceiver Speed Grade 1 | | | Transceiver Speed Grade 2 | | | Transceiver Speed Grade 3 | | | Unit |
|--|--|------------------------------|---------------|-----|------------------------------|---------------|-----|------------------------------|---------------|-----|---------------|
| | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| Differential on-chip termination resistors ⁽²¹⁾ | 85- Ω setting | — | 85 \pm 30% | — | — | 85 \pm 30% | — | — | 85 \pm 30% | — | Ω |
| | 100- Ω setting | — | 100 \pm 30% | — | — | 100 \pm 30% | — | — | 100 \pm 30% | — | Ω |
| | 120- Ω setting | — | 120 \pm 30% | — | — | 120 \pm 30% | — | — | 120 \pm 30% | — | Ω |
| | 150- Ω setting | — | 150 \pm 30% | — | — | 150 \pm 30% | — | — | 150 \pm 30% | — | Ω |
| V_{ICM} (AC and DC coupled) | $V_{CCR_GXB} = 0.85\text{ V}$ or 0.9 V full bandwidth | — | 600 | — | — | 600 | — | — | 600 | — | mV |
| | $V_{CCR_GXB} = 0.85\text{ V}$ or 0.9 V half bandwidth | — | 600 | — | — | 600 | — | — | 600 | — | mV |
| | $V_{CCR_GXB} = 1.0\text{ V}/1.05\text{ V}$ full bandwidth | — | 700 | — | — | 700 | — | — | 700 | — | mV |
| | $V_{CCR_GXB} = 1.0\text{ V}$ half bandwidth | — | 750 | — | — | 750 | — | — | 750 | — | mV |
| t_{LTR} ⁽¹¹⁾ | — | — | — | 10 | — | — | 10 | — | — | 10 | μs |
| t_{LTD} ⁽¹²⁾ | — | 4 | — | — | 4 | — | — | 4 | — | — | μs |
| t_{LTD_manual} ⁽¹³⁾ | — | 4 | — | — | 4 | — | — | 4 | — | — | μs |
| $t_{LTR_LTD_manual}$ ⁽¹⁴⁾ | — | 15 | — | — | 15 | — | — | 15 | — | — | μs |
| Run Length | — | — | — | 200 | — | — | 200 | — | — | 200 | UI |
| Programmable equalization (AC Gain) ⁽¹⁰⁾ | Full bandwidth (6.25 GHz) Half bandwidth (3.125 GHz) | — | — | 16 | — | — | 16 | — | — | 16 | dB |

Table 23. Transceiver Specifications for Stratix V GX and GS Devices ⁽¹⁾ (Part 5 of 7)

| Symbol/ Description | Conditions | Transceiver Speed Grade 1 | | | Transceiver Speed Grade 2 | | | Transceiver Speed Grade 3 | | | Unit |
|---|--|------------------------------|---------------------|-------|------------------------------|---------------------|-------|------------------------------|---------------------|-------------------------------------|----------|
| | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| Programmable DC gain | DC Gain Setting = 0 | — | 0 | — | — | 0 | — | — | 0 | — | dB |
| | DC Gain Setting = 1 | — | 2 | — | — | 2 | — | — | 2 | — | dB |
| | DC Gain Setting = 2 | — | 4 | — | — | 4 | — | — | 4 | — | dB |
| | DC Gain Setting = 3 | — | 6 | — | — | 6 | — | — | 6 | — | dB |
| | DC Gain Setting = 4 | — | 8 | — | — | 8 | — | — | 8 | — | dB |
| Transmitter | | | | | | | | | | | |
| Supported I/O Standards | — | 1.4-V and 1.5-V PCML | | | | | | | | | |
| Data rate (Standard PCS) | — | 600 | — | 12200 | 600 | — | 12200 | 600 | — | 8500/ 10312.5 ⁽²⁴⁾ | Mbps |
| Data rate (10G PCS) | — | 600 | — | 14100 | 600 | — | 12500 | 600 | — | 8500/ 10312.5 ⁽²⁴⁾ | Mbps |
| Differential on- chip termination resistors | 85- Ω setting | — | 85 \pm 20% | — | — | 85 \pm 20% | — | — | 85 \pm 20% | — | Ω |
| | 100- Ω setting | — | 100 \pm 20% | — | — | 100 \pm 20% | — | — | 100 \pm 20% | — | Ω |
| | 120- Ω setting | — | 120 \pm 20% | — | — | 120 \pm 20% | — | — | 120 \pm 20% | — | Ω |
| | 150- Ω setting | — | 150 \pm 20% | — | — | 150 \pm 20% | — | — | 150 \pm 20% | — | Ω |
| V _{OCM} (AC coupled) | 0.65-V setting | — | 650 | — | — | 650 | — | — | 650 | — | mV |
| V _{OCM} (DC coupled) | — | — | 650 | — | — | 650 | — | — | 650 | — | mV |
| Rise time ⁽⁷⁾ | 20% to 80% | 30 | — | 160 | 30 | — | 160 | 30 | — | 160 | ps |
| Fall time ⁽⁷⁾ | 80% to 20% | 30 | — | 160 | 30 | — | 160 | 30 | — | 160 | ps |
| Intra-differential pair skew | Tx V _{CM} = 0.5 V and slew rate of 15 ps | — | — | 15 | — | — | 15 | — | — | 15 | ps |
| Intra-transceiver block transmitter channel-to- channel skew | x6 PMA bonded mode | — | — | 120 | — | — | 120 | — | — | 120 | ps |

Table 23. Transceiver Specifications for Stratix V GX and GS Devices ⁽¹⁾ (Part 6 of 7)

| Symbol/ Description | Conditions | Transceiver Speed Grade 1 | | | Transceiver Speed Grade 2 | | | Transceiver Speed Grade 3 | | | Unit |
|---|--|------------------------------|-----|-------------------------------|------------------------------|-----|-------------------------------|------------------------------|-----|-------------------------------|------|
| | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| Inter-transceiver block transmitter channel-to- channel skew | xN PMA bonded mode | — | — | 500 | — | — | 500 | — | — | 500 | ps |
| CMU PLL | | | | | | | | | | | |
| Supported Data Range | — | 600 | — | 12500 | 600 | — | 12500 | 600 | — | 8500/ 10312.5 (24) | Mbps |
| t _{pll_powerdown} ⁽¹⁵⁾ | — | 1 | — | — | 1 | — | — | 1 | — | — | μs |
| t _{pll_lock} ⁽¹⁶⁾ | — | — | — | 10 | — | — | 10 | — | — | 10 | μs |
| ATX PLL | | | | | | | | | | | |
| Supported Data Rate Range | VCO post-divider L=2 | 8000 | — | 14100 | 8000 | — | 12500 | 8000 | — | 8500/ 10312.5 (24) | Mbps |
| | L=4 | 4000 | — | 7050 | 4000 | — | 6600 | 4000 | — | 6600 | Mbps |
| | L=8 | 2000 | — | 3525 | 2000 | — | 3300 | 2000 | — | 3300 | Mbps |
| | L=8, Local/Central Clock Divider =2 | 1000 | — | 1762.5 | 1000 | — | 1762.5 | 1000 | — | 1762.5 | Mbps |
| t _{pll_powerdown} ⁽¹⁵⁾ | — | 1 | — | — | 1 | — | — | 1 | — | — | μs |
| t _{pll_lock} ⁽¹⁶⁾ | — | — | — | 10 | — | — | 10 | — | — | 10 | μs |
| fPLL | | | | | | | | | | | |
| Supported Data Range | — | 600 | — | 3250/ 3125 ⁽²⁵⁾ | 600 | — | 3250/ 3125 ⁽²⁵⁾ | 600 | — | 3250/ 3125 ⁽²⁵⁾ | Mbps |
| t _{pll_powerdown} ⁽¹⁵⁾ | — | 1 | — | — | 1 | — | — | 1 | — | — | μs |

Table 24 shows the maximum transmitter data rate for the clock network.

Table 24. Clock Network Maximum Data Rate Transmitter Specifications ⁽¹⁾

| Clock Network | ATX PLL | | | CMU PLL ⁽²⁾ | | | fPLL | | |
|--------------------------------|------------------------|--------------------|---------------------------------------|------------------------|--------------------|---------------------------------------|------------------------|--------------------|---------------------------------------|
| | Non-bonded Mode (Gbps) | Bonded Mode (Gbps) | Channel Span | Non-bonded Mode (Gbps) | Bonded Mode (Gbps) | Channel Span | Non-bonded Mode (Gbps) | Bonded Mode (Gbps) | Channel Span |
| x1 ⁽³⁾ | 14.1 | — | 6 | 12.5 | — | 6 | 3.125 | — | 3 |
| x6 ⁽³⁾ | — | 14.1 | 6 | — | 12.5 | 6 | — | 3.125 | 6 |
| x6 PLL Feedback ⁽⁴⁾ | — | 14.1 | Side-wide | — | 12.5 | Side-wide | — | — | — |
| xN (PCIe) | — | 8.0 | 8 | — | 5.0 | 8 | — | — | — |
| xN (Native PHY IP) | 8.0 | 8.0 | Up to 13 channels above and below PLL | 7.99 | 7.99 | Up to 13 channels above and below PLL | 3.125 | 3.125 | Up to 13 channels above and below PLL |
| | — | 8.01 to 9.8304 | Up to 7 channels above and below PLL | | | | | | |

Notes to Table 24:

- (1) Valid data rates below the maximum specified in this table depend on the reference clock frequency and the PLL counter settings. Check the MegaWizard message during the PHY IP instantiation.
- (2) ATX PLL is recommended at 8 Gbps and above data rates for improved jitter performance.
- (3) Channel span is within a transceiver bank.
- (4) Side-wide channel bonding is allowed up to the maximum supported by the PHY IP.

Table 28. Transceiver Specifications for Stratix V GT Devices (Part 4 of 5) ⁽¹⁾

| Symbol/ Description | Conditions | Transceiver Speed Grade 2 | | | Transceiver Speed Grade 3 | | | Unit |
|--|--|------------------------------|-----|--------------------------------|------------------------------|-----|--------------------------------|------|
| | | Min | Typ | Max | Min | Typ | Max | |
| Data rate | GT channels | 19,600 | — | 28,050 | 19,600 | — | 25,780 | Mbps |
| Differential on-chip termination resistors | GT channels | — | 100 | — | — | 100 | — | Ω |
| | GX channels | (8) | | | | | | |
| V _{OCM} (AC coupled) | GT channels | — | 500 | — | — | 500 | — | mV |
| | GX channels | (8) | | | | | | |
| Rise/Fall time | GT channels | — | 15 | — | — | 15 | — | ps |
| | GX channels | (8) | | | | | | |
| Intra-differential pair skew | GX channels | (8) | | | | | | |
| Intra-transceiver block transmitter channel-to- channel skew | GX channels | (8) | | | | | | |
| Inter-transceiver block transmitter channel-to- channel skew | GX channels | (8) | | | | | | |
| CMU PLL | | | | | | | | |
| Supported Data Range | — | 600 | — | 12500 | 600 | — | 8500 | Mbps |
| t _{pll_powerdown} ⁽¹³⁾ | — | 1 | — | — | 1 | — | — | μs |
| t _{pll_lock} ⁽¹⁴⁾ | — | — | — | 10 | — | — | 10 | μs |
| ATX PLL | | | | | | | | |
| Supported Data Rate Range for GX Channels | VCO post- divider L=2 | 8000 | — | 12500 | 8000 | — | 8500 | Mbps |
| | L=4 | 4000 | — | 6600 | 4000 | — | 6600 | Mbps |
| | L=8 | 2000 | — | 3300 | 2000 | — | 3300 | Mbps |
| | L=8, Local/Central Clock Divider =2 | 1000 | — | 1762.5 | 1000 | — | 1762.5 | Mbps |
| Supported Data Rate Range for GT Channels | VCO post- divider L=2 | 9800 | — | 14025 | 9800 | — | 12890 | Mbps |
| t _{pll_powerdown} ⁽¹³⁾ | — | 1 | — | — | 1 | — | — | μs |
| t _{pll_lock} ⁽¹⁴⁾ | — | — | — | 10 | — | — | 10 | μs |
| fPLL | | | | | | | | |
| Supported Data Range | — | 600 | — | 3250/ 3.125 ⁽²³⁾ | 600 | — | 3250/ 3.125 ⁽²³⁾ | Mbps |
| t _{pll_powerdown} ⁽¹³⁾ | — | 1 | — | — | 1 | — | — | μs |

Table 28. Transceiver Specifications for Stratix V GT Devices (Part 5 of 5) ⁽¹⁾

| Symbol/ Description | Conditions | Transceiver Speed Grade 2 | | | Transceiver Speed Grade 3 | | | Unit |
|---------------------------------|------------|------------------------------|-----|-----|------------------------------|-----|-----|------|
| | | Min | Typ | Max | Min | Typ | Max | |
| t_{pll_lock} ⁽¹⁴⁾ | — | — | — | 10 | — | — | 10 | μs |

Notes to Table 28:

- (1) Speed grades shown refer to the PMA Speed Grade in the device ordering code. The maximum data rate could be restricted by the Core/PCS speed grade. Contact your Altera Sales Representative for the maximum data rate specifications in each speed grade combination offered. For more information about device ordering codes, refer to the *Stratix V Device Overview*.
- (2) The reference clock common mode voltage is equal to the VCCR_GXB power supply level.
- (3) The device cannot tolerate prolonged operation at this absolute maximum.
- (4) The differential eye opening specification at the receiver input pins assumes that receiver equalization is disabled. If you enable receiver equalization, the receiver circuitry can tolerate a lower minimum eye opening, depending on the equalization level.
- (5) Refer to Figure 5 for the GT channel AC gain curves. The total effective AC gain is the AC gain minus the DC gain.
- (6) Refer to Figure 6 for the GT channel DC gain curves.
- (7) CFP2 optical modules require the host interface to have the receiver data pins differentially terminated with 100 Ω. The internal OCT feature is available after the Stratix V FPGA configuration is completed. Altera recommends that FPGA configuration is completed before inserting the optical module. Otherwise, minimize unnecessary removal and insertion with unconfigured devices.
- (8) Specifications for this parameter are the same as for Stratix V GX and GS devices. See Table 23 for specifications.
- (9) t_{LTR} is the time required for the receive CDR to lock to the input reference clock frequency after coming out of reset.
- (10) t_{LTD} is time required for the receiver CDR to start recovering valid data after the $rx_is_lockedtodata$ signal goes high.
- (11) t_{LTD_manual} is the time required for the receiver CDR to start recovering valid data after the $rx_is_lockedtodata$ signal goes high when the CDR is functioning in the manual mode.
- (12) $t_{LTR_LTD_manual}$ is the time the receiver CDR must be kept in lock to reference (LTR) mode after the $rx_is_lockedtoref$ signal goes high when the CDR is functioning in the manual mode.
- (13) $tp11_powerdown$ is the PLL powerdown minimum pulse width.
- (14) $tp11_lock$ is the time required for the transmitter CMU/ATX PLL to lock to the input reference clock frequency after coming out of reset.
- (15) To calculate the REFCLK rms phase jitter requirement for PCIe at reference clock frequencies other than 100 MHz, use the following formula:
REFCLK rms phase jitter at f(MHz) = REFCLK rms phase jitter at 100 MHz × 100/f.
- (16) The maximum peak to peak differential input voltage V_{ID} after device configuration is equal to $4 \times (\text{absolute } V_{MAX} \text{ for receiver pin} - V_{ICM})$.
- (17) For ES devices, RREF is 2000 Ω ±1%.
- (18) To calculate the REFCLK phase noise requirement at frequencies other than 622 MHz, use the following formula: REFCLK phase noise at f(MHz) = REFCLK phase noise at 622 MHz + 20*log(f/622).
- (19) SFP/+ optical modules require the host interface to have RD+/- differentially terminated with 100 Ω. The internal OCT feature is available after the Stratix V FPGA configuration is completed. Altera recommends that FPGA configuration is completed before inserting the optical module. Otherwise, minimize unnecessary removal and insertion with unconfigured devices.
- (20) Refer to Figure 4.
- (21) For oversampling design to support data rates less than the minimum specification, the CDR needs to be in LTR mode only.
- (22) This supply follows VCCR_GXB for both GX and GT channels.
- (23) When you use fPLL as a TXPLL of the transceiver.

Figure 4 shows the differential transmitter output waveform.

Figure 4. Differential Transmitter/Receiver Output/Input Waveform

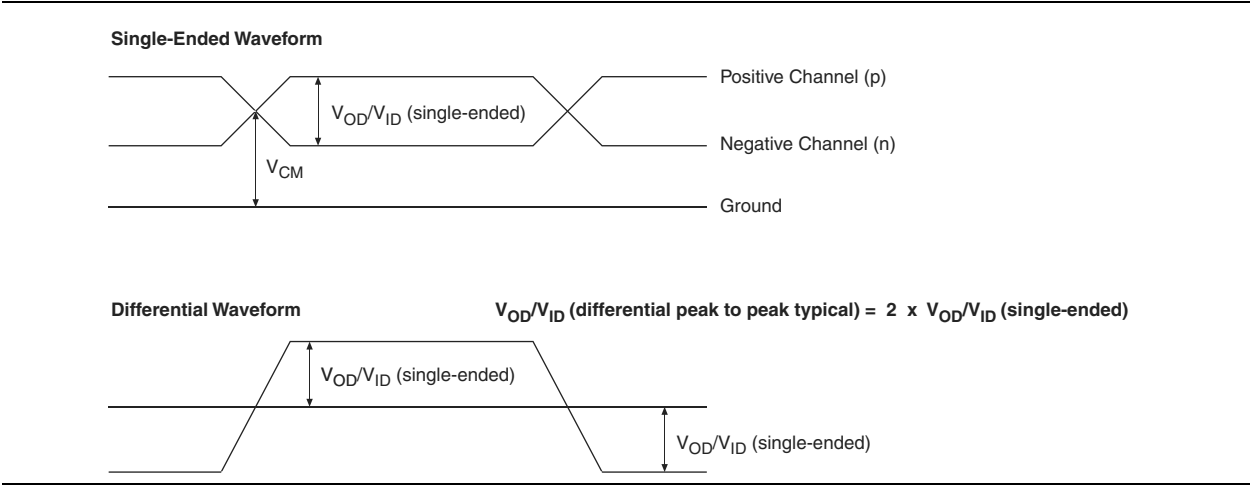


Figure 5 shows the Stratix V AC gain curves for GT channels.

Figure 5. AC Gain Curves for GT Channels

Table 33. Memory Block Performance Specifications for Stratix V Devices ^{(1), (2)} (Part 2 of 2)

| Memory | Mode | Resources Used | | Performance | | | | | | | Unit |
|------------|--|----------------|--------|-------------|---------|-----|-----|---------|---------------|-----|------|
| | | ALUTs | Memory | C1 | C2, C2L | C3 | C4 | I2, I2L | I3, I3L, I3YY | I4 | |
| M20K Block | Single-port, all supported widths | 0 | 1 | 700 | 700 | 650 | 550 | 700 | 500 | 450 | MHz |
| | Simple dual-port, all supported widths | 0 | 1 | 700 | 700 | 650 | 550 | 700 | 500 | 450 | MHz |
| | Simple dual-port with the read-during-write option set to Old Data , all supported widths | 0 | 1 | 525 | 525 | 455 | 400 | 525 | 455 | 400 | MHz |
| | Simple dual-port with ECC enabled, 512 × 32 | 0 | 1 | 450 | 450 | 400 | 350 | 450 | 400 | 350 | MHz |
| | Simple dual-port with ECC and optional pipeline registers enabled, 512 × 32 | 0 | 1 | 600 | 600 | 500 | 450 | 600 | 500 | 450 | MHz |
| | True dual port, all supported widths | 0 | 1 | 700 | 700 | 650 | 550 | 700 | 500 | 450 | MHz |
| | ROM, all supported widths | 0 | 1 | 700 | 700 | 650 | 550 | 700 | 500 | 450 | MHz |

Notes to Table 33:

- (1) To achieve the maximum memory block performance, use a memory block clock that comes through global clock routing from an on-chip PLL set to **50%** output duty cycle. Use the Quartus II software to report timing for this and other memory block clocking schemes.
- (2) When you use the error detection cyclical redundancy check (CRC) feature, there is no degradation in F_{MAX}.
- (3) The F_{MAX} specification is only achievable with Fitter options, **MLAB Implementation In 16-Bit Deep Mode** enabled.

Temperature Sensing Diode Specifications

Table 34 lists the internal TSD specification.

Table 34. Internal Temperature Sensing Diode Specification

| Temperature Range | Accuracy | Offset Calibrated Option | Sampling Rate | Conversion Time | Resolution | Minimum Resolution with no Missing Codes |
|-------------------|----------|--------------------------|----------------|-----------------|------------|--|
| –40°C to 100°C | ±8°C | No | 1 MHz, 500 KHz | < 100 ms | 8 bits | 8 bits |

Table 35 lists the specifications for the Stratix V external temperature sensing diode.

Table 35. External Temperature Sensing Diode Specifications for Stratix V Devices

| Description | Min | Typ | Max | Unit |
|--|-------|-------|-------|------|
| I _{bias} , diode source current | 8 | — | 200 | μA |
| V _{bias} , voltage across diode | 0.3 | — | 0.9 | V |
| Series resistance | — | — | < 1 | Ω |
| Diode ideality factor | 1.006 | 1.008 | 1.010 | — |

Table 40. DQS Phase Offset Delay Per Setting for Stratix V Devices ^{(1), (2)} (Part 2 of 2)

| Speed Grade | Min | Max | Unit |
|-------------|-----|-----|------|
| C4,I4 | 8 | 16 | ps |

Notes to Table 40:

- (1) The typical value equals the average of the minimum and maximum values.
- (2) The delay settings are linear with a cumulative delay variation of 40 ps for all speed grades. For example, when using a –2 speed grade and applying a 10-phase offset setting to a 90° phase shift at 400 MHz, the expected average cumulative delay is $[625 \text{ ps} + (10 \times 10 \text{ ps}) \pm 20 \text{ ps}] = 725 \text{ ps} \pm 20 \text{ ps}$.

Table 41 lists the DQS phase shift error for Stratix V devices.

Table 41. DQS Phase Shift Error Specification for DLL-Delayed Clock ($t_{\text{DQS_PSERR}}$) for Stratix V Devices ⁽¹⁾

| Number of DQS Delay Buffers | C1 | C2, C2L, I2, I2L | C3, I3, I3L, I3YY | C4,I4 | Unit |
|-----------------------------|-----|------------------|-------------------|-------|------|
| 1 | 28 | 28 | 30 | 32 | ps |
| 2 | 56 | 56 | 60 | 64 | ps |
| 3 | 84 | 84 | 90 | 96 | ps |
| 4 | 112 | 112 | 120 | 128 | ps |

Notes to Table 41:

- (1) This error specification is the absolute maximum and minimum error. For example, skew on three DQS delay buffers in a –2 speed grade is $\pm 78 \text{ ps}$ or $\pm 39 \text{ ps}$.

Table 42 lists the memory output clock jitter specifications for Stratix V devices.

Table 42. Memory Output Clock Jitter Specification for Stratix V Devices ^{(1), (Part 1 of 2)} ^{(2), (3)}

| Clock Network | Parameter | Symbol | C1 | | C2, C2L, I2, I2L | | C3, I3, I3L, I3YY | | C4,I4 | | Unit |
|---------------|------------------------------|------------------------|------|-----|------------------|-----|-------------------|------|-------|------|------|
| | | | Min | Max | Min | Max | Min | Max | Min | Max | |
| Regional | Clock period jitter | $t_{\text{JIT(per)}}$ | –50 | 50 | –50 | 50 | –55 | 55 | –55 | 55 | ps |
| | Cycle-to-cycle period jitter | $t_{\text{JIT(cc)}}$ | –100 | 100 | –100 | 100 | –110 | 110 | –110 | 110 | ps |
| | Duty cycle jitter | $t_{\text{JIT(duty)}}$ | –50 | 50 | –50 | 50 | –82.5 | 82.5 | –82.5 | 82.5 | ps |
| Global | Clock period jitter | $t_{\text{JIT(per)}}$ | –75 | 75 | –75 | 75 | –82.5 | 82.5 | –82.5 | 82.5 | ps |
| | Cycle-to-cycle period jitter | $t_{\text{JIT(cc)}}$ | –150 | 150 | –150 | 150 | –165 | 165 | –165 | 165 | ps |
| | Duty cycle jitter | $t_{\text{JIT(duty)}}$ | –75 | 75 | –75 | 75 | –90 | 90 | –90 | 90 | ps |

Table 42. Memory Output Clock Jitter Specification for Stratix V Devices ⁽¹⁾, (Part 2 of 2) ⁽²⁾, ⁽³⁾

| Clock Network | Parameter | Symbol | C1 | | C2, C2L, I2, I2L | | C3, I3, I3L, I3YY | | C4,I4 | | Unit |
|---------------|------------------------------|-----------------|-------|------|------------------|------|-------------------|-----|-------|-----|------|
| | | | Min | Max | Min | Max | Min | Max | Min | Max | |
| PHY Clock | Clock period jitter | $t_{JIT(per)}$ | -25 | 25 | -25 | 25 | -30 | 30 | -35 | 35 | ps |
| | Cycle-to-cycle period jitter | $t_{JIT(cc)}$ | -50 | 50 | -50 | 50 | -60 | 60 | -70 | 70 | ps |
| | Duty cycle jitter | $t_{JIT(duty)}$ | -37.5 | 37.5 | -37.5 | 37.5 | -45 | 45 | -56 | 56 | ps |

Notes to Table 42:

- (1) The clock jitter specification applies to the memory output clock pins generated using differential signal-splitter and DDIO circuits clocked by a PLL output routed on a PHY, regional, or global clock network as specified. Altera recommends using PHY clock networks whenever possible.
- (2) The clock jitter specification applies to the memory output clock pins clocked by an integer PLL.
- (3) The memory output clock jitter is applicable when an input jitter of 30 ps peak-to-peak is applied with bit error rate (BER) -12, equivalent to 14 sigma.

OCT Calibration Block Specifications

Table 43 lists the OCT calibration block specifications for Stratix V devices.

Table 43. OCT Calibration Block Specifications for Stratix V Devices

| Symbol | Description | Min | Typ | Max | Unit |
|----------------|---|-----|------|-----|--------|
| OCTUSRCLK | Clock required by the OCT calibration blocks | — | — | 20 | MHz |
| T_{OCTCAL} | Number of OCTUSRCLK clock cycles required for OCT R_S/R_T calibration | — | 1000 | — | Cycles |
| $T_{OCTSHIFT}$ | Number of OCTUSRCLK clock cycles required for the OCT code to shift out | — | 32 | — | Cycles |
| T_{RS_RT} | Time required between the <code>dyn_term_ctrl</code> and <code>oe</code> signal transitions in a bidirectional I/O buffer to dynamically switch between OCT R_S and R_T (Figure 10) | — | 2.5 | — | ns |

Figure 10 shows the timing diagram for the `oe` and `dyn_term_ctrl` signals.

Figure 10. Timing Diagram for `oe` and `dyn_term_ctrl` Signals

FPP Configuration Timing when DCLK-to-DATA [] = 1

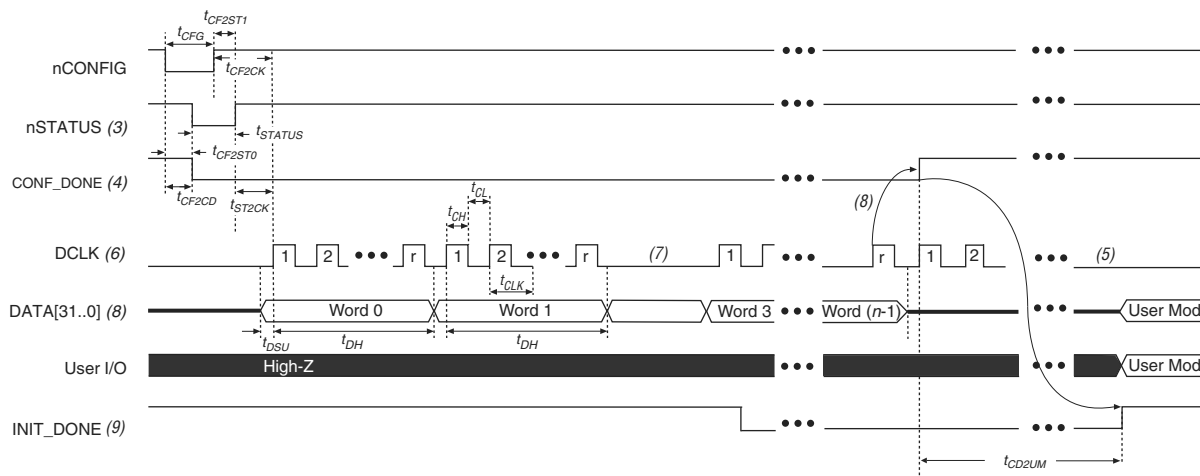
Figure 12 shows the timing waveform for FPP configuration when using a MAX II or MAX V device as an external host. This waveform shows timing when the DCLK-to-DATA [] ratio is 1.

Figure 12. FPP Configuration Timing Waveform When the DCLK-to-DATA[] Ratio is 1 ^{(1), (2)}



Notes to Figure 12:

- (1) Use this timing waveform when the DCLK-to-DATA [] ratio is 1.
- (2) The beginning of this waveform shows the device in user mode. In user mode, nCONFIG, nSTATUS, and CONF_DONE are at logic-high levels. When nCONFIG is pulled low, a reconfiguration cycle begins.
- (3) After power-up, the Stratix V device holds nSTATUS low for the time of the POR delay.
- (4) After power-up, before and during configuration, CONF_DONE is low.
- (5) Do not leave DCLK floating after configuration. DCLK is ignored after configuration is complete. It can toggle high or low if required.
- (6) For FPP x16, use DATA [15..0]. For FPP x8, use DATA [7..0]. DATA [31..0] are available as a user I/O pin after configuration. The state of this pin depends on the dual-purpose pin settings.
- (7) To ensure a successful configuration, send the entire configuration data to the Stratix V device. CONF_DONE is released high when the Stratix V device receives all the configuration data successfully. After CONF_DONE goes high, send two additional falling edges on DCLK to begin initialization and enter user mode.
- (8) After the option bit to enable the INIT_DONE pin is configured into the device, the INIT_DONE goes low.

Figure 13. FPP Configuration Timing Waveform When the DCLK-to-DATA[] Ratio is >1 (1), (2)**Notes to Figure 13:**

- (1) Use this timing waveform and parameters when the DCLK-to-DATA[] ratio is >1. To find out the DCLK-to-DATA[] ratio for your system, refer to Table 49 on page 55.
- (2) The beginning of this waveform shows the device in user mode. In user mode, nCONFIG, nSTATUS, and CONF_DONE are at logic high levels. When nCONFIG is pulled low, a reconfiguration cycle begins.
- (3) After power-up, the Stratix V device holds nSTATUS low for the time as specified by the POR delay.
- (4) After power-up, before and during configuration, CONF_DONE is low.
- (5) Do not leave DCLK floating after configuration. You can drive it high or low, whichever is more convenient.
- (6) "r" denotes the DCLK-to-DATA[] ratio. For the DCLK-to-DATA[] ratio based on the decompression and the design security feature enable settings, refer to Table 49 on page 55.
- (7) If needed, pause DCLK by holding it low. When DCLK restarts, the external host must provide data on the DATA[31..0] pins prior to sending the first DCLK rising edge.
- (8) To ensure a successful configuration, send the entire configuration data to the Stratix V device. CONF_DONE is released high after the Stratix V device receives all the configuration data successfully. After CONF_DONE goes high, send two additional falling edges on DCLK to begin initialization and enter user mode.
- (9) After the option bit to enable the INIT_DONE pin is configured into the device, the INIT_DONE goes low.

Document Revision History

Table 61 lists the revision history for this chapter.

Table 61. Document Revision History (Part 1 of 3)

| Date | Version | Changes |
|---------------|---------|---|
| June 2018 | 3.9 | <ul style="list-style-type: none"> ■ Added the “Stratix V Device Overshoot Duration” figure. |
| April 2017 | 3.8 | <ul style="list-style-type: none"> ■ Added a footnote to the “High-Speed I/O Specifications for Stratix V Devices” table. ■ Changed the minimum value for t_{CD2UMC} in the “PS Timing Parameters for Stratix V Devices” table. ■ Changed the condition for $100\text{-}\Omega$ R_D in the “OCT Without Calibration Resistance Tolerance Specifications for Stratix V Devices” table. ■ Changed the minimum value for t_{CD2UMC} in the “AS Timing Parameters for AS ‘1 and AS ‘4 Configurations in Stratix V Devices” table ■ Changed the minimum value for t_{CD2UMC} in the “FPP Timing Parameters for Stratix V Devices When the DCLK-to-DATA[] Ratio is >1” table. ■ Changed the minimum value for t_{CD2UMC} in the “FPP Timing Parameters for Stratix V Devices When the DCLK-to-DATA[] Ratio is >1” table. ■ Changed the minimum number of clock cycles value in the “Initialization Clock Source Option and the Maximum Frequency” table. |
| June 2016 | 3.7 | <ul style="list-style-type: none"> ■ Added the V_{ID} minimum specification for LVPECL in the “Differential I/O Standard Specifications for Stratix V Devices” table ■ Added the I_{OUT} specification to the “Absolute Maximum Ratings for Stratix V Devices” table. |
| December 2015 | 3.6 | <ul style="list-style-type: none"> ■ Added a footnote to the “High-Speed I/O Specifications for Stratix V Devices” table. |
| December 2015 | 3.5 | <ul style="list-style-type: none"> ■ Changed the transmitter, receiver, and ATX PLL data rate specifications in the “Transceiver Specifications for Stratix V GX and GS Devices” table. ■ Changed the configuration .rbf sizes in the “Uncompressed .rbf Sizes for Stratix V Devices” table. |
| July 2015 | 3.4 | <ul style="list-style-type: none"> ■ Changed the data rate specification for transceiver speed grade 3 in the following tables: <ul style="list-style-type: none"> ■ “Transceiver Specifications for Stratix V GX and GS Devices” ■ “Stratix V Standard PCS Approximate Maximum Date Rate” ■ “Stratix V 10G PCS Approximate Maximum Data Rate” ■ Changed the conditions for reference clock rise and fall time, and added a note to the “Transceiver Specifications for Stratix V GX and GS Devices” table. ■ Added a note to the “Minimum differential eye opening at receiver serial input pins” specification in the “Transceiver Specifications for Stratix V GX and GS Devices” table. ■ Changed the t_{CO} maximum value in the “AS Timing Parameters for AS ‘1 and AS ‘4 Configurations in Stratix V Devices” table. ■ Removed the CDR ppm tolerance specification from the “Transceiver Specifications for Stratix V GX and GS Devices” table. |

Table 61. Document Revision History (Part 2 of 3)

| Date | Version | Changes |
|---------------|---------|--|
| November 2014 | 3.3 | <ul style="list-style-type: none"> ■ Added the I3YY speed grade and changed the data rates for the GX channel in Table 1. ■ Added the I3YY speed grade to the V_{CC} description in Table 6. ■ Added the I3YY speed grade to V_{CCHIP_L}, V_{CCHIP_R}, V_{CCHSSI_L}, and V_{CCHSSI_R} descriptions in Table 7. ■ Added 240-Ω to Table 11. ■ Changed CDR PPM tolerance in Table 23. ■ Added additional max data rate for fPLL in Table 23. ■ Added the I3YY speed grade and changed the data rates for transceiver speed grade 3 in Table 25. ■ Added the I3YY speed grade and changed the data rates for transceiver speed grade 3 in Table 26. ■ Changed CDR PPM tolerance in Table 28. ■ Added additional max data rate for fPLL in Table 28. ■ Changed the mode descriptions for MLAB and M20K in Table 33. ■ Changed the Max value of f_{HCLK_OUT} for the C2, C2L, I2, I2L speed grades in Table 36. ■ Changed the frequency ranges for C1 and C2 in Table 39. ■ Changed the .rbf file sizes for 5SGSD6 and 5SGSD8 in Table 47. ■ Added note about nSTATUS to Table 50, Table 51, Table 54. ■ Changed the available settings in Table 58. ■ Changed the note in “Periphery Performance”. ■ Updated the “I/O Standard Specifications” section. ■ Updated the “Raw Binary File Size” section. ■ Updated the receiver voltage input range in Table 22. ■ Updated the max frequency for the LVDS clock network in Table 36. ■ Updated the DCLK note to Figure 11. ■ Updated Table 23 VO_{CM} (DC Coupled) condition. ■ Updated Table 6 and Table 7. ■ Added the DCLK specification to Table 55. ■ Updated the notes for Table 47. ■ Updated the list of parameters for Table 56. |
| November 2013 | 3.2 | ■ Updated Table 28 |
| November 2013 | 3.1 | ■ Updated Table 33 |
| November 2013 | 3.0 | ■ Updated Table 23 and Table 28 |
| October 2013 | 2.9 | ■ Updated the “Transceiver Characterization” section |
| October 2013 | 2.8 | <ul style="list-style-type: none"> ■ Updated Table 3, Table 12, Table 14, Table 19, Table 20, Table 23, Table 24, Table 28, Table 30, Table 31, Table 32, Table 33, Table 36, Table 39, Table 40, Table 41, Table 42, Table 47, Table 53, Table 58, and Table 59 ■ Added Figure 1 and Figure 3 ■ Added the “Transceiver Characterization” section ■ Removed all “Preliminary” designations. |