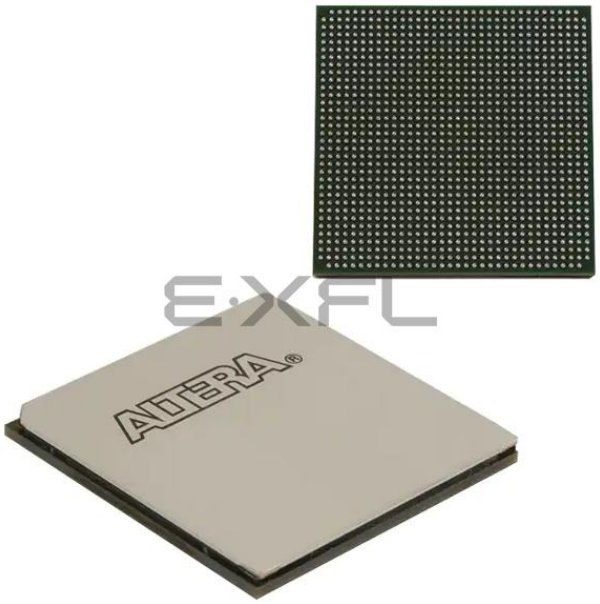

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The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	128300
Number of Logic Elements/Cells	340000
Total RAM Bits	19456000
Number of I/O	600
Number of Gates	-
Voltage - Supply	0.82V ~ 0.88V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	1152-BBGA, FCBGA
Supplier Device Package	1152-FBGA (35x35)
Purchase URL	https://www.e-xfl.com/product-detail/intel/5sgxma3h3f35c2ln

Table 1. Stratix V GX and GS Commercial and Industrial Speed Grade Offering (1), (2), (3) (Part 2 of 2)

Transceiver Speed Grade	Core Speed Grade							
	C1	C2, C2L	C3	C4	I2, I2L	I3, I3L	I3YY	I4
3 GX channel—8.5 Gbps	—	Yes	Yes	Yes	—	Yes	Yes (4)	Yes

Notes to Table 1:

(1) C = Commercial temperature grade; I = Industrial temperature grade.

(2) Lower number refers to faster speed grade.

(3) C2L, I2L, and I3L speed grades are for low-power devices.

(4) I3YY speed grades can achieve up to 10.3125 Gbps.

Table 2 lists the industrial and commercial speed grades for the Stratix V GT devices.

Table 2. Stratix V GT Commercial and Industrial Speed Grade Offering (1), (2)

Transceiver Speed Grade	Core Speed Grade			
	C1	C2	I2	I3
2 GX channel—12.5 Gbps GT channel—28.05 Gbps	Yes	Yes	—	—
3 GX channel—12.5 Gbps GT channel—25.78 Gbps	Yes	Yes	Yes	Yes

Notes to Table 2:

(1) C = Commercial temperature grade; I = Industrial temperature grade.

(2) Lower number refers to faster speed grade.

Absolute Maximum Ratings

Absolute maximum ratings define the maximum operating conditions for Stratix V devices. The values are based on experiments conducted with the devices and theoretical modeling of breakdown and damage mechanisms. The functional operation of the device is not implied for these conditions.

CAUTION

Conditions other than those listed in Table 3 may cause permanent damage to the device. Additionally, device operation at the absolute maximum ratings for extended periods of time may have adverse effects on the device.

Table 3. Absolute Maximum Ratings for Stratix V Devices (Part 1 of 2)

Symbol	Description	Minimum	Maximum	Unit
V_{CC}	Power supply for core voltage and periphery circuitry	–0.5	1.35	V
V_{CCPT}	Power supply for programmable power technology	–0.5	1.8	V
V_{CCPGM}	Power supply for configuration pins	–0.5	3.9	V
V_{CC_AUX}	Auxiliary supply for the programmable power technology	–0.5	3.4	V
V_{CCBAT}	Battery back-up power supply for design security volatile key register	–0.5	3.9	V
V_{CCPD}	I/O pre-driver power supply	–0.5	3.9	V
V_{CCIO}	I/O power supply	–0.5	3.9	V

Table 6. Recommended Operating Conditions for Stratix V Devices (Part 2 of 2)

Symbol	Description	Condition	Min (4)	Typ	Max (4)	Unit
t_{RAMP}	Power supply ramp time	Standard POR	200 µs	—	100 ms	—
		Fast POR	200 µs	—	4 ms	—

Notes to Table 6:

(1) V_{CCPD} must be 2.5 V when V_{CCIO} is 2.5, 1.8, 1.5, 1.35, 1.25 or 1.2 V. V_{CCPD} must be 3.0 V when V_{CCIO} is 3.0 V.

(2) If you do not use the design security feature in Stratix V devices, connect V_{CCBAT} to a 1.2- to 3.0-V power supply. Stratix V power-on-reset (POR) circuitry monitors V_{CCBAT}. Stratix V devices will not exit POR if V_{CCBAT} stays at logic low.

(3) C2L and I2L can also be run at 0.90 V for legacy boards that were designed for the C2 and I2 speed grades.

(4) The power supply value describes the budget for the DC (static) power supply tolerance and does not include the dynamic tolerance requirements. Refer to the PDN tool for the additional budget for the dynamic tolerance requirements.

Table 7 lists the transceiver power supply recommended operating conditions for Stratix V GX, GS, and GT devices.

Table 7. Recommended Transceiver Power Supply Operating Conditions for Stratix V GX, GS, and GT Devices (Part 1 of 2)

Symbol	Description	Devices	Minimum (4)	Typical	Maximum (4)	Unit
V_{CCA_GXBL} (1), (3)	Transceiver channel PLL power supply (left side)	GX, GS, GT	2.85	3.0	3.15	V
			2.375	2.5	2.625	
V_{CCA_GXBR} (1), (3)	Transceiver channel PLL power supply (right side)	GX, GS	2.85	3.0	3.15	V
			2.375	2.5	2.625	
V_{CCA_GTBR}	Transceiver channel PLL power supply (right side)	GT	2.85	3.0	3.15	V
V_{CCHIP_L}	Transceiver hard IP power supply (left side; C1, C2, I2, and I3YY speed grades)	GX, GS, GT	0.87	0.9	0.93	V
	Transceiver hard IP power supply (left side; C2L, C3, C4, I2L, I3, I3L, and I4 speed grades)	GX, GS, GT	0.82	0.85	0.88	V
V_{CCHIP_R}	Transceiver hard IP power supply (right side; C1, C2, I2, and I3YY speed grades)	GX, GS, GT	0.87	0.9	0.93	V
	Transceiver hard IP power supply (right side; C2L, C3, C4, I2L, I3, I3L, and I4 speed grades)	GX, GS, GT	0.82	0.85	0.88	V
V_{CCHSSI_L}	Transceiver PCS power supply (left side; C1, C2, I2, and I3YY speed grades)	GX, GS, GT	0.87	0.9	0.93	V
	Transceiver PCS power supply (left side; C2L, C3, C4, I2L, I3, I3L, and I4 speed grades)	GX, GS, GT	0.82	0.85	0.88	V
V_{CCHSSI_R}	Transceiver PCS power supply (right side; C1, C2, I2, and I3YY speed grades)	GX, GS, GT	0.87	0.9	0.93	V
	Transceiver PCS power supply (right side; C2L, C3, C4, I2L, I3, I3L, and I4 speed grades)	GX, GS, GT	0.82	0.85	0.88	V
V_{CCR_GXBL} (2)	Receiver analog power supply (left side)	GX, GS, GT	0.82	0.85	0.88	V
			0.87	0.90	0.93	
			0.97	1.0	1.03	
			1.03	1.05	1.07	

Table 23. Transceiver Specifications for Stratix V GX and GS Devices (1) (Part 2 of 7)

Symbol/ Description	Conditions	Transceiver Speed Grade 1			Transceiver Speed Grade 2			Transceiver Speed Grade 3			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Spread-spectrum downspread	PCIe	—	0 to –0.5	—	—	0 to –0.5	—	—	0 to –0.5	—	%
On-chip termination resistors (21)	—	—	100	—	—	100	—	—	100	—	Ω
Absolute V_{MAX} (5)	Dedicated reference clock pin	—	—	1.6	—	—	1.6	—	—	1.6	V
	RX reference clock pin	—	—	1.2	—	—	1.2	—	—	1.2	
Absolute V_{MIN}	—	–0.4	—	—	–0.4	—	—	–0.4	—	—	V
Peak-to-peak differential input voltage	—	200	—	1600	200	—	1600	200	—	1600	mV
V_{ICM} (AC coupled) (3)	Dedicated reference clock pin	1050/1000/900/850 (2)			1050/1000/900/850 (2)			1050/1000/900/850 (2)			mV
	RX reference clock pin	1.0/0.9/0.85 (4)			1.0/0.9/0.85 (4)			1.0/0.9/0.85 (4)			V
V_{ICM} (DC coupled)	HCSL I/O standard for PCIe reference clock	250	—	550	250	—	550	250	—	550	mV
Transmitter REFCLK Phase Noise (622 MHz) (20)	100 Hz	—	—	-70	—	—	-70	—	—	-70	dBc/Hz
	1 kHz	—	—	-90	—	—	-90	—	—	-90	dBc/Hz
	10 kHz	—	—	-100	—	—	-100	—	—	-100	dBc/Hz
	100 kHz	—	—	-110	—	—	-110	—	—	-110	dBc/Hz
	≥1 MHz	—	—	-120	—	—	-120	—	—	-120	dBc/Hz
Transmitter REFCLK Phase Jitter (100 MHz) (17)	10 kHz to 1.5 MHz (PCIe)	—	—	3	—	—	3	—	—	3	ps (rms)
R_{REF} (19)	—	—	1800 ±1%	—	—	1800 ±1%	—	—	1800 ±1%	—	Ω
Transceiver Clocks											
`fixedclk` clock frequency	PCIe Receiver Detect	—	100 or 125	—	—	100 or 125	—	—	100 or 125	—	MHz

Table 23. Transceiver Specifications for Stratix V GX and GS Devices (1) (Part 5 of 7)

Symbol/ Description	Conditions	Transceiver Speed Grade 1			Transceiver Speed Grade 2			Transceiver Speed Grade 3			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Programmable DC gain	DC Gain Setting = 0	—	0	—	—	0	—	—	0	—	dB
	DC Gain Setting = 1	—	2	—	—	2	—	—	2	—	dB
	DC Gain Setting = 2	—	4	—	—	4	—	—	4	—	dB
	DC Gain Setting = 3	—	6	—	—	6	—	—	6	—	dB
	DC Gain Setting = 4	—	8	—	—	8	—	—	8	—	dB
Transmitter											
Supported I/O Standards	—	1.4-V and 1.5-V PCML									
Data rate (Standard PCS)	—	600	—	12200	600	—	12200	600	—	8500/ 10312.5 (24)	Mbps
Data rate (10G PCS)	—	600	—	14100	600	—	12500	600	—	8500/ 10312.5 (24)	Mbps
Differential on-chip termination resistors	85-Ω setting	—	85 ± 20%	—	—	85 ± 20%	—	—	85 ± 20%	—	Ω
	100-Ω setting	—	100 ± 20%	—	—	100 ± 20%	—	—	100 ± 20%	—	Ω
	120-Ω setting	—	120 ± 20%	—	—	120 ± 20%	—	—	120 ± 20%	—	Ω
	150-Ω setting	—	150 ± 20%	—	—	150 ± 20%	—	—	150 ± 20%	—	Ω
V_{OCM} (AC coupled)	0.65-V setting	—	650	—	—	650	—	—	650	—	mV
V_{OCM} (DC coupled)	—	—	650	—	—	650	—	—	650	—	mV
Rise time (7)	20% to 80%	30	—	160	30	—	160	30	—	160	ps
Fall time (7)	80% to 20%	30	—	160	30	—	160	30	—	160	ps
Intra-differential pair skew	Tx V_{CM} = 0.5 V and slew rate of 15 ps	—	—	15	—	—	15	—	—	15	ps
Intra-transceiver block transmitter channel-to-channel skew	x6 PMA bonded mode	—	—	120	—	—	120	—	—	120	ps

Table 23. Transceiver Specifications for Stratix V GX and GS Devices (1) (Part 6 of 7)

Symbol/ Description	Conditions	Transceiver Speed Grade 1			Transceiver Speed Grade 2			Transceiver Speed Grade 3			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Inter-transceiver block transmitter channel-to-channel skew	xN PMA bonded mode	—	—	500	—	—	500	—	—	500	ps
CMU PLL											
Supported Data Range	—	600	—	12500	600	—	12500	600	—	8500/ 10312.5 (24)	Mbps
$t_{pll\_powerdown}$ (15)	—	1	—	—	1	—	—	1	—	—	µs
t_{pll_lock} (16)	—	—	—	10	—	—	10	—	—	10	µs
ATX PLL											
Supported Data Rate Range	VCO post-divider L=2	8000	—	14100	8000	—	12500	8000	—	8500/ 10312.5 (24)	Mbps
	L=4	4000	—	7050	4000	—	6600	4000	—	6600	Mbps
	L=8	2000	—	3525	2000	—	3300	2000	—	3300	Mbps
	L=8, Local/Central Clock Divider =2	1000	—	1762.5	1000	—	1762.5	1000	—	1762.5	Mbps
$t_{pll\_powerdown}$ (15)	—	1	—	—	1	—	—	1	—	—	µs
t_{pll_lock} (16)	—	—	—	10	—	—	10	—	—	10	µs
fPLL											
Supported Data Range	—	600	—	3250/ 3125 (25)	600	—	3250/ 3125 (25)	600	—	3250/ 3125 (25)	Mbps
$t_{pll\_powerdown}$ (15)	—	1	—	—	1	—	—	1	—	—	µs

Table 25 shows the approximate maximum data rate using the standard PCS.

Table 25. Stratix V Standard PCS Approximate Maximum Date Rate *(1), (3)*

Mode *(2)*	Transceiver Speed Grade	PMA Width	20	20	16	16	10	10	8	8
		PCS/Core Width	40	20	32	16	20	10	16	8
FIFO	1	C1, C2, C2L, I2, I2L core speed grade	12.2	11.4	9.76	9.12	6.5	5.8	5.2	4.72
	2	C1, C2, C2L, I2, I2L core speed grade	12.2	11.4	9.76	9.12	6.5	5.8	5.2	4.72
		C3, I3, I3L core speed grade	9.8	9.0	7.84	7.2	5.3	4.7	4.24	3.76
	3	C1, C2, C2L, I2, I2L core speed grade	8.5	8.5	8.5	8.5	6.5	5.8	5.2	4.72
		I3YY core speed grade	10.3125	10.3125	7.84	7.2	5.3	4.7	4.24	3.76
		C3, I3, I3L core speed grade	8.5	8.5	7.84	7.2	5.3	4.7	4.24	3.76
		C4, I4 core speed grade	8.5	8.2	7.04	6.56	4.8	4.2	3.84	3.44
Register	1	C1, C2, C2L, I2, I2L core speed grade	12.2	11.4	9.76	9.12	6.1	5.7	4.88	4.56
	2	C1, C2, C2L, I2, I2L core speed grade	12.2	11.4	9.76	9.12	6.1	5.7	4.88	4.56
		C3, I3, I3L core speed grade	9.8	9.0	7.92	7.2	4.9	4.5	3.96	3.6
	3	C1, C2, C2L, I2, I2L core speed grade	10.3125	10.3125	10.3125	10.3125	6.1	5.7	4.88	4.56
		I3YY core speed grade	10.3125	10.3125	7.92	7.2	4.9	4.5	3.96	3.6
		C3, I3, I3L core speed grade	8.5	8.5	7.92	7.2	4.9	4.5	3.96	3.6
		C4, I4 core speed grade	8.5	8.2	7.04	6.56	4.4	4.1	3.52	3.28

Notes to Table 25:

(1) The maximum data rate is in Gbps.

(2) The Phase Compensation FIFO can be configured in FIFO mode or register mode. In the FIFO mode, the pointers are not fixed, and the latency can vary. In the register mode the pointers are fixed for low latency.

(3) The maximum data rate is also constrained by the transceiver speed grade. Refer to Table 1 for the transceiver speed grade.

Table 27 shows the V_{OD} settings for the GX channel.

Table 27. Typical V_{OD} Setting for GX Channel, TX Termination = 100 Ω (2)

Symbol	V_{OD} Setting	V_{OD} Value (mV)	V_{OD} Setting	V_{OD} Value (mV)
V_{OD} differential peak to peak typical (3)	0 (1)	0	32	640
	1 (1)	20	33	660
	2 (1)	40	34	680
	3 (1)	60	35	700
	4 (1)	80	36	720
	5 (1)	100	37	740
	6	120	38	760
	7	140	39	780
	8	160	40	800
	9	180	41	820
	10	200	42	840
	11	220	43	860
	12	240	44	880
	13	260	45	900
	14	280	46	920
	15	300	47	940
	16	320	48	960
	17	340	49	980
	18	360	50	1000
	19	380	51	1020
	20	400	52	1040
	21	420	53	1060
	22	440	54	1080
	23	460	55	1100
	24	480	56	1120
	25	500	57	1140
	26	520	58	1160
	27	540	59	1180
	28	560	60	1200
	29	580	61	1220
	30	600	62	1240
	31	620	63	1260

Note to Table 27:

(1) If TX termination resistance = 100Ω, this VOD setting is illegal.

(2) The tolerance is +/-20% for all VOD settings except for settings 2 and below.

(3) Refer to Figure 2.

Table 28. Transceiver Specifications for Stratix V GT Devices (Part 4 of 5) (1)

Symbol/ Description	Conditions	Transceiver Speed Grade 2			Transceiver Speed Grade 3			Unit
		Min	Typ	Max	Min	Typ	Max	
Data rate	GT channels	19,600	—	28,050	19,600	—	25,780	Mbps
Differential on-chip termination resistors	GT channels	—	100	—	—	100	—	Ω
	GX channels	(8)						
V_{OCM} (AC coupled)	GT channels	—	500	—	—	500	—	mV
	GX channels	(8)						
Rise/Fall time	GT channels	—	15	—	—	15	—	ps
	GX channels	(8)						
Intra-differential pair skew	GX channels	(8)						
Intra-transceiver block transmitter channel-to-channel skew	GX channels	(8)						
Inter-transceiver block transmitter channel-to-channel skew	GX channels	(8)						
CMU PLL								
Supported Data Range	—	600	—	12500	600	—	8500	Mbps
$t_{pll\_powerdown}$ (13)	—	1	—	—	1	—	—	µs
t_{pll_lock} (14)	—	—	—	10	—	—	10	µs
ATX PLL								
Supported Data Rate Range for GX Channels	VCO post-divider L=2	8000	—	12500	8000	—	8500	Mbps
	L=4	4000	—	6600	4000	—	6600	Mbps
	L=8	2000	—	3300	2000	—	3300	Mbps
	L=8, Local/Central Clock Divider =2	1000	—	1762.5	1000	—	1762.5	Mbps
Supported Data Rate Range for GT Channels	VCO post-divider L=2	9800	—	14025	9800	—	12890	Mbps
$t_{pll\_powerdown}$ (13)	—	1	—	—	1	—	—	µs
t_{pll_lock} (14)	—	—	—	10	—	—	10	µs
fPLL								
Supported Data Range	—	600	—	3250/ 3.125 (23)	600	—	3250/ 3.125 (23)	Mbps
$t_{pll\_powerdown}$ (13)	—	1	—	—	1	—	—	µs

Table 29 shows the V_{OD} settings for the GT channel.

Table 29. Typical V_{OD} Setting for GT Channel, TX Termination = 100 Ω

Symbol	V_{OD} Setting	V_{OD} Value (mV)
V_{OD} differential peak to peak typical (1)	0	0
	1	200
	2	400
	3	600
	4	800
	5	1000

Note:

(1) Refer to Figure 4.

Figure 6 shows the Stratix V DC gain curves for GT channels.

Figure 6. DC Gain Curves for GT Channels

Transceiver Characterization

This section summarizes the Stratix V transceiver characterization results for compliance with the following protocols:

- Interlaken
- 40G (XLAUI)/100G (CAUI)
- 10GBase-KR
- QSGMII
- XAUI
- SFI
- Gigabit Ethernet (Gbe / GIGE)
- SPAUI
- Serial Rapid IO (SRIO)
- CPRI
- OBSAI
- Hyper Transport (HT)
- SATA
- SAS
- CEI

Table 32. Block Performance Specifications for Stratix V DSP Devices (Part 2 of 2)

Mode	Peformance							Unit
	C1	C2, C2L	I2, I2L	C3	I3, I3L, I3YY	C4	I4	
Modes using Three DSPs								
One complex 18 x 25	425	425	415	340	340	275	265	MHz
Modes using Four DSPs								
One complex 27 x 27	465	465	465	380	380	300	290	MHz

Memory Block Specifications

Table 33 lists the Stratix V memory block specifications.

Table 33. Memory Block Performance Specifications for Stratix V Devices (1), (2) (Part 1 of 2)

Memory	Mode	Resources Used		Performance							Unit
		ALUTs	Memory	C1	C2, C2L	C3	C4	I2, I2L	I3, I3L, I3YY	I4	
MLAB	Single port, all supported widths	0	1	450	450	400	315	450	400	315	MHz
	Simple dual-port, x32/x64 depth	0	1	450	450	400	315	450	400	315	MHz
	Simple dual-port, x16 depth (3)	0	1	675	675	533	400	675	533	400	MHz
	ROM, all supported widths	0	1	600	600	500	450	600	500	450	MHz

Table 33. Memory Block Performance Specifications for Stratix V Devices (1), (2) (Part 2 of 2)

Memory	Mode	Resources Used		Performance							Unit
		ALUTs	Memory	C1	C2, C2L	C3	C4	I2, I2L	I3, I3L, I3YY	I4	
M20K Block	Single-port, all supported widths	0	1	700	700	650	550	700	500	450	MHz
	Simple dual-port, all supported widths	0	1	700	700	650	550	700	500	450	MHz
	Simple dual-port with the read-during-write option set to **Old Data**, all supported widths	0	1	525	525	455	400	525	455	400	MHz
	Simple dual-port with ECC enabled, 512 × 32	0	1	450	450	400	350	450	400	350	MHz
	Simple dual-port with ECC and optional pipeline registers enabled, 512 × 32	0	1	600	600	500	450	600	500	450	MHz
	True dual port, all supported widths	0	1	700	700	650	550	700	500	450	MHz
	ROM, all supported widths	0	1	700	700	650	550	700	500	450	MHz

Notes to Table 33:

(1) To achieve the maximum memory block performance, use a memory block clock that comes through global clock routing from an on-chip PLL set to **50%** output duty cycle. Use the Quartus II software to report timing for this and other memory block clocking schemes.

(2) When you use the error detection cyclical redundancy check (CRC) feature, there is no degradation in F_{MAX}.

(3) The F_{MAX} specification is only achievable with Fitter options, **MLAB Implementation In 16-Bit Deep Mode** enabled.

Temperature Sensing Diode Specifications

Table 34 lists the internal TSD specification.

Table 34. Internal Temperature Sensing Diode Specification

Temperature Range	Accuracy	Offset Calibrated Option	Sampling Rate	Conversion Time	Resolution	Minimum Resolution with no Missing Codes
–40°C to 100°C	±8°C	No	1 MHz, 500 KHz	< 100 ms	8 bits	8 bits

Table 35 lists the specifications for the Stratix V external temperature sensing diode.

Table 35. External Temperature Sensing Diode Specifications for Stratix V Devices

Description	Min	Typ	Max	Unit
I_{bias}, diode source current	8	—	200	μA
$V_{bias,}$ voltage across diode	0.3	—	0.9	V
Series resistance	—	—	< 1	Ω
Diode ideality factor	1.006	1.008	1.010	—

Table 36. High-Speed I/O Specifications for Stratix V Devices (1), (2) (Part 2 of 4)

Symbol	Conditions	C1			C2, C2L, I2, I2L			C3, I3, I3L, I3YY			C4,I4			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Transmitter														
True Differential I/O Standards - f_{HSDR} (data rate)	SERDES factor J = 3 to 10 (9), (11), (12), (13), (14), (15), (16)	(6)	—	1600	(6)	—	1434	(6)	—	1250	(6)	—	1050	Mbps
	SERDES factor J ≥ 4 LVDS TX with DPA (12), (14), (15), (16)	(6)	—	1600	(6)	—	1600	(6)	—	1600	(6)	—	1250	Mbps
	SERDES factor J = 2, uses DDR Registers	(6)	—	(7)	(6)	—	(7)	(6)	—	(7)	(6)	—	(7)	Mbps
	SERDES factor J = 1, uses SDR Register	(6)	—	(7)	(6)	—	(7)	(6)	—	(7)	(6)	—	(7)	Mbps
Emulated Differential I/O Standards with Three External Output Resistor Networks - f_{HSDR} (data rate) (10)	SERDES factor J = 4 to 10 (17)	(6)	—	1100	(6)	—	1100	(6)	—	840	(6)	—	840	Mbps
$t_{x\ Jitter}$ - True Differential I/O Standards	Total Jitter for Data Rate 600 Mbps - 1.25 Gbps	—	—	160	—	—	160	—	—	160	—	—	160	ps
	Total Jitter for Data Rate < 600 Mbps	—	—	0.1	—	—	0.1	—	—	0.1	—	—	0.1	UI
$t_{x\ Jitter}$ - Emulated Differential I/O Standards with Three External Output Resistor Network	Total Jitter for Data Rate 600 Mbps - 1.25 Gbps	—	—	300	—	—	300	—	—	300	—	—	325	ps
	Total Jitter for Data Rate < 600 Mbps	—	—	0.2	—	—	0.2	—	—	0.2	—	—	0.25	UI

Figure 7 shows the dynamic phase alignment (DPA) lock time specifications with the DPA PLL calibration option enabled.

Figure 7. DPA Lock Time Specification with DPA PLL Calibration Enabled

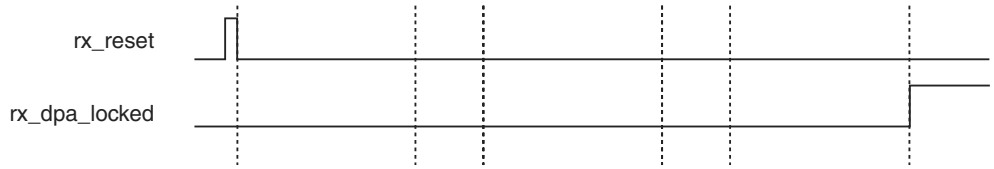


Table 37 lists the DPA lock time specifications for Stratix V devices.

Table 37. DPA Lock Time Specifications for Stratix V GX Devices Only *(1), (2), (3)*

Standard	Training Pattern	Number of Data Transitions in One Repetition of the Training Pattern	Number of Repetitions per 256 Data Transitions *(4)*	Maximum
SPI-4	00000000001111111111	2	128	640 data transitions
Parallel Rapid I/O	00001111	2	128	640 data transitions
	10010000	4	64	640 data transitions
Miscellaneous	10101010	8	32	640 data transitions
	01010101	8	32	640 data transitions

Notes to Table 37:

(1) The DPA lock time is for one channel.
(2) One data transition is defined as a 0-to-1 or 1-to-0 transition.
(3) The DPA lock time stated in this table applies to both commercial and industrial grade.
(4) This is the number of repetitions for the stated training pattern to achieve the 256 data transitions.

Figure 8 shows the **LVDS** soft-clock data recovery (CDR)/DPA sinusoidal jitter tolerance specification for a data rate ≥ 1.25 Gbps. Table 38 lists the **LVDS** soft-CDR/DPA sinusoidal jitter tolerance specification for a data rate ≥ 1.25 Gbps.

Figure 8. LVDS Soft-CDR/DPA Sinusoidal Jitter Tolerance Specification for a Data Rate ≥ 1.25 Gbps

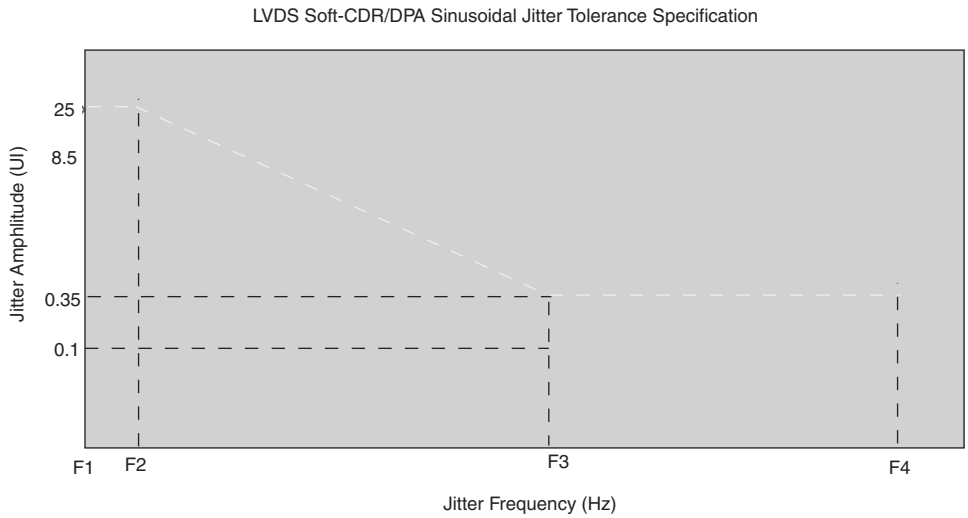


Table 46. JTAG Timing Parameters and Values for Stratix V Devices

Symbol	Description	Min	Max	Unit
t_{JPH}	JTAG port hold time	5	—	ns
t_{JPCO}	JTAG port clock to output	—	11 (1)	ns
t_{JPZX}	JTAG port high impedance to valid output	—	14 (1)	ns
t_{JPXZ}	JTAG port valid output to high impedance	—	14 (1)	ns

Notes to Table 46:

(1) A 1 ns adder is required for each V_{CCIO} voltage step down from 3.0 V. For example, t_{JPCO} = 12 ns if V_{CCIO} of the TDO I/O bank = 2.5 V, or 13 ns if it equals 1.8 V.

(2) The minimum TCK clock period is 167 ns if VCCBAT is within the range 1.2V-1.5V when you perform the volatile key programming.

Raw Binary File Size

For the POR delay specification, refer to the "POR Delay Specification" section of the "Configuration, Design Security, and Remote System Upgrades in Stratix V Devices".

Table 47 lists the uncompressed raw binary file (**.rbf**) sizes for Stratix V devices.

Table 47. Uncompressed .rbf Sizes for Stratix V Devices

Family	Device	Package	Configuration .rbf Size (bits)	IOCSR .rbf Size (bits) (4), (5)
Stratix V GX	5SGXA3	H35, F40, F35 (2)	213,798,880	562,392
		H29, F35 (3)	137,598,880	564,504
	5SGXA4	—	213,798,880	563,672
	5SGXA5	—	269,979,008	562,392
	5SGXA7	—	269,979,008	562,392
	5SGXA9	—	342,742,976	700,888
	5SGXAB	—	342,742,976	700,888
	5SGXB5	—	270,528,640	584,344
	5SGXB6	—	270,528,640	584,344
	5SGXB9	—	342,742,976	700,888
	5SGXBB	—	342,742,976	700,888
Stratix V GT	5SGTC5	—	269,979,008	562,392
	5SGTC7	—	269,979,008	562,392
Stratix V GS	5SGSD3	—	137,598,880	564,504
	5SGSD4	F1517	213,798,880	563,672
		—	137,598,880	564,504
	5SGSD5	—	213,798,880	563,672
	5SGSD6	—	293,441,888	565,528
	5SGSD8	—	293,441,888	565,528

Table 49. DCLK-to-DATA[] Ratio (1) (Part 2 of 2)

Configuration Scheme	Decompression	Design Security	DCLK-to-DATA[] Ratio
FPP ×32	Disabled	Disabled	1
	Disabled	Enabled	4
	Enabled	Disabled	8
	Enabled	Enabled	8

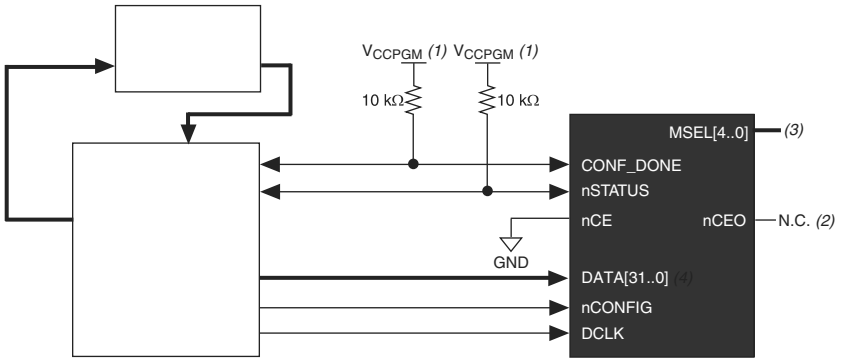
Note to Table 49:

(1) Depending on the DCLK-to-DATA[] ratio, the host must send a DCLK frequency that is r times the data rate in bytes per second (Bps), or words per second (Wps). For example, in FPP ×16 when the DCLK-to-DATA[] ratio is 2, the DCLK frequency must be 2 times the data rate in Wps. Stratix V devices use the additional clock cycles to decrypt and decompress the configuration data.

If the DCLK-to-DATA[] ratio is greater than 1, at the end of configuration, you can only stop the DCLK (DCLK-to-DATA[] ratio – 1) clock cycles after the last data is latched into the Stratix V device.

Figure 11 shows the configuration interface connections between the Stratix V device and a MAX II or MAX V device for single device configuration.

Figure 11. Single Device FPP Configuration Using an External Host



Notes to Figure 11:

(1) Connect the resistor to a supply that provides an acceptable input signal for the Stratix V device. V_{CCPGM} must be high enough to meet the V_{IH} specification of the I/O on the device and the external host. Altera recommends powering up all configuration system I/Os with V_{CCPGM}.

(2) You can leave the nCEO pin unconnected or use it as a user I/O pin when it does not feed another device's nCE pin.

(3) The MSEL pin settings vary for different data width, configuration voltage standards, and POR delay. To connect MSEL, refer to the MSEL Pin Settings section of the "Configuration, Design Security, and Remote System Upgrades in Stratix V Devices" chapter.

(4) If you use FPP ×8, use DATA[7..0]. If you use FPP ×16, use DATA[15..0].

Table 54 lists the PS configuration timing parameters for Stratix V devices.

Table 54. PS Timing Parameters for Stratix V Devices

Symbol	Parameter	Minimum	Maximum	Units
t_{CF2CD}	nCONFIG low to CONF_DONE low	—	600	ns
t_{CF2ST0}	nCONFIG low to nSTATUS low	—	600	ns
t_{CFG}	nCONFIG low pulse width	2	—	µs
t_{STATUS}	nSTATUS low pulse width	268	1,506 (1)	µs
t_{CF2ST1}	nCONFIG high to nSTATUS high	—	1,506 (2)	µs
t_{CF2CK} (5)	nCONFIG high to first rising edge on DCLK	1,506	—	µs
t_{ST2CK} (5)	nSTATUS high to first rising edge of DCLK	2	—	µs
t_{DSU}	DATA[] setup time before rising edge on DCLK	5.5	—	ns
t_{DH}	DATA[] hold time after rising edge on DCLK	0	—	ns
t_{CH}	DCLK high time	$0.45 \times 1/f_{MAX}$	—	s
t_{CL}	DCLK low time	$0.45 \times 1/f_{MAX}$	—	s
t_{CLK}	DCLK period	$1/f_{MAX}$	—	s
f_{MAX}	DCLK frequency	—	125	MHz
t_{CD2UM}	CONF_DONE high to user mode (3)	175	437	µs
t_{CD2CU}	CONF_DONE high to CLKUSR enabled	4 × maximum DCLK period	—	—
t_{CD2UMC}	CONF_DONE high to user mode with CLKUSR option on	t_{CD2CU} + (8576 × CLKUSR period) (4)	—	—

Notes to Table 54:

(1) This value is applicable if you do not delay configuration by extending the nCONFIG or nSTATUS low pulse width.

(2) This value is applicable if you do not delay configuration by externally holding the nSTATUS low.

(3) The minimum and maximum numbers apply only if you choose the internal oscillator as the clock source for initializing the device.

(4) To enable the CLKUSR pin as the initialization clock source and to obtain the maximum frequency specification on these pins, refer to the "Initialization" section.

(5) If nSTATUS is monitored, follow the t_{ST2CK} specification. If nSTATUS is not monitored, follow the t_{CF2CK} specification.

Initialization

Table 55 lists the initialization clock source option, the applicable configuration schemes, and the maximum frequency.

Table 55. Initialization Clock Source Option and the Maximum Frequency

Initialization Clock Source	Configuration Schemes	Maximum Frequency	Minimum Number of Clock Cycles (1)
Internal Oscillator	AS, PS, FPP	12.5 MHz	8576
CLKUSR	AS, PS, FPP (2)	125 MHz	
DCLK	PS, FPP	125 MHz	

Notes to Table 55:

(1) The minimum number of clock cycles required for device initialization.

(2) To enable CLKUSR as the initialization clock source, turn on the **Enable user-supplied start-up clock (CLKUSR)** option in the Quartus II software from the **General** panel of the **Device and Pin Options** dialog box.

Table 58. IOE Programmable Delay for Stratix V Devices (Part 2 of 2)

Parameter (1)	Available Settings	Min Offset (2)	Fast Model		Slow Model							
			Industrial	Commercial	C1	C2	C3	C4	I2	I3, I3YY	I4	Unit
D3	8	0	1.587	1.699	2.793	2.793	2.992	3.192	2.811	3.047	3.257	ns
D4	64	0	0.464	0.492	0.838	0.838	0.924	1.011	0.843	0.920	1.006	ns
D5	64	0	0.464	0.493	0.838	0.838	0.924	1.011	0.844	0.921	1.006	ns
D6	32	0	0.229	0.244	0.415	0.415	0.458	0.503	0.418	0.456	0.499	ns

Notes to Table 58:

(1) You can set this value in the Quartus II software by selecting **D1**, **D2**, **D3**, **D5**, and **D6** in the **Assignment Name** column of **Assignment Editor**.

(2) Minimum offset does not include the intrinsic delay.

Programmable Output Buffer Delay

Table 59 lists the delay chain settings that control the rising and falling edge delays of the output buffer. The default delay is 0 ps.

Table 59. Programmable Output Buffer Delay for Stratix V Devices (1)

Symbol	Parameter	Typical	Unit
D_{OUTBUF}	Rising and/or falling edge delay	0 (default)	ps
		25	ps
		50	ps
		75	ps

Note to Table 59:

(1) You can set the programmable output buffer delay in the Quartus II software by setting the **Output Buffer Delay Control** assignment to either positive, negative, or both edges, with the specific values stated here (in ps) for the **Output Buffer Delay** assignment.

Glossary

Table 60 lists the glossary for this chapter.

Table 60. Glossary (Part 1 of 4)

Letter	Subject	Definitions
A B C	—	—
D	—	—
E	—	—
F	f_{HSCLK}	Left and right PLL input clock frequency.
	f_{HSDR}	High-speed I/O block—Maximum and minimum **LVDS** data transfer rate (f_{HSDR} = 1/TUI), non-DPA.
	$f_{HSDRDPA}$	High-speed I/O block—Maximum and minimum **LVDS** data transfer rate ($f_{HSDRDPA}$ = 1/TUI), DPA.

Table 60. Glossary (Part 4 of 4)

Letter	Subject	Definitions
V	$V_{CM(DC)}$	DC common mode input voltage.
	V_{ICM}	Input common mode voltage—The common mode of the differential signal at the receiver.
	V_{ID}	Input differential voltage swing—The difference in voltage between the positive and complementary conductors of a differential transmission at the receiver.
	$V_{DIF(AC)}$	AC differential input voltage—Minimum AC input differential voltage required for switching.
	$V_{DIF(DC)}$	DC differential input voltage— Minimum DC input differential voltage required for switching.
	V_{IH}	Voltage input high—The minimum positive voltage applied to the input which is accepted by the device as a logic high.
	$V_{IH(AC)}$	High-level AC input voltage
	$V_{IH(DC)}$	High-level DC input voltage
	V_{IL}	Voltage input low—The maximum positive voltage applied to the input which is accepted by the device as a logic low.
	$V_{IL(AC)}$	Low-level AC input voltage
	$V_{IL(DC)}$	Low-level DC input voltage
	V_{OCM}	Output common mode voltage—The common mode of the differential signal at the transmitter.
	V_{OD}	Output differential voltage swing—The difference in voltage between the positive and complementary conductors of a differential transmission at the transmitter.
	V_{SWING}	Differential input voltage
	V_X	Input differential cross point voltage
	V_{OX}	Output differential cross point voltage
W	W	High-speed I/O block—clock boost factor
X Y Z	—	—

Table 61. Document Revision History (Part 2 of 3)

Date	Version	Changes
November 2014	3.3	■ Added the I3YY speed grade and changed the data rates for the GX channel in Table 1. ■ Added the I3YY speed grade to the V_{CC} description in Table 6. ■ Added the I3YY speed grade to V_{CCHIP_L}, V_{CCHIP_R}, V_{CCHSSI_L}, and V_{CCHSSI_R} descriptions in Table 7. ■ Added 240-Ω to Table 11. ■ Changed CDR PPM tolerance in Table 23. ■ Added additional max data rate for fPLL in Table 23. ■ Added the I3YY speed grade and changed the data rates for transceiver speed grade 3 in Table 25. ■ Added the I3YY speed grade and changed the data rates for transceiver speed grade 3 in Table 26. ■ Changed CDR PPM tolerance in Table 28. ■ Added additional max data rate for fPLL in Table 28. ■ Changed the mode descriptions for MLAB and M20K in Table 33. ■ Changed the Max value of f_{HSCLK_OUT} for the C2, C2L, I2, I2L speed grades in Table 36. ■ Changed the frequency ranges for C1 and C2 in Table 39. ■ Changed the **.rbf** file sizes for 5SGSD6 and 5SGSD8 in Table 47. ■ Added note about `nSTATUS` to Table 50, Table 51, Table 54. ■ Changed the available settings in Table 58. ■ Changed the note in “Periphery Performance”. ■ Updated the “I/O Standard Specifications” section. ■ Updated the “Raw Binary File Size” section. ■ Updated the receiver voltage input range in Table 22. ■ Updated the max frequency for the LVDS clock network in Table 36. ■ Updated the `DCLK` note to Figure 11. ■ Updated Table 23 VO_{CM} (DC Coupled) condition. ■ Updated Table 6 and Table 7. ■ Added the `DCLK` specification to Table 55. ■ Updated the notes for Table 47. ■ Updated the list of parameters for Table 56.
November 2013	3.2	■ Updated Table 28
November 2013	3.1	■ Updated Table 33
November 2013	3.0	■ Updated Table 23 and Table 28
October 2013	2.9	■ Updated the “Transceiver Characterization” section
October 2013	2.8	■ Updated Table 3, Table 12, Table 14, Table 19, Table 20, Table 23, Table 24, Table 28, Table 30, Table 31, Table 32, Table 33, Table 36, Table 39, Table 40, Table 41, Table 42, Table 47, Table 53, Table 58, and Table 59 ■ Added Figure 1 and Figure 3 ■ Added the “Transceiver Characterization” section ■ Removed all “Preliminary” designations.