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Intel - 5SGXMA3K3F35C2N Datasheet



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Understanding <u>Embedded - FPGAs (Field</u> <u>Programmable Gate Array)</u>

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Detuns	
Product Status	Obsolete
Number of LABs/CLBs	128300
Number of Logic Elements/Cells	340000
Total RAM Bits	19456000
Number of I/O	600
Number of Gates	-
Voltage - Supply	0.87V ~ 0.93V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	1152-BBGA, FCBGA
Supplier Device Package	1152-FBGA (35x35)
Purchase URL	https://www.e-xfl.com/product-detail/intel/5sgxma3k3f35c2n

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Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

Table 8 shows the transceiver power supply voltage requirements for various conditions.

Table 8. Transceiver Power Supply Voltage Requirements

Conditions	Core Speed Grade	VCCR_GXB & VCCT_GXB ⁽²⁾	VCCA_GXB	VCCH_GXB	Unit
If BOTH of the following conditions are true:	All	1.05			
 Data rate > 10.3 Gbps. DFE is used. 	All	1.05			
If ANY of the following conditions are true ⁽¹⁾ :			3.0		
ATX PLL is used.					
■ Data rate > 6.5Gbps.	All	1.0			
■ DFE (data rate ≤ 10.3 Gbps), AEQ, or EyeQ feature is used.				1.5	V
If ALL of the following	C1, C2, I2, and I3YY	0.90	2.5		
conditions are true:ATX PLL is not used.					
■ Data rate ≤ 6.5Gbps.	C2L, C3, C4, I2L, I3, I3L, and I4	0.85	2.5		
 DFE, AEQ, and EyeQ are not used. 					

Notes to Table 8:

(1) Choose this power supply voltage requirement option if you plan to upgrade your design later with any of the listed conditions.

(2) If the VCCR_GXB and VCCT_GXB supplies are set to 1.0 V or 1.05 V, they cannot be shared with the VCC core supply. If the VCCR_GXB and VCCT_GXB are set to either 0.90 V or 0.85 V, they can be shared with the VCC core supply.

DC Characteristics

This section lists the supply current, I/O pin leakage current, input pin capacitance, on-chip termination tolerance, and hot socketing specifications.

Supply Current

Supply current is the current drawn from the respective power rails used for power budgeting. Use the Excel-based Early Power Estimator (EPE) to get supply current estimates for your design because these currents vary greatly with the resources you use.

For more information about power estimation tools, refer to the *PowerPlay Early Power Estimator User Guide* and the *PowerPlay Power Analysis* chapter in the *Quartus II Handbook*.

Symbol	Description	V _{CCIO} (V)	Typical	Unit
		3.0	0.189	
		2.5	0.208	
dR/dT	OCT variation with temperature without recalibration	1.8	0.266	%/°C
	without robalibration	1.5	0.273	
		1.2	0.317	

Table 13. OCT Variation after Power-Up Calibration for Stratix V Devices (Part 2 of 2)⁽¹⁾

Note to Table 13:

(1) Valid for a V_{CCIO} range of $\pm 5\%$ and a temperature range of 0° to 85°C.

Pin Capacitance

Table 14 lists the Stratix V device family pin capacitance.

Table 14. Pin Capacitance for Stratix V Devices

Symbol	Description	Value	Unit
C _{IOTB}	Input capacitance on the top and bottom I/O pins	6	pF
C _{IOLR}	Input capacitance on the left and right I/O pins	6	рF
C _{OUTFB}	Input capacitance on dual-purpose clock output and feedback pins	6	рF

Hot Socketing

Table 15 lists the hot socketing specifications for Stratix V devices.

Table 15.	Hot Socketing Specifications for Stratix V Devices
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Symbol	Description	Maximum
I _{IOPIN (DC)}	DC current per I/O pin	300 μA
I _{IOPIN (AC)}	AC current per I/O pin	8 mA ⁽¹⁾
I _{XCVR-TX (DC)}	DC current per transceiver transmitter pin	100 mA
I _{XCVR-RX (DC)}	DC current per transceiver receiver pin	50 mA

Note to Table 15:

(1) The I/O ramp rate is 10 ns or more. For ramp rates faster than 10 ns, $|I_{10PIN}| = C dv/dt$, in which C is the I/O pin capacitance and dv/dt is the slew rate.

Symbol/	Conditions	Trai	nsceive Grade	r Speed 1	Trai	nsceive Grade	r Speed 2	Transceiver Speed Grade 3			Unit
Description		Min	Тур	Max	Min	Тур	Max	Min	Тур	Max	
Reconfiguration clock (mgmt_clk_clk) frequency	_	100	_	125	100		125	100		125	MHz
Receiver											
Supported I/O Standards	_			1.4-V PCM	L, 1.5-V	PCML,	2.5-V PCM	L, LVPE	CL, and	d LVDS	
Data rate (Standard PCS) (9), (23)	_	600	_	12200	600	_	12200	600	_	8500/ 10312.5 (24)	Mbps
Data rate (10G PCS) ^{(9),} ⁽²³⁾		600	_	14100	600	_	12500	600	_	8500/ 10312.5 (24)	Mbps
Absolute V_{MAX} for a receiver pin (5)		_	_	1.2	—	_	1.2	—	_	1.2	V
Absolute V _{MIN} for a receiver pin	_	-0.4	_		-0.4	_	_	-0.4	_	_	V
Maximum peak- to-peak differential input voltage V _{ID} (diff p- p) before device configuration ⁽²²⁾	_	_	_	1.6	_	_	1.6	_	_	1.6	V
Maximum peak- to-peak	V _{CCR_GXB} = 1.0 V/1.05 V (V _{ICM} = 0.70 V)	_	_	2.0	_	_	2.0	_	_	2.0	V
differential input voltage V_{ID} (diff p- p) after device configuration ⁽¹⁸⁾ ,	$V_{CCR_GXB} = 0.90 V$ (V _{ICM} = 0.6 V)	_	_	2.4	_	_	2.4	_	_	2.4	V
(22)	$V_{CCR_GXB} = 0.85 V$ (V _{ICM} = 0.6 V)			2.4			2.4			2.4	V
Minimum differential eye opening at receiver serial input pins ^{(6), (22),} (27)	_	85		_	85		_	85	_	_	mV

Table 23. Transceiver Specifications for Stratix V GX and GS Devices ⁽¹⁾ (Part 3 of 7)

Symbol/ Description	Conditions	Tra	nsceive Grade	r Speed 1	Tra	nsceive Grade	r Speed 2	Trai	nsceive Grade	r Speed 3	Unit
Description		Min	Тур	Max	Min	Тур	Max	Min	Тур	Max	
	85– Ω setting		85 ± 30%		—	85 ± 30%			85 ± 30%		Ω
Differential on-	100–Ω setting	_	100 ± 30%		_	100 ± 30%		_	100 ± 30%		Ω
chip termination resistors ⁽²¹⁾	120–Ω setting	_	120 ± 30%		_	120 ± 30%		_	120 ± 30%		Ω
	150-Ω setting	_	150 ± 30%	_	_	150 ± 30%		_	150 ± 30%		Ω
V _{ICM} (AC and DC	V _{CCR_GXB} = 0.85 V or 0.9 V full bandwidth		600		_	600	_		600		mV
	V _{CCR_GXB} = 0.85 V or 0.9 V half bandwidth	_	600	_	_	600	_	_	600	_	mV
coupled)	V _{CCR_GXB} = 1.0 V/1.05 V full bandwidth	_	700		_	700			700		mV
	V _{CCR_GXB} = 1.0 V half bandwidth	_	750	_	_	750	_	_	750	_	mV
t _{LTR} ⁽¹¹⁾	_	—	—	10	—	—	10	—	—	10	μs
t _{LTD} (12)	_	4			4			4			μs
t _{LTD_manual} ⁽¹³⁾		4			4			4	_		μs
t _{LTR_LTD_manual} ⁽¹⁴⁾		15			15	—		15	—		μs
Run Length	_	_		200		—	200		—	200	UI
Programmable equalization (AC Gain) ⁽¹⁰⁾	Full bandwidth (6.25 GHz) Half bandwidth (3.125 GHz)			16	_		16	_		16	dB

 Table 23. Transceiver Specifications for Stratix V GX and GS Devices ⁽¹⁾ (Part 4 of 7)

Symbol/	Conditions	Tra	nsceive Grade	r Speed 1	Transceiver Speed Grade 2			Trar	isceive Grade	r Speed 3	Unit
Description		Min	Тур	Max	Min	Тур	Max	Min	Тур	Max	
	DC Gain Setting = 0		0	_	_	0		_	0	—	dB
	DC Gain Setting = 1	_	2	_	—	2	_	_	2	_	dB
Programmable DC gain	DC Gain Setting = 2	_	4	_	_	4	_	_	4	_	dB
	DC Gain Setting = 3	_	6	_	_	6	_	_	6	_	dB
	DC Gain Setting = 4	_	8	_	_	8	_	_	8	—	dB
Transmitter											
Supported I/O Standards	_				-	I.4-V ar	nd 1.5-V PC	ML			
Data rate (Standard PCS)	_	600	_	12200	600	_	12200	600	_	8500/ 10312.5 (24)	Mbps
Data rate (10G PCS)	_	600	_	14100	600		12500	600		8500/ 10312.5 (24)	Mbps
	85-Ω setting		85 ± 20%	_	_	85 ± 20%		_	85 ± 20%	_	Ω
Differential on-	100-Ω setting	_	100 ± 20%	_	_	100 ± 20%	_	_	100 ± 20%	_	Ω
chip termination resistors	120-Ω setting	_	120 ± 20%			120 ± 20%		_	120 ± 20%		Ω
	150-Ω setting		150 ± 20%			150 ± 20%			150 ± 20%		Ω
V _{OCM} (AC coupled)	0.65-V setting		650		_	650		_	650	_	mV
V _{OCM} (DC coupled)	_		650		_	650		_	650	_	mV
Rise time (7)	20% to 80%	30		160	30		160	30		160	ps
Fall time ⁽⁷⁾	80% to 20%	30		160	30		160	30		160	ps
Intra-differential pair skew	Tx V _{CM} = 0.5 V and slew rate of 15 ps			15			15			15	ps
Intra-transceiver block transmitter channel-to- channel skew	x6 PMA bonded mode			120			120			120	ps

Table 23. Transceiver Specifications for Stratix V GX and GS Devices ⁽¹⁾ (Part 5 of 7)

Table 23. Transceiver Specifications for Stratix V GX and GS Devices ⁽¹⁾ (Part 6 of 7)

Symbol/	Conditions	Trai	isceive Grade	r Speed 1	Trar	isceive Grade	r Speed 2	Transceiver Speed Grade 3			Unit
Description		Min	Тур	Max	Min	Тур	Max	Min	Тур	Max	
Inter-transceiver block transmitter channel-to- channel skew	xN PMA bonded mode			500	_		500	_		500	ps
CMU PLL											
Supported Data Range	_	600		12500	600	_	12500	600	_	8500/ 10312.5 (24)	Mbps
t _{pll_powerdown} ⁽¹⁵⁾	_	1		—	1	—	—	1	—	—	μs
t _{pll_lock} (16)	_		_	10	—	_	10	—	—	10	μs
ATX PLL	1										
	VCO post-divider L=2	8000		14100	8000	_	12500	8000	_	8500/ 10312.5 (24)	Mbps
Current and Date	L=4	4000	_	7050	4000	_	6600	4000	—	6600	Mbps
Supported Data Rate Range	L=8	2000	_	3525	2000	_	3300	2000	_	3300	Mbps
	L=8, Local/Central Clock Divider =2	1000	_	1762.5	1000		1762.5	1000		1762.5	Mbps
t _{pll_powerdown} (15)	_	1		_	1			1	—	_	μs
t _{pll_lock} ⁽¹⁶⁾	—			10	—	—	10	—	—	10	μs
fPLL	•			•					•		
Supported Data Range	_	600	_	3250/ 3125 ⁽²⁵⁾	600	_	3250/ 3125 ⁽²⁵⁾	600	_	3250/ 3125 ⁽²⁵⁾	Mbps
t _{pll_powerdown} ⁽¹⁵⁾	_	1	_	_	1	_	—	1	—	—	μs

Table 24 shows the maximum transmitter data rate for the clock network.

Table 24. Clock Network Maximum Data Rate Transmitter Specifications (1)

		ATX PLL			CMU PLL ⁽²⁾)		fPLL	
Clock Network	Non- bonded Mode (Gbps)	Bonded Mode (Gbps)	Channel Span	Non- bonded Mode (Gbps)	Bonded Mode (Gbps)	Channel Span	Non- bonded Mode (Gbps)	Bonded Mode (Gbps)	Channel Span
x1 ⁽³⁾	14.1	—	6	12.5	_	6	3.125	_	3
x6 ⁽³⁾	_	14.1	6	_	12.5	6	_	3.125	6
x6 PLL Feedback ⁽⁴⁾	_	14.1	Side- wide	_	12.5	Side- wide		_	_
xN (PCIe)	_	8.0	8	_	5.0	8	_	_	_
VN (Native DHV ID)	8.0	8.0	Up to 13 channels above and below PLL	7.99	7.99	Up to 13 channels above	3.125	3.125	Up to 13 channels above
xN (Native PHY IP)	_	8.01 to 9.8304	Up to 7 channels above and below PLL	7.55	7.55	and below PLL	3.120	0.120	and below PLL

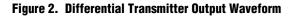
Notes to Table 24:

(1) Valid data rates below the maximum specified in this table depend on the reference clock frequency and the PLL counter settings. Check the MegaWizard message during the PHY IP instantiation.

(2) ATX PLL is recommended at 8 Gbps and above data rates for improved jitter performance.

(3) Channel span is within a transceiver bank.

(4) Side-wide channel bonding is allowed up to the maximum supported by the PHY IP.



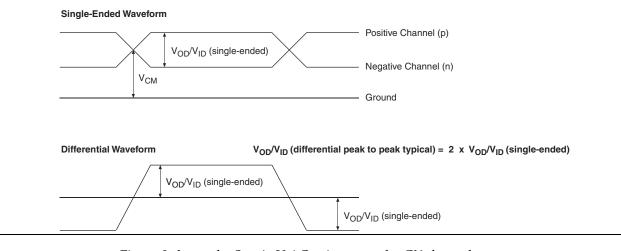


Figure 3 shows the Stratix V AC gain curves for GX channels.

Figure 3. AC Gain Curves for GX Channels (full bandwidth)

Stratix V GT devices contain both GX and GT channels. All transceiver specifications for the GX channels not listed in Table 28 are the same as those listed in Table 23.

Table 28 lists the Stratix V GT transceiver specifications.

Symbol/ Description	Conditions	:	Transceive Speed Grade			Transceive peed Grade		Unit				
Description		Min	Тур	Max	Min	Тур	Max					
Reference Clock												
Supported I/O Standards	Dedicated reference clock pin	1.2-V PCN	1.2-V PCML, 1.4-V PCML, 1.5-V PCML, 2.5-V PCML, Differential LVPECL, LVDS and HCSL									
	RX reference clock pin	1.4-V PCML, 1.5-V PCML, 2.5-V PCML, LVPECL, and LVDS										
Input Reference Clock Frequency (CMU PLL) ⁽⁶⁾	_	40	_	710	40	_	710	MHz				
Input Reference Clock Frequency (ATX PLL) ⁽⁶⁾	_	100	-	710	100	_	710	MHz				
Rise time	20% to 80%		_	400		—	400					
Fall time	80% to 20%			400	—		400	ps				
Duty cycle	—	45		55	45		55	%				
Spread-spectrum modulating clock frequency	PCI Express (PCIe)	30	_	33	30	_	33	kHz				
Spread-spectrum downspread	PCle	_	0 to -0.5		_	0 to -0.5	_	%				
On-chip termination resistors ⁽¹⁹⁾	_	_	100	_	_	100	_	Ω				
Absolute V _{MAX} ⁽³⁾	Dedicated reference clock pin		_	1.6	_	_	1.6	V				
	RX reference clock pin	_	_	1.2	_	_	1.2					
Absolute V _{MIN}	—	-0.4	—	—	-0.4	—	—	V				
Peak-to-peak differential input voltage	_	200	_	1600	200	_	1600	mV				
V _{ICM} (AC coupled)	Dedicated reference clock pin		1050/1000 (2)		1050/1000 (2)	mV				
	RX reference clock pin	1	.0/0.9/0.85 (22)	1	1.0/0.9/0.85 (22)						
V _{ICM} (DC coupled)	HCSL I/O standard for PCIe reference clock	250	_	550	250	_	550	mV				

Table 28. Transceiver Specifications for Stratix V GT Devices (Part 1 of 5) ⁽¹⁾

Symbol	Parameter	Min	Тур	Max	Unit
+ (3) (4)	Input clock cycle-to-cycle jitter ($f_{REF} \ge 100 \text{ MHz}$)	_	—	0.15	UI (p-p)
t _{INCCJ} ^{(3),} ⁽⁴⁾	Input clock cycle-to-cycle jitter (f _{REF} < 100 MHz)	-750	_	+750	ps (p-p)
t	Period Jitter for dedicated clock output (f_{OUT} \geq 100 MHz)	_	_	175 ⁽¹⁾	ps (p-p)
t _{outpj_dc} ⁽⁵⁾	Period Jitter for dedicated clock output (f _{OUT} < 100 MHz)	_		17.5 ⁽¹⁾	mUI (p-p)
+ (5)	Period Jitter for dedicated clock output in fractional PLL ($f_{0UT} \geq 100 \mbox{ MHz})$	_	_	250 ⁽¹¹⁾ , 175 ⁽¹²⁾	ps (p-p)
t _{foutpj_dc} ⁽⁵⁾	Period Jitter for dedicated clock output in fractional PLL (f _{OUT} < 100 MHz)	_	_	25 ⁽¹¹⁾ , 17.5 ⁽¹²⁾	mUI (p-p)
+	Cycle-to-Cycle Jitter for a dedicated clock output ($f_{OUT} \ge 100 \text{ MHz}$)	_	_	175	ps (p-p)
t _{outccj_dc} ⁽⁵⁾	Cycle-to-Cycle Jitter for a dedicated clock output (f _{0UT} < 100 MHz)	_	_	17.5	mUI (p-p)
+ <i>(5)</i>	Cycle-to-cycle Jitter for a dedicated clock output in fractional PLL (f_{OUT} \geq 100 MHz)	_	_	250 ⁽¹¹⁾ , 175 ⁽¹²⁾	ps (p-p)
t _{FOUTCCJ_DC} ⁽⁵⁾	Cycle-to-cycle Jitter for a dedicated clock output in fractional PLL ($f_{OUT} < 100 \text{ MHz}$)+	_	_	25 ⁽¹¹⁾ , 17.5 ⁽¹²⁾	mUI (p-p)
t _{outpj_io} (5),	Period Jitter for a clock output on a regular I/O in integer PLL (f_{OUT} \geq 100 MHz)	_	_	600	ps (p-p)
(8)	Period Jitter for a clock output on a regular I/O (f _{OUT} < 100 MHz)	_	_	60	mUI (p-p)
t _{FOUTPJ_IO} (5),	Period Jitter for a clock output on a regular I/O in fractional PLL ($f_{OUT} \ge 100 \text{ MHz}$)	_	_	600 (10)	ps (p-p)
(8), (11)	Period Jitter for a clock output on a regular I/O in fractional PLL (f _{OUT} < 100 MHz)	_	_	60 ⁽¹⁰⁾	mUI (p-p)
t _{outccj_io} (5),	Cycle-to-cycle Jitter for a clock output on a regular I/O in integer PLL (f_{OUT} \geq 100 MHz)	_	_	600	ps (p-p)
(8)	Cycle-to-cycle Jitter for a clock output on a regular I/O in integer PLL (f_{OUT} < 100 MHz)	_	_	60 ⁽¹⁰⁾	mUI (p-p)
t _{foutccj_10} ^{(5),}	Cycle-to-cycle Jitter for a clock output on a regular I/O in fractional PLL ($f_{0UT} \geq 100 \mbox{ MHz})$	_	_	600 ⁽¹⁰⁾	ps (p-p)
(8), (11)	Cycle-to-cycle Jitter for a clock output on a regular I/O in fractional PLL ($f_{OUT} < 100 \text{ MHz}$)	_	_	60	mUI (p-p)
t _{casc_outpj_dc}	Period Jitter for a dedicated clock output in cascaded PLLs (f_{0UT} \geq 100 MHz)		_	175	ps (p-p)
(5), (6)	Period Jitter for a dedicated clock output in cascaded PLLs (f _{OUT} < 100 MHz)		_	17.5	mUI (p-p)
f _{DRIFT}	Frequency drift after PFDENA is disabled for a duration of 100 μs	_	_	±10	%
dK _{BIT}	Bit number of Delta Sigma Modulator (DSM)	8	24	32	Bits
k _{value}	Numerator of Fraction	128	8388608	2147483648	

Table 31. PLL Specifications for Stratix V Devices (Part 2 of 3)

Table 31. PLL Specifications for Stratix V Devices (Part 3 of 3)

Symbol	Parameter		Тур	Max	Unit
f _{RES}	Resolution of VCO frequency ($f_{INPFD} = 100 \text{ MHz}$)	390625	5.96	0.023	Hz

Notes to Table 31:

(1) This specification is limited in the Quartus II software by the I/O maximum frequency. The maximum I/O frequency is different for each I/O standard.

(2) This specification is limited by the lower of the two: I/O f_{MAX} or f_{OUT} of the PLL.

- (3) A high input jitter directly affects the PLL output jitter. To have low PLL output clock jitter, you must provide a clean clock source < 120 ps.
- (4) f_{REF} is fIN/N when N = 1.
- (5) Peak-to-peak jitter with a probability level of 10⁻¹² (14 sigma, 99.9999999974404% confidence level). The output jitter specification applies to the intrinsic jitter of the PLL, when an input jitter of 30 ps is applied. The external memory interface clock output jitter specifications use a different measurement method and are available in Table 44 on page 52.
- (6) The cascaded PLL specification is only applicable with the following condition: a. Upstream PLL: 0.59Mhz ≤ Upstream PLL BW < 1 MHz b. Downstream PLL: Downstream PLL BW > 2 MHz
- (7) High bandwidth PLL settings are not supported in external feedback mode.
- (8) The external memory interface clock output jitter specifications use a different measurement method, which is available in Table 42 on page 50.
- (9) The VCO frequency reported by the Quartus II software in the PLL Usage Summary section of the compilation report takes into consideration the VCO post-scale counter K value. Therefore, if the counter K has a value of 2, the frequency reported can be lower than the f_{VCO} specification.
- (10) This specification only covers fractional PLL for low bandwidth. The f_{VCO} for fractional value range 0.05 0.95 must be \geq 1000 MHz, while f_{VCO} for fractional value range 0.20 0.80 must be \geq 1200 MHz.
- (11) This specification only covered fractional PLL for low bandwidth. The f_{VC0} for fractional value range 0.05-0.95 must be \geq 1000 MHz.
- (12) This specification only covered fractional PLL for low bandwidth. The f_{VC0} for fractional value range 0.20-0.80 must be \geq 1200 MHz.

DSP Block Specifications

Table 32 lists the Stratix V DSP block performance specifications.

			I	Peforman	ce					
Mode	C1	C2, C2L	12, 12L	C3	13, 13L, 13YY	C4	14	Unit		
Modes using one DSP										
Three 9 x 9	600	600	600	480	480	420	420	MHz		
One 18 x 18	600	600	600	480	480	420	400	MHz		
Two partial 18 x 18 (or 16 x 16)	600	600	600	480	480	420	400	MHz		
One 27 x 27	500	500	500	400	400	350	350	MHz		
One 36 x 18	500	500	500	400	400	350	350	MHz		
One sum of two 18 x 18(One sum of 2 16 x 16)	500	500	500	400	400	350	350	MHz		
One sum of square	500	500	500	400	400	350	350	MHz		
One 18 x 18 plus 36 (a x b) + c	500	500	500	400	400	350	350	MHz		
		Modes u	sing two l	DSPs	1		•	1		
Three 18 x 18	500	500	500	400	400	350	350	MHz		
One sum of four 18 x 18	475	475	475	380	380	300	300	MHz		
One sum of two 27 x 27	465	465	450	380	380	300	290	MHz		
One sum of two 36 x 18	475	475	475	380	380	300	300	MHz		
One complex 18 x 18	500	500	500	400	400	350	350	MHz		
One 36 x 36	475	475	475	380	380	300	300	MHz		

Table 32. Block Performance Specifications for Stratix V DSP Devices (Part 1 of 2)

Mode	Peformance							
	C1	C2, C2L	12, 12L	C3	13, 13L, 13YY	C4	14	Unit
		Modes us	ing Three	DSPs				
One complex 18 x 25	425	425	415	340	340	275	265	MHz
Modes using Four DSPs								
One complex 27 x 27	465	465	465	380	380	300	290	MHz

Table 32. Block Performance Specifications for Stratix V DSP Devices (Part 2 of 2)

Memory Block Specifications

Table 33 lists the Stratix V memory block specifications.

Table 33. Memory Block Performance Specifications for Stratix V Devices ^{(1), (2)} (Part 1 of 2)

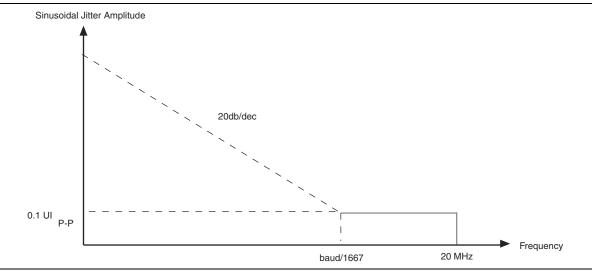
		Resources Used		Performance							
Memory	Mode	ALUTS	Memory	C1	C2, C2L	C3	C4	12, 12L	13, 13L, 13YY	14	Unit
	Single port, all supported widths	0	1	450	450	400	315	450	400	315	MHz
MLAB	Simple dual-port, x32/x64 depth	0	1	450	450	400	315	450	400	315	MHz
IVILAD	Simple dual-port, x16 depth ⁽³⁾	0	1	675	675	533	400	675	533	400	MHz
	ROM, all supported widths	0	1	600	600	500	450	600	500	450	MHz

Jitter Fre	Sinusoidal Jitter (UI)	
F1	10,000	25.000
F2	17,565	25.000
F3	1,493,000	0.350
F4	50,000,000	0.350

Table 38.	LVDS Soft-CDR/D	PA Sinusoidal	Jitter Mask Valu	es for a Data Ra	te > 1.25 Gbps
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Figure 9 shows the **LVDS** soft-CDR/DPA sinusoidal jitter tolerance specification for a data rate < 1.25 Gbps.





DLL Range, DQS Logic Block, and Memory Output Clock Jitter Specifications

Table 39 lists the DLL range specification for Stratix V devices. The DLL is always in 8-tap mode in Stratix V devices.

Table 39. DLL Range Specifications for Stratix V Devices (1)

C1	C2, C2L, I2, I2L	C3, I3, I3L, I3YY	C4,I4	Unit
300-933	300-933	300-890	300-890	MHz

Note to Table 39:

(1) Stratix V devices support memory interface frequencies lower than 300 MHz, although the reference clock that feeds the DLL must be at least 300 MHz. To support interfaces below 300 MHz, multiply the reference clock feeding the DLL to ensure the frequency is within the supported range of the DLL.

Table 40 lists the DQS phase offset delay per stage for Stratix V devices.

Table 40. DQS Phase Offset Delay Per Setting for Stratix V Devices ^{(1), (2)} (Part 1 of 2)

Speed Grade	Min	Max	Unit
C1	8	14	ps
C2, C2L, I2, I2L	8	14	ps
C3,I3, I3L, I3YY	8	15	ps

Speed Grade	Min	Max	Unit
C4,I4	8	16	ps

Table 40. DQS Phase Offset Delay Per Setting for Stratix V Devices ^{(1), (2)} (Part 2 of 2)

Notes to Table 40:

(1) The typical value equals the average of the minimum and maximum values.

(2) The delay settings are linear with a cumulative delay variation of 40 ps for all speed grades. For example, when using a -2 speed grade and applying a 10-phase offset setting to a 90° phase shift at 400 MHz, the expected average cumulative delay is [625 ps + (10 × 10 ps) ± 20 ps] = 725 ps ± 20 ps.

Table 41 lists the DQS phase shift error for Stratix V devices.

Table 41. DQS Phase Shift Error Specification for DLL-Delayed Clock (t_{DQS_PSERR}) for Stratix V Devices ⁽¹⁾

Number of DQS Delay Buffers	C1	C2, C2L, I2, I2L	C3, I3, I3L, I3YY	C4,14	Unit
1	28	28	30	32	ps
2	56	56	60	64	ps
3	84	84	90	96	ps
4	112	112	120	128	ps

Notes to Table 41:

(1) This error specification is the absolute maximum and minimum error. For example, skew on three DQS delay buffers in a -2 speed grade is ± 78 ps or ± 39 ps.

Table 42 lists the memory output clock jitter specifications for Stratix V devices.

Clock Network	Parameter	Symbol	C	1	C2, C2L	, 12, 12L	C3, I3 I3		C4	,14	Unit
NELWUIK		-	Min	Max	Min	Max	Min	Max	Min	Max	
	Clock period jitter	t _{JIT(per)}	-50	50	-50	50	-55	55	-55	55	ps
Regional	Cycle-to-cycle period jitter	$t_{\rm JIT(cc)}$	-100	100	-100	100	-110	110	-110	110	ps
	Duty cycle jitter	$t_{JIT(duty)}$	-50	50	-50	50	-82.5	82.5	-82.5	82.5	ps
	Clock period jitter	t _{JIT(per)}	-75	75	-75	75	-82.5	82.5	-82.5	82.5	ps
Global	Cycle-to-cycle period jitter	$t_{\text{JIT(cc)}}$	-150	150	-150	150	-165	165	-165	165	ps
	Duty cycle jitter	$t_{JIT(duty)}$	-75	75	-75	75	-90	90	-90	90	ps

	Member		Active Serial (1))	Fast Passive Parallel ⁽²⁾			
Variant	Code	Width	DCLK (MHz)	Min Config Time (s)	Width	DCLK (MHz)	Min Config Time (s)	
	D3	4	100	0.344	32	100	0.043	
	D4	4	100	0.534	32	100	0.067	
GS	D4	4	100	0.344	32	100	0.043	
65	D5	4	100	0.534	32	100	0.067	
	D6	4	100	0.741	32	100	0.093	
	D8	4	100	0.741	32	100	0.093	
Е	E9	4	100	0.857	32	100	0.107	
	EB	4	100	0.857	32	100	0.107	

Table 48. Minimum Configuration Time Estimation for Stratix V Devices

Notes to Table 48:

(1) DCLK frequency of 100 MHz using external CLKUSR.

(2) Max FPGA FPP bandwidth may exceed bandwidth available from some external storage or control logic.

Fast Passive Parallel Configuration Timing

This section describes the fast passive parallel (FPP) configuration timing parameters for Stratix V devices.

DCLK-to-DATA[] Ratio for FPP Configuration

FPP configuration requires a different DCLK-to-DATA[]ratio when you enable the design security, decompression, or both features. Table 49 lists the DCLK-to-DATA[]ratio for each combination.

Configuration Scheme	Decompression	Design Security	DCLK-to-DATA[] Ratio
	Disabled	Disabled	1
FPP ×8	Disabled	Enabled	1
FFF X0	Enabled	Disabled	2
	Enabled	Enabled	2
	Disabled	Disabled	1
FPP ×16	Disabled	Enabled	2
	Enabled	Disabled	4
	Enabled	Enabled	4

 Table 49. DCLK-to-DATA[] Ratio ⁽¹⁾ (Part 1 of 2)

Active Serial Configuration Timing

Table 52 lists the DCLK frequency specification in the AS configuration scheme.

Table 52.	DCLK Frequency	Specification in the <i>l</i>	AS Configuration Scheme	(1), (2)
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Minimum	Typical	Maximum	Unit
5.3	7.9	12.5	MHz
10.6	15.7	25.0	MHz
21.3	31.4	50.0	MHz
42.6	62.9	100.0	MHz

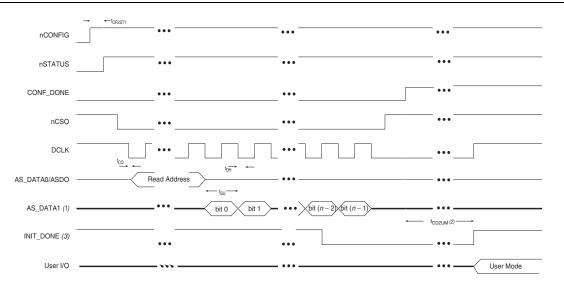
Notes to Table 52:

(1) This applies to the DCLK frequency specification when using the internal oscillator as the configuration clock source.

(2) The AS multi-device configuration scheme does not support DCLK frequency of 100 MHz.

Figure 14 shows the single-device configuration setup for an AS ×1 mode.





Notes to Figure 14:

- (1) If you are using AS $\times 4$ mode, this signal represents the AS_DATA[3..0] and EPCQ sends in 4-bits of data for each DCLK cycle.
- (2) The initialization clock can be from internal oscillator or CLKUSR pin.
- (3) After the option bit to enable the INIT_DONE pin is configured into the device, the INIT_DONE goes low.

Table 53 lists the timing parameters for AS $\times 1$ and AS $\times 4$ configurations in Stratix V devices.

Symbol	Parameter	Minimum	Maximum	Units
t _{CO}	DCLK falling edge to AS_DATA0/ASDO output	—	2	ns
t _{SU}	Data setup time before falling edge on DCLK	1.5	—	ns
t _H	Data hold time after falling edge on DCLK	0	—	ns

Symbol	Parameter	Minimum	Maximum	Units
t _{CD2UM}	CONF_DONE high to user mode (3)	175	437	μS
t _{CD2CU}	CONF_DONE high to CLKUSR enabled	4 × maximum DCLK period	_	—
t _{CD2UMC}	CONF_DONE high to user mode with CLKUSR option on	t _{cd2cu} + (8576 × clkusr period)	_	—

Table 53. AS Timing Parameters for AS \times 1 and AS \times 4 Configurations in Stratix V Devices ^{(1), (2)} (Part 2 of 2)

Notes to Table 53:

(1) The minimum and maximum numbers apply only if you choose the internal oscillator as the clock source for initializing the device.

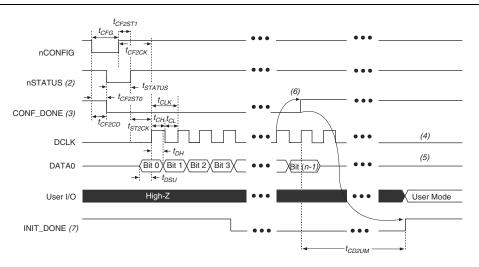
(2) t_{CF2CD}, t_{CF2ST0}, t_{CF2ST0}, t_{CF6}, t_{STATUS}, and t_{CF2ST1} timing parameters are identical to the timing parameters for PS mode listed in Table 54 on page 63.

(3) To enable the CLKUSR pin as the initialization clock source and to obtain the maximum frequency specification on this pin, refer to the Initialization section of the "Configuration, Design Security, and Remote System Upgrades in Stratix V Devices" chapter.

Passive Serial Configuration Timing

Figure 15 shows the timing waveform for a passive serial (PS) configuration when using a MAX II device, MAX V device, or microprocessor as an external host.

Figure 15. PS Configuration Timing Waveform ⁽¹⁾



Notes to Figure 15:

- (1) The beginning of this waveform shows the device in user mode. In user mode, nCONFIG, nSTATUS, and CONF_DONE are at logic high levels. When nCONFIG is pulled low, a reconfiguration cycle begins.
- (2) After power-up, the Stratix V device holds <code>nSTATUS</code> low for the time of the POR delay.
- (3) After power-up, before and during configuration, CONF DONE is low.
- (4) Do not leave DCLK floating after configuration. You can drive it high or low, whichever is more convenient.
- (5) DATAO is available as a user I/O pin after configuration. The state of this pin depends on the dual-purpose pin settings in the **Device and Pins Option**.
- (6) To ensure a successful configuration, send the entire configuration data to the Stratix V device. CONF_DONE is released high after the Stratix V device receives all the configuration data successfully. After CONF_DONE goes high, send two additional falling edges on DCLK to begin initialization and enter user mode.
- (7) After the option bit to enable the INIT DONE pin is configured into the device, the INIT DONE goes low.

Remote System Upgrades

Table 56 lists the timing parameter specifications for the remote system upgrade circuitry.

Table 56. Remote System Upgrade Circuitry Timing Specifications	Table 56.	Remote System	Upgrade Circuitry	y Timing S	Specifications
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Parameter	Minimum	Maximum	Unit
t _{RU_nCONFIG} ⁽¹⁾	250	—	ns
t _{RU_nRSTIMER} ⁽²⁾	250	—	ns

Notes to Table 56:

- (1) This is equivalent to strobing the reconfiguration input of the ALTREMOTE_UPDATE megafunction high for the minimum timing specification. For more information, refer to the Remote System Upgrade State Machine section of the "Configuration, Design Security, and Remote System Upgrades in Stratix V Devices" chapter.
- (2) This is equivalent to strobing the reset_timer input of the ALTREMOTE_UPDATE megafunction high for the minimum timing specification. For more information, refer to the User Watchdog Timer section of the "Configuration, Design Security, and Remote System Upgrades in Stratix V Devices" chapter.

User Watchdog Internal Circuitry Timing Specification

Table 57 lists the operating range of the 12.5-MHz internal oscillator.

Table 57. 12.5-MHz Internal Oscillator Specifications

Minimum	Typical	Maximum	Units
5.3	7.9	12.5	MHz

I/O Timing

Altera offers two ways to determine I/O timing—the Excel-based I/O Timing and the Quartus II Timing Analyzer.

Excel-based I/O timing provides pin timing performance for each device density and speed grade. The data is typically used prior to designing the FPGA to get an estimate of the timing budget as part of the link timing analysis. The Quartus II Timing Analyzer provides a more accurate and precise I/O timing data based on the specifics of the design after you complete place-and-route.

 You can download the Excel-based I/O Timing spreadsheet from the Stratix V Devices Documentation web page.

Programmable IOE Delay

Table 58 lists the Stratix V IOE programmable delay settings.

Table 58. IOE Programmable Delay for Stratix V Devices (Part 1 of 2)

Deremeter	Available	Min	Fast	Model				Slow N	lodel			
Parameter (1)	Available Settings	Offset (2)	Industrial	Commercial	C1	C2	C3	C4	12	13, 13YY	14	Unit
D1	64	0	0.464	0.493	0.838	0.838	0.924	1.011	0.844	0.921	1.006	ns
D2	32	0	0.230	0.244	0.415	0.415	0.459	0.503	0.417	0.456	0.500	ns

Parameter	Available	Min	Fast	Model				Slow N	lodel			
(1)	Settings	Offset (2)	Industrial	Commercial	C1	C2	C3	C4	12	13, 13YY	14	Unit
D3	8	0	1.587	1.699	2.793	2.793	2.992	3.192	2.811	3.047	3.257	ns
D4	64	0	0.464	0.492	0.838	0.838	0.924	1.011	0.843	0.920	1.006	ns
D5	64	0	0.464	0.493	0.838	0.838	0.924	1.011	0.844	0.921	1.006	ns
D6	32	0	0.229	0.244	0.415	0.415	0.458	0.503	0.418	0.456	0.499	ns

Notes to Table 58:

(1) You can set this value in the Quartus II software by selecting D1, D2, D3, D5, and D6 in the Assignment Name column of Assignment Editor.

(2) Minimum offset does not include the intrinsic delay.

Programmable Output Buffer Delay

Table 59 lists the delay chain settings that control the rising and falling edge delays of the output buffer. The default delay is 0 ps.

Table 59. Programmable Output Buffer Delay for Stratix V Devices (Table 59.	Programmable Out	put Buffer Delay	y for Stratix V Devices (
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Symbol	Parameter	Typical	Unit
		0 (default)	ps
D	Rising and/or falling edge delay	25	ps
D _{OUTBUF}		50	ps
		75	ps

Note to Table 59:

(1) You can set the programmable output buffer delay in the Quartus II software by setting the Output Buffer Delay Control assignment to either positive, negative, or both edges, with the specific values stated here (in ps) for the Output Buffer Delay assignment.

Glossary

Table 60 lists the glossary for this chapter.

Table 60. Glossary (Part 1 of 4)

Letter	Subject	ect Definitions		
Α				
В	—	—		
С				
D	_	_		
E	—	_		
	f _{HSCLK}	Left and right PLL input clock frequency.		
F	f _{HSDR}	High-speed I/O block—Maximum and minimum LVDS data transfer rate (f _{HSDR} = 1/TUI), non-DPA.		
	f _{hsdrdpa}	High-speed I/O block—Maximum and minimum LVDS data transfer rate (f _{HSDRDPA} = 1/TUI), DPA.		

Letter	Subject	Definitions				
	V _{CM(DC)}	DC common mode input voltage.				
	V _{ICM}	Input common mode voltage—The common mode of the differential signal at the receiver.				
	V _{ID}	Input differential voltage swing—The difference in voltage between the positive and complementary conductors of a differential transmission at the receiver.				
	V _{DIF(AC)}	AC differential input voltage—Minimum AC input differential voltage required for switching.				
	V _{DIF(DC)}	DC differential input voltage— Minimum DC input differential voltage required for switching.				
	V _{IH}	Voltage input high—The minimum positive voltage applied to the input which is accepted by the device as a logic high.				
	V _{IH(AC)}	High-level AC input voltage				
	V _{IH(DC)}	High-level DC input voltage				
V	V _{IL}	Voltage input low—The maximum positive voltage applied to the input which is accepted by the device as a logic low.				
	V _{IL(AC)}	Low-level AC input voltage				
	V _{IL(DC)}	Low-level DC input voltage				
	V _{OCM}	Output common mode voltage—The common mode of the differential signal at the transmitter.				
	V _{OD}	Output differential voltage swing—The difference in voltage between the positive and complementary conductors of a differential transmission at the transmitter.				
	V _{SWING}	Differential input voltage				
	V _X	Input differential cross point voltage				
	V _{OX}	Output differential cross point voltage				
W	W	High-speed I/O block—clock boost factor				
X						
Y	_	_				
Z						

Table 60. Glossary (Part 4 of 4)