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Intel - 5SGXMA3K3F35C4N Datasheet



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The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Obsolete
Number of LABs/CLBs	128300
Number of Logic Elements/Cells	340000
Total RAM Bits	19456000
Number of I/O	600
Number of Gates	-
Voltage - Supply	0.82V ~ 0.88V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	1152-BBGA, FCBGA
Supplier Device Package	1152-FBGA (35x35)
Purchase URL	https://www.e-xfl.com/product-detail/intel/5sgxma3k3f35c4n

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Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

								1
Transceiver Speed				Core Spe	ed Grade			
Grade	C1	C2, C2L	C3	C4	12, 12L	13, 13L	I 3YY	14
3 GX channel—8.5 Gbps	_	Yes	Yes	Yes	_	Yes	Yes ⁽⁴⁾	Yes

Table 1. Stratix V GX and GS Commercial and Industrial Speed Grade Offering ^{(1), (2), (3)} (Part 2 of 2)

Notes to Table 1:

(1) C = Commercial temperature grade; I = Industrial temperature grade.

(2) Lower number refers to faster speed grade.

(3) C2L, I2L, and I3L speed grades are for low-power devices.

(4) I3YY speed grades can achieve up to 10.3125 Gbps.

Table 2 lists the industrial and commercial speed grades for the Stratix V GT devices. **Table 2. Stratix V GT Commercial and Industrial Speed Grade Offering** ⁽¹⁾, ⁽²⁾

Transseiver Speed Grade	Core Speed Grade							
Transceiver Speeu draue	C1	C2	12	13				
2 GX channel—12.5 Gbps GT channel—28.05 Gbps	Yes	Yes	_	_				
3 GX channel—12.5 Gbps GT channel—25.78 Gbps	Yes	Yes	Yes	Yes				

Notes to Table 2:

(1) C = Commercial temperature grade; I = Industrial temperature grade.

(2) Lower number refers to faster speed grade.

Absolute Maximum Ratings

Absolute maximum ratings define the maximum operating conditions for Stratix V devices. The values are based on experiments conducted with the devices and theoretical modeling of breakdown and damage mechanisms. The functional operation of the device is not implied for these conditions.



Conditions other than those listed in Table 3 may cause permanent damage to the device. Additionally, device operation at the absolute maximum ratings for extended periods of time may have adverse effects on the device.

TANIC J. ANSULULC MAXIMUM NALINYS IVI SUALIX V DEVICES (FAIL I UI Z)	Table 3.	Absolute Maximum	Ratings	for Stratix \	/ Devices	(Part 1 of 2)
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Symbol	Description	Minimum	Maximum	Unit
V _{CC}	Power supply for core voltage and periphery circuitry	-0.5	1.35	V
V _{CCPT}	Power supply for programmable power technology	-0.5	1.8	V
V _{CCPGM}	Power supply for configuration pins	-0.5	3.9	V
V _{CC_AUX}	Auxiliary supply for the programmable power technology	-0.5	3.4	V
V _{CCBAT}	Battery back-up power supply for design security volatile key register	-0.5	3.9	V
V _{CCPD}	I/O pre-driver power supply	-0.5	3.9	V
V _{CCIO}	I/O power supply	-0.5	3.9	V

I/O Pin Leakage Current

Table 9 lists the Stratix V I/O pin leakage current specifications.

Table 9.	I/O Pin	Leakage	Current for	Stratix V	Devices (1)
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Symbol	Description	Conditions	Min	Тур	Max	Unit
I _I	Input pin	$V_I = 0 V \text{ to } V_{CCIOMAX}$	-30	_	30	μA
I _{OZ}	Tri-stated I/O pin	$V_0 = 0 V \text{ to } V_{\text{CCIOMAX}}$	-30		30	μA

Note to Table 9:

(1) If $V_0 = V_{CCI0}$ to $V_{CCI0Max}$, 100 μ A of leakage current per I/O is expected.

Bus Hold Specifications

Table 10 lists the Stratix V device family bus hold specifications.

Table 10. Bus Hold Parameters for Stratix V Devices

			V _{CCIO}										
Parameter	Symbol	Conditions	1.2	2 V	1.	5 V	1.8	B V	2.5	5 V	3.0	V	Unit
			Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Low sustaining current	I _{SUSL}	V _{IN} > V _{IL} (maximum)	22.5	_	25.0	_	30.0	_	50.0	_	70.0	_	μA
High sustaining current	I _{SUSH}	V _{IN} < V _{IH} (minimum)	-22.5		-25.0	_	-30.0	_	-50.0	_	-70.0		μA
Low overdrive current	I _{odl}	$0V < V_{IN} < V_{CCIO}$		120		160		200	_	300		500	μA
High overdrive current	I _{odh}	$0V < V_{IN} < V_{CCIO}$		-120		-160		-200		-300		-500	μΑ
Bus-hold trip point	V _{TRIP}	_	0.45	0.95	0.50	1.00	0.68	1.07	0.70	1.70	0.80	2.00	۷

On-Chip Termination (OCT) Specifications

If you enable OCT calibration, calibration is automatically performed at power-up for I/Os connected to the calibration block. Table 11 lists the Stratix V OCT termination calibration accuracy specifications.

Table 11. OCT Calibration Accuracy Specifications for Stratix V Devices ⁽¹⁾ (Part 1 of 2)

				Calibratio	n Accuracy		
Symbol	Description	Conditions	C1	C2,12	C3,I3, I3YY	C4,14	Unit
25- $Ω$ R _S	Internal series termination with calibration (25- Ω setting)	V _{CCI0} = 3.0, 2.5, 1.8, 1.5, 1.2 V	±15	±15	±15	±15	%

Symbol/	Conditions	Transceiver Speed Grade 1			Transceiver Speed Grade 2			Transceiver Speed Grade 3			Unit
Description		Min	Тур	Max	Min	Тур	Max	Min	Тур	Max	
Spread-spectrum downspread	PCIe	_	0 to 0.5	_	_	0 to 0.5	_	_	0 to 0.5	_	%
On-chip termination resistors ⁽²¹⁾	_	_	100		_	100		_	100		Ω
Absolute V _{MAX} ⁽⁵⁾	Dedicated reference clock pin	_	_	1.6	_	_	1.6	_	_	1.6	V
	RX reference clock pin	_		1.2		_	1.2			1.2	
Absolute V _{MIN}	—	-0.4	-	_	-0.4	_		-0.4	—		V
Peak-to-peak differential input voltage	_	200	_	1600	200	_	1600	200	_	1600	mV
V _{ICM} (AC	Dedicated reference clock pin	1050/	(1000/90	00/850 ⁽²⁾	1050/	1000/9	00/850 ⁽²⁾	1050/	1000/9	00/850 ⁽²⁾	mV
coupled) (9	RX reference clock pin	1	.0/0.9/0	.85 (4)	1.	.0/0.9/0	.85 (4)	1.	.0/0.9/0	.85 ⁽⁴⁾	V
V _{ICM} (DC coupled)	HCSL I/O standard for PCIe reference clock	250		550	250		550	250	_	550	mV
	100 Hz	—	—	-70	—	—	-70	—	—	-70	dBc/Hz
Transmitter	1 kHz	—	—	-90	—	—	-90	—	—	-90	dBc/Hz
REFCLK Phase	10 kHz	—	—	-100	—	—	-100	—	—	-100	dBc/Hz
(622 MHz) ⁽²⁰⁾	100 kHz	—	—	-110	—	—	-110	—	—	-110	dBc/Hz
	≥1 MHz	—	—	-120		—	-120	—	—	-120	dBc/Hz
Transmitter REFCLK Phase Jitter (100 MHz) ⁽¹⁷⁾	10 kHz to 1.5 MHz (PCIe)	_	_	3	_	_	3	_	_	3	ps (rms)
R _{REF} (19)	_	_	1800 ±1%	_	_	1800 ±1%	_	_	180 0 ±1%	_	Ω
Transceiver Clock	s										
fixedclk clock frequency	PCIe Receiver Detect		100 or 125			100 or 125		_	100 or 125		MHz

Table 23. Transceiver Specifications for Stratix V GX and GS Devices ⁽¹⁾ (Part 2 of 7)

Table 24 shows the maximum transmitter data rate for the clock network.

Table 24. Clock Network Maximum Data Rate Transmitter Specifications (1)

		ATX PLL		CMU PLL ⁽²⁾			fPLL		
Clock Network	Non- bonded Mode (Gbps)	Bonded Mode (Gbps)	Channel Span	Non- bonded Mode (Gbps)	Bonded Mode (Gbps)	Channel Span	Non- bonded Mode (Gbps)	Bonded Mode (Gbps)	Channel Span
x1 ⁽³⁾	14.1	_	6	12.5	_	6	3.125	—	3
x6 ⁽³⁾	_	14.1	6	—	12.5	6	—	3.125	6
x6 PLL Feedback ⁽⁴⁾	_	14.1	Side- wide	_	12.5	Side- wide	_	_	_
xN (PCIe)	_	8.0	8	—	5.0	8	—	—	—
VNI (Native DHV ID)	8.0	8.0	Up to 13 channels above and below PLL	7 00	7 00	Up to 13 channels above	3 125	3 125	Up to 13 channels above
xN (Native PHY IP)	_	8.01 to 9.8304	Up to 7 channels above and below PLL	7.99	7.99	and below PLL	0.120	0.120	and below PLL

Notes to Table 24:

(1) Valid data rates below the maximum specified in this table depend on the reference clock frequency and the PLL counter settings. Check the MegaWizard message during the PHY IP instantiation.

(2) ATX PLL is recommended at 8 Gbps and above data rates for improved jitter performance.

(3) Channel span is within a transceiver bank.

(4) Side-wide channel bonding is allowed up to the maximum supported by the PHY IP.

	Table 28.	Transceiver S	pecifications	for Stratix V	GT Devices	(Part 4 of 5) (1)
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Symbol/	Conditions	s	Transceive peed Grade	r 2	ר Sp	Fransceive Deed Grade	r 3	Unit
Description		Min	Тур	Max	Min	Тур	Max	
Data rate	GT channels	19,600	_	28,050	19,600		25,780	Mbps
Differential on-chip	GT channels	_	100	—		100	_	Ω
termination resistors	GX channels				(8)			
	GT channels	_	500	_		500	_	mV
V _{OCM} (AC Coupled)	GX channels		•	•	(8)		•	
Dice/Fell time	GT channels	_	15	—	—	15	—	ps
Rise/Fail lime	GX channels				(8)			
Intra-differential pair skew	GX channels				(8)			
Intra-transceiver block transmitter channel-to- channel skew	GX channels				(8)			
Inter-transceiver block transmitter channel-to- channel skew	GX channels				(8)			
CMU PLL								
Supported Data Range	—	600		12500	600		8500	Mbps
t _{pll_powerdown} ⁽¹³⁾	—	1	—	—	1	_	—	μs
t _{pll_lock} ⁽¹⁴⁾	—	_	—	10	_	_	10	μs
ATX PLL								
	VCO post- divider L=2	8000	_	12500	8000	_	8500	Mbps
	L=4	4000	—	6600	4000	_	6600	Mbps
Supported Data Rate	L=8	2000	—	3300	2000	_	3300	Mbps
Range for GX Channels	L=8, Local/Central Clock Divider =2	1000	_	1762.5	1000	_	1762.5	Mbps
Supported Data Rate Range for GT Channels	VCO post- divider L=2	9800	_	14025	9800	_	12890	Mbps
t _{pll_powerdown} ⁽¹³⁾	—	1	—	—	1	_	—	μs
t _{pll_lock} ⁽¹⁴⁾	—	_	—	10	_	_	10	μs
fPLL								
Supported Data Range		600		3250/ 3.125 ⁽²³⁾	600		3250/ 3.125 ⁽²³⁾	Mbps
t _{pll_powerdown} ⁽¹³⁾	—	1	—	—	1	—	—	μs

Figure 6 shows the Stratix V DC gain curves for GT channels.

Figure 6. DC Gain Curves for GT Channels

Transceiver Characterization

This section summarizes the Stratix V transceiver characterization results for compliance with the following protocols:

- Interlaken
- 40G (XLAUI)/100G (CAUI)
- 10GBase-KR
- QSGMII
- XAUI
- SFI
- Gigabit Ethernet (Gbe / GIGE)
- SPAUI
- Serial Rapid IO (SRIO)
- CPRI
- OBSAI
- Hyper Transport (HT)
- SATA
- SAS
- CEI

Symbol	Parameter	Min	Тур	Max	Unit
+ (3) (4)	Input clock cycle-to-cycle jitter ($f_{REF} \ge 100 \text{ MHz}$)			0.15	UI (p-p)
LINCCJ (0), (1)	Input clock cycle-to-cycle jitter (f _{REF} < 100 MHz)	-750		+750	ps (p-p)
+ (5)	Period Jitter for dedicated clock output (f_{OUT} \geq 100 MHz)	_	_	175 ⁽¹⁾	ps (p-p)
CUTPJ_DC	Period Jitter for dedicated clock output (f _{OUT} < 100 MHz)	_	_	17.5 ⁽¹⁾	mUI (p-p)
+ (5)	Period Jitter for dedicated clock output in fractional PLL ($f_{OUT} \ge 100$ MHz)	_	_	250 ⁽¹¹⁾ , 175 ⁽¹²⁾	ps (p-p)
FOUTPJ_DC	Period Jitter for dedicated clock output in fractional PLL (f _{OUT} < 100 MHz)	_	_	25 ⁽¹¹⁾ , 17.5 ⁽¹²⁾	mUI (p-p)
+ (5)	Cycle-to-Cycle Jitter for a dedicated clock output ($f_{\text{OUT}} \geq 100 \text{ MHz})$		_	175	ps (p-p)
COUTCCJ_DC	Cycle-to-Cycle Jitter for a dedicated clock output $(f_{OUT} < 100 \text{ MHz})$		_	17.5	mUI (p-p)
+ (5)	Cycle-to-cycle Jitter for a dedicated clock output in fractional PLL ($f_{OUT} \ge 100 \text{ MHz}$)		_	250 ⁽¹¹⁾ , 175 ⁽¹²⁾	ps (p-p)
FOUTCCJ_DC	Cycle-to-cycle Jitter for a dedicated clock output in fractional PLL ($f_{OUT} < 100 \text{ MHz}$)+		_	25 ⁽¹¹⁾ , 17.5 ⁽¹²⁾	mUI (p-p)
t _{outpj 10} (5),	Period Jitter for a clock output on a regular I/O in integer PLL ($f_{OUT} \ge 100 \text{ MHz}$)		_	600	ps (p-p)
(8)	Period Jitter for a clock output on a regular I/O $(f_{OUT} < 100 \text{ MHz})$		_	60	mUI (p-p)
t _{foutpj 10} ^{(5),}	Period Jitter for a clock output on a regular I/O in fractional PLL ($f_{OUT} \ge 100 \text{ MHz}$)	_	_	600 ⁽¹⁰⁾	ps (p-p)
(8), (11)	Period Jitter for a clock output on a regular I/O in fractional PLL (f _{OUT} < 100 MHz)	_	_	60 ⁽¹⁰⁾	mUI (p-p)
t _{outccj_io} (5),	Cycle-to-cycle Jitter for a clock output on a regular I/O in integer PLL ($f_{OUT} \geq 100 \mbox{ MHz})$	_	_	600	ps (p-p)
(8)	Cycle-to-cycle Jitter for a clock output on a regular I/O in integer PLL (f _{OUT} < 100 MHz)	_	_	60 ⁽¹⁰⁾	mUI (p-p)
t _{FOUTCCJ 10} (5),	Cycle-to-cycle Jitter for a clock output on a regular I/O in fractional PLL ($f_{OUT} \ge 100$ MHz)		_	600 ⁽¹⁰⁾	ps (p-p)
(8), (11)	Cycle-to-cycle Jitter for a clock output on a regular I/O in fractional PLL (f _{OUT} < 100 MHz)	_	_	60	mUI (p-p)
t _{CASC OUTPJ DC}	Period Jitter for a dedicated clock output in cascaded PLLs ($f_{OUT} \ge 100 \text{ MHz}$)	_	_	175	ps (p-p)
(5), (6)	Period Jitter for a dedicated clock output in cascaded PLLs (f_{OUT} < 100 MHz)	_	_	17.5	mUI (p-p)
f _{DRIFT}	Frequency drift after PFDENA is disabled for a duration of 100 μs		_	±10	%
dK _{BIT}	Bit number of Delta Sigma Modulator (DSM)	8	24	32	Bits
k _{VALUE}	Numerator of Fraction	128	8388608	2147483648	—

Table 31. PLL Specifications for Stratix V Devices (Part 2 of 3)

Table 31. PLL Specifications for Stratix V Devices (Part 3 of 3)

Symbol	Parameter	Min	Тур	Max	Unit
f _{RES}	Resolution of VCO frequency ($f_{INPFD} = 100 \text{ MHz}$)	390625	5.96	0.023	Hz

Notes to Table 31:

(1) This specification is limited in the Quartus II software by the I/O maximum frequency. The maximum I/O frequency is different for each I/O standard.

(2) This specification is limited by the lower of the two: I/O f_{MAX} or f_{OUT} of the PLL.

- (3) A high input jitter directly affects the PLL output jitter. To have low PLL output clock jitter, you must provide a clean clock source < 120 ps.
- (4) f_{REF} is fIN/N when N = 1.
- (5) Peak-to-peak jitter with a probability level of 10⁻¹² (14 sigma, 99.9999999974404% confidence level). The output jitter specification applies to the intrinsic jitter of the PLL, when an input jitter of 30 ps is applied. The external memory interface clock output jitter specifications use a different measurement method and are available in Table 44 on page 52.
- (6) The cascaded PLL specification is only applicable with the following condition: a. Upstream PLL: 0.59Mhz ≤ Upstream PLL BW < 1 MHz b. Downstream PLL: Downstream PLL BW > 2 MHz
- (7) High bandwidth PLL settings are not supported in external feedback mode.
- (8) The external memory interface clock output jitter specifications use a different measurement method, which is available in Table 42 on page 50.
- (9) The VCO frequency reported by the Quartus II software in the PLL Usage Summary section of the compilation report takes into consideration the VCO post-scale counter K value. Therefore, if the counter K has a value of 2, the frequency reported can be lower than the f_{VCO} specification.
- (10) This specification only covers fractional PLL for low bandwidth. The f_{VCO} for fractional value range 0.05 0.95 must be \geq 1000 MHz, while f_{VCO} for fractional value range 0.20 0.80 must be \geq 1200 MHz.
- (11) This specification only covered fractional PLL for low bandwidth. The f_{VC0} for fractional value range 0.05-0.95 must be \geq 1000 MHz.
- (12) This specification only covered fractional PLL for low bandwidth. The f_{VC0} for fractional value range 0.20-0.80 must be \geq 1200 MHz.

DSP Block Specifications

Table 32 lists the Stratix V DSP block performance specifications.

			F	Peformanc	e			
Mode	C1	C2, C2L	12, 12L	C3	13, 13L, 13YY	C4	14	Unit
		Modes ı	using one	DSP				
Three 9 x 9	600	600	600	480	480	420	420	MHz
One 18 x 18	600	600	600	480	480	420	400	MHz
Two partial 18 x 18 (or 16 x 16)	600	600	600	480	480	420	400	MHz
One 27 x 27	500	500	500	400	400	350	350	MHz
One 36 x 18	500	500	500	400	400	350	350	MHz
One sum of two 18 x 18(One sum of 2 16 x 16)	500	500	500	400	400	350	350	MHz
One sum of square	500	500	500	400	400	350	350	MHz
One 18 x 18 plus 36 (a x b) + c	500	500	500	400	400	350	350	MHz
		Modes u	sing two l	DSPs				
Three 18 x 18	500	500	500	400	400	350	350	MHz
One sum of four 18 x 18	475	475	475	380	380	300	300	MHz
One sum of two 27 x 27	465	465	450	380	380	300	290	MHz
One sum of two 36 x 18	475	475	475	380	380	300	300	MHz
One complex 18 x 18	500	500	500	400	400	350	350	MHz
One 36 x 36	475	475	475	380	380	300	300	MHz

Table 32. Block Performance Specifications for Stratix V DSP Devices (Part 1 of 2)

		Resour	ces Used			Pe	erforman	ce			
Memory	Mode	ALUTS	Memory	C1	C2, C2L	C3	C4	12, 12L	13, 13L, 13YY	14	Unit
	Single-port, all supported widths	0	1	700	700	650	550	700	500	450	MHz
	Simple dual-port, all supported widths	0	1	700	700	650	550	700	500	450	MHz
	Simple dual-port with the read-during-write option set to Old Data , all supported widths	0	1	525	525	455	400	525	455	400	MHz
M20K Block	Simple dual-port with ECC enabled, 512 × 32	0	1	450	450	400	350	450	400	350	MHz
	Simple dual-port with ECC and optional pipeline registers enabled, 512 × 32	0	1	600	600	500	450	600	500	450	MHz
	True dual port, all supported widths	0	1	700	700	650	550	700	500	450	MHz
	ROM, all supported widths	0	1	700	700	650	550	700	500	450	MHz

Table 33. Memory Block Performance Specifications for Stratix V Devices ^{(1), (2)} (Part 2 of 2)

Notes to Table 33:

(1) To achieve the maximum memory block performance, use a memory block clock that comes through global clock routing from an on-chip PLL set to **50**% output duty cycle. Use the Quartus II software to report timing for this and other memory block clocking schemes.

(2) When you use the error detection cyclical redundancy check (CRC) feature, there is no degradation in F_{MAX}.

(3) The F_{MAX} specification is only achievable with Fitter options, MLAB Implementation In 16-Bit Deep Mode enabled.

Temperature Sensing Diode Specifications

Table 34 lists the internal TSD specification.

Table 34. Internal Temperature Sensing Diode Specification

Temperature Range	Accuracy	Offset Calibrated Option	Sampling Rate	Conversion Time	Resolution	Minimum Resolution with no Missing Codes
-40°C to 100°C	±8°C	No	1 MHz, 500 KHz	< 100 ms	8 bits	8 bits

Table 35 lists the specifications for the Stratix V external temperature sensing diode.

Table 35.	External	Temperature	Sensing D	iode Speci	fications f	for Stratix V	Devices
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Description	Min	Тур	Max	Unit
I _{bias} , diode source current	8	—	200	μA
V _{bias,} voltage across diode	0.3	—	0.9	V
Series resistance	—	_	< 1	Ω
Diode ideality factor	1.006	1.008	1.010	_

Periphery Performance

This section describes periphery performance, including high-speed I/O and external memory interface.

I/O performance supports several system interfaces, such as the **LVDS** high-speed I/O interface, external memory interface, and the **PCI/PCI-X** bus interface. General-purpose I/O standards such as 3.3-, 2.5-, 1.8-, and 1.5-**LVTTL/LVCMOS** are capable of a typical 167 MHz and 1.2-**LVCMOS** at 100 MHz interfacing frequency with a 10 pF load.

The actual achievable frequency depends on design- and system-specific factors. Ensure proper timing closure in your design and perform HSPICE/IBIS simulations based on your specific design and system setup to determine the maximum achievable frequency in your system.

High-Speed I/O Specification

Table 36 lists high-speed I/O timing for Stratix V devices.

Table 36. High-Speed I/O Specifications for Stratix V Devices (1), (2) (Part 1 of 4)

Sumbol	Conditions		C1		C2,	C2L, I	2, I2L	C3,	13, 13 1	., I3YY		C4,I	4	11
Symbol	Conditions	Min	Тур	Max	Min	Тур	Max	Min	Тур	Max	Min	Тур	Max	UNIT
f _{HSCLK_in} (input clock frequency) True Differential I/O Standards	Clock boost factor W = 1 to 40 $^{(4)}$	5	_	800	5		800	5		625	5		525	MHz
f _{HSCLK_in} (input clock frequency) Single Ended I/O Standards ⁽³⁾	Clock boost factor W = 1 to 40 $^{(4)}$	5		800	5		800	5		625	5		525	MHz
f _{HSCLK_in} (input clock frequency) Single Ended I/O Standards	Clock boost factor W = 1 to 40 $^{(4)}$	5	_	520	5		520	5	_	420	5	_	420	MHz
f _{HSCLK_OUT} (output clock frequency)	_	5	_	800	5	_	800	5	_	625 (5)	5	_	525 (5)	MHz

Symbol	Conditiono		C1		C2,	C2L, I	2, I2L	C3,	13, 131	L, I3YY	C4,I4			Unit
əyiinuu	Conultions	Min	Тур	Max	Min	Тур	Max	Min	Тур	Max	Min	Тур	Max	Umt
	SERDES factor J = 3 to 10	(6)		(8)	(6)	_	(8)	(6)		(8)	(6)		(8)	Mbps
f _{HSDR} (data rate)	SERDES factor J = 2, uses DDR Registers	(6)		(7)	(6)	_	(7)	(6)	_	(7)	(6)		(7)	Mbps
	SERDES factor J = 1, uses SDR Register	(6)	_	(7)	(6)	_	(7)	(6)	_	(7)	(6)	_	(7)	Mbps
DPA Mode														
DPA run length	_			1000 0		_	1000 0	_		1000 0	_		1000 0	UI
Soft CDR mode														
Soft-CDR PPM tolerance	_	_	_	300	_	_	300	_	_	300	_	_	300	± PPM
Non DPA Mode														
Sampling Window	_			300			300			300			300	ps

Table 36. High-Speed I/O Specifications for Stratix V Devices (1), (2) (Part 4 of 4)

Notes to Table 36:

(1) When J = 3 to 10, use the serializer/deserializer (SERDES) block.

(2) When J = 1 or 2, bypass the SERDES block.

(3) This only applies to DPA and soft-CDR modes.

(4) Clock Boost Factor (W) is the ratio between the input data rate to the input clock rate.

(5) This is achieved by using the **LVDS** clock network.

- (6) The minimum specification depends on the clock source (for example, the PLL and clock pin) and the clock routing resource (global, regional, or local) that you use. The I/O differential buffer and input register do not have a minimum toggle rate.
- (7) The maximum ideal frequency is the SERDES factor (J) x the PLL maximum output frequency (fOUT) provided you can close the design timing and the signal integrity simulation is clean.
- (8) You can estimate the achievable maximum data rate for non-DPA mode by performing link timing closure analysis. You must consider the board skew margin, transmitter delay margin, and receiver sampling margin to determine the maximum data rate supported.

(9) If the receiver with DPA enabled and transmitter are using shared PLLs, the minimum data rate is 150 Mbps.

- (10) You must calculate the leftover timing margin in the receiver by performing link timing closure analysis. You must consider the board skew margin, transmitter channel-to-channel skew, and receiver sampling margin to determine leftover timing margin.
- (11) The F_{MAX} specification is based on the fast clock used for serial data. The interface F_{MAX} is also dependent on the parallel clock domain which is design-dependent and requires timing analysis.
- (12) Stratix V RX LVDS will need DPA. For Stratix V TX LVDS, the receiver side component must have DPA.
- (13) Stratix V LVDS serialization and de-serialization factor needs to be x4 and above.
- (14) Requires package skew compensation with PCB trace length.
- (15) Do not mix single-ended I/O buffer within LVDS I/O bank.
- (16) Chip-to-chip communication only with a maximum load of 5 pF.
- (17) When using True LVDS RX channels for emulated LVDS TX channel, only serialization factors 1 and 2 are supported.

Figure 7 shows the dynamic phase alignment (DPA) lock time specifications with the DPA PLL calibration option enabled.

Figure 7. DPA Lock Time Specification with DPA PLL Calibration Enabled

rx_reset			
rx_dpa_locked			<u> </u>
			-

Table 37 lists the DPA lock time specifications for Stratix V devices.

Table 37. DPA Lock Time Specifications for Stratix V GX Devices Only (1), (2), (3)

Standard	Training Pattern	Number of Data Transitions in One Repetition of the Training Pattern	Number of Repetitions per 256 Data Transitions ⁽⁴⁾	Maximum
SPI-4	00000000001111111111	2	128	640 data transitions
Parallel Rapid I/O	00001111	2	128	640 data transitions
	10010000	4	64	640 data transitions
Miscellaneous	10101010	8	32	640 data transitions
Wiscenareous	01010101	8	32	640 data transitions

Notes to Table 37:

(1) The DPA lock time is for one channel.

(2) One data transition is defined as a 0-to-1 or 1-to-0 transition.

(3) The DPA lock time stated in this table applies to both commercial and industrial grade.

(4) This is the number of repetitions for the stated training pattern to achieve the 256 data transitions.

Figure 8 shows the **LVDS** soft-clock data recovery (CDR)/DPA sinusoidal jitter tolerance specification for a data rate \geq 1.25 Gbps. Table 38 lists the **LVDS** soft-CDR/DPA sinusoidal jitter tolerance specification for a data rate \geq 1.25 Gbps.





Speed Grade	Min	Max	Unit
C4,I4	8	16	ps

Table 40. DQS Phase Offset Delay Per Setting for Stratix V Devices ^{(1), (2)} (Part 2 of 2)

Notes to Table 40:

(1) The typical value equals the average of the minimum and maximum values.

(2) The delay settings are linear with a cumulative delay variation of 40 ps for all speed grades. For example, when using a -2 speed grade and applying a 10-phase offset setting to a 90° phase shift at 400 MHz, the expected average cumulative delay is [625 ps + (10 × 10 ps) ± 20 ps] = 725 ps ± 20 ps.

Table 41 lists the DQS phase shift error for Stratix V devices.

Table 41. DQS Phase Shift Error Specification for DLL-Delayed Clock (t_{DQS_PSERR}) for Stratix V Devices ⁽¹⁾

Number of DQS Delay Buffers	C1	C2, C2L, I2, I2L	C3, I3, I3L, I3YY	C4,14	Unit
1	28	28	30	32	ps
2	56	56	60	64	ps
3	84	84	90	96	ps
4	112	112	120	128	ps

Notes to Table 41:

(1) This error specification is the absolute maximum and minimum error. For example, skew on three DQS delay buffers in a -2 speed grade is ± 78 ps or ± 39 ps.

Table 42 lists the memory output clock jitter specifications for Stratix V devices.

Table 42. Memory Output Clock Jitter Specification for Stratix V Devices (1	^{),} (Part 1 of 2) ^{(2), (3)}
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Clock	Parameter Symb		C	1	C2, C2L	, 12, 12L	C3, I3 I3	8, 13L, YY	C4	,14	Unit
NGLWUIK		-	Min	Max	Min	Max	Min	Max	Min	Max	
	Clock period jitter	$t_{JIT(per)}$	-50	50	-50	50	-55	55	-55	55	ps
Regional	Cycle-to-cycle period jitter	$t_{\text{JIT(cc)}}$	-100	100	-100	100	-110	110	-110	110	ps
	Duty cycle jitter	$t_{JIT(duty)}$	-50	50	-50	50	-82.5	82.5	-82.5	82.5	ps
	Clock period jitter	$t_{JIT(per)}$	-75	75	-75	75	-82.5	82.5	-82.5	82.5	ps
Global	Cycle-to-cycle period jitter	$t_{\text{JIT(cc)}}$	-150	150	-150	150	-165	165	-165	165	ps
	Duty cycle jitter	$t_{JIT(duty)}$	-75	75	-75	75	-90	90	-90	90	ps

Clock Notwork Parameter		Symbol	C	1	C2, C2L	, 12, 12L	C3, I3 I3	8, 13L , YY	C4	,14	Unit
Network			Min	Max	Min	Max	Min	Max	Min	Max	
	Clock period jitter	$t_{JIT(per)}$	-25	25	-25	25	-30	30	-35	35	ps
PHY Clock	Cycle-to-cycle period jitter	$t_{\rm JIT(cc)}$	-50	50	-50	50	-60	60	-70	70	ps
	Duty cycle jitter	$t_{JIT(duty)}$	-37.5	37.5	-37.5	37.5	-45	45	-56	56	ps

Table 42. Memory Output Clock Jitter Specification for Stratix V Devices (1), (Part 2 of 2) (2), (3)

Notes to Table 42:

(1) The clock jitter specification applies to the memory output clock pins generated using differential signal-splitter and DDIO circuits clocked by a PLL output routed on a PHY, regional, or global clock network as specified. Altera recommends using PHY clock networks whenever possible.

(2) The clock jitter specification applies to the memory output clock pins clocked by an integer PLL.

(3) The memory output clock jitter is applicable when an input jitter of 30 ps peak-to-peak is applied with bit error rate (BER) -12, equivalent to 14 sigma.

OCT Calibration Block Specifications

Table 43 lists the OCT calibration block specifications for Stratix V devices.

Table 43. OCT Calibration Block Specifications for Stratix V Devices

Symbol	Description	Min	Тур	Max	Unit
OCTUSRCLK	Clock required by the OCT calibration blocks	—	—	20	MHz
T _{OCTCAL}	Number of OCTUSRCLK clock cycles required for OCT $\rm R_S/R_T$ calibration		1000	_	Cycles
T _{OCTSHIFT}	Number of OCTUSRCLK clock cycles required for the OCT code to shift out	_	32	_	Cycles
T _{RS_RT}	Time required between the dyn_term_ctrl and oe signal transitions in a bidirectional I/O buffer to dynamically switch between OCT R_S and R_T (Figure 10)		2.5		ns

Figure 10 shows the timing diagram for the oe and dyn_term_ctrl signals.

Figure 10. Timing Diagram for oe and dyn_term_ctrl Signals



Duty Cycle Distortion (DCD) Specifications

Table 44 lists the worst-case DCD for Stratix V devices.

Table 44. Worst-Case DCD on Stratix V I/O Pins (1)

Symbol	C	1	C2, C2	L, 12, 12L	C3, I I3	3, I3L, BYY	C4	4,14	Unit
-	Min	Max	Min	Max	Min	Max	Min	Max	
Output Duty Cycle	45	55	45	55	45	55	45	55	%

Note to Table 44:

(1) The DCD numbers do not cover the core clock network.

Configuration Specification

POR Delay Specification

Power-on reset (POR) delay is defined as the delay between the time when all the power supplies monitored by the POR circuitry reach the minimum recommended operating voltage to the time when the nSTATUS is released high and your device is ready to begin configuration.



For more information about the POR delay, refer to the *Hot Socketing and Power-On Reset in Stratix V Devices* chapter.

Table 45 lists the fast and standard POR delay specification.

Table 45. Fast and Standard POR Delay Specification (1)

POR Delay	Minimum	Maximum
Fast	4 ms	12 ms
Standard	100 ms	300 ms

Note to Table 45:

(1) You can select the POR delay based on the MSEL settings as described in the MSEL Pin Settings section of the "Configuration, Design Security, and Remote System Upgrades in Stratix V Devices" chapter.

JTAG Configuration Specifications

Table 46 lists the JTAG timing parameters and values for Stratix V devices.

Table 46. JTAG Timing Parameters and Values for Stratix V Devices

Symbol	Description	Min	Max	Unit
t _{JCP}	TCK clock period ⁽²⁾	30		ns
t _{JCP}	TCK clock period ⁽²⁾	167	—	ns
t _{JCH}	TCK clock high time ⁽²⁾	14	—	ns
t _{JCL}	TCK clock low time ⁽²⁾	14		ns
t _{JPSU (TDI)}	TDI JTAG port setup time	2	—	ns
t _{JPSU (TMS)}	TMS JTAG port setup time	3	_	ns

Symbol	Description	Min	Max	Unit
t _{JPH}	JTAG port hold time	5	—	ns
t _{JPCO}	JTAG port clock to output	—	11 ⁽¹⁾	ns
t _{JPZX}	JTAG port high impedance to valid output	—	14 ⁽¹⁾	ns
t _{JPXZ}	JTAG port valid output to high impedance	—	14 ⁽¹⁾	ns

Table 46. JTAG Timing Parameters and Values for Stratix V Devices

Notes to Table 46:

(1) A 1 ns adder is required for each V_{CCI0} voltage step down from 3.0 V. For example, $t_{JPC0} = 12$ ns if V_{CCI0} of the TDO I/O bank = 2.5 V, or 13 ns if it equals 1.8 V.

(2) The minimum TCK clock period is 167 ns if VCCBAT is within the range 1.2V-1.5V when you perform the volatile key programming.

Raw Binary File Size

For the POR delay specification, refer to the "POR Delay Specification" section of the "Configuration, Design Security, and Remote System Upgrades in Stratix V Devices".

Table 47 lists the uncompressed raw binary file (.rbf) sizes for Stratix V devices.

Family	Device	Package	Configuration .rbf Size (bits)	IOCSR .rbf Size (bits) ^{(4), (5)}
	500742	H35, F40, F35 ⁽²⁾	213,798,880	562,392
	JOUNAS	H29, F35 ⁽³⁾	137,598,880	564,504
	5SGXA4	—	213,798,880	563,672
	5SGXA5	—	269,979,008	562,392
	5SGXA7	—	269,979,008	562,392
Stratix V GX	5SGXA9	—	342,742,976	700,888
	5SGXAB	—	342,742,976	700,888
	5SGXB5	—	270,528,640	584,344
	5SGXB6	—	270,528,640	584,344
	5SGXB9	_	342,742,976	700,888
	5SGXBB	—	342,742,976	700,888
Stratix V CT	5SGTC5	—	269,979,008	562,392
	5SGTC7	_	269,979,008	562,392
	5SGSD3	—	137,598,880	564,504
	590904	F1517	213,798,880	563,672
Strativ V CS	J303D4		137,598,880	564,504
	5SGSD5		213,798,880	563,672
	5SGSD6		293,441,888	565,528
	5SGSD8	—	293,441,888	565,528

Table 47. Uncompressed .rbf Sizes for Stratix V Devices

Configuration Scheme Decompression		Design Security	DCLK-to-DATA[] Ratio
	Disabled	Disabled	1
	Disabled	Enabled	4
IFF XJZ	Enabled	Disabled	8
	Enabled	Enabled	8

Table 49.	DCLK-to-DATA[]	Ratio ⁽¹⁾	(Part 2 of 2)
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Note to Table 49:

(1) Depending on the DCLK-to-DATA [] ratio, the host must send a DCLK frequency that is r times the data rate in bytes per second (Bps), or words per second (Wps). For example, in FPP ×16 when the DCLK-to-DATA [] ratio is 2, the DCLK frequency must be 2 times the data rate in Wps. Stratix V devices use the additional clock cycles to decrypt and decompress the configuration data.

Figure 11 shows the configuration interface connections between the Stratix V device and a MAX II or MAX V device for single device configuration.

Figure 11. Single Device FPP Configuration Using an External Host



Notes to Figure 11:

- (1) Connect the resistor to a supply that provides an acceptable input signal for the Stratix V device. V_{CCPGM} must be high enough to meet the V_{IH} specification of the I/O on the device and the external host. Altera recommends powering up all configuration system I/Os with V_{CCPGM} .
- (2) You can leave the nCEO pin unconnected or use it as a user I/O pin when it does not feed another device's nCE pin.
- (3) The MSEL pin settings vary for different data width, configuration voltage standards, and POR delay. To connect MSEL, refer to the MSEL Pin Settings section of the "Configuration, Design Security, and Remote System Upgrades in Stratix V Devices" chapter.
- (4) If you use FPP ×8, use DATA [7..0]. If you use FPP ×16, use DATA [15..0].

IF the DCLK-to-DATA[] ratio is greater than 1, at the end of configuration, you can only stop the DCLK (DCLK-to-DATA[] ratio – 1) clock cycles after the last data is latched into the Stratix V device.

Table 54 lists the PS configuration timing parameters for Stratix V devices.

Table 54. PS Timing Parameters for Stratix V Devices

Symbol	Parameter	Minimum	Maximum	Units
t _{CF2CD}	nCONFIG low to CONF_DONE low	—	600	ns
t _{CF2ST0}	nCONFIG low to nSTATUS low	—	600	ns
t _{CFG}	nCONFIG low pulse width	2	—	μS
t _{status}	nSTATUS low pulse width	268	1,506 ⁽¹⁾	μS
t _{CF2ST1}	nCONFIG high to nSTATUS high	—	1,506 ⁽²⁾	μS
t _{CF2CK} (5)	nCONFIG high to first rising edge on DCLK	1,506	—	μS
t _{ST2CK} (5)	nSTATUS high to first rising edge of DCLK	2	—	μS
t _{DSU}	DATA[] setup time before rising edge on DCLK	5.5	—	ns
t _{DH}	DATA [] hold time after rising edge on DCLK	0	—	ns
t _{CH}	DCLK high time	$0.45\times 1/f_{MAX}$	—	S
t _{CL}	DCLK low time	$0.45\times 1/f_{MAX}$	—	S
t _{CLK}	DCLK period	1/f _{MAX}	—	S
f _{MAX}	DCLK frequency	—	125	MHz
t _{CD2UM}	CONF_DONE high to user mode ⁽³⁾	175	437	μS
t _{CD2CU}	CONF_DONE high to CLKUSR enabled	4 × maximum DCLK period	_	_
t _{cd2UMC}	$_{\rm UMC}$ $_{\rm CONF_DONE}$ high to user mode with <code>CLKUSR</code> option on ${\rm t_{CD2CU}} + (8576 \times {\rm CLKUSR} \ {\rm period})^{(4)}$		_	_

Notes to Table 54:

(1) This value is applicable if you do not delay configuration by extending the nCONFIG or nSTATUS low pulse width.

(2) This value is applicable if you do not delay configuration by externally holding the nSTATUS low.

(3) The minimum and maximum numbers apply only if you choose the internal oscillator as the clock source for initializing the device.

(4) To enable the CLKUSR pin as the initialization clock source and to obtain the maximum frequency specification on these pins, refer to the "Initialization" section.

(5) If nSTATUS is monitored, follow the t_{ST2CK} specification. If nSTATUS is not monitored, follow the t_{CF2CK} specification.

Initialization

Table 55 lists the initialization clock source option, the applicable configuration schemes, and the maximum frequency.

Table 55.	Initialization	Clock Source	Option	and the	Maximum	Frequency

Initialization Clock Source	Configuration Schemes	Maximum Frequency	Minimum Number of Clock Cycles ⁽¹⁾
Internal Oscillator	AS, PS, FPP	12.5 MHz	
CLKUSR	AS, PS, FPP ⁽²⁾	125 MHz	8576
DCLK	PS, FPP	125 MHz	

Notes to Table 55:

(1) The minimum number of clock cycles required for device initialization.

(2) To enable CLKUSR as the initialization clock source, turn on the Enable user-supplied start-up clock (CLKUSR) option in the Quartus II software from the General panel of the Device and Pin Options dialog box.

Table 60.	Glossary	(Part 3 of 4)
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Letter	Subject	Definitions			
	SW (sampling window)	Timing Diagram—the period of time during which the data must be valid in order to capture it correctly. The setup and hold times determine the ideal strobe position within the sampling window, as shown: Bit Time 0.5 x TCCS RSKM Sampling Window RSKM 0.5 x TCCS RSKM			
S	Single-ended voltage referenced I/O standard	The JEDEC standard for SSTL and HSTL I/O defines both the AC and DC input signal values. The AC values indicate the voltage levels at which the receiver must meet its timing specifications. The DC values indicate the voltage levels at which the final logic state of the receiver is unambiguously defined. After the receiver input has crossed the AC value, the receiver changes to the new logic state. The new logic state is then maintained as long as the input stays beyond the DC threshold. This approach is intended to provide predictable receiver timing in the presence of input waveform ringing: <i>Single-Ended Voltage Referenced I/O Standard</i> 			
	t _C	High-speed receiver and transmitter input and output clock period.			
	TCCS (channel- to-channel-skew)	The timing difference between the fastest and slowest output edges, including t_{CO} variation and clock skew, across channels driven by the same PLL. The clock is included in the TCCS measurement (refer to the <i>Timing Diagram</i> figure under SW in this table).			
	touty	High-speed I/O block—Duty cycle on the high-speed transmitter output clock.			
т		Timing Unit Interval (TUI) The timing budget allowed for skew, propagation delays, and the data sampling window.			
		(TUI = 1/(receiver input clock frequency multiplication factor) = t_c/w)			
	t _{FALL}	Signal high-to-low transition time (80-20%)			
	t _{INCCJ}	Cycle-to-cycle jitter tolerance on the PLL clock input.			
	t _{outpj_i0}	Period jitter on the general purpose I/O driven by a PLL.			
	t _{outpj_dc}	Period jitter on the dedicated clock output driven by a PLL.			
	t _{RISE}	Signal low-to-high transition time (20-80%)			
U		_			

Letter	Subject	Definitions
	V _{CM(DC)}	DC common mode input voltage.
	V _{ICM}	Input common mode voltage—The common mode of the differential signal at the receiver.
	V _{ID}	Input differential voltage swing—The difference in voltage between the positive and complementary conductors of a differential transmission at the receiver.
	V _{DIF(AC)}	AC differential input voltage—Minimum AC input differential voltage required for switching.
	V _{DIF(DC)}	DC differential input voltage— Minimum DC input differential voltage required for switching.
	V _{IH}	Voltage input high—The minimum positive voltage applied to the input which is accepted by the device as a logic high.
	V _{IH(AC)}	High-level AC input voltage
	V _{IH(DC)}	High-level DC input voltage
V	V _{IL}	Voltage input low—The maximum positive voltage applied to the input which is accepted by the device as a logic low.
	V _{IL(AC)}	Low-level AC input voltage
	V _{IL(DC)}	Low-level DC input voltage
	V _{OCM}	Output common mode voltage—The common mode of the differential signal at the transmitter.
	V _{OD}	Output differential voltage swing—The difference in voltage between the positive and complementary conductors of a differential transmission at the transmitter.
	V _{SWING}	Differential input voltage
	V _X	Input differential cross point voltage
	V _{OX}	Output differential cross point voltage
W	W	High-speed I/O block—clock boost factor
X		
Y	—	—
Z		

Table 60. Glossary (Part 4 of 4)