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Intel - 5SGXMA4H2F35C3N Datasheet



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The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Obsolete
Number of LABs/CLBs	158500
Number of Logic Elements/Cells	420000
Total RAM Bits	37888000
Number of I/O	600
Number of Gates	-
Voltage - Supply	0.82V ~ 0.88V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	1152-BBGA, FCBGA
Supplier Device Package	1152-FBGA (35x35)
Purchase URL	https://www.e-xfl.com/product-detail/intel/5sgxma4h2f35c3n

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Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

Symbol	Description	Minimum	Maximum	Unit
V _{CCD_FPLL}	PLL digital power supply	-0.5	1.8	V
V _{CCA_FPLL}	PLL analog power supply	-0.5	3.4	V
VI	DC input voltage	-0.5	3.8	V
TJ	Operating junction temperature	-55	125	°C
T _{STG}	Storage temperature (No bias)	-65	150	°C
I _{OUT}	DC output current per pin	-25	40	mA

Table 3. Absolute Maximum Ratings for Stratix V Devices (Part 2 of 2)

Table 4 lists the absolute conditions for the transceiver power supply for Stratix V GX, GS, and GT devices.

Table 4. Transceiver Power Supply Absolute Conditions for Stratix V GX, GS, and GT Devices

Symbol	Description	Devices	Minimum	Maximum	Unit
V _{CCA_GXBL}	Transceiver channel PLL power supply (left side)	GX, GS, GT	-0.5	3.75	V
V _{CCA_GXBR}	Transceiver channel PLL power supply (right side)	GX, GS	-0.5	3.75	V
V _{CCA_GTBR}	Transceiver channel PLL power supply (right side)	GT	-0.5	3.75	V
V _{CCHIP_L}	Transceiver hard IP power supply (left side)	GX, GS, GT	-0.5	1.35	V
V _{CCHIP_R}	Transceiver hard IP power supply (right side)	GX, GS, GT	-0.5	1.35	V
V _{CCHSSI_L}	Transceiver PCS power supply (left side)	GX, GS, GT	-0.5	1.35	V
V _{CCHSSI_R}	Transceiver PCS power supply (right side)	GX, GS, GT	-0.5	1.35	V
V _{CCR_GXBL}	Receiver analog power supply (left side)	GX, GS, GT	-0.5	1.35	V
V _{CCR_GXBR}	Receiver analog power supply (right side)	GX, GS, GT	-0.5	1.35	V
V _{CCR_GTBR}	Receiver analog power supply for GT channels (right side)	GT	-0.5	1.35	V
V _{CCT_GXBL}	Transmitter analog power supply (left side)	GX, GS, GT	-0.5	1.35	V
V _{CCT_GXBR}	Transmitter analog power supply (right side)	GX, GS, GT	-0.5	1.35	V
V _{CCT_GTBR}	Transmitter analog power supply for GT channels (right side)	GT	-0.5	1.35	V
V _{CCL_GTBR}	Transmitter clock network power supply (right side)	GT	-0.5	1.35	V
V _{CCH_GXBL}	Transmitter output buffer power supply (left side)	GX, GS, GT	-0.5	1.8	V
V _{CCH_GXBR}	Transmitter output buffer power supply (right side)	GX, GS, GT	-0.5	1.8	V

Maximum Allowed Overshoot and Undershoot Voltage

During transitions, input signals may overshoot to the voltage shown in Table 5 and undershoot to -2.0 V for input currents less than 100 mA and periods shorter than 20 ns.

Table 5 lists the maximum allowed input overshoot voltage and the duration of the overshoot voltage as a percentage of device lifetime. The maximum allowed overshoot duration is specified as a percentage of high time over the lifetime of the device. A DC signal is equivalent to 100% of the duty cycle. For example, a signal that overshoots to 3.95 V can be at 3.95 V for only ~21% over the lifetime of the device; for a device lifetime of 10 years, the overshoot duration amounts to ~2 years.

Symbol	Description	Condition (V)	Overshoot Duration as % @ T _J = 100°C	Unit				
		3.8	100	%				
		3.85	64	%				
		3.9	36	%				
		3.95	21	%				
Vi (AC)	AC input voltage	4	12	%				
		4.05	7	%				
		4.1	4	%				
		4.15	2	%				
		4.2	1	%				

Table 5. Maximum Allowed Overshoot During Transitions

Figure 1. Stratix V Device Overshoot Duration



Symbol	Description	Condition	Min ⁽⁴⁾	Тур	Max ⁽⁴⁾	Unit
t _{RAMP}	Power supply ramp time	Standard POR	200 µs	_	100 ms	—
	Power supply ramp time	Fast POR	200 µs		4 ms	

Table 6. Recommended Operating Conditions for Stratix V Devices (Part 2 of 2)

Notes to Table 6:

(1) V_{CCPD} must be 2.5 V when V_{CCI0} is 2.5, 1.8, 1.5, 1.35, 1.25 or 1.2 V. V_{CCPD} must be 3.0 V when V_{CCI0} is 3.0 V.

(2) If you do not use the design security feature in Stratix V devices, connect V_{CCBAT} to a 1.2- to 3.0-V power supply. Stratix V power-on-reset (POR) circuitry monitors V_{CCBAT}. Stratix V devices will not exit POR if V_{CCBAT} stays at logic low.

(3) C2L and I2L can also be run at 0.90 V for legacy boards that were designed for the C2 and I2 speed grades.

(4) The power supply value describes the budget for the DC (static) power supply tolerance and does not include the dynamic tolerance requirements. Refer to the PDN tool for the additional budget for the dynamic tolerance requirements.

Table 7 lists the transceiver power supply recommended operating conditions for Stratix V GX, GS, and GT devices.

Table 7. Recommended Transceiver Power Supply Operating Conditions for Stratix V GX, GS, and GT Devices (Part 1 of 2)

Symbol	Description	Devices	Minimum ⁽⁴⁾	Typical	Maximum ⁽⁴⁾	Unit
V _{CCA GXBL}	Transceiver channel PLL power supply (left		2.85	3.0	3.15	V
(1), (3)	side)	un, us, ui	2.375	2.5	2.625	v
V _{CCA_GXBR}	Transceiver channel PLL power supply (right	CV CS	2.85	3.0	3.15	V
(1), (3)	side)	ux, us	2.375	2.5	2.625	v
V _{CCA_GTBR}	Transceiver channel PLL power supply (right side)	GT	2.85	3.0	3.15	V
	Transceiver hard IP power supply (left side; C1, C2, I2, and I3YY speed grades)	GX, GS, GT	0.87	0.9	0.93	V
V _{CCHIP_L}	Transceiver hard IP power supply (left side; C2L, C3, C4, I2L, I3, I3L, and I4 speed grades)	GX, GS, GT	0.82	0.85	0.88	V
V _{CCHIP_R}	Transceiver hard IP power supply (right side; C1, C2, I2, and I3YY speed grades)	GX, GS, GT	0.87	0.9	0.93	V
	Transceiver hard IP power supply (right side; C2L, C3, C4, I2L, I3, I3L, and I4 speed grades)	GX, GS, GT	0.82	0.85	0.88	V
	Transceiver PCS power supply (left side; C1, C2, I2, and I3YY speed grades)	GX, GS, GT	0.87	0.9	0.93	V
V _{CCHSSI_L}	Transceiver PCS power supply (left side; C2L, C3, C4, I2L, I3, I3L, and I4 speed grades)	GX, GS, GT	0.82	0.85	0.88	V
	Transceiver PCS power supply (right side; C1, C2, I2, and I3YY speed grades)	GX, GS, GT	0.87	0.9	0.93	V
V _{CCHSSI_R}	Transceiver PCS power supply (right side; C2L, C3, C4, I2L, I3, I3L, and I4 speed grades)	GX, GS, GT	0.82	0.85	0.88	V
			0.82	0.85	0.88	
V _{CCR_GXBL}	Receiver analog nower supply (left side)		0.87	0.90	0.93	v
V _{CCA_GTBR} V _{CCHIP_L} V _{CCHIP_R} V _{CCHSSI_L} V _{CCHSSI_R} V _{CCR_GXBL}	Therefore analog power supply (left Slue)	un, uo, ui	0.97	1.0	1.03	v
			1.03	1.05	1.07	

Table 8 shows the transceiver power supply voltage requirements for various conditions.

Table 8. Transceiver Power Supply Voltage Requirements

Conditions	Core Speed Grade	VCCR_GXB & VCCT_GXB ⁽²⁾	VCCA_GXB	VCCH_GXB	Unit
If BOTH of the following conditions are true:	A11	1.05			
■ Data rate > 10.3 Gbps.	All	1.00			
 DFE is used. 					
If ANY of the following conditions are true ⁽¹⁾ :			3.0		
 ATX PLL is used. 					
■ Data rate > 6.5Gbps.	All	1.0			
■ DFE (data rate ≤ 10.3 Gbps), AEQ, or EyeQ feature is used.				1.5	V
If ALL of the following	C1, C2, I2, and I3YY	0.90	2.5		
 ATX PLL is not used. 					
■ Data rate \leq 6.5Gbps.	C2L, C3, C4, I2L, I3, I3L, and I4	0.85	2.5		
 DFE, AEQ, and EyeQ are not used. 					

Notes to Table 8:

(1) Choose this power supply voltage requirement option if you plan to upgrade your design later with any of the listed conditions.

(2) If the VCCR_GXB and VCCT_GXB supplies are set to 1.0 V or 1.05 V, they cannot be shared with the VCC core supply. If the VCCR_GXB and VCCT_GXB are set to either 0.90 V or 0.85 V, they can be shared with the VCC core supply.

DC Characteristics

This section lists the supply current, I/O pin leakage current, input pin capacitance, on-chip termination tolerance, and hot socketing specifications.

Supply Current

Supply current is the current drawn from the respective power rails used for power budgeting. Use the Excel-based Early Power Estimator (EPE) to get supply current estimates for your design because these currents vary greatly with the resources you use.

For more information about power estimation tools, refer to the *PowerPlay Early Power Estimator User Guide* and the *PowerPlay Power Analysis* chapter in the *Quartus II Handbook*.

Symbol	Description	V _{CCIO} (V)	Typical	Unit	
dR/dT		3.0	0.189		
		2.5	0.208		
	OCT variation with temperature without recalibration	1.8	0.266	%/°C	
	without robalibration	1.5	0.273		
		1.2	0.317		

Table 13. OCT Variation after Power-Up Calibration for Stratix V Devices (Part 2 of 2)⁽¹⁾

Note to Table 13:

(1) Valid for a V_{CCIO} range of $\pm 5\%$ and a temperature range of 0° to 85°C.

Pin Capacitance

Table 14 lists the Stratix V device family pin capacitance.

Table 14. Pin Capacitance for Stratix V Devices

Symbol	Description	Value	Unit
CIOTB	Input capacitance on the top and bottom I/O pins	6	pF
C _{IOLR}	Input capacitance on the left and right I/O pins	6	рF
C _{OUTFB}	Input capacitance on dual-purpose clock output and feedback pins	6	pF

Hot Socketing

Table 15 lists the hot socketing specifications for Stratix V devices.

Symbol	Description	Maximum
I _{IOPIN (DC)}	DC current per I/O pin	300 μA
I _{IOPIN (AC)}	AC current per I/O pin	8 mA ⁽¹⁾
IXCVR-TX (DC)	DC current per transceiver transmitter pin	100 mA
IXCVR-RX (DC)	DC current per transceiver receiver pin	50 mA

Note to Table 15:

(1) The I/O ramp rate is 10 ns or more. For ramp rates faster than 10 ns, $|I_{10PIN}| = C dv/dt$, in which C is the I/O pin capacitance and dv/dt is the slew rate.

Symbol/	Conditions	Transceiver Speed Grade 1		Transceiver Speed Grade 2			Transceiver Speed Grade 3			Unit	
Description		Min	Тур	Max	Min	Тур	Max	Min	Тур	Max	l
Reconfiguration clock (mgmt_clk_clk) frequency	_	100		125	100		125	100	_	125	MHz
Receiver	Receiver										
Supported I/O Standards	_	1.4-V PCML, 1.5-V PCML, 2.5-V PCML, LVPECL, and LVDS									
Data rate (Standard PCS) (9), (23)	_	600	_	12200	600	_	12200	600	_	8500/ 10312.5 (24)	Mbps
Data rate (10G PCS) ^{(9),} ⁽²³⁾	_	600	_	14100	600	_	12500	600	_	8500/ 10312.5 (24)	Mbps
Absolute V _{MAX} for a receiver pin ⁽⁵⁾	_	_	_	1.2	_	_	1.2	_	_	1.2	V
Absolute V _{MIN} for a receiver pin	_	-0.4	_	_	-0.4	_	_	-0.4	_	_	V
Maximum peak- to-peak differential input voltage V _{ID} (diff p- p) before device configuration ⁽²²⁾	_	_	_	1.6	_	_	1.6	_		1.6	V
Maximum peak- to-peak	V _{CCR_GXB} = 1.0 V/1.05 V (V _{ICM} = 0.70 V)	_	_	2.0	_	_	2.0		_	2.0	V
voltage V_{ID} (diff p- p) after device configuration ⁽¹⁸⁾ .	V _{CCR_GXB} = 0.90 V (V _{ICM} = 0.6 V)			2.4			2.4			2.4	V
(22)	$V_{CCR_GXB} = 0.85 V$ (V _{ICM} = 0.6 V)			2.4			2.4		_	2.4	V
Minimum differential eye opening at receiver serial input pins ^{(6), (22),} (27)	_	85			85			85	_	_	mV

Table 23. Transceiver Specifications for Stratix V GX and GS Devices ⁽¹⁾ (Part 3 of 7)

Table 26 shows the approximate maximum data rate using the 10G PCS.

Mada (2)	Transceiver	PMA Width	64	40	40	40	32	32	
mode ""	Speed Grade	PCS Width	64	66/67	50	40	64/66/67	32	
	1	C1, C2, C2L, I2, I2L core speed grade	14.1	14.1	10.69	14.1	13.6	13.6	
2	2	C1, C2, C2L, I2, I2L core speed grade	12.5	12.5	10.69	12.5	12.5	12.5	
	L	C3, I3, I3L core speed grade	12.5	12.5	10.69	12.5	10.88	10.88	
FIFO or Register	2	C1, C2, C2L, I2, I2L core speed grade							
		C3, I3, I3L core speed grade	8.5 Gbps						
	5	C4, I4 core speed grade							
		I3YY core speed grade			10.312	25 Gbps			

Notes to Table 26:

(1) The maximum data rate is in Gbps.

(2) The Phase Compensation FIFO can be configured in FIFO mode or register mode. In the FIFO mode, the pointers are not fixed, and the latency can vary. In the register mode the pointers are fixed for low latency.





Figure 3 shows the Stratix V AC gain curves for GX channels.

Figure 3. AC Gain Curves for GX Channels (full bandwidth)

Stratix V GT devices contain both GX and GT channels. All transceiver specifications for the GX channels not listed in Table 28 are the same as those listed in Table 23.

Table 28 lists the Stratix V GT transceiver specifications.

Figure 4 shows the differential transmitter output waveform.





Figure 5 shows the Stratix V AC gain curves for GT channels.

Figure 5. AC Gain Curves for GT Channels

Table 31. PLL Specifications for Stratix V Devices (Part 3 of 3)

Symbol	Parameter	Min	Тур	Max	Unit
f _{RES}	Resolution of VCO frequency ($f_{INPFD} = 100 \text{ MHz}$)	390625	5.96	0.023	Hz

Notes to Table 31:

(1) This specification is limited in the Quartus II software by the I/O maximum frequency. The maximum I/O frequency is different for each I/O standard.

(2) This specification is limited by the lower of the two: I/O f_{MAX} or f_{OUT} of the PLL.

- (3) A high input jitter directly affects the PLL output jitter. To have low PLL output clock jitter, you must provide a clean clock source < 120 ps.
- (4) f_{REF} is fIN/N when N = 1.
- (5) Peak-to-peak jitter with a probability level of 10⁻¹² (14 sigma, 99.9999999974404% confidence level). The output jitter specification applies to the intrinsic jitter of the PLL, when an input jitter of 30 ps is applied. The external memory interface clock output jitter specifications use a different measurement method and are available in Table 44 on page 52.
- (6) The cascaded PLL specification is only applicable with the following condition: a. Upstream PLL: 0.59Mhz ≤ Upstream PLL BW < 1 MHz b. Downstream PLL: Downstream PLL BW > 2 MHz
- (7) High bandwidth PLL settings are not supported in external feedback mode.
- (8) The external memory interface clock output jitter specifications use a different measurement method, which is available in Table 42 on page 50.
- (9) The VCO frequency reported by the Quartus II software in the PLL Usage Summary section of the compilation report takes into consideration the VCO post-scale counter K value. Therefore, if the counter K has a value of 2, the frequency reported can be lower than the f_{VCO} specification.
- (10) This specification only covers fractional PLL for low bandwidth. The f_{VCO} for fractional value range 0.05 0.95 must be \geq 1000 MHz, while f_{VCO} for fractional value range 0.20 0.80 must be \geq 1200 MHz.
- (11) This specification only covered fractional PLL for low bandwidth. The f_{VC0} for fractional value range 0.05-0.95 must be \geq 1000 MHz.
- (12) This specification only covered fractional PLL for low bandwidth. The f_{VC0} for fractional value range 0.20-0.80 must be \geq 1200 MHz.

DSP Block Specifications

Table 32 lists the Stratix V DSP block performance specifications.

			F	Peformanc	e				
Mode	C1	C2, C2L	12, 12L	C3	13, 13L, 13YY	C4	14	Unit	
	Modes using one DSP								
Three 9 x 9	600	600	600	480	480	420	420	MHz	
One 18 x 18	600	600	600	480	480	420	400	MHz	
Two partial 18 x 18 (or 16 x 16)	600	600	600	480	480	420	400	MHz	
One 27 x 27	500	500	500	400	400	350	350	MHz	
One 36 x 18	500	500	500	400	400	350	350	MHz	
One sum of two 18 x 18(One sum of 2 16 x 16)	500	500	500	400	400	350	350	MHz	
One sum of square	500	500	500	400	400	350	350	MHz	
One 18 x 18 plus 36 (a x b) + c	500	500	500	400	400	350	350	MHz	
		Modes u	sing two l	DSPs					
Three 18 x 18	500	500	500	400	400	350	350	MHz	
One sum of four 18 x 18	475	475	475	380	380	300	300	MHz	
One sum of two 27 x 27	465	465	450	380	380	300	290	MHz	
One sum of two 36 x 18	475	475	475	380	380	300	300	MHz	
One complex 18 x 18	500	500	500	400	400	350	350	MHz	
One 36 x 36	475	475	475	380	380	300	300	MHz	

Table 32. Block Performance Specifications for Stratix V DSP Devices (Part 1 of 2)

		Resour	ces Used			Pe	erforman	ce			
Memory	Mode	ALUTS	Memory	C1	C2, C2L	C3	C4	12, 12L	13, 13L, 13YY	14	Unit
	Single-port, all supported widths	0	1	700	700	650	550	700	500	450	MHz
	Simple dual-port, all supported widths	0	1	700	700	650	550	700	500	450	MHz
	Simple dual-port with the read-during-write option set to Old Data , all supported widths	0	1	525	525	455	400	525	455	400	MHz
M20K Block	Simple dual-port with ECC enabled, 512 × 32	0	1	450	450	400	350	450	400	350	MHz
	Simple dual-port with ECC and optional pipeline registers enabled, 512 × 32	0	1	600	600	500	450	600	500	450	MHz
	True dual port, all supported widths	0	1	700	700	650	550	700	500	450	MHz
	ROM, all supported widths	0	1	700	700	650	550	700	500	450	MHz

Table 33. Memory Block Performance Specifications for Stratix V Devices ^{(1), (2)} (Part 2 of 2)

Notes to Table 33:

(1) To achieve the maximum memory block performance, use a memory block clock that comes through global clock routing from an on-chip PLL set to **50**% output duty cycle. Use the Quartus II software to report timing for this and other memory block clocking schemes.

(2) When you use the error detection cyclical redundancy check (CRC) feature, there is no degradation in F_{MAX}.

(3) The F_{MAX} specification is only achievable with Fitter options, MLAB Implementation In 16-Bit Deep Mode enabled.

Temperature Sensing Diode Specifications

Table 34 lists the internal TSD specification.

Table 34. Internal Temperature Sensing Diode Specification

Temperature Range	Accuracy	Offset Calibrated Option	Sampling Rate	Conversion Time	Resolution	Minimum Resolution with no Missing Codes
-40°C to 100°C	±8°C	No	1 MHz, 500 KHz	< 100 ms	8 bits	8 bits

Table 35 lists the specifications for the Stratix V external temperature sensing diode.

Table 35.	External	Temperature	Sensing D	iode Speci	fications f	for Stratix V	Devices
-----------	----------	-------------	-----------	------------	-------------	---------------	---------

Description	Min	Тур	Max	Unit
I _{bias} , diode source current	8	—	200	μA
V _{bias,} voltage across diode	0.3	—	0.9	V
Series resistance	—	_	< 1	Ω
Diode ideality factor	1.006	1.008	1.010	_

Symbol	Conditions		C1		C2,	C2L, I	2, I2L	C3,	13, 131	., I3YY	C4,I4			Unit
Symbol	Conditions	Min	Тур	Max	Min	Тур	Max	Min	Тур	Max	Min	Тур	Max	UIIIL
Transmitter														
True Differential I/O Standards	SERDES factor J = 3 to 10 ⁽⁹⁾ , ⁽¹¹⁾ , ⁽¹²⁾ , ⁽¹³⁾ , ⁽¹⁴⁾ , ⁽¹⁵⁾ , ⁽¹⁶⁾	(6)	_	1600	(6)	_	1434	(6)	_	1250	(6)	_	1050	Mbps
	SERDES factor J ≥ 4 LVDS TX with DPA (12), (14), (15), (16)	(6)		1600	(6)		1600	(6)		1600	(6)	_	1250	Mbps
- f _{HSDR} (data rate)	SERDES factor J = 2, uses DDR Registers	(6)	_	(7)	(6)	_	(7)	(6)	_	(7)	(6)		(7)	Mbps
	SERDES factor J = 1, uses SDR Register	(6)	_	(7)	(6)	_	(7)	(6)	_	(7)	(6)	_	(7)	Mbps
Emulated Differential I/O Standards with Three External Output Resistor Networks - f _{HSDR} (data rate) ⁽¹⁰⁾	SERDES factor J = 4 to 10 $(^{17})$	(6)		1100	(6)		1100	(6)		840	(6)		840	Mbps
t _{x Jitter} - True Differential	Total Jitter for Data Rate 600 Mbps - 1.25 Gbps		_	160		_	160		_	160			160	ps
I/O Standards	Total Jitter for Data Rate < 600 Mbps		_	0.1			0.1			0.1		_	0.1	UI
t _{x Jitter} - Emulated Differential I/O Standards	Total Jitter for Data Rate 600 Mbps - 1.25 Gbps	_	_	300	_	_	300	_	_	300	_		325	ps
with Three External Output Resistor Network	Total Jitter for Data Rate < 600 Mbps	_	_	0.2	_	_	0.2	_	_	0.2	_	_	0.25	UI

Table 36. High-Speed I/O Specifications for Stratix V Devices (1), (2) (Part 2 of 4)

Symbol	Conditiono		C1		C2,	C2, C2L, I2, I2L		C3, I3, I3L, I3YY		C4,14			Unit	
əyiinuu	Conditions	Min	Тур	Max	Min	Тур	Max	Min	Тур	Max	Min	Тур	Max	Umt
	SERDES factor J = 3 to 10	(6)		(8)	(6)	_	(8)	(6)		(8)	(6)		(8)	Mbps
f _{HSDR} (data rate)	SERDES factor J = 2, uses DDR Registers	(6)		(7)	(6)	_	(7)	(6)	_	(7)	(6)		(7)	Mbps
	SERDES factor J = 1, uses SDR Register	(6)	_	(7)	(6)	_	(7)	(6)	_	(7)	(6)	_	(7)	Mbps
DPA Mode														
DPA run length	_			1000 0		_	1000 0	_		1000 0	_		1000 0	UI
Soft CDR mode														
Soft-CDR PPM tolerance	_	_	_	300	_	_	300	_	_	300	_	_	300	± PPM
Non DPA Mode														
Sampling Window	_			300			300			300			300	ps

Table 36. High-Speed I/O Specifications for Stratix V Devices (1), (2) (Part 4 of 4)

Notes to Table 36:

(1) When J = 3 to 10, use the serializer/deserializer (SERDES) block.

(2) When J = 1 or 2, bypass the SERDES block.

(3) This only applies to DPA and soft-CDR modes.

(4) Clock Boost Factor (W) is the ratio between the input data rate to the input clock rate.

(5) This is achieved by using the **LVDS** clock network.

(6) The minimum specification depends on the clock source (for example, the PLL and clock pin) and the clock routing resource (global, regional, or local) that you use. The I/O differential buffer and input register do not have a minimum toggle rate.

(7) The maximum ideal frequency is the SERDES factor (J) x the PLL maximum output frequency (fOUT) provided you can close the design timing and the signal integrity simulation is clean.

(8) You can estimate the achievable maximum data rate for non-DPA mode by performing link timing closure analysis. You must consider the board skew margin, transmitter delay margin, and receiver sampling margin to determine the maximum data rate supported.

(9) If the receiver with DPA enabled and transmitter are using shared PLLs, the minimum data rate is 150 Mbps.

(10) You must calculate the leftover timing margin in the receiver by performing link timing closure analysis. You must consider the board skew margin, transmitter channel-to-channel skew, and receiver sampling margin to determine leftover timing margin.

(11) The F_{MAX} specification is based on the fast clock used for serial data. The interface F_{MAX} is also dependent on the parallel clock domain which is design-dependent and requires timing analysis.

(12) Stratix V RX LVDS will need DPA. For Stratix V TX LVDS, the receiver side component must have DPA.

(13) Stratix V LVDS serialization and de-serialization factor needs to be x4 and above.

(14) Requires package skew compensation with PCB trace length.

(15) Do not mix single-ended I/O buffer within LVDS I/O bank.

(16) Chip-to-chip communication only with a maximum load of 5 pF.

(17) When using True LVDS RX channels for emulated LVDS TX channel, only serialization factors 1 and 2 are supported.

Figure 7 shows the dynamic phase alignment (DPA) lock time specifications with the DPA PLL calibration option enabled.

Figure 7. DPA Lock Time Specification with DPA PLL Calibration Enabled

rx_reset			
rx_dpa_locked			<u> </u>
			-

Table 37 lists the DPA lock time specifications for Stratix V devices.

Table 37. DPA Lock Time Specifications for Stratix V GX Devices Only (1), (2), (3)

Standard	Training Pattern	Number of Data Transitions in One Repetition of the Training Pattern	Number of Repetitions per 256 Data Transitions ⁽⁴⁾	Maximum
SPI-4	00000000001111111111	2	128	640 data transitions
Parallel Rapid I/O	00001111	2	128	640 data transitions
	10010000	4	64	640 data transitions
Miscellaneous	10101010	8	32	640 data transitions
Wiscenareous	01010101	8	32	640 data transitions

Notes to Table 37:

(1) The DPA lock time is for one channel.

(2) One data transition is defined as a 0-to-1 or 1-to-0 transition.

(3) The DPA lock time stated in this table applies to both commercial and industrial grade.

(4) This is the number of repetitions for the stated training pattern to achieve the 256 data transitions.

Figure 8 shows the **LVDS** soft-clock data recovery (CDR)/DPA sinusoidal jitter tolerance specification for a data rate \geq 1.25 Gbps. Table 38 lists the **LVDS** soft-CDR/DPA sinusoidal jitter tolerance specification for a data rate \geq 1.25 Gbps.





Duty Cycle Distortion (DCD) Specifications

Table 44 lists the worst-case DCD for Stratix V devices.

Table 44. Worst-Case DCD on Stratix V I/O Pins (1)

Symbol	C	1	C2, C2	L, 12, 12L	C3, I3, I3L, I3YY		C3, I3, I3L, I3YY C4,I4		Unit	
	Min	Max	Min	Max	Min	Max	Min	Max		
Output Duty Cycle	45	55	45	55	45	55	45	55	%	

Note to Table 44:

(1) The DCD numbers do not cover the core clock network.

Configuration Specification

POR Delay Specification

Power-on reset (POR) delay is defined as the delay between the time when all the power supplies monitored by the POR circuitry reach the minimum recommended operating voltage to the time when the nSTATUS is released high and your device is ready to begin configuration.



For more information about the POR delay, refer to the *Hot Socketing and Power-On Reset in Stratix V Devices* chapter.

Table 45 lists the fast and standard POR delay specification.

Table 45. Fast and Standard POR Delay Specification (1)

POR Delay	Minimum	Maximum		
Fast	4 ms	12 ms		
Standard	100 ms	300 ms		

Note to Table 45:

(1) You can select the POR delay based on the MSEL settings as described in the MSEL Pin Settings section of the "Configuration, Design Security, and Remote System Upgrades in Stratix V Devices" chapter.

JTAG Configuration Specifications

Table 46 lists the JTAG timing parameters and values for Stratix V devices.

Table 46. JTAG Timing Parameters and Values for Stratix V Devices

Symbol	Description	Min	Max	Unit
t _{JCP}	TCK clock period ⁽²⁾	30		ns
t _{JCP}	TCK clock period ⁽²⁾	167	—	ns
t _{JCH}	TCK clock high time ⁽²⁾	14	—	ns
t _{JCL}	TCK clock low time ⁽²⁾	14		ns
t _{JPSU (TDI)}	TDI JTAG port setup time	2	—	ns
t _{JPSU (TMS)}	TMS JTAG port setup time	3	_	ns

Symbol	Description	Min	Max	Unit
t _{JPH}	JTAG port hold time	5	—	ns
t _{JPCO}	JTAG port clock to output	—	11 ⁽¹⁾	ns
t _{JPZX}	JTAG port high impedance to valid output	—	14 ⁽¹⁾	ns
t _{JPXZ}	JTAG port valid output to high impedance	—	14 ⁽¹⁾	ns

Table 46. JTAG Timing Parameters and Values for Stratix V Devices

Notes to Table 46:

(1) A 1 ns adder is required for each V_{CCI0} voltage step down from 3.0 V. For example, $t_{JPC0} = 12$ ns if V_{CCI0} of the TDO I/O bank = 2.5 V, or 13 ns if it equals 1.8 V.

(2) The minimum TCK clock period is 167 ns if VCCBAT is within the range 1.2V-1.5V when you perform the volatile key programming.

Raw Binary File Size

For the POR delay specification, refer to the "POR Delay Specification" section of the "Configuration, Design Security, and Remote System Upgrades in Stratix V Devices".

Table 47 lists the uncompressed raw binary file (.rbf) sizes for Stratix V devices.

Family	Device	Package	Configuration .rbf Size (bits)	IOCSR .rbf Size (bits) ^{(4), (5)}	
	500742	H35, F40, F35 ⁽²⁾	213,798,880	562,392	
	JOUNAS	H29, F35 ⁽³⁾	137,598,880	564,504	
	5SGXA4	—	213,798,880	563,672	
	5SGXA5	—	269,979,008	562,392	
	5SGXA7	—	269,979,008	562,392	
Stratix V GX	5SGXA9	—	342,742,976	700,888	
	5SGXAB	—	342,742,976	700,888	
	5SGXB5	—	270,528,640	584,344	
	5SGXB6	—	270,528,640	584,344	
	5SGXB9	_	342,742,976	700,888	
	5SGXBB	—	342,742,976	700,888	
Stratix V CT	5SGTC5	—	269,979,008	562,392	
	5SGTC7	_	269,979,008	562,392	
	5SGSD3	—	137,598,880	564,504	
	590904	F1517	213,798,880	563,672	
Stratix V GS	J303D4	_	137,598,880	564,504	
	5SGSD5		213,798,880	563,672	
	5SGSD6		293,441,888	565,528	
	5SGSD8	—	293,441,888	565,528	

Table 47. Uncompressed .rbf Sizes for Stratix V Devices

FPP Configuration Timing when DCLK-to-DATA [] = 1

Figure 12 shows the timing waveform for FPP configuration when using a MAX II or MAX V device as an external host. This waveform shows timing when the DCLK-to-DATA[] ratio is 1.





Notes to Figure 12:

- (1) Use this timing waveform when the DCLK-to-DATA [] ratio is 1.
- (2) The beginning of this waveform shows the device in user mode. In user mode, nCONFIG, nSTATUS, and CONF_DONE are at logic-high levels. When nCONFIG is pulled low, a reconfiguration cycle begins.
- (3) After power-up, the Stratix V device holds nstatus low for the time of the POR delay.
- (4) After power-up, before and during configuration, CONF_DONE is low.
- (5) Do not leave DCLK floating after configuration. DCLK is ignored after configuration is complete. It can toggle high or low if required.
- (6) For FPP ×16, use DATA [15..0]. For FPP ×8, use DATA [7..0]. DATA [31..0] are available as a user I/O pin after configuration. The state of this pin depends on the dual-purpose pin settings.
- (7) To ensure a successful configuration, send the entire configuration data to the Stratix V device. CONF_DONE is released high when the Stratix V device receives all the configuration data successfully. After CONF_DONE goes high, send two additional falling edges on DCLK to begin initialization and enter user mode.
- (8) After the option bit to enable the INIT_DONE pin is configured into the device, the INIT DONE goes low.

Symbol	Parameter	Minimum	Maximum	Units
t _{CD2UM}	CONF_DONE high to user mode (3)	175	437	μS
t _{CD2CU}	CONF_DONE high to CLKUSR enabled	4 × maximum DCLK period	_	—
t _{CD2UMC}	CONF_DONE high to user mode with CLKUSR option on	t _{cd2cu} + (8576 × clkusr period)	_	—

Table 53. AS Timing Parameters for AS \times 1 and AS \times 4 Configurations in Stratix V Devices ^{(1), (2)} (Part 2 of 2)

Notes to Table 53:

(1) The minimum and maximum numbers apply only if you choose the internal oscillator as the clock source for initializing the device.

(2) t_{CF2CD}, t_{CF2ST0}, t_{CF2ST0}, t_{CF6}, t_{STATUS}, and t_{CF2ST1} timing parameters are identical to the timing parameters for PS mode listed in Table 54 on page 63.

(3) To enable the CLKUSR pin as the initialization clock source and to obtain the maximum frequency specification on this pin, refer to the Initialization section of the "Configuration, Design Security, and Remote System Upgrades in Stratix V Devices" chapter.

Passive Serial Configuration Timing

Figure 15 shows the timing waveform for a passive serial (PS) configuration when using a MAX II device, MAX V device, or microprocessor as an external host.

Figure 15. PS Configuration Timing Waveform ⁽¹⁾



Notes to Figure 15:

- (1) The beginning of this waveform shows the device in user mode. In user mode, nCONFIG, nSTATUS, and CONF_DONE are at logic high levels. When nCONFIG is pulled low, a reconfiguration cycle begins.
- (2) After power-up, the Stratix V device holds nSTATUS low for the time of the POR delay.
- (3) After power-up, before and during configuration, CONF DONE is low.
- (4) Do not leave DCLK floating after configuration. You can drive it high or low, whichever is more convenient.
- (5) DATAO is available as a user I/O pin after configuration. The state of this pin depends on the dual-purpose pin settings in the **Device and Pins Option**.
- (6) To ensure a successful configuration, send the entire configuration data to the Stratix V device. CONF_DONE is released high after the Stratix V device receives all the configuration data successfully. After CONF_DONE goes high, send two additional falling edges on DCLK to begin initialization and enter user mode.
- (7) After the option bit to enable the INIT DONE pin is configured into the device, the INIT DONE goes low.

Table 54 lists the PS configuration timing parameters for Stratix V devices.

Table 54. PS Timing Parameters for Stratix V Devices

Symbol	Parameter	Minimum	Maximum	Units
t _{CF2CD}	nCONFIG low to CONF_DONE low	—	600	ns
t _{CF2ST0}	nCONFIG low to nSTATUS low	—	600	ns
t _{CFG}	nCONFIG low pulse width	2	—	μS
t _{status}	nSTATUS low pulse width	268	1,506 ⁽¹⁾	μS
t _{CF2ST1}	nCONFIG high to nSTATUS high	—	1,506 ⁽²⁾	μS
t _{CF2CK} (5)	nCONFIG high to first rising edge on DCLK	1,506	—	μS
t _{ST2CK} (5)	nSTATUS high to first rising edge of DCLK	2	—	μS
t _{DSU}	DATA[] setup time before rising edge on DCLK	5.5	—	ns
t _{DH}	DATA [] hold time after rising edge on DCLK	0	—	ns
t _{CH}	DCLK high time	$0.45\times 1/f_{MAX}$	—	S
t _{CL}	DCLK low time	$0.45\times 1/f_{MAX}$	—	S
t _{CLK}	DCLK period	1/f _{MAX}	—	S
f _{MAX}	DCLK frequency	—	125	MHz
t _{CD2UM}	CONF_DONE high to user mode ⁽³⁾	175	437	μS
t _{CD2CU}	CONF_DONE high to CLKUSR enabled	4 × maximum DCLK period	_	_
t _{cd2UMC}	CONF_DONE high to user mode with CLKUSR option on	t_{CD2CU} + (8576 × CLKUSR period) ⁽⁴⁾	_	_

Notes to Table 54:

(1) This value is applicable if you do not delay configuration by extending the nCONFIG or nSTATUS low pulse width.

(2) This value is applicable if you do not delay configuration by externally holding the nSTATUS low.

(3) The minimum and maximum numbers apply only if you choose the internal oscillator as the clock source for initializing the device.

(4) To enable the CLKUSR pin as the initialization clock source and to obtain the maximum frequency specification on these pins, refer to the "Initialization" section.

(5) If nSTATUS is monitored, follow the t_{ST2CK} specification. If nSTATUS is not monitored, follow the t_{CF2CK} specification.

Initialization

Table 55 lists the initialization clock source option, the applicable configuration schemes, and the maximum frequency.

Table 55.	Initialization	Clock Source	e Option	and the	Maximum	Frequency

Initialization Clock Source	Configuration Schemes	Maximum Frequency	Minimum Number of Clock Cycles ⁽¹⁾
Internal Oscillator	AS, PS, FPP	12.5 MHz	
CLKUSR	AS, PS, FPP ⁽²⁾	125 MHz	8576
DCLK	PS, FPP	125 MHz	

Notes to Table 55:

(1) The minimum number of clock cycles required for device initialization.

(2) To enable CLKUSR as the initialization clock source, turn on the Enable user-supplied start-up clock (CLKUSR) option in the Quartus II software from the General panel of the Device and Pin Options dialog box.

Parameter Available (1) Settings	Availabla	Min	Fast Model		Slow Model							
	Settings	0ffset (2)	Industrial	Commercial	C1	C2	C3	C4	12	13, 13YY	14	Unit
D3	8	0	1.587	1.699	2.793	2.793	2.992	3.192	2.811	3.047	3.257	ns
D4	64	0	0.464	0.492	0.838	0.838	0.924	1.011	0.843	0.920	1.006	ns
D5	64	0	0.464	0.493	0.838	0.838	0.924	1.011	0.844	0.921	1.006	ns
D6	32	0	0.229	0.244	0.415	0.415	0.458	0.503	0.418	0.456	0.499	ns

Table 58.	IOE Pro	grammable De	lay for	Stratix V	V Devices	(Part 2 of 2)
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Notes to Table 58:

(1) You can set this value in the Quartus II software by selecting D1, D2, D3, D5, and D6 in the Assignment Name column of Assignment Editor.

(2) Minimum offset does not include the intrinsic delay.

Programmable Output Buffer Delay

Table 59 lists the delay chain settings that control the rising and falling edge delays of the output buffer. The default delay is 0 ps.

Symbol	Parameter	Typical	Unit
D _{outbuf}	Rising and/or falling edge delay	0 (default)	ps
		25	ps
		50	ps
		75	ps

Note to Table 59:

(1) You can set the programmable output buffer delay in the Quartus II software by setting the Output Buffer Delay Control assignment to either positive, negative, or both edges, with the specific values stated here (in ps) for the Output Buffer Delay assignment.

Glossary

Table 60 lists the glossary for this chapter.

Table 60. Glossary (Part 1 of 4)

Letter	Subject	Definitions	
Α			
В	—	—	
С			
D	—	_	
E	—	_	
F	f _{HSCLK}	Left and right PLL input clock frequency.	
	f _{HSDR}	High-speed I/O block—Maximum and minimum LVDS data transfer rate (f _{HSDR} = 1/TUI), non-DPA.	
	f _{hsdrdpa}	High-speed I/O block—Maximum and minimum LVDS data transfer rate (f _{HSDRDPA} = 1/TUI), DPA.	