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Intel - 5SGXMA4K1F35C1N Datasheet



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The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Obsolete
Number of LABs/CLBs	158500
Number of Logic Elements/Cells	420000
Total RAM Bits	37888000
Number of I/O	600
Number of Gates	-
Voltage - Supply	0.87V ~ 0.93V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	1152-BBGA, FCBGA
Supplier Device Package	1152-FBGA (35x35)
Purchase URL	https://www.e-xfl.com/product-detail/intel/5sgxma4k1f35c1n

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This section lists the functional operating limits for the AC and DC parameters for Stratix V devices. Table 6 lists the steady-state voltage and current values expected from Stratix V devices. Power supply ramps must all be strictly monotonic, without plateaus.

Table 6. Recommended Operating Conditions for Stratix V Devices (Part 1 of 2)

Symbol	Description	Condition	Min ⁽⁴⁾	Тур	Max ⁽⁴⁾	Unit		
	Core voltage and periphery circuitry power supply (C1, C2, I2, and I3YY speed grades)	_	0.87	0.9	0.93	V		
V _{CC}	Core voltage and periphery circuitry power supply (C2L, C3, C4, I2L, I3, I3L, and I4 speed grades) ⁽³⁾		0.82	0.85	0.88	V		
V _{CCPT}	Power supply for programmable power technology	_	1.45	1.50	1.55	V		
V _{CC_AUX}	Auxiliary supply for the programmable power technology		2.375	2.5	2.625	V		
VI (1)	I/O pre-driver (3.0 V) power supply	_	2.85	3.0	3.15	V V		
VCCPD	I/O pre-driver (2.5 V) power supply		2.375	2.5	2.625	V		
	I/O buffers (3.0 V) power supply	_	2.85	3.0	3.15	V		
	I/O buffers (2.5 V) power supply		2.375	2.5	2.625	V		
V _{CC} Image: Second state V _{CCPT} Image: Second state V _{CCPD} (1) Image: Second state V _{CCPGM} Image: Second state V _{CCD_FPLL} Image: Second state V _{CCBAT} (2) Image: Second state V _I Image: Second state V _I Image: Second state V _I Image: Second state T _J Image: Second state	I/O buffers (1.8 V) power supply	_	1.71	1.8	1.89	V		
	I/O buffers (1.5 V) power supply	_	1.425	1.5	1.575	V		
	I/O buffers (1.35 V) power supply		1.283	1.35	1.45	V		
	I/O buffers (1.25 V) power supply	_	1.19	1.25	1.31	V		
	I/O buffers (1.2 V) power supply	Condition Min (4) Typ Max (4) 0.87 0.9 0.93 0.82 0.85 0.88 1.45 1.50 1.55 2.375 2.5 2.625 2.375 2.5 2.625 2.85 3.0 3.15 2.85 3.0 3.15 2.375 2.5 2.625 2.375 2.5 2.625 2.375 2.5 2.625 2.375 2.5 2.625 2.375 2.5 2.625 1.71 1.8 1.89 1.71 1.8 1.89 1.425 1.5 1.55 1.71 1.8 1.89 2.375 2.5 2.625 1.71 1.8 1.89	1.26	V				
	Configuration pins (3.0 V) power supply		2.85	3.0	3.15	V		
V _{CCPGM}	Configuration pins (2.5 V) power supply	_	2.375	2.5	2.625	V		
	Configuration pins (1.8 V) power supply	-	1.71	1.8	1.89	V		
V _{CCA_FPLL}	PLL analog voltage regulator power supply		2.375	2.5	2.625	V V V V V V V V V V V V V V V V V V V		
V _{CCD_FPLL}	PLL digital voltage regulator power supply	-	1.45	1.5	1.55	V		
V _{CCBAT} (2)	Battery back-up power supply (For design security volatile key register)	_	1.2	_	3.0	V		
VI	DC input voltage	_	-0.5	—	3.6	V		
V ₀	Output voltage		0	_	V _{CCIO}	V		
т	Operating junction temperature	Commercial	0	—	85	°C		
IJ		Industrial	-40	_	100	°C		

Symbol	Description	Condition	Min ⁽⁴⁾	Тур	Max ⁽⁴⁾	Unit
t _{RAMP}	Power supply ramp time	Standard POR	200 µs	_	100 ms	—
		Fast POR	200 µs		4 ms	

Table 6. Recommended Operating Conditions for Stratix V Devices (Part 2 of 2)

Notes to Table 6:

(1) V_{CCPD} must be 2.5 V when V_{CCI0} is 2.5, 1.8, 1.5, 1.35, 1.25 or 1.2 V. V_{CCPD} must be 3.0 V when V_{CCI0} is 3.0 V.

(2) If you do not use the design security feature in Stratix V devices, connect V_{CCBAT} to a 1.2- to 3.0-V power supply. Stratix V power-on-reset (POR) circuitry monitors V_{CCBAT}. Stratix V devices will not exit POR if V_{CCBAT} stays at logic low.

(3) C2L and I2L can also be run at 0.90 V for legacy boards that were designed for the C2 and I2 speed grades.

(4) The power supply value describes the budget for the DC (static) power supply tolerance and does not include the dynamic tolerance requirements. Refer to the PDN tool for the additional budget for the dynamic tolerance requirements.

Table 7 lists the transceiver power supply recommended operating conditions for Stratix V GX, GS, and GT devices.

Table 7. Recommended Transceiver Power Supply Operating Conditions for Stratix V GX, GS, and GT Devices (Part 1 of 2)

Symbol	Description	Devices	Minimum ⁽⁴⁾	Typical	Maximum ⁽⁴⁾	Unit
V _{CCA GXBL}	Transceiver channel PLL power supply (left		2.85	3.0	3.15	V
(1), (3)	side)	un, us, ui	2.375	2.5	2.625	v
V _{CCA_GXBR}	Transceiver channel PLL power supply (right	CV CS	2.85	3.0	3.15	V
(1), (3)	side)	ux, us	2.375	2.5	2.625	v
V _{CCA_GTBR}	Transceiver channel PLL power supply (right side)	GT	2.85	3.0	3.15	V
	Transceiver hard IP power supply (left side; C1, C2, I2, and I3YY speed grades)	GX, GS, GT	0.87	0.9	0.93	V
V _{CCHIP_L}	Transceiver hard IP power supply (left side; C2L, C3, C4, I2L, I3, I3L, and I4 speed grades)	GX, GS, GT	0.82	0.85	0.88	V
	Transceiver hard IP power supply (right side; C1, C2, I2, and I3YY speed grades)	GX, GS, GT	0.87	0.9	0.93	V
V _{CCHIP_R}	Transceiver hard IP power supply (right side; C2L, C3, C4, I2L, I3, I3L, and I4 speed grades)	GX, GS, GT	0.82	0.85	0.88	V
	Transceiver PCS power supply (left side; C1, C2, I2, and I3YY speed grades)	GX, GS, GT	0.87	0.9	0.93	V
V _{CCHSSI_L}	Transceiver PCS power supply (left side; C2L, C3, C4, I2L, I3, I3L, and I4 speed grades)	GX, GS, GT	0.82	0.85	0.88	V
	Transceiver PCS power supply (right side; C1, C2, I2, and I3YY speed grades)	GX, GS, GT	0.87	0.9	0.93	V
V _{CCHSSI_R}	Transceiver PCS power supply (right side; C2L, C3, C4, I2L, I3, I3L, and I4 speed grades)	GX, GS, GT	0.82	0.85	0.88	V
			0.82	0.85	0.88	
V _{CCR_GXBL}	Receiver analog nower supply (left side)		0.87	0.90	0.93	v
(2) _	Therefore analog power supply (left Slue)	un, uo, ui	0.97	1.0	1.03	v
			1.03	1.05	1.07	

			Resistance Tolerance					
Symbol	Description	Conditions	C1	C2,I2	C3, I3, I3YY	C4, I4	Unit	
50-Ω R _S	Internal series termination without calibration (50- Ω setting)	$V_{CCIO} = 1.8$ and 1.5 V	±30	±30	±40	±40	%	
50-Ω R _S	Internal series termination without calibration (50- Ω setting)	V _{CCI0} = 1.2 V	±35	±35	±50	±50	%	
100-Ω R _D	Internal differential termination (100- Ω setting)	V _{CCPD} = 2.5 V	±25	±25	±25	±25	%	

Table 12. OCT Without Calibration Resistance Tolerance Specifications for Stratix V Devices (Part 2 of 2)

Calibration accuracy for the calibrated series and parallel OCTs are applicable at the moment of calibration. When voltage and temperature conditions change after calibration, the tolerance may change.

OCT calibration is automatically performed at power-up for OCT-enabled I/Os. Table 13 lists the OCT variation with temperature and voltage after power-up calibration. Use Table 13 to determine the OCT variation after power-up calibration and Equation 1 to determine the OCT variation without recalibration.

Equation 1. OCT Variation Without Recalibration for Stratix V Devices (1), (2), (3), (4), (5), (6)

$$R_{OCT} \,=\, R_{SCAL} \Big(1 + \langle \frac{dR}{dT} \times \Delta T \rangle \pm \langle \frac{dR}{dV} \times \Delta V \rangle \Big) \label{eq:ROCT}$$

Notes to Equation 1:

- (1) The R_{OCT} value shows the range of OCT resistance with the variation of temperature and V_{CCIO} .
- (2) R_{SCAL} is the OCT resistance value at power-up.
- (3) ΔT is the variation of temperature with respect to the temperature at power-up.
- (4) ΔV is the variation of voltage with respect to the V_{CCIO} at power-up.
- (5) dR/dT is the percentage change of R_{SCAL} with temperature.
- (6) dR/dV is the percentage change of $\mathsf{R}_{\mathsf{SCAL}}$ with voltage.

Table 13 lists the on-chip termination variation after power-up calibration.

Table 13. OCT Variation after Power-Up Calibration for Stratix V Devices (Part 1 of 2)
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Symbol	Description	V _{CCIO} (V)	Typical	Unit
		3.0	0.0297	
		2.5	0.0344	
dR/dV	OCT variation with voltage without recalibration	1.8	0.0499	%/mV
		1.5	0.0744	
		1.2	0.1241	

Internal Weak Pull-Up Resistor

Table 16 lists the weak pull-up resistor values for Stratix V devices.

Symbol	Description	V _{CCIO} Conditions (V) ⁽³⁾	Value ⁽⁴⁾	Unit
		3.0 ±5%	25	kΩ
R _{PU}		2.5 ±5%	kΩ	
	Value of the I/O pin pull-up resistor before	1.8 ±5%	25	kΩ
	and during configuration, as well as user mode if you enable the programmable	1.5 ±5%	25	kΩ
	pull-up resistor option.	1.35 ±5%	25	kΩ
		1.25 ±5%	25	kΩ
		1.2 ±5%	25	kΩ

Table 16. Internal Weak Pull-Up Resistor for Stratix V Devices (1), (2)

Notes to Table 16:

(1) All I/O pins have an option to enable the weak pull-up resistor except the configuration, test, and JTAG pins.

(2) The internal weak pull-down feature is only available for the JTAG TCK pin. The typical value for this internal weak pull-down resistor is approximately 25 k Ω .

- (3) The pin pull-up resistance values may be lower if an external source drives the pin higher than V_{CCIO}.
- (4) These specifications are valid with a $\pm 10\%$ tolerance to cover changes over PVT.

I/O Standard Specifications

Table 17 through Table 22 list the input voltage (V_{IH} and V_{IL}), output voltage (V_{OH} and V_{OL}), and current drive characteristics (I_{OH} and I_{OL}) for various I/O standards supported by Stratix V devices. These tables also show the Stratix V device family I/O standard specifications. The V_{OL} and V_{OH} values are valid at the corresponding I_{OH} and I_{OL}, respectively.

For an explanation of the terms used in Table 17 through Table 22, refer to "Glossary" on page 65. For tolerance calculations across all SSTL and HSTL I/O standards, refer to Altera knowledge base solution rd07262012_486.

I/O	V _{CCIO} (V)			V _{IL} (V)		V _{IH} (V)		V _{OL} (V)	V _{OH} (V)	I _{OL}	I _{oh}
Standard	Min	Тур	Max	Min	Max	Min	Max	Max	Min	(mA)	(mA)
LVTTL	2.85	3	3.15	-0.3	0.8	1.7	3.6	0.4	2.4	2	-2
LVCMOS	2.85	3	3.15	-0.3	0.8	1.7	3.6	0.2	$V_{CCIO} - 0.2$	0.1	-0.1
2.5 V	2.375	2.5	2.625	-0.3	0.7	1.7	3.6	0.4	2	1	-1
1.8 V	1.71	1.8	1.89	-0.3	0.35 * V _{CCIO}	0.65 * V _{CCIO}	V _{CCI0} + 0.3	0.45	V _{CCI0} – 0.45	2	-2
1.5 V	1.425	1.5	1.575	-0.3	0.35 * V _{CCI0}	0.65 * V _{CCI0}	V _{CCI0} + 0.3	0.25 * V _{CCIO}	0.75 * V _{CCIO}	2	-2
1.2 V	1.14	1.2	1.26	-0.3	0.35 * V _{CCI0}	0.65 * V _{CCI0}	V _{CCI0} + 0.3	0.25 * V _{CCIO}	0.75 * V _{CCIO}	2	-2

Table 17. Single-Ended I/O Standards for Stratix V Devices

I/O	V _{CC10} (V)			V _{DIF(DC)} (V)			V _{X(AC)} (V)			V _{CM(DC)} (V)	V _{DIF(AC)} (V)	
Standard	Min	Тур	Max	Min	Max	Min	Тур	Max	Min	Тур	Max	Min	Max
HSTL-12 Class I, II	1.14	1.2	1.26	0.16	V _{CCI0} + 0.3	_	0.5* V _{CCI0}	_	0.4* V _{CCIO}	0.5* V _{CCIO}	0.6* V _{CCI0}	0.3	V _{CCI0} + 0.48
HSUL-12	1.14	1.2	1.3	0.26	0.26	0.5*V _{CCI0} - 0.12	0.5* V _{CCI0}	0.5*V _{CCI0} + 0.12	0.4* V _{CCIO}	0.5* V _{CCIO}	0.6* V _{CCIO}	0.44	0.44

Table 21. Differential HSTL and HSUL I/O Standards for Stratix V Devices (Part 2 of 2)

Table 22. Differential I/O Standard Specifications for Stratix V Devices (7)

I/O	Vc	ссіо (V) ⁽¹⁰⁾ V _{ID} (mV) ⁽⁸⁾ V _{ICM(DC)} (V) V _{OI}		V _{ICM(DC)} (V)			_D (V) (6)	V _{OCM} (V) ⁽⁶⁾						
Standard	Min	Тур	Max	Min	Condition	Max	Min	Condition	Max	Min	Тур	Max	Min	Тур	Max
PCML	Trar	nsmitte	er, receiv transmi	ver, and itter, rec	input referer ceiver, and re	nce cloo eference	ck pins e clock	of the high-s I/O pin speci	peed tra fications	nsceiver , refer to	rs use o Table	the PC e 23 on	ML I/O s page 18	standard 3.	. For
2.5 V	2 375	25	2 625	100	V _{CM} =	_	0.05	D _{MAX} ≤ 700 Mbps	1.8	0.247	_	0.6	1.125	1.25	1.375
LVDS (1) 2.3	2.375 2.	2.5 2.0	2.025	100	1.25 V	_	1.05	D _{MAX} > 700 Mbps	1.55	0.247	_	0.6	1.125	1.25	1.375
BLVDS (5)	2.375	2.5	2.625	100	_	—	_	_	_	_	_	—	_	—	
RSDS (HIO) ⁽²⁾	2.375	2.5	2.625	100	V _{CM} = 1.25 V	_	0.3	_	1.4	0.1	0.2	0.6	0.5	1.2	1.4
Mini- LVDS (HIO) ⁽³⁾	2.375	2.5	2.625	200	_	600	0.4	_	1.325	0.25	_	0.6	1	1.2	1.4
LVPECL (4	_	_	_	300	_		0.6	D _{MAX} ≤ 700 Mbps	1.8	_	_	_	_	_	_
), (9)				300			1	D _{MAX} > 700 Mbps	1.6						

Notes to Table 22:

(1) For optimized LVDS receiver performance, the receiver voltage input range must be between 1.0 V to 1.6 V for data rates above 700 Mbps, and 0 V to 1.85 V for data rates below 700 Mbps.

(2) For optimized RSDS receiver performance, the receiver voltage input range must be between 0.25 V to 1.45 V.

(3) For optimized Mini-LVDS receiver performance, the receiver voltage input range must be between 0.3 V to 1.425 V.

- (4) For optimized LVPECL receiver performance, the receiver voltage input range must be between 0.85 V to 1.75 V for data rate above 700 Mbps and 0.45 V to 1.95 V for data rate below 700 Mbps.
- (5) There are no fixed V_{ICM} , V_{OD} , and V_{OCM} specifications for BLVDS. They depend on the system topology.
- (6) RL range: $90 \le RL \le 110 \Omega$.
- (7) The 1.4-V and 1.5-V PCML transceiver I/O standard specifications are described in "Transceiver Performance Specifications" on page 18.
- (8) The minimum VID value is applicable over the entire common mode range, VCM.
- (9) LVPECL is only supported on dedicated clock input pins.
- (10) Differential inputs are powered by VCCPD which requires 2.5 V.

Power Consumption

Altera offers two ways to estimate power consumption for a design—the Excel-based Early Power Estimator and the Quartus[®] II PowerPlay Power Analyzer feature.

Switching Characteristics

This section provides performance characteristics of the Stratix V core and periphery blocks.

These characteristics can be designated as Preliminary or Final.

- Preliminary characteristics are created using simulation results, process data, and other known parameters. The title of these tables show the designation as "Preliminary."
- Final numbers are based on actual silicon characterization and testing. The numbers reflect the actual performance of the device under worst-case silicon process, voltage, and junction temperature conditions. There are no designations on finalized tables.

Transceiver Performance Specifications

This section describes transceiver performance specifications.

Table 23 lists the Stratix V GX and GS transceiver specifications.

Table 23.	Transceiver 3	Specifications	for Stratix	V GX	and GS	Devices	(1)	(Part 1	nf 7	۱
Table 20.	TIANSUCIACI	opeonitionationa	IUI UIIAIIA	I UA	anu uu	DEVICES	• •	(1 61 6 1		

Symbol/	Conditions	Tra	nsceive Grade	r Speed 1	Trai	nsceive Grade	r Speed 2	Trai	isceive Grade	er Speed e 3	Unit
Description		Min	Тур	Max	Min	Тур	Max	Min	Тур	Max	
Reference Clock											
Supported I/O	Supported I/O Standards							/DS, and			
Standards	RX reference clock pin			1.4-V PCMI	L, 1.5-V	PCML,	2.5-V PCM	l, lvpe	CL, and	d LVDS	
Input Reference Clock Frequency (CMU PLL) ⁽⁸⁾	_	40		710	40	_	710	40	_	710	MHz
Input Reference Clock Frequency (ATX PLL) ⁽⁸⁾		100		710	100		710	100	_	710	MHz
Rise time	Measure at ±60 mV of differential signal ⁽²⁶⁾			400	_		400			400	ns
Fall time	Measure at ±60 mV of differential signal ⁽²⁶⁾		_	400	_		400			400	μσ
Duty cycle		45		55	45		55	45	—	55	%
Spread-spectrum modulating clock frequency	PCI Express® (PCIe [®])	30		33	30		33	30	_	33	kHz

Table 24 shows the maximum transmitter data rate for the clock network.

Table 24. Clock Network Maximum Data Rate Transmitter Specifications (1)

		ATX PLL			CMU PLL ⁽²⁾)	fPLL			
Clock Network	Non- bonded Mode (Gbps)	Bonded Mode (Gbps)	Channel Span	Non- bonded Mode (Gbps)	Bonded Mode (Gbps)	Channel Span	Non- bonded Mode (Gbps)	Bonded Mode (Gbps)	Channel Span	
x1 ⁽³⁾	14.1	_	6	12.5	_	6	3.125	—	3	
x6 ⁽³⁾	_	14.1	6	—	12.5	6	—	3.125	6	
x6 PLL Feedback ⁽⁴⁾	_	14.1	Side- wide	_	12.5	Side- wide	_	_	_	
xN (PCIe)	_	8.0	8	—	5.0	8	—	—	—	
VNI (Native DHV ID)	8.0	8.0	Up to 13 channels above and below PLL	7 00	7 00	Up to 13 channels above	3 125	3 125	Up to 13 channels above	
xN (Native PHY IP)	_	8.01 to 9.8304	Up to 7 channels above and below PLL	7.99	7.99	and below PLL	0.120	0.120	and below PLL	

Notes to Table 24:

(1) Valid data rates below the maximum specified in this table depend on the reference clock frequency and the PLL counter settings. Check the MegaWizard message during the PHY IP instantiation.

(2) ATX PLL is recommended at 8 Gbps and above data rates for improved jitter performance.

(3) Channel span is within a transceiver bank.

(4) Side-wide channel bonding is allowed up to the maximum supported by the PHY IP.

Table 27 shows the V_{OD} settings for the GX channel.

Symbol	V _{op} Setting	V _{od} Value (mV)	V _{op} Setting	V _{op} Value (mV)
	0 (1)	0	32	640
	1 (1)	20	33	660
	2 (1)	40	34	680
	3 (1)	60	35	700
	4 (1)	80	36	720
	5 ⁽¹⁾	100	37	740
	6	120	38	760
	7	140	39	780
	8	160	40	800
	9	180	41	820
	10	200	42	840
	11	220	43	860
	12	240	44	880
	13	260	45	900
	14	280	46	920
V_{0D} differential peak to peak	15	300	47	940
typical ⁽³⁾	16	320	48	960
	17	340	49	980
	18	360	50	1000
	19	380	51	1020
	20	400	52	1040
	21	420	53	1060
	22	440	54	1080
	23	460	55	1100
	24	480	56	1120
	25	500	57	1140
	26	520	58	1160
	27	540	59	1180
	28	560	60	1200
	29	580	61	1220
	30	600	62	1240
	31	620	63	1260

Table 27. Typical V_{0D} Setting for GX Channel, TX Termination = 100 $\Omega^{\left(2\right)}$

Note to Table 27:

(1) If TX termination resistance = 100Ω , this VOD setting is illegal.

(2) The tolerance is +/-20% for all VOD settings except for settings 2 and below.

(3) Refer to Figure 2.

Table 28. Transceiver Specifications for Stratix V GT Devices (Part 2 of 5)⁽¹⁾

Symbol/	Conditions	S	Transceive peed Grade	r 2	SI	Fransceive Deed Grade	r 3	Unit
Description		Min	Тур	Max	Min	Тур	Max	
	100 Hz	—	—	-70			-70	
Transmitter REFCLK	1 kHz		_	-90	_	_	-90	
Phase Noise (622	10 kHz		—	-100	_		-100	dBc/Hz
MHz) ⁽¹⁸⁾	100 kHz			-110			-110	
	\geq 1 MHz	—	—	-120	_	_	-120	
Transmitter REFCLK Phase Jitter (100 MHz) ⁽¹⁵⁾	10 kHz to 1.5 MHz (PCle)	_	_	3		_	3	ps (rms)
RREF ⁽¹⁷⁾	_	_	1800 ± 1%	—	_	1800 ± 1%	_	Ω
Transceiver Clocks								
fixedclk clock frequency	PCIe Receiver Detect	_	100 or 125	_	_	100 or 125	_	MHz
Reconfiguration clock (mgmt_clk_clk) frequency	_	100	_	125	100	_	125	MHz
Receiver	•							
Supported I/O Standards	_		1.4-V PCML	., 1.5-V PCMI	L, 2.5-V PCI	VIL, LVPEC	L, and LVDS	6
Data rate (Standard PCS) ⁽²¹⁾	GX channels	600	_	8500	600	_	8500	Mbps
Data rate (10G PCS) ⁽²¹⁾	GX channels	600	_	12,500	600	_	12,500	Mbps
Data rate	GT channels	19,600	—	28,050	19,600		25,780	Mbps
Absolute V _{MAX} for a receiver pin ⁽³⁾	GT channels	_	_	1.2	_	_	1.2	V
Absolute V _{MIN} for a receiver pin	GT channels	-0.4	_	—	-0.4	_	_	V
Maximum peak-to-peak	GT channels	_		1.6	—	_	1.6	V
differential input voltage V _{ID} (diff p-p) before device configuration ⁽²⁰⁾	GX channels				(8)			
	GT channels							
Maximum peak-to-peak differential input voltage V_{ID} (diff p-p) after device	V _{CCR_GTB} = 1.05 V (V _{ICM} = 0.65 V)	_	_	2.2	_	_	2.2	V
	GX channels		1	1 1	(8)			1
Minimum differential	GT channels	200	_	—	200		_	mV
eye opening at receiver serial input pins ⁽⁴⁾ , ⁽²⁰⁾	GX channels			·	(8)			

Table 28. Tra	nsceiver Specifi	cations for Stra	tix V GT Devices	(Part 5 of 5) ⁽¹⁾
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Symbol/ Description	Conditions	S	Transceivei peed Grade	2	ן Sr	Unit		
		Min	Тур	Max	Min	Тур	Max	
t _{pll_lock} ⁽¹⁴⁾	—	—	_	10	—	—	10	μs

Notes to Table 28:

- (1) Speed grades shown refer to the PMA Speed Grade in the device ordering code. The maximum data rate could be restricted by the Core/PCS speed grade. Contact your Altera Sales Representative for the maximum data rate specifications in each speed grade combination offered. For more information about device ordering codes, refer to the Stratix V Device Overview.
- (2) The reference clock common mode voltage is equal to the VCCR_GXB power supply level.
- (3) The device cannot tolerate prolonged operation at this absolute maximum.
- (4) The differential eye opening specification at the receiver input pins assumes that receiver equalization is disabled. If you enable receiver equalization, the receiver circuitry can tolerate a lower minimum eye opening, depending on the equalization level.
- (5) Refer to Figure 5 for the GT channel AC gain curves. The total effective AC gain is the AC gain minus the DC gain.
- (6) Refer to Figure 6 for the GT channel DC gain curves.
- (7) CFP2 optical modules require the host interface to have the receiver data pins differentially terminated with 100 Ω. The internal OCT feature is available after the Stratix V FPGA configuration is completed. Altera recommends that FPGA configuration is completed before inserting the optical module. Otherwise, minimize unnecessary removal and insertion with unconfigured devices.
- (8) Specifications for this parameter are the same as for Stratix V GX and GS devices. See Table 23 for specifications.
- (9) t_{1 TR} is the time required for the receive CDR to lock to the input reference clock frequency after coming out of reset.
- (10) t_{LTD} is time required for the receiver CDR to start recovering valid data after the rx is lockedtodata signal goes high.
- (11) t_{LTD_manual} is the time required for the receiver CDR to start recovering valid data after the rx_is_lockedtodata signal goes high when the CDR is functioning in the manual mode.
- (12) t_{LTR_LTD_manual} is the time the receiver CDR must be kept in lock to reference (LTR) mode after the rx_is_lockedtoref signal goes high when the CDR is functioning in the manual mode.
- (13) tpll_powerdown is the PLL powerdown minimum pulse width.
- (14) tpll lock is the time required for the transmitter CMU/ATX PLL to lock to the input reference clock frequency after coming out of reset.
- (15) To calculate the REFCLK rms phase jitter requirement for PCle at reference clock frequencies other than 100 MHz, use the following formula: REFCLK rms phase jitter at f(MHz) = REFCLK rms phase jitter at 100 MHz × 100/f.
- (16) The maximum peak to peak differential input voltage V_{ID} after device configuration is equal to 4 × (absolute V_{MAX} for receiver pin V_{ICM}).
- (17) For ES devices, RREF is 2000 $\Omega \pm 1\%$.
- (18) To calculate the REFCLK phase noise requirement at frequencies other than 622 MHz, use the following formula: REFCLK phase noise at f(MHz) = REFCLK phase noise at 622 MHz + 20*log(f/622).
- (19) SFP/+ optical modules require the host interface to have RD+/- differentially terminated with 100 Ω. The internal OCT feature is available after the Stratix V FPGA configuration is completed. Altera recommends that FPGA configuration is completed before inserting the optical module. Otherwise, minimize unnecessary removal and insertion with unconfigured devices.
- (20) Refer to Figure 4.
- (21) For oversampling design to support data rates less than the minimum specification, the CDR needs to be in LTR mode only.
- (22) This supply follows VCCR_GXB for both GX and GT channels.
- (23) When you use fPLL as a TXPLL of the transceiver.

- XFI
- ASI
- HiGig/HiGig+
- HiGig2/HiGig2+
- Serial Data Converter (SDC)
- GPON
- SDI
- SONET
- Fibre Channel (FC)
- PCIe
- QPI
- SFF-8431

Download the Stratix V Characterization Report Tool to view the characterization report summary for these protocols.

Core Performance Specifications

This section describes the clock tree, phase-locked loop (PLL), digital signal processing (DSP), memory blocks, configuration, and JTAG specifications.

Clock Tree Specifications

Table 30 lists the clock tree specifications for Stratix V devices.

Table 30. Clock Tree Performance for Stratix V Devices (1)

	Performance								
Symbol	C1, C2, C2L, I2, and I2L	C3, I3, I3L, and I3YY	C4, I4	Unit					
Global and Regional Clock	717	650	580	MHz					
Periphery Clock	550	500	500	MHz					

Note to Table 30:

(1) The Stratix V ES devices are limited to 600 MHz core clock tree performance.

Mode	C1	C2, C2L	12, 12L	C3	13, 13L, 13YY	C4	14	Unit	
		Modes us	ing Three	DSPs					
One complex 18 x 25	425	425	415	340	340	275	265	MHz	
Modes using Four DSPs									
One complex 27 x 27	465	465	465	380	380	300	290	MHz	

Table 32. Block Performance Specifications for Stratix V DSP Devices (Part 2 of 2)

Memory Block Specifications

Table 33 lists the Stratix V memory block specifications.

Table 33. Memory Block Performance Specifications for Stratix V Devices (1), (2) (Part 1 of 2)

		Resources Used		Performance							
Memory	Mode	ALUTS	Memory	C1	C2, C2L	C3	C4	12, 12L	13, 13L, 13YY	14	Unit
	Single port, all supported widths	0	1	450	450	400	315	450	400	315	MHz
MLAR	Simple dual-port, x32/x64 depth	0	1	450	450	400	315	450	400	315	MHz
WILAD	Simple dual-port, x16 depth ⁽³⁾	0	1	675	675	533	400	675	533	400	MHz
	ROM, all supported widths	0	1	600	600	500	450	600	500	450	MHz

Periphery Performance

This section describes periphery performance, including high-speed I/O and external memory interface.

I/O performance supports several system interfaces, such as the **LVDS** high-speed I/O interface, external memory interface, and the **PCI/PCI-X** bus interface. General-purpose I/O standards such as 3.3-, 2.5-, 1.8-, and 1.5-**LVTTL/LVCMOS** are capable of a typical 167 MHz and 1.2-**LVCMOS** at 100 MHz interfacing frequency with a 10 pF load.

The actual achievable frequency depends on design- and system-specific factors. Ensure proper timing closure in your design and perform HSPICE/IBIS simulations based on your specific design and system setup to determine the maximum achievable frequency in your system.

High-Speed I/O Specification

Table 36 lists high-speed I/O timing for Stratix V devices.

Table 36. High-Speed I/O Specifications for Stratix V Devices (1), (2) (Part 1 of 4)

Sumbol	Conditions		C1		C2,	C2L, I	2, I2L	C3,	13, 13 1	., I3YY		C4,I	4	11
Symbol	Conditions	Min	Тур	Max	Min	Тур	Max	Min	Тур	Max	Min	Тур	Max	UNIT
f _{HSCLK_in} (input clock frequency) True Differential I/O Standards	Clock boost factor W = 1 to 40 $^{(4)}$	5	_	800	5		800	5		625	5		525	MHz
f _{HSCLK_in} (input clock frequency) Single Ended I/O Standards ⁽³⁾	Clock boost factor W = 1 to 40 $^{(4)}$	5		800	5		800	5		625	5		525	MHz
f _{HSCLK_in} (input clock frequency) Single Ended I/O Standards	Clock boost factor W = 1 to 40 $^{(4)}$	5	_	520	5		520	5	_	420	5	_	420	MHz
f _{HSCLK_OUT} (output clock frequency)	_	5	_	800	5	_	800	5	_	625 (5)	5	_	525 (5)	MHz

Figure 7 shows the dynamic phase alignment (DPA) lock time specifications with the DPA PLL calibration option enabled.

Figure 7. DPA Lock Time Specification with DPA PLL Calibration Enabled

rx_reset			
rx_dpa_locked			<u> </u>
			-

Table 37 lists the DPA lock time specifications for Stratix V devices.

Table 37. DPA Lock Time Specifications for Stratix V GX Devices Only (1), (2), (3)

Standard	Training Pattern	Number of Data Transitions in One Repetition of the Training Pattern	Number of Repetitions per 256 Data Transitions ⁽⁴⁾	Maximum
SPI-4	00000000001111111111	2	128	640 data transitions
Parallel Rapid I/O	00001111	2	128	640 data transitions
	10010000	4	64	640 data transitions
Miscellaneous	10101010	8	32	640 data transitions
Wiscenareous	01010101	8	32	640 data transitions

Notes to Table 37:

(1) The DPA lock time is for one channel.

(2) One data transition is defined as a 0-to-1 or 1-to-0 transition.

(3) The DPA lock time stated in this table applies to both commercial and industrial grade.

(4) This is the number of repetitions for the stated training pattern to achieve the 256 data transitions.

Figure 8 shows the **LVDS** soft-clock data recovery (CDR)/DPA sinusoidal jitter tolerance specification for a data rate \geq 1.25 Gbps. Table 38 lists the **LVDS** soft-CDR/DPA sinusoidal jitter tolerance specification for a data rate \geq 1.25 Gbps.





Jitter Free	quency (Hz)	Sinusoidal Jitter (UI)
F1	10,000	25.000
F2	17,565	25.000
F3	1,493,000	0.350
F4	50,000,000	0.350

iadie 38. lvus sott-luk/upa sinusoidai jitter mask vaiues tor a uata kate > 1.2	25 G	.2	1.	1	>	>		Ì	e	F	Ł	đ	a	2	1	R	P							Ľ	I.		I.	Ì	1	3	a	3	a	2	2	2	ŀ	t	t	t	ſ	ľ	3	2	2	2	2	2	1)	D		I		Ľ	1	2	2	ź	â	i		۴	۴	r	r		I	I	Ì	1	Π	٥	٢	i	F	f	f	1	1		5	S	S	S	2	2	e	E	I	U	h	I	١	a	ŀ	I	V	۱			ľ	٢	k	k	s	S	S	1	a	2	2		И	V	N			•	۴	r	r	1	1	1	2	2	2	2	e	e	e	E	t	t	i	ŀ	t	ľ	i	i	f	f	ŀ	ŀ	li
---	------	----	----	---	---	---	--	---	---	---	---	---	---	---	---	---	---	--	--	--	--	--	--	---	----	--	----	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---	--	---	--	---	---	---	---	---	---	---	--	---	---	---	---	--	---	---	---	---	---	---	---	---	---	---	---	---	---	--	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---	--	--	---	---	---	---	---	---	---	---	---	---	---	--	---	---	---	--	--	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---	----

Figure 9 shows the **LVDS** soft-CDR/DPA sinusoidal jitter tolerance specification for a data rate < 1.25 Gbps.





DLL Range, DQS Logic Block, and Memory Output Clock Jitter Specifications

Table 39 lists the DLL range specification for Stratix V devices. The DLL is always in 8-tap mode in Stratix V devices.

Table 39. DLL Range Specifications for Stratix V Devices (1)

C1	C2, C2L, I2, I2L	C3, I3, I3L, I3YY	C4,I4	Unit
300-933	300-933	300-890	300-890	MHz

Note to Table 39:

(1) Stratix V devices support memory interface frequencies lower than 300 MHz, although the reference clock that feeds the DLL must be at least 300 MHz. To support interfaces below 300 MHz, multiply the reference clock feeding the DLL to ensure the frequency is within the supported range of the DLL.

Table 40 lists the DQS phase offset delay per stage for Stratix V devices.

Table 40. DQS Phase Offset Delay Per Setting for Stratix V Devices ^{(1), (2)} (Part 1 of 2)

Speed Grade	Min	Max	Unit
C1	8	14	ps
C2, C2L, I2, I2L	8	14	ps
C3,I3, I3L, I3YY	8	15	ps

Clock	Parameter	Symbol	C	1	C2, C2L	, 12, 12L	C3, I3 I3	8, 13L , YY	C4	,14	Unit
NELWUIK		-	Min	Max	Min	Max	Min	Max	Min	Max	
	Clock period jitter	$t_{JIT(per)}$	-25	25	-25	25	-30	30	-35	35	ps
PHY Clock	Cycle-to-cycle period jitter	$t_{\rm JIT(cc)}$	-50	50	-50	50	-60	60	-70	70	ps
	Duty cycle jitter	$t_{JIT(duty)}$	-37.5	37.5	-37.5	37.5	-45	45	-56	56	ps

Table 42. Memory Output Clock Jitter Specification for Stratix V Devices (1), (Part 2 of 2) (2), (3)

Notes to Table 42:

(1) The clock jitter specification applies to the memory output clock pins generated using differential signal-splitter and DDIO circuits clocked by a PLL output routed on a PHY, regional, or global clock network as specified. Altera recommends using PHY clock networks whenever possible.

(2) The clock jitter specification applies to the memory output clock pins clocked by an integer PLL.

(3) The memory output clock jitter is applicable when an input jitter of 30 ps peak-to-peak is applied with bit error rate (BER) -12, equivalent to 14 sigma.

OCT Calibration Block Specifications

Table 43 lists the OCT calibration block specifications for Stratix V devices.

Table 43. OCT Calibration Block Specifications for Stratix V Devices

Symbol	Description	Min	Тур	Max	Unit
OCTUSRCLK	Clock required by the OCT calibration blocks	—	—	20	MHz
T _{OCTCAL}	Number of OCTUSRCLK clock cycles required for OCT $\rm R_S/R_T$ calibration		1000	_	Cycles
T _{OCTSHIFT}	Number of OCTUSRCLK clock cycles required for the OCT code to shift out	_	32	_	Cycles
T _{RS_RT}	Time required between the dyn_term_ctrl and oe signal transitions in a bidirectional I/O buffer to dynamically switch between OCT R_S and R_T (Figure 10)		2.5		ns

Figure 10 shows the timing diagram for the oe and dyn_term_ctrl signals.

Figure 10. Timing Diagram for oe and dyn_term_ctrl Signals



Duty Cycle Distortion (DCD) Specifications

Table 44 lists the worst-case DCD for Stratix V devices.

Table 44. Worst-Case DCD on Stratix V I/O Pins (1)

Symbol	C	1	C2, C2	L, 12, 12L	C3, I I3	3, I3L, IYY	C4	4,14	Unit
-	Min	Max	Min	Max	Min	Max	Min	Max	
Output Duty Cycle	45	55	45	55	45	55	45	55	%

Note to Table 44:

(1) The DCD numbers do not cover the core clock network.

Configuration Specification

POR Delay Specification

Power-on reset (POR) delay is defined as the delay between the time when all the power supplies monitored by the POR circuitry reach the minimum recommended operating voltage to the time when the nSTATUS is released high and your device is ready to begin configuration.



For more information about the POR delay, refer to the *Hot Socketing and Power-On Reset in Stratix V Devices* chapter.

Table 45 lists the fast and standard POR delay specification.

Table 45. Fast and Standard POR Delay Specification (1)

POR Delay	Minimum	Maximum
Fast	4 ms	12 ms
Standard	100 ms	300 ms

Note to Table 45:

(1) You can select the POR delay based on the MSEL settings as described in the MSEL Pin Settings section of the "Configuration, Design Security, and Remote System Upgrades in Stratix V Devices" chapter.

JTAG Configuration Specifications

Table 46 lists the JTAG timing parameters and values for Stratix V devices.

Table 46. JTAG Timing Parameters and Values for Stratix V Devices

Symbol	Description	Min	Max	Unit
t _{JCP}	TCK clock period ⁽²⁾	30		ns
t _{JCP}	TCK clock period ⁽²⁾	167	—	ns
t _{JCH}	TCK clock high time ⁽²⁾	14	—	ns
t _{JCL}	TCK clock low time ⁽²⁾	14		ns
t _{JPSU (TDI)}	TDI JTAG port setup time	2	—	ns
t _{JPSU (TMS)}	TMS JTAG port setup time	3	_	ns

Configuration Scheme	Decompression	Design Security	DCLK-to-DATA[] Ratio
	Disabled	Disabled	1
	Disabled	Enabled	4
IFF XJZ	Enabled	Disabled	8
	Enabled	Enabled	8

Table 49.	DCLK-to-DATA[]	Ratio ⁽¹⁾	(Part 2 of 2)
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Note to Table 49:

(1) Depending on the DCLK-to-DATA [] ratio, the host must send a DCLK frequency that is r times the data rate in bytes per second (Bps), or words per second (Wps). For example, in FPP ×16 when the DCLK-to-DATA [] ratio is 2, the DCLK frequency must be 2 times the data rate in Wps. Stratix V devices use the additional clock cycles to decrypt and decompress the configuration data.

Figure 11 shows the configuration interface connections between the Stratix V device and a MAX II or MAX V device for single device configuration.

Figure 11. Single Device FPP Configuration Using an External Host



Notes to Figure 11:

- (1) Connect the resistor to a supply that provides an acceptable input signal for the Stratix V device. V_{CCPGM} must be high enough to meet the V_{IH} specification of the I/O on the device and the external host. Altera recommends powering up all configuration system I/Os with V_{CCPGM} .
- (2) You can leave the nCEO pin unconnected or use it as a user I/O pin when it does not feed another device's nCE pin.
- (3) The MSEL pin settings vary for different data width, configuration voltage standards, and POR delay. To connect MSEL, refer to the MSEL Pin Settings section of the "Configuration, Design Security, and Remote System Upgrades in Stratix V Devices" chapter.
- (4) If you use FPP ×8, use DATA [7..0]. If you use FPP ×16, use DATA [15..0].

IF the DCLK-to-DATA[] ratio is greater than 1, at the end of configuration, you can only stop the DCLK (DCLK-to-DATA[] ratio – 1) clock cycles after the last data is latched into the Stratix V device.

Active Serial Configuration Timing

Table 52 lists the DCLK frequency specification in the AS configuration scheme.

Fable 52.	DCLK Frequency	Specification in th	e AS Configuration	Scheme ^{(1),}	(2)
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Minimum	Typical	Maximum	Unit
5.3	7.9	12.5	MHz
10.6	15.7	25.0	MHz
21.3	31.4	50.0	MHz
42.6	62.9	100.0	MHz

Notes to Table 52:

(1) This applies to the DCLK frequency specification when using the internal oscillator as the configuration clock source.

(2) The AS multi-device configuration scheme does not support DCLK frequency of 100 MHz.

Figure 14 shows the single-device configuration setup for an AS ×1 mode.





Notes to Figure 14:

- (1) If you are using AS $\times 4$ mode, this signal represents the AS_DATA[3..0] and EPCQ sends in 4-bits of data for each DCLK cycle.
- (2) The initialization clock can be from internal oscillator or CLKUSR pin.
- (3) After the option bit to enable the INIT_DONE pin is configured into the device, the INIT_DONE goes low.

Table 53 lists the timing parameters for AS $\times 1$ and AS $\times 4$ configurations in Stratix V devices.

Table JS. As fining falancees for as $\times 1$ and as $\times 4$ configurations in straits V devices $(2, 2, 2, 3, 3, 3, 3, 3, 3, 3, 3, 3, 3, 3, 3, 3,$	Table 53.	AS Timing	Parameters for AS	\times 1 and AS \times 4 Confi	gurations in Stratix V	/ Devices ^{(1), (2)}	(Part 1 of 2)
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Symbol	Parameter	Minimum	Maximum	Units
t _{CO}	DCLK falling edge to AS_DATA0/ASDO output	—	2	ns
t _{SU}	Data setup time before falling edge on DCLK	1.5	_	ns
t _H	Data hold time after falling edge on DCLK	0	_	ns

Table 54 lists the PS configuration timing parameters for Stratix V devices.

Table 54. PS Timing Parameters for Stratix V Devices

Symbol	Parameter	Minimum	Maximum	Units
t _{CF2CD}	nCONFIG low to CONF_DONE low	—	600	ns
t _{CF2ST0}	nCONFIG low to nSTATUS low	—	600	ns
t _{CFG}	nCONFIG low pulse width	2	—	μS
t _{status}	nSTATUS low pulse width	268	1,506 ⁽¹⁾	μS
t _{CF2ST1}	nCONFIG high to nSTATUS high	—	1,506 ⁽²⁾	μS
t _{CF2CK} (5)	nCONFIG high to first rising edge on DCLK	1,506	—	μS
t _{ST2CK} (5)	nSTATUS high to first rising edge of DCLK	2	—	μS
t _{DSU}	DATA[] setup time before rising edge on DCLK	5.5	—	ns
t _{DH}	DATA [] hold time after rising edge on DCLK	0	—	ns
t _{CH}	DCLK high time	$0.45\times 1/f_{MAX}$	—	S
t _{CL}	DCLK low time	$0.45\times 1/f_{MAX}$	—	S
t _{CLK}	DCLK period	1/f _{MAX}	—	S
f _{MAX}	DCLK frequency	—	125	MHz
t _{CD2UM}	CONF_DONE high to user mode ⁽³⁾	175	437	μS
t _{CD2CU}	CONF_DONE high to CLKUSR enabled	4 × maximum DCLK period	_	_
t _{cd2UMC}	CONF_DONE high to user mode with CLKUSR option on	t_{CD2CU} + (8576 × CLKUSR period) ⁽⁴⁾	_	_

Notes to Table 54:

(1) This value is applicable if you do not delay configuration by extending the nCONFIG or nSTATUS low pulse width.

(2) This value is applicable if you do not delay configuration by externally holding the nSTATUS low.

(3) The minimum and maximum numbers apply only if you choose the internal oscillator as the clock source for initializing the device.

(4) To enable the CLKUSR pin as the initialization clock source and to obtain the maximum frequency specification on these pins, refer to the "Initialization" section.

(5) If nSTATUS is monitored, follow the t_{ST2CK} specification. If nSTATUS is not monitored, follow the t_{CF2CK} specification.

Initialization

Table 55 lists the initialization clock source option, the applicable configuration schemes, and the maximum frequency.

Table 55.	Initialization	Clock Source	Option	and the	Maximum	Frequency

Initialization Clock Source	Configuration Schemes	Maximum Frequency	Minimum Number of Clock Cycles ⁽¹⁾
Internal Oscillator	AS, PS, FPP	12.5 MHz	
CLKUSR	AS, PS, FPP ⁽²⁾	125 MHz	8576
DCLK	PS, FPP	125 MHz	

Notes to Table 55:

(1) The minimum number of clock cycles required for device initialization.

(2) To enable CLKUSR as the initialization clock source, turn on the Enable user-supplied start-up clock (CLKUSR) option in the Quartus II software from the General panel of the Device and Pin Options dialog box.