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Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Obsolete
Number of LABs/CLBs	158500
Number of Logic Elements/Cells	420000
Total RAM Bits	37888000
Number of I/O	600
Number of Gates	-
Voltage - Supply	0.87V ~ 0.93V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	1152-BBGA, FCBGA
Supplier Device Package	1152-FBGA (35x35)
Purchase URL	https://www.e-xfl.com/product-detail/intel/5sgxma4k1f35i2n

Table 3. Absolute Maximum Ratings for Stratix V Devices (Part 2 of 2)

Symbol	Description	Minimum	Maximum	Unit
V _{CCD_FPLL}	PLL digital power supply	−0.5	1.8	V
V _{CCA_FPLL}	PLL analog power supply	−0.5	3.4	V
V _I	DC input voltage	−0.5	3.8	V
T _J	Operating junction temperature	−55	125	°C
T _{STG}	Storage temperature (No bias)	−65	150	°C
I _{OUT}	DC output current per pin	−25	40	mA

Table 4 lists the absolute conditions for the transceiver power supply for Stratix V GX, GS, and GT devices.

Table 4. Transceiver Power Supply Absolute Conditions for Stratix V GX, GS, and GT Devices

Symbol	Description	Devices	Minimum	Maximum	Unit
V _{CCA_GXBL}	Transceiver channel PLL power supply (left side)	GX, GS, GT	−0.5	3.75	V
V _{CCA_GXBR}	Transceiver channel PLL power supply (right side)	GX, GS	−0.5	3.75	V
V _{CCA_GTBR}	Transceiver channel PLL power supply (right side)	GT	−0.5	3.75	V
V _{CCHIP_L}	Transceiver hard IP power supply (left side)	GX, GS, GT	−0.5	1.35	V
V _{CCHIP_R}	Transceiver hard IP power supply (right side)	GX, GS, GT	−0.5	1.35	V
V _{CCHSSI_L}	Transceiver PCS power supply (left side)	GX, GS, GT	−0.5	1.35	V
V _{CCHSSI_R}	Transceiver PCS power supply (right side)	GX, GS, GT	−0.5	1.35	V
V _{CCR_GXBL}	Receiver analog power supply (left side)	GX, GS, GT	−0.5	1.35	V
V _{CCR_GXBR}	Receiver analog power supply (right side)	GX, GS, GT	−0.5	1.35	V
V _{CCR_GTBR}	Receiver analog power supply for GT channels (right side)	GT	−0.5	1.35	V
V _{CCT_GXBL}	Transmitter analog power supply (left side)	GX, GS, GT	−0.5	1.35	V
V _{CCT_GXBR}	Transmitter analog power supply (right side)	GX, GS, GT	−0.5	1.35	V
V _{CCT_GTBR}	Transmitter analog power supply for GT channels (right side)	GT	−0.5	1.35	V
V _{CCL_GTBR}	Transmitter clock network power supply (right side)	GT	−0.5	1.35	V
V _{CCH_GXBL}	Transmitter output buffer power supply (left side)	GX, GS, GT	−0.5	1.8	V
V _{CCH_GXBR}	Transmitter output buffer power supply (right side)	GX, GS, GT	−0.5	1.8	V

Maximum Allowed Overshoot and Undershoot Voltage

During transitions, input signals may overshoot to the voltage shown in Table 5 and undershoot to −2.0 V for input currents less than 100 mA and periods shorter than 20 ns.

Internal Weak Pull-Up Resistor

Table 16 lists the weak pull-up resistor values for Stratix V devices.

Table 16. Internal Weak Pull-Up Resistor for Stratix V Devices ^{(1), (2)}

Symbol	Description	V _{CCIO} Conditions (V) ⁽³⁾	Value ⁽⁴⁾	Unit
R _{PU}	Value of the I/O pin pull-up resistor before and during configuration, as well as user mode if you enable the programmable pull-up resistor option.	3.0 ±5%	25	kΩ
		2.5 ±5%	25	kΩ
		1.8 ±5%	25	kΩ
		1.5 ±5%	25	kΩ
		1.35 ±5%	25	kΩ
		1.25 ±5%	25	kΩ
		1.2 ±5%	25	kΩ

Notes to Table 16:

- (1) All I/O pins have an option to enable the weak pull-up resistor except the configuration, test, and JTAG pins.
- (2) The internal weak pull-down feature is only available for the JTAG TCK pin. The typical value for this internal weak pull-down resistor is approximately 25 kΩ.
- (3) The pin pull-up resistance values may be lower if an external source drives the pin higher than V_{CCIO}.
- (4) These specifications are valid with a ±10% tolerance to cover changes over PVT.

I/O Standard Specifications

Table 17 through Table 22 list the input voltage (V_{IH} and V_{IL}), output voltage (V_{OH} and V_{OL}), and current drive characteristics (I_{OH} and I_{OL}) for various I/O standards supported by Stratix V devices. These tables also show the Stratix V device family I/O standard specifications. The V_{OL} and V_{OH} values are valid at the corresponding I_{OH} and I_{OL}, respectively.

For an explanation of the terms used in Table 17 through Table 22, refer to “Glossary” on page 65. For tolerance calculations across all SSTL and HSTL I/O standards, refer to Altera knowledge base solution rd07262012_486.

Table 17. Single-Ended I/O Standards for Stratix V Devices

I/O Standard	V _{CCIO} (V)			V _{IL} (V)		V _{IH} (V)		V _{OL} (V)	V _{OH} (V)	I _{OL} (mA)	I _{OH} (mA)
	Min	Typ	Max	Min	Max	Min	Max	Max	Min		
LVTTTL	2.85	3	3.15	−0.3	0.8	1.7	3.6	0.4	2.4	2	−2
LVC MOS	2.85	3	3.15	−0.3	0.8	1.7	3.6	0.2	V _{CCIO} − 0.2	0.1	−0.1
2.5 V	2.375	2.5	2.625	−0.3	0.7	1.7	3.6	0.4	2	1	−1
1.8 V	1.71	1.8	1.89	−0.3	0.35 * V _{CCIO}	0.65 * V _{CCIO}	V _{CCIO} + 0.3	0.45	V _{CCIO} − 0.45	2	−2
1.5 V	1.425	1.5	1.575	−0.3	0.35 * V _{CCIO}	0.65 * V _{CCIO}	V _{CCIO} + 0.3	0.25 * V _{CCIO}	0.75 * V _{CCIO}	2	−2
1.2 V	1.14	1.2	1.26	−0.3	0.35 * V _{CCIO}	0.65 * V _{CCIO}	V _{CCIO} + 0.3	0.25 * V _{CCIO}	0.75 * V _{CCIO}	2	−2

Table 18. Single-Ended SSTL, HSTL, and HSUL I/O Reference Voltage Specifications for Stratix V Devices

I/O Standard	V_{CCIO} (V)			V_{REF} (V)			V_{TT} (V)		
	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max
SSTL-2 Class I, II	2.375	2.5	2.625	$0.49 * V_{CCIO}$	$0.5 * V_{CCIO}$	$0.51 * V_{CCIO}$	$V_{REF} - 0.04$	V_{REF}	$V_{REF} + 0.04$
SSTL-18 Class I, II	1.71	1.8	1.89	0.833	0.9	0.969	$V_{REF} - 0.04$	V_{REF}	$V_{REF} + 0.04$
SSTL-15 Class I, II	1.425	1.5	1.575	$0.49 * V_{CCIO}$	$0.5 * V_{CCIO}$	$0.51 * V_{CCIO}$	$0.49 * V_{CCIO}$	$0.5 * V_{CCIO}$	$0.51 * V_{CCIO}$
SSTL-135 Class I, II	1.283	1.35	1.418	$0.49 * V_{CCIO}$	$0.5 * V_{CCIO}$	$0.51 * V_{CCIO}$	$0.49 * V_{CCIO}$	$0.5 * V_{CCIO}$	$0.51 * V_{CCIO}$
SSTL-125 Class I, II	1.19	1.25	1.26	$0.49 * V_{CCIO}$	$0.5 * V_{CCIO}$	$0.51 * V_{CCIO}$	$0.49 * V_{CCIO}$	$0.5 * V_{CCIO}$	$0.51 * V_{CCIO}$
SSTL-12 Class I, II	1.14	1.20	1.26	$0.49 * V_{CCIO}$	$0.5 * V_{CCIO}$	$0.51 * V_{CCIO}$	$0.49 * V_{CCIO}$	$0.5 * V_{CCIO}$	$0.51 * V_{CCIO}$
HSTL-18 Class I, II	1.71	1.8	1.89	0.85	0.9	0.95	—	$V_{CCIO}/2$	—
HSTL-15 Class I, II	1.425	1.5	1.575	0.68	0.75	0.9	—	$V_{CCIO}/2$	—
HSTL-12 Class I, II	1.14	1.2	1.26	$0.47 * V_{CCIO}$	$0.5 * V_{CCIO}$	$0.53 * V_{CCIO}$	—	$V_{CCIO}/2$	—
HSUL-12	1.14	1.2	1.3	$0.49 * V_{CCIO}$	$0.5 * V_{CCIO}$	$0.51 * V_{CCIO}$	—	—	—

Table 19. Single-Ended SSTL, HSTL, and HSUL I/O Standards Signal Specifications for Stratix V Devices (Part 1 of 2)

I/O Standard	$V_{IL(DC)}$ (V)		$V_{IH(DC)}$ (V)		$V_{IL(AC)}$ (V)	$V_{IH(AC)}$ (V)	V_{OL} (V)	V_{OH} (V)	I_{OI} (mA)	I_{OH} (mA)
	Min	Max	Min	Max	Max	Min	Max	Min		
SSTL-2 Class I	-0.3	$V_{REF} - 0.15$	$V_{REF} + 0.15$	$V_{CCIO} + 0.3$	$V_{REF} - 0.31$	$V_{REF} + 0.31$	$V_{TT} - 0.608$	$V_{TT} + 0.608$	8.1	-8.1
SSTL-2 Class II	-0.3	$V_{REF} - 0.15$	$V_{REF} + 0.15$	$V_{CCIO} + 0.3$	$V_{REF} - 0.31$	$V_{REF} + 0.31$	$V_{TT} - 0.81$	$V_{TT} + 0.81$	16.2	-16.2
SSTL-18 Class I	-0.3	$V_{REF} - 0.125$	$V_{REF} + 0.125$	$V_{CCIO} + 0.3$	$V_{REF} - 0.25$	$V_{REF} + 0.25$	$V_{TT} - 0.603$	$V_{TT} + 0.603$	6.7	-6.7
SSTL-18 Class II	-0.3	$V_{REF} - 0.125$	$V_{REF} + 0.125$	$V_{CCIO} + 0.3$	$V_{REF} - 0.25$	$V_{REF} + 0.25$	0.28	$V_{CCIO} - 0.28$	13.4	-13.4
SSTL-15 Class I	—	$V_{REF} - 0.1$	$V_{REF} + 0.1$	—	$V_{REF} - 0.175$	$V_{REF} + 0.175$	$0.2 * V_{CCIO}$	$0.8 * V_{CCIO}$	8	-8
SSTL-15 Class II	—	$V_{REF} - 0.1$	$V_{REF} + 0.1$	—	$V_{REF} - 0.175$	$V_{REF} + 0.175$	$0.2 * V_{CCIO}$	$0.8 * V_{CCIO}$	16	-16
SSTL-135 Class I, II	—	$V_{REF} - 0.09$	$V_{REF} + 0.09$	—	$V_{REF} - 0.16$	$V_{REF} + 0.16$	$0.2 * V_{CCIO}$	$0.8 * V_{CCIO}$	—	—
SSTL-125 Class I, II	—	$V_{REF} - 0.85$	$V_{REF} + 0.85$	—	$V_{REF} - 0.15$	$V_{REF} + 0.15$	$0.2 * V_{CCIO}$	$0.8 * V_{CCIO}$	—	—
SSTL-12 Class I, II	—	$V_{REF} - 0.1$	$V_{REF} + 0.1$	—	$V_{REF} - 0.15$	$V_{REF} + 0.15$	$0.2 * V_{CCIO}$	$0.8 * V_{CCIO}$	—	—

Switching Characteristics

This section provides performance characteristics of the Stratix V core and periphery blocks.

These characteristics can be designated as Preliminary or Final.

- Preliminary characteristics are created using simulation results, process data, and other known parameters. The title of these tables show the designation as “Preliminary.”
- Final numbers are based on actual silicon characterization and testing. The numbers reflect the actual performance of the device under worst-case silicon process, voltage, and junction temperature conditions. There are no designations on finalized tables.

Transceiver Performance Specifications

This section describes transceiver performance specifications.

Table 23 lists the Stratix V GX and GS transceiver specifications.

Table 23. Transceiver Specifications for Stratix V GX and GS Devices ⁽¹⁾ (Part 1 of 7)

Symbol/ Description	Conditions	Transceiver Speed Grade 1			Transceiver Speed Grade 2			Transceiver Speed Grade 3			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Reference Clock											
Supported I/O Standards	Dedicated reference clock pin	1.2-V PCML, 1.4-V PCML, 1.5-V PCML, 2.5-V PCML, Differential LVPECL, LVDS, and HCSL									
	RX reference clock pin	1.4-V PCML, 1.5-V PCML, 2.5-V PCML, LVPECL, and LVDS									
Input Reference Clock Frequency (CMU PLL) ⁽⁸⁾	—	40	—	710	40	—	710	40	—	710	MHz
Input Reference Clock Frequency (ATX PLL) ⁽⁸⁾	—	100	—	710	100	—	710	100	—	710	MHz
Rise time	Measure at ±60 mV of differential signal ⁽²⁶⁾	—	—	400	—	—	400	—	—	400	ps
Fall time	Measure at ±60 mV of differential signal ⁽²⁶⁾	—	—	400	—	—	400	—	—	400	
Duty cycle	—	45	—	55	45	—	55	45	—	55	%
Spread-spectrum modulating clock frequency	PCI Express® (PCIe®)	30	—	33	30	—	33	30	—	33	kHz

Table 23. Transceiver Specifications for Stratix V GX and GS Devices ⁽¹⁾ (Part 2 of 7)

Symbol/ Description	Conditions	Transceiver Speed Grade 1			Transceiver Speed Grade 2			Transceiver Speed Grade 3			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Spread-spectrum downspread	PCIe	—	0 to -0.5	—	—	0 to -0.5	—	—	0 to -0.5	—	%
On-chip termination resistors ⁽²¹⁾	—	—	100	—	—	100	—	—	100	—	Ω
Absolute V_{MAX} ⁽⁵⁾	Dedicated reference clock pin	—	—	1.6	—	—	1.6	—	—	1.6	V
	RX reference clock pin	—	—	1.2	—	—	1.2	—	—	1.2	
Absolute V_{MIN}	—	-0.4	—	—	-0.4	—	—	-0.4	—	—	V
Peak-to-peak differential input voltage	—	200	—	1600	200	—	1600	200	—	1600	mV
V_{ICM} (AC coupled) ⁽³⁾	Dedicated reference clock pin	1050/1000/900/850 ⁽²⁾			1050/1000/900/850 ⁽²⁾			1050/1000/900/850 ⁽²⁾			mV
	RX reference clock pin	1.0/0.9/0.85 ⁽⁴⁾			1.0/0.9/0.85 ⁽⁴⁾			1.0/0.9/0.85 ⁽⁴⁾			V
V_{ICM} (DC coupled)	HCSL I/O standard for PCIe reference clock	250	—	550	250	—	550	250	—	550	mV
Transmitter REFCLK Phase Noise (622 MHz) ⁽²⁰⁾	100 Hz	—	—	-70	—	—	-70	—	—	-70	dBc/Hz
	1 kHz	—	—	-90	—	—	-90	—	—	-90	dBc/Hz
	10 kHz	—	—	-100	—	—	-100	—	—	-100	dBc/Hz
	100 kHz	—	—	-110	—	—	-110	—	—	-110	dBc/Hz
	≥ 1 MHz	—	—	-120	—	—	-120	—	—	-120	dBc/Hz
Transmitter REFCLK Phase Jitter (100 MHz) ⁽¹⁷⁾	10 kHz to 1.5 MHz (PCIe)	—	—	3	—	—	3	—	—	3	ps (rms)
R_{REF} ⁽¹⁹⁾	—	—	1800 $\pm 1\%$	—	—	1800 $\pm 1\%$	—	—	1800 $\pm 1\%$	—	Ω
Transceiver Clocks											
fixedclk clock frequency	PCIe Receiver Detect	—	100 or 125	—	—	100 or 125	—	—	100 or 125	—	MHz

Table 26 shows the approximate maximum data rate using the 10G PCS.

Table 26. Stratix V 10G PCS Approximate Maximum Data Rate ⁽¹⁾

Mode ⁽²⁾	Transceiver Speed Grade	PMA Width	64	40	40	40	32	32
		PCS Width	64	66/67	50	40	64/66/67	32
FIFO or Register	1	C1, C2, C2L, I2, I2L core speed grade	14.1	14.1	10.69	14.1	13.6	13.6
	2	C1, C2, C2L, I2, I2L core speed grade	12.5	12.5	10.69	12.5	12.5	12.5
		C3, I3, I3L core speed grade	12.5	12.5	10.69	12.5	10.88	10.88
	3	C1, C2, C2L, I2, I2L core speed grade	8.5 Gbps					
		C3, I3, I3L core speed grade						
		C4, I4 core speed grade						
		I3YY core speed grade	10.3125 Gbps					

Notes to Table 26:

- (1) The maximum data rate is in Gbps.
- (2) The Phase Compensation FIFO can be configured in FIFO mode or register mode. In the FIFO mode, the pointers are not fixed, and the latency can vary. In the register mode the pointers are fixed for low latency.

Table 27 shows the V_{OD} settings for the GX channel.

Table 27. Typical V_{OD} Setting for GX Channel, TX Termination = 100 Ω ⁽²⁾

Symbol	V_{OD} Setting	V_{OD} Value (mV)	V_{OD} Setting	V_{OD} Value (mV)
V_{OD} differential peak to peak typical ⁽³⁾	0 ⁽¹⁾	0	32	640
	1 ⁽¹⁾	20	33	660
	2 ⁽¹⁾	40	34	680
	3 ⁽¹⁾	60	35	700
	4 ⁽¹⁾	80	36	720
	5 ⁽¹⁾	100	37	740
	6	120	38	760
	7	140	39	780
	8	160	40	800
	9	180	41	820
	10	200	42	840
	11	220	43	860
	12	240	44	880
	13	260	45	900
	14	280	46	920
	15	300	47	940
	16	320	48	960
	17	340	49	980
	18	360	50	1000
	19	380	51	1020
	20	400	52	1040
	21	420	53	1060
	22	440	54	1080
	23	460	55	1100
	24	480	56	1120
	25	500	57	1140
	26	520	58	1160
	27	540	59	1180
	28	560	60	1200
	29	580	61	1220
	30	600	62	1240
	31	620	63	1260

Note to Table 27:

- (1) If TX termination resistance = 100 Ω , this VOD setting is illegal.
- (2) The tolerance is +/-20% for all VOD settings except for settings 2 and below.
- (3) Refer to Figure 2.

Table 28. Transceiver Specifications for Stratix V GT Devices (Part 1 of 5) ⁽¹⁾

Symbol/ Description	Conditions	Transceiver Speed Grade 2			Transceiver Speed Grade 3			Unit
		Min	Typ	Max	Min	Typ	Max	
Reference Clock								
Supported I/O Standards	Dedicated reference clock pin	1.2-V PCML, 1.4-V PCML, 1.5-V PCML, 2.5-V PCML, Differential LVPECL, LVDS, and HCSL						
	RX reference clock pin	1.4-V PCML, 1.5-V PCML, 2.5-V PCML, LVPECL, and LVDS						
Input Reference Clock Frequency (CMU PLL) ⁽⁶⁾	—	40	—	710	40	—	710	MHz
Input Reference Clock Frequency (ATX PLL) ⁽⁶⁾	—	100	—	710	100	—	710	MHz
Rise time	20% to 80%	—	—	400	—	—	400	ps
Fall time	80% to 20%	—	—	400	—	—	400	
Duty cycle	—	45	—	55	45	—	55	%
Spread-spectrum modulating clock frequency	PCI Express (PCIe)	30	—	33	30	—	33	kHz
Spread-spectrum downspread	PCIe	—	0 to −0.5	—	—	0 to −0.5	—	%
On-chip termination resistors ⁽¹⁹⁾	—	—	100	—	—	100	—	Ω
Absolute V _{MAX} ⁽³⁾	Dedicated reference clock pin	—	—	1.6	—	—	1.6	V
	RX reference clock pin	—	—	1.2	—	—	1.2	
Absolute V _{MIN}	—	-0.4	—	—	-0.4	—	—	V
Peak-to-peak differential input voltage	—	200	—	1600	200	—	1600	mV
V _{ICM} (AC coupled)	Dedicated reference clock pin	1050/1000 ⁽²⁾			1050/1000 ⁽²⁾			mV
	RX reference clock pin	1.0/0.9/0.85 ⁽²²⁾			1.0/0.9/0.85 ⁽²²⁾			V
V _{ICM} (DC coupled)	HCSL I/O standard for PCIe reference clock	250	—	550	250	—	550	mV

Table 28. Transceiver Specifications for Stratix V GT Devices (Part 3 of 5) ⁽¹⁾

Symbol/ Description	Conditions	Transceiver Speed Grade 2			Transceiver Speed Grade 3			Unit
		Min	Typ	Max	Min	Typ	Max	
Differential on-chip termination resistors ⁽⁷⁾	GT channels	—	100	—	—	100	—	Ω
Differential on-chip termination resistors for GX channels ⁽¹⁹⁾	85- Ω setting	—	$85 \pm 30\%$	—	—	$85 \pm 30\%$	—	Ω
	100- Ω setting	—	$100 \pm 30\%$	—	—	$100 \pm 30\%$	—	Ω
	120- Ω setting	—	$120 \pm 30\%$	—	—	$120 \pm 30\%$	—	Ω
	150- Ω setting	—	$150 \pm 30\%$	—	—	$150 \pm 30\%$	—	Ω
V _{ICM} (AC coupled)	GT channels	—	650	—	—	650	—	mV
VICM (AC and DC coupled) for GX Channels	VCCR_GXB = 0.85 V or 0.9 V	—	600	—	—	600	—	mV
	VCCR_GXB = 1.0 V full bandwidth	—	700	—	—	700	—	mV
	VCCR_GXB = 1.0 V half bandwidth	—	750	—	—	750	—	mV
t _{LTR} ⁽⁹⁾	—	—	—	10	—	—	10	μ s
t _{LTD} ⁽¹⁰⁾	—	4	—	—	4	—	—	μ s
t _{LTD_manual} ⁽¹¹⁾	—	4	—	—	4	—	—	μ s
t _{LTR_LTD_manual} ⁽¹²⁾	—	15	—	—	15	—	—	μ s
Run Length	GT channels	—	—	72	—	—	72	CID
	GX channels	⁽⁸⁾						
CDR PPM	GT channels	—	—	1000	—	—	1000	\pm PPM
	GX channels	⁽⁸⁾						
Programmable equalization (AC Gain) ⁽⁵⁾	GT channels	—	—	14	—	—	14	dB
	GX channels	⁽⁸⁾						
Programmable DC gain ⁽⁶⁾	GT channels	—	—	7.5	—	—	7.5	dB
	GX channels	⁽⁸⁾						
Differential on-chip termination resistors ⁽⁷⁾	GT channels	—	100	—	—	100	—	Ω
Transmitter								
Supported I/O Standards	—	1.4-V and 1.5-V PCML						
Data rate (Standard PCS)	GX channels	600	—	8500	600	—	8500	Mbps
Data rate (10G PCS)	GX channels	600	—	12,500	600	—	12,500	Mbps

Table 28. Transceiver Specifications for Stratix V GT Devices (Part 5 of 5) ⁽¹⁾

Symbol/ Description	Conditions	Transceiver Speed Grade 2			Transceiver Speed Grade 3			Unit
		Min	Typ	Max	Min	Typ	Max	
t_{pll_lock} ⁽¹⁴⁾	—	—	—	10	—	—	10	μs

Notes to Table 28:

- (1) Speed grades shown refer to the PMA Speed Grade in the device ordering code. The maximum data rate could be restricted by the Core/PCS speed grade. Contact your Altera Sales Representative for the maximum data rate specifications in each speed grade combination offered. For more information about device ordering codes, refer to the *Stratix V Device Overview*.
- (2) The reference clock common mode voltage is equal to the VCCR_GXB power supply level.
- (3) The device cannot tolerate prolonged operation at this absolute maximum.
- (4) The differential eye opening specification at the receiver input pins assumes that receiver equalization is disabled. If you enable receiver equalization, the receiver circuitry can tolerate a lower minimum eye opening, depending on the equalization level.
- (5) Refer to Figure 5 for the GT channel AC gain curves. The total effective AC gain is the AC gain minus the DC gain.
- (6) Refer to Figure 6 for the GT channel DC gain curves.
- (7) CFP2 optical modules require the host interface to have the receiver data pins differentially terminated with 100 Ω. The internal OCT feature is available after the Stratix V FPGA configuration is completed. Altera recommends that FPGA configuration is completed before inserting the optical module. Otherwise, minimize unnecessary removal and insertion with unconfigured devices.
- (8) Specifications for this parameter are the same as for Stratix V GX and GS devices. See Table 23 for specifications.
- (9) t_{LTR} is the time required for the receive CDR to lock to the input reference clock frequency after coming out of reset.
- (10) t_{LTD} is time required for the receiver CDR to start recovering valid data after the $rx_is_lockedto\ data$ signal goes high.
- (11) t_{LTD_manual} is the time required for the receiver CDR to start recovering valid data after the $rx_is_lockedto\ data$ signal goes high when the CDR is functioning in the manual mode.
- (12) $t_{LTR_LTD_manual}$ is the time the receiver CDR must be kept in lock to reference (LTR) mode after the $rx_is_lockedto\ ref$ signal goes high when the CDR is functioning in the manual mode.
- (13) $tp11_powerdown$ is the PLL powerdown minimum pulse width.
- (14) $tp11_lock$ is the time required for the transmitter CMU/ATX PLL to lock to the input reference clock frequency after coming out of reset.
- (15) To calculate the REFCLK rms phase jitter requirement for PCIe at reference clock frequencies other than 100 MHz, use the following formula:
REFCLK rms phase jitter at f(MHz) = REFCLK rms phase jitter at 100 MHz × 100/f.
- (16) The maximum peak to peak differential input voltage V_{ID} after device configuration is equal to $4 \times (\text{absolute } V_{MAX} \text{ for receiver pin} - V_{ICM})$.
- (17) For ES devices, RREF is 2000 Ω ±1%.
- (18) To calculate the REFCLK phase noise requirement at frequencies other than 622 MHz, use the following formula: REFCLK phase noise at f(MHz) = REFCLK phase noise at 622 MHz + 20*log(f/622).
- (19) SFP/+ optical modules require the host interface to have RD+/- differentially terminated with 100 Ω. The internal OCT feature is available after the Stratix V FPGA configuration is completed. Altera recommends that FPGA configuration is completed before inserting the optical module. Otherwise, minimize unnecessary removal and insertion with unconfigured devices.
- (20) Refer to Figure 4.
- (21) For oversampling design to support data rates less than the minimum specification, the CDR needs to be in LTR mode only.
- (22) This supply follows VCCR_GXB for both GX and GT channels.
- (23) When you use fPLL as a TXPLL of the transceiver.

Table 36. High-Speed I/O Specifications for Stratix V Devices ^{(1), (2)} (Part 2 of 4)

Symbol	Conditions	C1			C2, C2L, I2, I2L			C3, I3, I3L, I3YY			C4,I4			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Transmitter														
True Differential I/O Standards - f _{HSDR} (data rate)	SERDES factor J = 3 to 10 ^{(9), (11), (12), (13), (14), (15), (16)}	(6)	—	1600	(6)	—	1434	(6)	—	1250	(6)	—	1050	Mbps
	SERDES factor J ≥ 4 LVDS TX with DPA ^{(12), (14), (15), (16)}	(6)	—	1600	(6)	—	1600	(6)	—	1600	(6)	—	1250	Mbps
	SERDES factor J = 2, uses DDR Registers	(6)	—	(7)	(6)	—	(7)	(6)	—	(7)	(6)	—	(7)	Mbps
	SERDES factor J = 1, uses SDR Register	(6)	—	(7)	(6)	—	(7)	(6)	—	(7)	(6)	—	(7)	Mbps
Emulated Differential I/O Standards with Three External Output Resistor Networks - f _{HSDR} (data rate) ⁽¹⁰⁾	SERDES factor J = 4 to 10 ⁽¹⁷⁾	(6)	—	1100	(6)	—	1100	(6)	—	840	(6)	—	840	Mbps
t _{x Jitter} - True Differential I/O Standards	Total Jitter for Data Rate 600 Mbps - 1.25 Gbps	—	—	160	—	—	160	—	—	160	—	—	160	ps
	Total Jitter for Data Rate < 600 Mbps	—	—	0.1	—	—	0.1	—	—	0.1	—	—	0.1	UI
t _{x Jitter} - Emulated Differential I/O Standards with Three External Output Resistor Network	Total Jitter for Data Rate 600 Mbps - 1.25 Gbps	—	—	300	—	—	300	—	—	300	—	—	325	ps
	Total Jitter for Data Rate < 600 Mbps	—	—	0.2	—	—	0.2	—	—	0.2	—	—	0.25	UI

Figure 7 shows the dynamic phase alignment (DPA) lock time specifications with the DPA PLL calibration option enabled.

Figure 7. DPA Lock Time Specification with DPA PLL Calibration Enabled

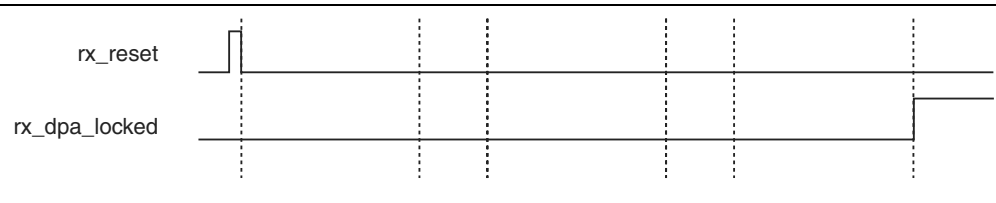


Table 37 lists the DPA lock time specifications for Stratix V devices.

Table 37. DPA Lock Time Specifications for Stratix V GX Devices Only ^{(1), (2), (3)}

Standard	Training Pattern	Number of Data Transitions in One Repetition of the Training Pattern	Number of Repetitions per 256 Data Transitions ⁽⁴⁾	Maximum
SPI-4	00000000001111111111	2	128	640 data transitions
Parallel Rapid I/O	00001111	2	128	640 data transitions
	10010000	4	64	640 data transitions
Miscellaneous	10101010	8	32	640 data transitions
	01010101	8	32	640 data transitions

Notes to Table 37:

- (1) The DPA lock time is for one channel.
- (2) One data transition is defined as a 0-to-1 or 1-to-0 transition.
- (3) The DPA lock time stated in this table applies to both commercial and industrial grade.
- (4) This is the number of repetitions for the stated training pattern to achieve the 256 data transitions.

Figure 8 shows the LVDS soft-clock data recovery (CDR)/DPA sinusoidal jitter tolerance specification for a data rate ≥ 1.25 Gbps. Table 38 lists the LVDS soft-CDR/DPA sinusoidal jitter tolerance specification for a data rate ≥ 1.25 Gbps.

Figure 8. LVDS Soft-CDR/DPA Sinusoidal Jitter Tolerance Specification for a Data Rate ≥ 1.25 Gbps



Table 42. Memory Output Clock Jitter Specification for Stratix V Devices ⁽¹⁾, (Part 2 of 2) ⁽²⁾, ⁽³⁾

Clock Network	Parameter	Symbol	C1		C2, C2L, I2, I2L		C3, I3, I3L, I3YY		C4,I4		Unit
			Min	Max	Min	Max	Min	Max	Min	Max	
PHY Clock	Clock period jitter	$t_{JIT(per)}$	-25	25	-25	25	-30	30	-35	35	ps
	Cycle-to-cycle period jitter	$t_{JIT(cc)}$	-50	50	-50	50	-60	60	-70	70	ps
	Duty cycle jitter	$t_{JIT(duty)}$	-37.5	37.5	-37.5	37.5	-45	45	-56	56	ps

Notes to Table 42:

- (1) The clock jitter specification applies to the memory output clock pins generated using differential signal-splitter and DDIO circuits clocked by a PLL output routed on a PHY, regional, or global clock network as specified. Altera recommends using PHY clock networks whenever possible.
- (2) The clock jitter specification applies to the memory output clock pins clocked by an integer PLL.
- (3) The memory output clock jitter is applicable when an input jitter of 30 ps peak-to-peak is applied with bit error rate (BER) -12, equivalent to 14 sigma.

OCT Calibration Block Specifications

Table 43 lists the OCT calibration block specifications for Stratix V devices.

Table 43. OCT Calibration Block Specifications for Stratix V Devices

Symbol	Description	Min	Typ	Max	Unit
OCTUSRCLK	Clock required by the OCT calibration blocks	—	—	20	MHz
T_{OCTCAL}	Number of OCTUSRCLK clock cycles required for OCT R_S/R_T calibration	—	1000	—	Cycles
$T_{OCTSHIFT}$	Number of OCTUSRCLK clock cycles required for the OCT code to shift out	—	32	—	Cycles
T_{RS_RT}	Time required between the <code>dyn_term_ctrl</code> and <code>oe</code> signal transitions in a bidirectional I/O buffer to dynamically switch between OCT R_S and R_T (Figure 10)	—	2.5	—	ns

Figure 10 shows the timing diagram for the `oe` and `dyn_term_ctrl` signals.

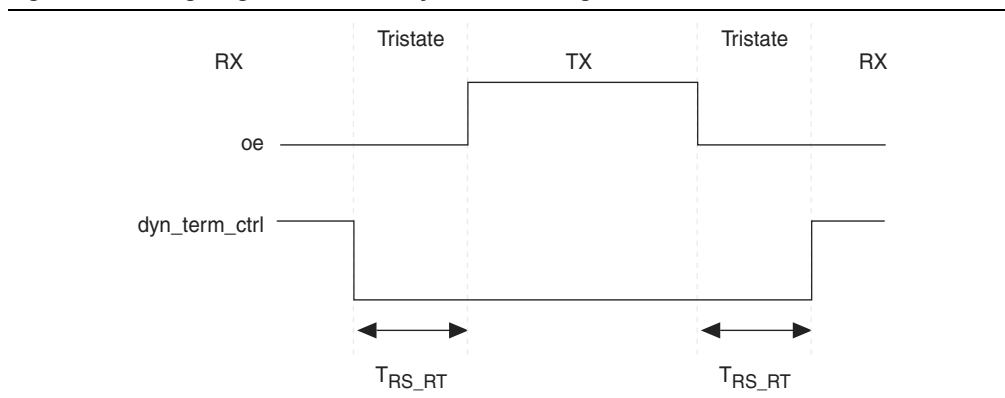
Figure 10. Timing Diagram for `oe` and `dyn_term_ctrl` Signals

Table 48. Minimum Configuration Time Estimation for Stratix V Devices

Variant	Member Code	Active Serial ⁽¹⁾			Fast Passive Parallel ⁽²⁾		
		Width	DCLK (MHz)	Min Config Time (s)	Width	DCLK (MHz)	Min Config Time (s)
GS	D3	4	100	0.344	32	100	0.043
	D4	4	100	0.534	32	100	0.067
		4	100	0.344	32	100	0.043
	D5	4	100	0.534	32	100	0.067
	D6	4	100	0.741	32	100	0.093
	D8	4	100	0.741	32	100	0.093
E	E9	4	100	0.857	32	100	0.107
	EB	4	100	0.857	32	100	0.107

Notes to Table 48:

(1) DCLK frequency of 100 MHz using external CLKUSR.

(2) Max FPGA FPP bandwidth may exceed bandwidth available from some external storage or control logic.

Fast Passive Parallel Configuration Timing

This section describes the fast passive parallel (FPP) configuration timing parameters for Stratix V devices.

DCLK-to-DATA[] Ratio for FPP Configuration

FPP configuration requires a different DCLK-to-DATA [] ratio when you enable the design security, decompression, or both features. Table 49 lists the DCLK-to-DATA [] ratio for each combination.

Table 49. DCLK-to-DATA[] Ratio ⁽¹⁾ (Part 1 of 2)

Configuration Scheme	Decompression	Design Security	DCLK-to-DATA[] Ratio
FPP ×8	Disabled	Disabled	1
	Disabled	Enabled	1
	Enabled	Disabled	2
	Enabled	Enabled	2
FPP ×16	Disabled	Disabled	1
	Disabled	Enabled	2
	Enabled	Disabled	4
	Enabled	Enabled	4

Table 50 lists the timing parameters for Stratix V devices for FPP configuration when the DCLK-to-DATA [] ratio is 1.

Table 50. FPP Timing Parameters for Stratix V Devices ⁽¹⁾

Symbol	Parameter	Minimum	Maximum	Units
t _{CF2CD}	nCONFIG low to CONF_DONE low	—	600	ns
t _{CF2ST0}	nCONFIG low to nSTATUS low	—	600	ns
t _{CFG}	nCONFIG low pulse width	2	—	μs
t _{STATUS}	nSTATUS low pulse width	268	1,506 ⁽²⁾	μs
t _{CF2ST1}	nCONFIG high to nSTATUS high	—	1,506 ⁽³⁾	μs
t _{CF2CK} ⁽⁶⁾	nCONFIG high to first rising edge on DCLK	1,506	—	μs
t _{ST2CK} ⁽⁶⁾	nSTATUS high to first rising edge of DCLK	2	—	μs
t _{DSU}	DATA [] setup time before rising edge on DCLK	5.5	—	ns
t _{DH}	DATA [] hold time after rising edge on DCLK	0	—	ns
t _{CH}	DCLK high time	$0.45 \times 1/f_{\text{MAX}}$	—	s
t _{CL}	DCLK low time	$0.45 \times 1/f_{\text{MAX}}$	—	s
t _{CLK}	DCLK period	$1/f_{\text{MAX}}$	—	s
f _{MAX}	DCLK frequency (FPP $\times 8/\times 16$)	—	125	MHz
	DCLK frequency (FPP $\times 32$)	—	100	MHz
t _{CD2UM}	CONF_DONE high to user mode ⁽⁴⁾	175	437	μs
t _{CD2CU}	CONF_DONE high to CLKUSR enabled	4 × maximum DCLK period	—	—
t _{CD2UMC}	CONF_DONE high to user mode with CLKUSR option on	t _{CD2CU} + (8576 × CLKUSR period) ⁽⁵⁾	—	—

Notes to Table 50:

- (1) Use these timing parameters when the decompression and design security features are disabled.
- (2) This value is applicable if you do not delay configuration by extending the nCONFIG or nSTATUS low pulse width.
- (3) This value is applicable if you do not delay configuration by externally holding the nSTATUS low.
- (4) The minimum and maximum numbers apply only if you chose the internal oscillator as the clock source for initializing the device.
- (5) To enable the CLKUSR pin as the initialization clock source and to obtain the maximum frequency specification on these pins, refer to the Initialization section of the “Configuration, Design Security, and Remote System Upgrades in Stratix V Devices” chapter.
- (6) If nSTATUS is monitored, follow the t_{ST2CK} specification. If nSTATUS is not monitored, follow the t_{CF2CK} specification.

FPP Configuration Timing when DCLK-to-DATA [] > 1

Figure 13 shows the timing waveform for FPP configuration when using a MAX II device, MAX V device, or microprocessor as an external host. This waveform shows timing when the DCLK-to-DATA [] ratio is more than 1.

Figure 13. FPP Configuration Timing Waveform When the DCLK-to-DATA[] Ratio is >1 (1), (2)**Notes to Figure 13:**

- (1) Use this timing waveform and parameters when the DCLK-to-DATA[] ratio is >1. To find out the DCLK-to-DATA[] ratio for your system, refer to Table 49 on page 55.
- (2) The beginning of this waveform shows the device in user mode. In user mode, nCONFIG, nSTATUS, and CONF_DONE are at logic high levels. When nCONFIG is pulled low, a reconfiguration cycle begins.
- (3) After power-up, the Stratix V device holds nSTATUS low for the time as specified by the POR delay.
- (4) After power-up, before and during configuration, CONF_DONE is low.
- (5) Do not leave DCLK floating after configuration. You can drive it high or low, whichever is more convenient.
- (6) "r" denotes the DCLK-to-DATA[] ratio. For the DCLK-to-DATA[] ratio based on the decompression and the design security feature enable settings, refer to Table 49 on page 55.
- (7) If needed, pause DCLK by holding it low. When DCLK restarts, the external host must provide data on the DATA[31..0] pins prior to sending the first DCLK rising edge.
- (8) To ensure a successful configuration, send the entire configuration data to the Stratix V device. CONF_DONE is released high after the Stratix V device receives all the configuration data successfully. After CONF_DONE goes high, send two additional falling edges on DCLK to begin initialization and enter user mode.
- (9) After the option bit to enable the INIT_DONE pin is configured into the device, the INIT_DONE goes low.

Active Serial Configuration Timing

Table 52 lists the DCLK frequency specification in the AS configuration scheme.

Table 52. DCLK Frequency Specification in the AS Configuration Scheme ^{(1), (2)}

Minimum	Typical	Maximum	Unit
5.3	7.9	12.5	MHz
10.6	15.7	25.0	MHz
21.3	31.4	50.0	MHz
42.6	62.9	100.0	MHz

Notes to Table 52:

- (1) This applies to the DCLK frequency specification when using the internal oscillator as the configuration clock source.
- (2) The AS multi-device configuration scheme does not support DCLK frequency of 100 MHz.

Figure 14 shows the single-device configuration setup for an AS ×1 mode.

Figure 14. AS Configuration Timing



Notes to Figure 14:

- (1) If you are using AS ×4 mode, this signal represents the AS_DATA [3 : 0] and EPCQ sends in 4-bits of data for each DCLK cycle.
- (2) The initialization clock can be from internal oscillator or CLKUSR pin.
- (3) After the option bit to enable the INIT_DONE pin is configured into the device, the INIT_DONE goes low.

Table 53 lists the timing parameters for AS ×1 and AS ×4 configurations in Stratix V devices.

Table 53. AS Timing Parameters for AS ×1 and AS ×4 Configurations in Stratix V Devices ^{(1), (2)} (Part 1 of 2)

Symbol	Parameter	Minimum	Maximum	Units
t _{CO}	DCLK falling edge to AS_DATA0/ASDO output	—	2	ns
t _{SU}	Data setup time before falling edge on DCLK	1.5	—	ns
t _H	Data hold time after falling edge on DCLK	0	—	ns

Remote System Upgrades

Table 56 lists the timing parameter specifications for the remote system upgrade circuitry.

Table 56. Remote System Upgrade Circuitry Timing Specifications

Parameter	Minimum	Maximum	Unit
$t_{RU_nCONFIG}^{(1)}$	250	—	ns
$t_{RU_nRSTIMER}^{(2)}$	250	—	ns

Notes to Table 56:

- (1) This is equivalent to strobing the reconfiguration input of the ALTREMOTE_UPDATE megafunction high for the minimum timing specification. For more information, refer to the Remote System Upgrade State Machine section of the “Configuration, Design Security, and Remote System Upgrades in Stratix V Devices” chapter.
- (2) This is equivalent to strobing the reset_timer input of the ALTREMOTE_UPDATE megafunction high for the minimum timing specification. For more information, refer to the User Watchdog Timer section of the “Configuration, Design Security, and Remote System Upgrades in Stratix V Devices” chapter.

User Watchdog Internal Circuitry Timing Specification

Table 57 lists the operating range of the 12.5-MHz internal oscillator.

Table 57. 12.5-MHz Internal Oscillator Specifications

Minimum	Typical	Maximum	Units
5.3	7.9	12.5	MHz

I/O Timing

Altera offers two ways to determine I/O timing—the Excel-based I/O Timing and the Quartus II Timing Analyzer.

Excel-based I/O timing provides pin timing performance for each device density and speed grade. The data is typically used prior to designing the FPGA to get an estimate of the timing budget as part of the link timing analysis. The Quartus II Timing Analyzer provides a more accurate and precise I/O timing data based on the specifics of the design after you complete place-and-route.



You can download the Excel-based I/O Timing spreadsheet from the Stratix V Devices Documentation web page.

Programmable IOE Delay

Table 58 lists the Stratix V IOE programmable delay settings.

Table 58. IOE Programmable Delay for Stratix V Devices (Part 1 of 2)

Parameter (1)	Available Settings	Min Offset (2)	Fast Model		Slow Model							
			Industrial	Commercial	C1	C2	C3	C4	I2	I3, I3YY	I4	Unit
D1	64	0	0.464	0.493	0.838	0.838	0.924	1.011	0.844	0.921	1.006	ns
D2	32	0	0.230	0.244	0.415	0.415	0.459	0.503	0.417	0.456	0.500	ns

Table 60. Glossary (Part 3 of 4)

Letter	Subject	Definitions
S	SW (sampling window)	<p>Timing Diagram—the period of time during which the data must be valid in order to capture it correctly. The setup and hold times determine the ideal strobe position within the sampling window, as shown:</p>
	Single-ended voltage referenced I/O standard	<p>The JEDEC standard for SSTL and HSTL I/O defines both the AC and DC input signal values. The AC values indicate the voltage levels at which the receiver must meet its timing specifications. The DC values indicate the voltage levels at which the final logic state of the receiver is unambiguously defined. After the receiver input has crossed the AC value, the receiver changes to the new logic state.</p> <p>The new logic state is then maintained as long as the input stays beyond the DC threshold. This approach is intended to provide predictable receiver timing in the presence of input waveform ringing:</p> <p><i>Single-Ended Voltage Referenced I/O Standard</i></p>
T	t_c	High-speed receiver and transmitter input and output clock period.
	TCCS (channel-to-channel-skew)	The timing difference between the fastest and slowest output edges, including t_{CO} variation and clock skew, across channels driven by the same PLL. The clock is included in the TCCS measurement (refer to the <i>Timing Diagram</i> figure under SW in this table).
	t_{DUTY}	<p>High-speed I/O block—Duty cycle on the high-speed transmitter output clock.</p> <p>Timing Unit Interval (TUI)</p> <p>The timing budget allowed for skew, propagation delays, and the data sampling window. (TUI = $1/(\text{receiver input clock frequency multiplication factor}) = t_c/w$)</p>
	t_{FALL}	Signal high-to-low transition time (80-20%)
	t_{INCCJ}	Cycle-to-cycle jitter tolerance on the PLL clock input.
	t_{OUTPJ_IO}	Period jitter on the general purpose I/O driven by a PLL.
	t_{OUTPJ_DC}	Period jitter on the dedicated clock output driven by a PLL.
	t_{RISE}	Signal low-to-high transition time (20-80%)
U	—	—

