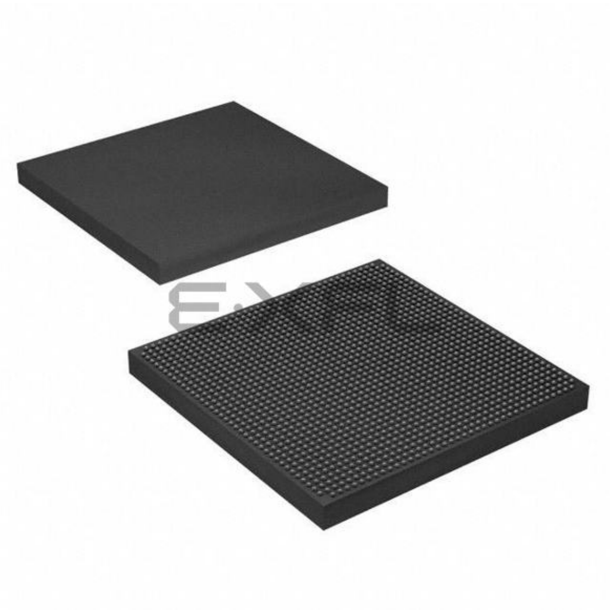

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The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	158500
Number of Logic Elements/Cells	420000
Total RAM Bits	37888000
Number of I/O	600
Number of Gates	-
Voltage - Supply	0.87V ~ 0.93V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	1517-BBGA, FCBGA
Supplier Device Package	1517-FBGA (40x40)
Purchase URL	https://www.e-xfl.com/product-detail/intel/5sgxma4k1f40i2n

Table 6. Recommended Operating Conditions for Stratix V Devices (Part 2 of 2)

Symbol	Description	Condition	Min (4)	Typ	Max (4)	Unit
t_{RAMP}	Power supply ramp time	Standard POR	200 µs	—	100 ms	—
		Fast POR	200 µs	—	4 ms	—

Notes to Table 6:

(1) V_{CCPD} must be 2.5 V when V_{CCIO} is 2.5, 1.8, 1.5, 1.35, 1.25 or 1.2 V. V_{CCPD} must be 3.0 V when V_{CCIO} is 3.0 V.

(2) If you do not use the design security feature in Stratix V devices, connect V_{CCBAT} to a 1.2- to 3.0-V power supply. Stratix V power-on-reset (POR) circuitry monitors V_{CCBAT}. Stratix V devices will not exit POR if V_{CCBAT} stays at logic low.

(3) C2L and I2L can also be run at 0.90 V for legacy boards that were designed for the C2 and I2 speed grades.

(4) The power supply value describes the budget for the DC (static) power supply tolerance and does not include the dynamic tolerance requirements. Refer to the PDN tool for the additional budget for the dynamic tolerance requirements.

Table 7 lists the transceiver power supply recommended operating conditions for Stratix V GX, GS, and GT devices.

Table 7. Recommended Transceiver Power Supply Operating Conditions for Stratix V GX, GS, and GT Devices (Part 1 of 2)

Symbol	Description	Devices	Minimum (4)	Typical	Maximum (4)	Unit
V_{CCA_GXBL} (1), (3)	Transceiver channel PLL power supply (left side)	GX, GS, GT	2.85	3.0	3.15	V
			2.375	2.5	2.625	
V_{CCA_GXBR} (1), (3)	Transceiver channel PLL power supply (right side)	GX, GS	2.85	3.0	3.15	V
			2.375	2.5	2.625	
V_{CCA_GTBR}	Transceiver channel PLL power supply (right side)	GT	2.85	3.0	3.15	V
V_{CCHIP_L}	Transceiver hard IP power supply (left side; C1, C2, I2, and I3YY speed grades)	GX, GS, GT	0.87	0.9	0.93	V
	Transceiver hard IP power supply (left side; C2L, C3, C4, I2L, I3, I3L, and I4 speed grades)	GX, GS, GT	0.82	0.85	0.88	V
V_{CCHIP_R}	Transceiver hard IP power supply (right side; C1, C2, I2, and I3YY speed grades)	GX, GS, GT	0.87	0.9	0.93	V
	Transceiver hard IP power supply (right side; C2L, C3, C4, I2L, I3, I3L, and I4 speed grades)	GX, GS, GT	0.82	0.85	0.88	V
V_{CCHSSI_L}	Transceiver PCS power supply (left side; C1, C2, I2, and I3YY speed grades)	GX, GS, GT	0.87	0.9	0.93	V
	Transceiver PCS power supply (left side; C2L, C3, C4, I2L, I3, I3L, and I4 speed grades)	GX, GS, GT	0.82	0.85	0.88	V
V_{CCHSSI_R}	Transceiver PCS power supply (right side; C1, C2, I2, and I3YY speed grades)	GX, GS, GT	0.87	0.9	0.93	V
	Transceiver PCS power supply (right side; C2L, C3, C4, I2L, I3, I3L, and I4 speed grades)	GX, GS, GT	0.82	0.85	0.88	V
V_{CCR_GXBL} (2)	Receiver analog power supply (left side)	GX, GS, GT	0.82	0.85	0.88	V
			0.87	0.90	0.93	
			0.97	1.0	1.03	
			1.03	1.05	1.07	

I/O Pin Leakage Current

Table 9 lists the Stratix V I/O pin leakage current specifications.

Table 9. I/O Pin Leakage Current for Stratix V Devices (1)

Symbol	Description	Conditions	Min	Typ	Max	Unit
I_I	Input pin	V_I = 0 V to $V_{CCIOMAX}$	–30	—	30	µA
I_{OZ}	Tri-stated I/O pin	V_O = 0 V to $V_{CCIOMAX}$	–30	—	30	µA

Note to Table 9:

(1) If V_O = V_{CCIO} to $V_{CCIOMax}$, 100 µA of leakage current per I/O is expected.

Bus Hold Specifications

Table 10 lists the Stratix V device family bus hold specifications.

Table 10. Bus Hold Parameters for Stratix V Devices

Parameter	Symbol	Conditions	V_{CCIO}										Unit
			1.2 V		1.5 V		1.8 V		2.5 V		3.0 V		
			Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Low sustaining current	I_{SUSL}	$V_{IN} > V_{IL}$ (maximum)	22.5	—	25.0	—	30.0	—	50.0	—	70.0	—	µA
High sustaining current	I_{SUSH}	$V_{IN} < V_{IH}$ (minimum)	–22.5	—	–25.0	—	–30.0	—	–50.0	—	–70.0	—	µA
Low overdrive current	I_{ODL}	$0V < V_{IN} < V_{CCIO}$	—	120	—	160	—	200	—	300	—	500	µA
High overdrive current	I_{ODH}	$0V < V_{IN} < V_{CCIO}$	—	–120	—	–160	—	–200	—	–300	—	–500	µA
Bus-hold trip point	V_{TRIP}	—	0.45	0.95	0.50	1.00	0.68	1.07	0.70	1.70	0.80	2.00	V

On-Chip Termination (OCT) Specifications

If you enable OCT calibration, calibration is automatically performed at power-up for I/Os connected to the calibration block. Table 11 lists the Stratix V OCT termination calibration accuracy specifications.

Table 11. OCT Calibration Accuracy Specifications for Stratix V Devices (1) (Part 1 of 2)

Symbol	Description	Conditions	Calibration Accuracy				Unit
			C1	C2,I2	C3,I3, I3YY	C4,I4	
25-Ω R_S	Internal series termination with calibration (25-Ω setting)	V_{CCIO} = 3.0, 2.5, 1.8, 1.5, 1.2 V	±15	±15	±15	±15	%

Table 12. OCT Without Calibration Resistance Tolerance Specifications for Stratix V Devices (Part 2 of 2)

Symbol	Description	Conditions	Resistance Tolerance				Unit
			C1	C2,I2	C3, I3, I3YY	C4, I4	
50-Ω R_S	Internal series termination without calibration (50-Ω setting)	V_{CCIO} = 1.8 and 1.5 V	±30	±30	±40	±40	%
50-Ω R_S	Internal series termination without calibration (50-Ω setting)	V_{CCIO} = 1.2 V	±35	±35	±50	±50	%
100-Ω R_D	Internal differential termination (100-Ω setting)	V_{CCPD} = 2.5 V	±25	±25	±25	±25	%

Calibration accuracy for the calibrated series and parallel OCTs are applicable at the moment of calibration. When voltage and temperature conditions change after calibration, the tolerance may change.

OCT calibration is automatically performed at power-up for OCT-enabled I/Os. Table 13 lists the OCT variation with temperature and voltage after power-up calibration. Use Table 13 to determine the OCT variation after power-up calibration and Equation 1 to determine the OCT variation without recalibration.

Equation 1. OCT Variation Without Recalibration for Stratix V Devices *(1), (2), (3), (4), (5), (6)*

$$R_{OCT} = R_{SCAL}\left(1 + \langle \frac{dR}{dT} \times \Delta T\rangle \pm \langle \frac{dR}{dV} \times \Delta V\rangle\right)$$

Notes to Equation 1:

(1) The R_{OCT} value shows the range of OCT resistance with the variation of temperature and V_{CCIO}.

(2) R_{SCAL} is the OCT resistance value at power-up.

(3) ΔT is the variation of temperature with respect to the temperature at power-up.

(4) ΔV is the variation of voltage with respect to the V_{CCIO} at power-up.

(5) dR/dT is the percentage change of R_{SCAL} with temperature.

(6) dR/dV is the percentage change of R_{SCAL} with voltage.

Table 13 lists the on-chip termination variation after power-up calibration.

Table 13. OCT Variation after Power-Up Calibration for Stratix V Devices (Part 1 of 2) *(1)*

Symbol	Description	V_{CCIO} (V)	Typical	Unit
dR/dV	OCT variation with voltage without recalibration	3.0	0.0297	%/mV
		2.5	0.0344	
		1.8	0.0499	
		1.5	0.0744	
		1.2	0.1241	

Internal Weak Pull-Up Resistor

Table 16 lists the weak pull-up resistor values for Stratix V devices.

Table 16. Internal Weak Pull-Up Resistor for Stratix V Devices (1), (2)

Symbol	Description	V_{CCIO} Conditions (V) (3)	Value (4)	Unit
R_{PU}	Value of the I/O pin pull-up resistor before and during configuration, as well as user mode if you enable the programmable pull-up resistor option.	3.0 ±5%	25	kΩ
		2.5 ±5%	25	kΩ
		1.8 ±5%	25	kΩ
		1.5 ±5%	25	kΩ
		1.35 ±5%	25	kΩ
		1.25 ±5%	25	kΩ
		1.2 ±5%	25	kΩ

Notes to Table 16:

(1) All I/O pins have an option to enable the weak pull-up resistor except the configuration, test, and JTAG pins.

(2) The internal weak pull-down feature is only available for the JTAG TCK pin. The typical value for this internal weak pull-down resistor is approximately 25 kΩ.

(3) The pin pull-up resistance values may be lower if an external source drives the pin higher than V_{CCIO}.

(4) These specifications are valid with a ±10% tolerance to cover changes over PVT.

I/O Standard Specifications

Table 17 through Table 22 list the input voltage (V_{IH} and V_{IL}), output voltage (V_{OH} and V_{OL}), and current drive characteristics (I_{OH} and I_{OL}) for various I/O standards supported by Stratix V devices. These tables also show the Stratix V device family I/O standard specifications. The V_{OL} and V_{OH} values are valid at the corresponding I_{OH} and I_{OL}, respectively.

For an explanation of the terms used in Table 17 through Table 22, refer to "Glossary" on page 65. For tolerance calculations across all SSTL and HSTL I/O standards, refer to Altera knowledge base solution rd07262012_486.

Table 17. Single-Ended I/O Standards for Stratix V Devices

I/O Standard	V_{CCIO} (V)			V_{IL} (V)		V_{IH} (V)		V_{OL} (V)	V_{OH} (V)	I_{OL} (mA)	I_{OH} (mA)
	Min	Typ	Max	Min	Max	Min	Max	Max	Min		
LVTTL	2.85	3	3.15	–0.3	0.8	1.7	3.6	0.4	2.4	2	–2
LVCMOS	2.85	3	3.15	–0.3	0.8	1.7	3.6	0.2	V_{CCIO} – 0.2	0.1	–0.1
2.5 V	2.375	2.5	2.625	–0.3	0.7	1.7	3.6	0.4	2	1	–1
1.8 V	1.71	1.8	1.89	–0.3	0.35 * V_{CCIO}	0.65 * V_{CCIO}	V_{CCIO} + 0.3	0.45	V_{CCIO} – 0.45	2	–2
1.5 V	1.425	1.5	1.575	–0.3	0.35 * V_{CCIO}	0.65 * V_{CCIO}	V_{CCIO} + 0.3	0.25 * V_{CCIO}	0.75 * V_{CCIO}	2	–2
1.2 V	1.14	1.2	1.26	–0.3	0.35 * V_{CCIO}	0.65 * V_{CCIO}	V_{CCIO} + 0.3	0.25 * V_{CCIO}	0.75 * V_{CCIO}	2	–2

Table 18. Single-Ended SSTL, HSTL, and HSUL I/O Reference Voltage Specifications for Stratix V Devices

I/O Standard	V_{CCIO} (V)			V_{REF} (V)			V_{TT} (V)		
	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max
SSTL-2 Class I, II	2.375	2.5	2.625	0.49 * V_{CCIO}	0.5 * V_{CCIO}	0.51 * V_{CCIO}	V_{REF} – 0.04	V_{REF}	V_{REF} + 0.04
SSTL-18 Class I, II	1.71	1.8	1.89	0.833	0.9	0.969	V_{REF} – 0.04	V_{REF}	V_{REF} + 0.04
SSTL-15 Class I, II	1.425	1.5	1.575	0.49 * V_{CCIO}	0.5 * V_{CCIO}	0.51 * V_{CCIO}	0.49 * V_{CCIO}	0.5 * VCCIO	0.51 * V_{CCIO}
SSTL-135 Class I, II	1.283	1.35	1.418	0.49 * V_{CCIO}	0.5 * V_{CCIO}	0.51 * V_{CCIO}	0.49 * V_{CCIO}	0.5 * V_{CCIO}	0.51 * V_{CCIO}
SSTL-125 Class I, II	1.19	1.25	1.26	0.49 * V_{CCIO}	0.5 * V_{CCIO}	0.51 * V_{CCIO}	0.49 * V_{CCIO}	0.5 * VCCIO	0.51 * V_{CCIO}
SSTL-12 Class I, II	1.14	1.20	1.26	0.49 * V_{CCIO}	0.5 * V_{CCIO}	0.51 * V_{CCIO}	0.49 * V_{CCIO}	0.5 * VCCIO	0.51 * V_{CCIO}
HSTL-18 Class I, II	1.71	1.8	1.89	0.85	0.9	0.95	—	V_{CCIO}/2	—
HSTL-15 Class I, II	1.425	1.5	1.575	0.68	0.75	0.9	—	V_{CCIO}/2	—
HSTL-12 Class I, II	1.14	1.2	1.26	0.47 * V_{CCIO}	0.5 * V_{CCIO}	0.53 * V_{CCIO}	—	V_{CCIO}/2	—
HSUL-12	1.14	1.2	1.3	0.49 * V_{CCIO}	0.5 * V_{CCIO}	0.51 * V_{CCIO}	—	—	—

Table 19. Single-Ended SSTL, HSTL, and HSUL I/O Standards Signal Specifications for Stratix V Devices (Part 1 of 2)

I/O Standard	$V_{IL(DC)}$ (V)		$V_{IH(DC)}$ (V)		$V_{IL(AC)}$ (V)	$V_{IH(AC)}$ (V)	V_{OL} (V)	V_{OH} (V)	I_{ol} (mA)	I_{oh} (mA)
	Min	Max	Min	Max	Max	Min	Max	Min		
SSTL-2 Class I	–0.3	V_{REF} – 0.15	V_{REF} + 0.15	V_{CCIO} + 0.3	V_{REF} – 0.31	V_{REF} + 0.31	V_{TT} – 0.608	V_{TT} + 0.608	8.1	–8.1
SSTL-2 Class II	–0.3	V_{REF} – 0.15	V_{REF} + 0.15	V_{CCIO} + 0.3	V_{REF} – 0.31	V_{REF} + 0.31	V_{TT} – 0.81	V_{TT} + 0.81	16.2	–16.2
SSTL-18 Class I	–0.3	V_{REF} – 0.125	V_{REF} + 0.125	V_{CCIO} + 0.3	V_{REF} – 0.25	V_{REF} + 0.25	V_{TT} – 0.603	V_{TT} + 0.603	6.7	–6.7
SSTL-18 Class II	–0.3	V_{REF} – 0.125	V_{REF} + 0.125	V_{CCIO} + 0.3	V_{REF} – 0.25	V_{REF} + 0.25	0.28	V_{CCIO} – 0.28	13.4	–13.4
SSTL-15 Class I	—	V_{REF} – 0.1	V_{REF} + 0.1	—	V_{REF} – 0.175	V_{REF} + 0.175	0.2 * V_{CCIO}	0.8 * V_{CCIO}	8	–8
SSTL-15 Class II	—	V_{REF} – 0.1	V_{REF} + 0.1	—	V_{REF} – 0.175	V_{REF} + 0.175	0.2 * V_{CCIO}	0.8 * V_{CCIO}	16	–16
SSTL-135 Class I, II	—	V_{REF} – 0.09	V_{REF} + 0.09	—	V_{REF} – 0.16	V_{REF} + 0.16	0.2 * V_{CCIO}	0.8 * V_{CCIO}	—	—
SSTL-125 Class I, II	—	V_{REF} – 0.85	V_{REF} + 0.85	—	V_{REF} – 0.15	V_{REF} + 0.15	0.2 * V_{CCIO}	0.8 * V_{CCIO}	—	—
SSTL-12 Class I, II	—	V_{REF} – 0.1	V_{REF} + 0.1	—	V_{REF} – 0.15	V_{REF} + 0.15	0.2 * V_{CCIO}	0.8 * V_{CCIO}	—	—

Table 23. Transceiver Specifications for Stratix V GX and GS Devices (1) (Part 3 of 7)

Symbol/ Description	Conditions	Transceiver Speed Grade 1			Transceiver Speed Grade 2			Transceiver Speed Grade 3			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Reconfiguration clock (`mgmt_clk_clk`) frequency	—	100	—	125	100	—	125	100	—	125	MHz
Receiver											
Supported I/O Standards	—	1.4-V PCML, 1.5-V PCML, 2.5-V PCML, LVPECL, and LVDS									
Data rate (Standard PCS) (9), (23)	—	600	—	12200	600	—	12200	600	—	8500/ 10312.5 (24)	Mbps
Data rate (10G PCS) (9), (23)	—	600	—	14100	600	—	12500	600	—	8500/ 10312.5 (24)	Mbps
Absolute V_{MAX} for a receiver pin (5)	—	—	—	1.2	—	—	1.2	—	—	1.2	V
Absolute V_{MIN} for a receiver pin	—	–0.4	—	—	–0.4	—	—	–0.4	—	—	V
Maximum peak-to-peak differential input voltage V_{ID} (diff p-p) before device configuration (22)	—	—	—	1.6	—	—	1.6	—	—	1.6	V
Maximum peak-to-peak differential input voltage V_{ID} (diff p-p) after device configuration (18), (22)	V_{CCR_GXB} = 1.0 V/1.05 V (V_{ICM} = 0.70 V)	—	—	2.0	—	—	2.0	—	—	2.0	V
	V_{CCR_GXB} = 0.90 V (V_{ICM} = 0.6 V)	—	—	2.4	—	—	2.4	—	—	2.4	V
	V_{CCR_GXB} = 0.85 V (V_{ICM} = 0.6 V)	—	—	2.4	—	—	2.4	—	—	2.4	V
Minimum differential eye opening at receiver serial input pins (6), (22), (27)	—	85	—	—	85	—	—	85	—	—	mV

Table 23. Transceiver Specifications for Stratix V GX and GS Devices (1) (Part 4 of 7)

Symbol/ Description	Conditions	Transceiver Speed Grade 1			Transceiver Speed Grade 2			Transceiver Speed Grade 3			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Differential on-chip termination resistors (21)	85–Ω setting	—	85 ± 30%	—	—	85 ± 30%	—	—	85 ± 30%	—	Ω
	100–Ω setting	—	100 ± 30%	—	—	100 ± 30%	—	—	100 ± 30%	—	Ω
	120–Ω setting	—	120 ± 30%	—	—	120 ± 30%	—	—	120 ± 30%	—	Ω
	150-Ω setting	—	150 ± 30%	—	—	150 ± 30%	—	—	150 ± 30%	—	Ω
V_{ICM} (AC and DC coupled)	V_{CCR_GXB} = 0.85 V or 0.9 V full bandwidth	—	600	—	—	600	—	—	600	—	mV
	V_{CCR_GXB} = 0.85 V or 0.9 V half bandwidth	—	600	—	—	600	—	—	600	—	mV
	V_{CCR_GXB} = 1.0 V/1.05 V full bandwidth	—	700	—	—	700	—	—	700	—	mV
	V_{CCR_GXB} = 1.0 V half bandwidth	—	750	—	—	750	—	—	750	—	mV
t_{LTR} (11)	—	—	—	10	—	—	10	—	—	10	µs
t_{LTD} (12)	—	4	—	—	4	—	—	4	—	—	µs
t_{LTD_manual} (13)	—	4	—	—	4	—	—	4	—	—	µs
$t_{LTR\_LTD\_manual}$ (14)	—	15	—	—	15	—	—	15	—	—	µs
Run Length	—	—	—	200	—	—	200	—	—	200	UI
Programmable equalization (AC Gain) (10)	Full bandwidth (6.25 GHz) Half bandwidth (3.125 GHz)	—	—	16	—	—	16	—	—	16	dB

Table 23. Transceiver Specifications for Stratix V GX and GS Devices *(1)* **(Part 7 of 7)**

Symbol/ Description	Conditions	Transceiver Speed Grade 1			Transceiver Speed Grade 2			Transceiver Speed Grade 3			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
t_{pll_lock} *(16)*	—	—	—	10	—	—	10	—	—	10	µs

Notes to Table 23:

(1) Speed grades shown in Table 23 refer to the PMA Speed Grade in the device ordering code. The maximum data rate could be restricted by the Core/PCS speed grade. Contact your Altera Sales Representative for the maximum data rate specifications in each speed grade combination offered. For more information about device ordering codes, refer to the *Stratix V Device Overview*.

(2) The reference clock common mode voltage is equal to the V_{CCR_GXB} power supply level.

(3) This supply must be connected to 1.0 V if the transceiver is configured at a data rate > 6.5 Gbps, and to 1.05 V if configured at a data rate > 10.3 Gbps when DFE is used. For data rates up to 6.5 Gbps, you can connect this supply to 0.85 V.

(4) This supply follows VCCR_GXB.

(5) The device cannot tolerate prolonged operation at this absolute maximum.

(6) The differential eye opening specification at the receiver input pins assumes that **Receiver Equalization** is disabled. If you enable **Receiver Equalization**, the receiver circuitry can tolerate a lower minimum eye opening, depending on the equalization level.

(7) The Quartus II software automatically selects the appropriate slew rate depending on the configured data rate or functional mode.

(8) The input reference clock frequency options depend on the data rate and the device speed grade.

(9) The line data rate may be limited by PCS-FPGA interface speed grade.

(10) Refer to Figure 1 for the GX channel AC gain curves. The total effective AC gain is the AC gain minus the DC gain.

(11) t_{LTR} is the time required for the receive CDR to lock to the input reference clock frequency after coming out of reset.

(12) t_{LTD} is time required for the receiver CDR to start recovering valid data after the rx_is_lockedtodata signal goes high.

(13) t_{LTD_manual} is the time required for the receiver CDR to start recovering valid data after the rx_is_lockedtodata signal goes high when the CDR is functioning in the manual mode.

(14) $t_{LTR\_LTD\_manual}$ is the time the receiver CDR must be kept in lock to reference (LTR) mode after the rx_is_lockedtoref signal goes high when the CDR is functioning in the manual mode.

(15) $t_{pll\_powerdown}$ is the PLL powerdown minimum pulse width.

(16) t_{pll_lock} is the time required for the transmitter CMU/ATX PLL to lock to the input reference clock frequency after coming out of reset.

(17) To calculate the REFCLK rms phase jitter requirement for PCIe at reference clock frequencies other than 100 MHz, use the following formula: REFCLK rms phase jitter at f(MHz) = REFCLK rms phase jitter at 100 MHz × 100/f.

(18) The maximum peak to peak differential input voltage V_{ID} after device configuration is equal to 4 × (absolute V_{MAX} for receiver pin - V_{ICM}).

(19) For ES devices, R_{REF} is 2000 Ω ±1%.

(20) To calculate the REFCLK phase noise requirement at frequencies other than 622 MHz, use the following formula: REFCLK phase noise at f(MHz) = REFCLK phase noise at 622 MHz + 20*log(f/622).

(21) SFP/+ optical modules require the host interface to have RD+/- differentially terminated with 100 Ω. The internal OCT feature is available after the Stratix V FPGA configuration is completed. Altera recommends that FPGA configuration is completed before inserting the optical module. Otherwise, minimize unnecessary removal and insertion with unconfigured devices.

(22) Refer to Figure 2.

(23) For oversampling designs to support data rates less than the minimum specification, the CDR needs to be in LTR mode only.

(24) I3YY devices can achieve data rates up to 10.3125 Gbps.

(25) When you use fPLL as a TXPLL of the transceiver.

(26) `REFCLK` performance requires to meet transmitter `REFCLK` phase noise specification.

(27) Minimum eye opening of 85 mV is only for the unstressed input eye condition.

Table 28. Transceiver Specifications for Stratix V GT Devices (Part 1 of 5) *(1)*

Symbol/ Description	Conditions	Transceiver Speed Grade 2			Transceiver Speed Grade 3			Unit
		Min	Typ	Max	Min	Typ	Max	
Reference Clock								
Supported I/O Standards	Dedicated reference clock pin	1.2-V PCML, 1.4-V PCML, 1.5-V PCML, 2.5-V PCML, Differential LVPECL, LVDS, and HCSL						
	RX reference clock pin	1.4-V PCML, 1.5-V PCML, 2.5-V PCML, LVPECL, and LVDS						
Input Reference Clock Frequency (CMU PLL) *(6)*	—	40	—	710	40	—	710	MHz
Input Reference Clock Frequency (ATX PLL) *(6)*	—	100	—	710	100	—	710	MHz
Rise time	20% to 80%	—	—	400	—	—	400	ps
Fall time	80% to 20%	—	—	400	—	—	400	
Duty cycle	—	45	—	55	45	—	55	%
Spread-spectrum modulating clock frequency	PCI Express (PCIe)	30	—	33	30	—	33	kHz
Spread-spectrum downspread	PCIe	—	0 to –0.5	—	—	0 to –0.5	—	%
On-chip termination resistors *(19)*	—	—	100	—	—	100	—	Ω
Absolute V_{MAX} *(3)*	Dedicated reference clock pin	—	—	1.6	—	—	1.6	V
	RX reference clock pin	—	—	1.2	—	—	1.2	
Absolute V_{MIN}	—	-0.4	—	—	-0.4	—	—	V
Peak-to-peak differential input voltage	—	200	—	1600	200	—	1600	mV
V_{ICM} (AC coupled)	Dedicated reference clock pin	1050/1000 *(2)*			1050/1000 *(2)*			mV
	RX reference clock pin	1.0/0.9/0.85 *(22)*			1.0/0.9/0.85 *(22)*			V
V_{ICM} (DC coupled)	HCSL I/O standard for PCIe reference clock	250	—	550	250	—	550	mV

Table 28. Transceiver Specifications for Stratix V GT Devices (Part 5 of 5) *(1)*

Symbol/ Description	Conditions	Transceiver Speed Grade 2			Transceiver Speed Grade 3			Unit
		Min	Typ	Max	Min	Typ	Max	
t_{pll_lock} *(14)*	—	—	—	10	—	—	10	µs

Notes to Table 28:

(1) Speed grades shown refer to the PMA Speed Grade in the device ordering code. The maximum data rate could be restricted by the Core/PCS speed grade. Contact your Altera Sales Representative for the maximum data rate specifications in each speed grade combination offered. For more information about device ordering codes, refer to the *Stratix V Device Overview*.

(2) The reference clock common mode voltage is equal to the VCCR_GXB power supply level.

(3) The device cannot tolerate prolonged operation at this absolute maximum.

(4) The differential eye opening specification at the receiver input pins assumes that receiver equalization is disabled. If you enable receiver equalization, the receiver circuitry can tolerate a lower minimum eye opening, depending on the equalization level.

(5) Refer to Figure 5 for the GT channel AC gain curves. The total effective AC gain is the AC gain minus the DC gain.

(6) Refer to Figure 6 for the GT channel DC gain curves.

(7) CFP2 optical modules require the host interface to have the receiver data pins differentially terminated with 100 Ω. The internal OCT feature is available after the Stratix V FPGA configuration is completed. Altera recommends that FPGA configuration is completed before inserting the optical module. Otherwise, minimize unnecessary removal and insertion with unconfigured devices.

(8) Specifications for this parameter are the same as for Stratix V GX and GS devices. See Table 23 for specifications.

(9) t_{LTR} is the time required for the receive CDR to lock to the input reference clock frequency after coming out of reset.

(10) t_{LTD} is time required for the receiver CDR to start recovering valid data after the `rx_is_lockedtodata` signal goes high.

(11) t_{LTD_manual} is the time required for the receiver CDR to start recovering valid data after the `rx_is_lockedtodata` signal goes high when the CDR is functioning in the manual mode.

(12) $t_{LTR\_LTD\_manual}$ is the time the receiver CDR must be kept in lock to reference (LTR) mode after the `rx_is_lockedtoref` signal goes high when the CDR is functioning in the manual mode.

(13) `tpll_powerdown` is the PLL powerdown minimum pulse width.

(14) `tpll_lock` is the time required for the transmitter CMU/ATX PLL to lock to the input reference clock frequency after coming out of reset.

(15) To calculate the REFCLK rms phase jitter requirement for PCIe at reference clock frequencies other than 100 MHz, use the following formula: REFCLK rms phase jitter at f(MHz) = REFCLK rms phase jitter at 100 MHz × 100/f.

(16) The maximum peak to peak differential input voltage V_{ID} after device configuration is equal to 4 × (absolute V_{MAX} for receiver pin - V_{ICM}).

(17) For ES devices, RREF is 2000 Ω ±1%.

(18) To calculate the REFCLK phase noise requirement at frequencies other than 622 MHz, use the following formula: REFCLK phase noise at f(MHz) = REFCLK phase noise at 622 MHz + 20*log(f/622).

(19) SFP/+ optical modules require the host interface to have RD+/- differentially terminated with 100 Ω. The internal OCT feature is available after the Stratix V FPGA configuration is completed. Altera recommends that FPGA configuration is completed before inserting the optical module. Otherwise, minimize unnecessary removal and insertion with unconfigured devices.

(20) Refer to Figure 4.

(21) For oversampling design to support data rates less than the minimum specification, the CDR needs to be in LTR mode only.

(22) This supply follows VCCR_GXB for both GX and GT channels.

(23) When you use fPLL as a TXPLL of the transceiver.

Table 32. Block Performance Specifications for Stratix V DSP Devices (Part 2 of 2)

Mode	Peformance							Unit
	C1	C2, C2L	I2, I2L	C3	I3, I3L, I3YY	C4	I4	
Modes using Three DSPs								
One complex 18 x 25	425	425	415	340	340	275	265	MHz
Modes using Four DSPs								
One complex 27 x 27	465	465	465	380	380	300	290	MHz

Memory Block Specifications

Table 33 lists the Stratix V memory block specifications.

Table 33. Memory Block Performance Specifications for Stratix V Devices (1), (2) (Part 1 of 2)

Memory	Mode	Resources Used		Performance							Unit
		ALUTs	Memory	C1	C2, C2L	C3	C4	I2, I2L	I3, I3L, I3YY	I4	
MLAB	Single port, all supported widths	0	1	450	450	400	315	450	400	315	MHz
	Simple dual-port, x32/x64 depth	0	1	450	450	400	315	450	400	315	MHz
	Simple dual-port, x16 depth (3)	0	1	675	675	533	400	675	533	400	MHz
	ROM, all supported widths	0	1	600	600	500	450	600	500	450	MHz

Periphery Performance

This section describes periphery performance, including high-speed I/O and external memory interface.

I/O performance supports several system interfaces, such as the **LVDS** high-speed I/O interface, external memory interface, and the **PCI/PCI-X** bus interface. General-purpose I/O standards such as 3.3-, 2.5-, 1.8-, and 1.5-**LVTTL/LVCMOS** are capable of a typical 167 MHz and 1.2-**LVCMOS** at 100 MHz interfacing frequency with a 10 pF load.

☞ The actual achievable frequency depends on design- and system-specific factors. Ensure proper timing closure in your design and perform HSPICE/IBIS simulations based on your specific design and system setup to determine the maximum achievable frequency in your system.

High-Speed I/O Specification

Table 36 lists high-speed I/O timing for Stratix V devices.

Table 36. High-Speed I/O Specifications for Stratix V Devices (1), (2) (Part 1 of 4)

Symbol	Conditions	C1			C2, C2L, I2, I2L			C3, I3, I3L, I3YY			C4,I4			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
f_{HSCLK_in} (input clock frequency) True Differential I/O Standards	Clock boost factor W = 1 to 40 (4)	5	—	800	5	—	800	5	—	625	5	—	525	MHz
f_{HSCLK_in} (input clock frequency) Single Ended I/O Standards (3)	Clock boost factor W = 1 to 40 (4)	5	—	800	5	—	800	5	—	625	5	—	525	MHz
f_{HSCLK_in} (input clock frequency) Single Ended I/O Standards	Clock boost factor W = 1 to 40 (4)	5	—	520	5	—	520	5	—	420	5	—	420	MHz
f_{HSCLK_OUT} (output clock frequency)	—	5	—	800	5	—	800	5	—	625 (5)	5	—	525 (5)	MHz

Table 36. High-Speed I/O Specifications for Stratix V Devices *(1), (2)* **(Part 4 of 4)**

Symbol	Conditions	C1			C2, C2L, I2, I2L			C3, I3, I3L, I3YY			C4,I4			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
f_{HSDR} (data rate)	SERDES factor J = 3 to 10	*(6)*	—	*(8)*	*(6)*	—	*(8)*	*(6)*	—	*(8)*	*(6)*	—	*(8)*	Mbps
	SERDES factor J = 2, uses DDR Registers	*(6)*	—	*(7)*	*(6)*	—	*(7)*	*(6)*	—	*(7)*	*(6)*	—	*(7)*	Mbps
	SERDES factor J = 1, uses SDR Register	*(6)*	—	*(7)*	*(6)*	—	*(7)*	*(6)*	—	*(7)*	*(6)*	—	*(7)*	Mbps
DPA Mode														
DPA run length	—	—	—	10000	—	—	10000	—	—	10000	—	—	10000	UI
Soft CDR mode														
Soft-CDR PPM tolerance	—	—	—	300	—	—	300	—	—	300	—	—	300	± PPM
Non DPA Mode														
Sampling Window	—	—	—	300	—	—	300	—	—	300	—	—	300	ps

Notes to Table 36:

(1) When J = 3 to 10, use the serializer/deserializer (SERDES) block.

(2) When J = 1 or 2, bypass the SERDES block.

(3) This only applies to DPA and soft-CDR modes.

(4) Clock Boost Factor (W) is the ratio between the input data rate to the input clock rate.

(5) This is achieved by using the **LVDS** clock network.

(6) The minimum specification depends on the clock source (for example, the PLL and clock pin) and the clock routing resource (global, regional, or local) that you use. The I/O differential buffer and input register do not have a minimum toggle rate.

(7) The maximum ideal frequency is the SERDES factor (J) x the PLL maximum output frequency (fOUT) provided you can close the design timing and the signal integrity simulation is clean.

(8) You can estimate the achievable maximum data rate for non-DPA mode by performing link timing closure analysis. You must consider the board skew margin, transmitter delay margin, and receiver sampling margin to determine the maximum data rate supported.

(9) If the receiver with DPA enabled and transmitter are using shared PLLs, the minimum data rate is 150 Mbps.

(10) You must calculate the leftover timing margin in the receiver by performing link timing closure analysis. You must consider the board skew margin, transmitter channel-to-channel skew, and receiver sampling margin to determine leftover timing margin.

(11) The F_{MAX} specification is based on the fast clock used for serial data. The interface F_{MAX} is also dependent on the parallel clock domain which is design-dependent and requires timing analysis.

(12) Stratix V RX LVDS will need DPA. For Stratix V TX LVDS, the receiver side component must have DPA.

(13) Stratix V LVDS serialization and de-serialization factor needs to be x4 and above.

(14) Requires package skew compensation with PCB trace length.

(15) Do not mix single-ended I/O buffer within LVDS I/O bank.

(16) Chip-to-chip communication only with a maximum load of 5 pF.

(17) When using True LVDS RX channels for emulated LVDS TX channel, only serialization factors 1 and 2 are supported.

Figure 7 shows the dynamic phase alignment (DPA) lock time specifications with the DPA PLL calibration option enabled.

Figure 7. DPA Lock Time Specification with DPA PLL Calibration Enabled

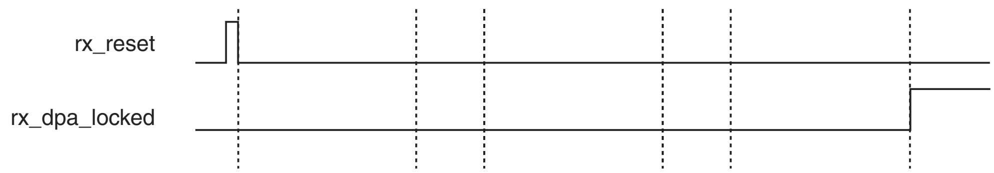


Table 37 lists the DPA lock time specifications for Stratix V devices.

Table 37. DPA Lock Time Specifications for Stratix V GX Devices Only *(1), (2), (3)*

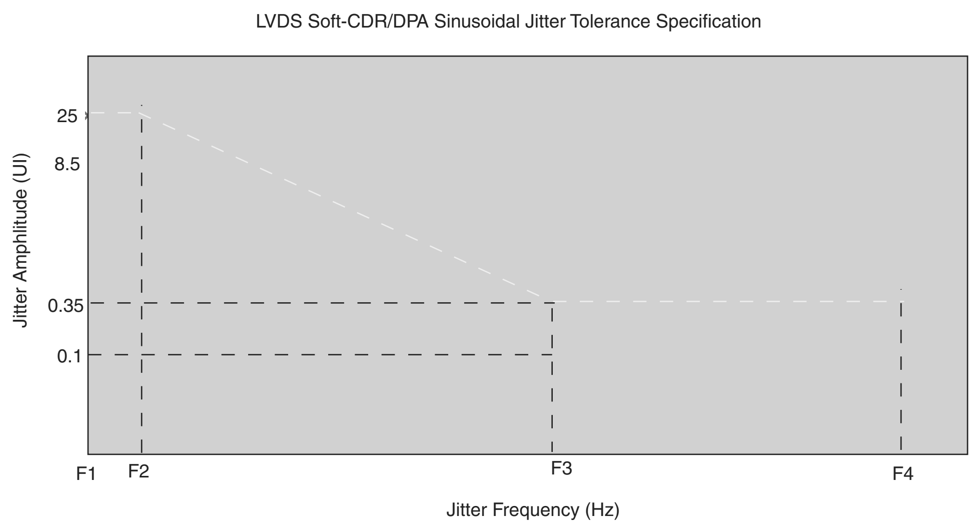
Standard	Training Pattern	Number of Data Transitions in One Repetition of the Training Pattern	Number of Repetitions per 256 Data Transitions *(4)*	Maximum
SPI-4	00000000001111111111	2	128	640 data transitions
Parallel Rapid I/O	00001111	2	128	640 data transitions
	10010000	4	64	640 data transitions
Miscellaneous	10101010	8	32	640 data transitions
	01010101	8	32	640 data transitions

Notes to Table 37:

(1) The DPA lock time is for one channel.
(2) One data transition is defined as a 0-to-1 or 1-to-0 transition.
(3) The DPA lock time stated in this table applies to both commercial and industrial grade.
(4) This is the number of repetitions for the stated training pattern to achieve the 256 data transitions.

Figure 8 shows the **LVDS** soft-clock data recovery (CDR)/DPA sinusoidal jitter tolerance specification for a data rate ≥ 1.25 Gbps. Table 38 lists the **LVDS** soft-CDR/DPA sinusoidal jitter tolerance specification for a data rate ≥ 1.25 Gbps.

Figure 8. LVDS Soft-CDR/DPA Sinusoidal Jitter Tolerance Specification for a Data Rate ≥ 1.25 Gbps



Duty Cycle Distortion (DCD) Specifications

Table 44 lists the worst-case DCD for Stratix V devices.

Table 44. Worst-Case DCD on Stratix V I/O Pins (1)

Symbol	C1		C2, C2L, I2, I2L		C3, I3, I3L, I3YY		C4,I4		Unit
	Min	Max	Min	Max	Min	Max	Min	Max	
Output Duty Cycle	45	55	45	55	45	55	45	55	%

Note to Table 44:

(1) The DCD numbers do not cover the core clock network.

Configuration Specification

POR Delay Specification

Power-on reset (POR) delay is defined as the delay between the time when all the power supplies monitored by the POR circuitry reach the minimum recommended operating voltage to the time when the nSTATUS is released high and your device is ready to begin configuration.

For more information about the POR delay, refer to the *Hot Socketing and Power-On Reset in Stratix V Devices* chapter.

Table 45 lists the fast and standard POR delay specification.

Table 45. Fast and Standard POR Delay Specification (1)

POR Delay	Minimum	Maximum
Fast	4 ms	12 ms
Standard	100 ms	300 ms

Note to Table 45:

(1) You can select the POR delay based on the MSEL settings as described in the MSEL Pin Settings section of the "Configuration, Design Security, and Remote System Upgrades in Stratix V Devices" chapter.

JTAG Configuration Specifications

Table 46 lists the JTAG timing parameters and values for Stratix V devices.

Table 46. JTAG Timing Parameters and Values for Stratix V Devices

Symbol	Description	Min	Max	Unit
t_{JCP}	TCK clock period (2)	30	—	ns
t_{JCP}	TCK clock period (2)	167	—	ns
t_{JCH}	TCK clock high time (2)	14	—	ns
t_{JCL}	TCK clock low time (2)	14	—	ns
$t_{JPSU (TDI)}$	TDI JTAG port setup time	2	—	ns
$t_{JPSU (TMS)}$	TMS JTAG port setup time	3	—	ns

Table 50 lists the timing parameters for Stratix V devices for FPP configuration when the DCLK-to-DATA[] ratio is 1.

Table 50. FPP Timing Parameters for Stratix V Devices *(1)*

Symbol	Parameter	Minimum	Maximum	Units
t_{CF2CD}	nCONFIG low to CONF_DONE low	—	600	ns
t_{CF2ST0}	nCONFIG low to nSTATUS low	—	600	ns
t_{CFG}	nCONFIG low pulse width	2	—	µs
t_{STATUS}	nSTATUS low pulse width	268	1,506 *(2)*	µs
t_{CF2ST1}	nCONFIG high to nSTATUS high	—	1,506 *(3)*	µs
t_{CF2CK} *(6)*	nCONFIG high to first rising edge on DCLK	1,506	—	µs
t_{ST2CK} *(6)*	nSTATUS high to first rising edge of DCLK	2	—	µs
t_{DSU}	DATA[] setup time before rising edge on DCLK	5.5	—	ns
t_{DH}	DATA[] hold time after rising edge on DCLK	0	—	ns
t_{CH}	DCLK high time	$0.45 \times 1/f_{MAX}$	—	s
t_{CL}	DCLK low time	$0.45 \times 1/f_{MAX}$	—	s
t_{CLK}	DCLK period	$1/f_{MAX}$	—	s
f_{MAX}	DCLK frequency (FPP ×8/×16)	—	125	MHz
	DCLK frequency (FPP ×32)	—	100	MHz
t_{CD2UM}	CONF_DONE high to user mode *(4)*	175	437	µs
t_{CD2CU}	CONF_DONE high to CLKUSR enabled	4 × maximum DCLK period	—	—
t_{CD2UMC}	CONF_DONE high to user mode with CLKUSR option on	t_{CD2CU} + (8576 × CLKUSR period) *(5)*	—	—

Notes to Table 50:

(1) Use these timing parameters when the decompression and design security features are disabled.

(2) This value is applicable if you do not delay configuration by extending the nCONFIG or nSTATUS low pulse width.

(3) This value is applicable if you do not delay configuration by externally holding the nSTATUS low.

(4) The minimum and maximum numbers apply only if you chose the internal oscillator as the clock source for initializing the device.

(5) To enable the CLKUSR pin as the initialization clock source and to obtain the maximum frequency specification on these pins, refer to the Initialization section of the "Configuration, Design Security, and Remote System Upgrades in Stratix V Devices" chapter.

(6) If nSTATUS is monitored, follow the t_{ST2CK} specification. If nSTATUS is not monitored, follow the t_{CF2CK} specification.

FPP Configuration Timing when DCLK-to-DATA [] > 1

Figure 13 shows the timing waveform for FPP configuration when using a MAX II device, MAX V device, or microprocessor as an external host. This waveform shows timing when the DCLK-to-DATA[] ratio is more than 1.

Table 51 lists the timing parameters for Stratix V devices for FPP configuration when the DCLK-to-DATA[] ratio is more than 1.

Table 51. FPP Timing Parameters for Stratix V Devices When the DCLK-to-DATA[] Ratio is >1 (1)

Symbol	Parameter	Minimum	Maximum	Units
t_{CF2CD}	nCONFIG low to CONF_DONE low	—	600	ns
t_{CF2ST0}	nCONFIG low to nSTATUS low	—	600	ns
t_{CFG}	nCONFIG low pulse width	2	—	µs
t_{STATUS}	nSTATUS low pulse width	268	1,506 (2)	µs
t_{CF2ST1}	nCONFIG high to nSTATUS high	—	1,506 (2)	µs
t_{CF2CK} (5)	nCONFIG high to first rising edge on DCLK	1,506	—	µs
t_{ST2CK} (5)	nSTATUS high to first rising edge of DCLK	2	—	µs
t_{DSU}	DATA[] setup time before rising edge on DCLK	5.5	—	ns
t_{DH}	DATA[] hold time after rising edge on DCLK	$N–1/f_{DCLK}$ (5)	—	s
t_{CH}	DCLK high time	$0.45 \times 1/f_{MAX}$	—	s
t_{CL}	DCLK low time	$0.45 \times 1/f_{MAX}$	—	s
t_{CLK}	DCLK period	$1/f_{MAX}$	—	s
f_{MAX}	DCLK frequency (FPP ×8/×16)	—	125	MHz
	DCLK frequency (FPP ×32)	—	100	MHz
t_R	Input rise time	—	40	ns
t_F	Input fall time	—	40	ns
t_{CD2UM}	CONF_DONE high to user mode (3)	175	437	µs
t_{CD2CU}	CONF_DONE high to CLKUSR enabled	4 × maximum DCLK period	—	—
t_{CD2UMC}	CONF_DONE high to user mode with CLKUSR option on	t_{CD2CU} + (8576 × CLKUSR period) (4)	—	—

Notes to Table 51:

(1) Use these timing parameters when you use the decompression and design security features.

(2) You can obtain this value if you do not delay configuration by extending the nCONFIG or nSTATUS low pulse width.

(3) The minimum and maximum numbers apply only if you use the internal oscillator as the clock source for initializing the device.

(4) To enable the CLKUSR pin as the initialization clock source and to obtain the maximum frequency specification on these pins, refer to the Initialization section of the "Configuration, Design Security, and Remote System Upgrades in Stratix V Devices" chapter.

(5) N is the DCLK-to-DATA ratio and f_{DCLK} is the DCLK frequency the system is operating.

(6) If nSTATUS is monitored, follow the t_{ST2CK} specification. If nSTATUS is not monitored, follow the t_{CF2CK} specification.

Table 53. AS Timing Parameters for AS ×1 and AS ×4 Configurations in Stratix V Devices (1), (2) (Part 2 of 2)

Symbol	Parameter	Minimum	Maximum	Units
t_{CD2UM}	CONF_DONE high to user mode (3)	175	437	µs
t_{CD2CU}	CONF_DONE high to CLKUSR enabled	4 × maximum DCLK period	—	—
t_{CD2UMC}	CONF_DONE high to user mode with CLKUSR option on	t_{CD2CU} + (8576 × CLKUSR period)	—	—

Notes to Table 53:

(1) The minimum and maximum numbers apply only if you choose the internal oscillator as the clock source for initializing the device.

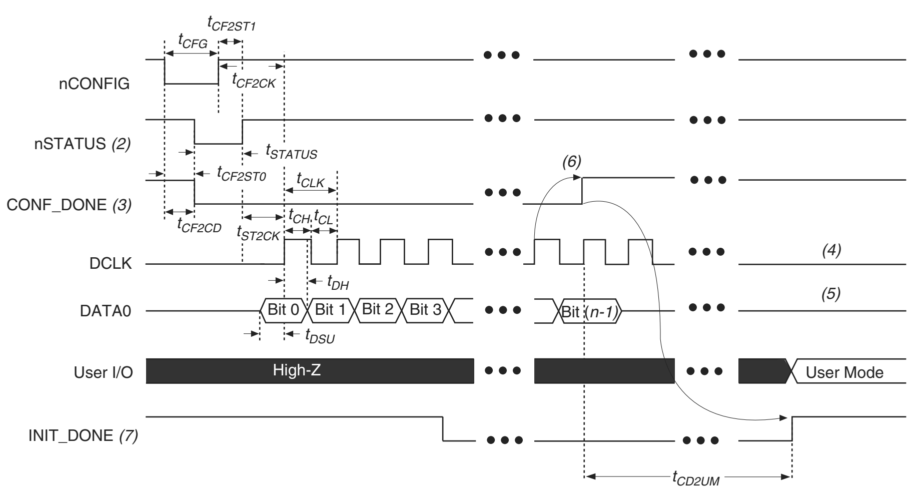
(2) t_{CF2CD}, t_{CF2ST0}, t_{CFG}, t_{STATUS}, and t_{CF2ST1} timing parameters are identical to the timing parameters for PS mode listed in Table 54 on page 63.

(3) To enable the CLKUSR pin as the initialization clock source and to obtain the maximum frequency specification on this pin, refer to the Initialization section of the "Configuration, Design Security, and Remote System Upgrades in Stratix V Devices" chapter.

Passive Serial Configuration Timing

Figure 15 shows the timing waveform for a passive serial (PS) configuration when using a MAX II device, MAX V device, or microprocessor as an external host.

Figure 15. PS Configuration Timing Waveform (1)



Notes to Figure 15:

(1) The beginning of this waveform shows the device in user mode. In user mode, nCONFIG, nSTATUS, and CONF_DONE are at logic high levels. When nCONFIG is pulled low, a reconfiguration cycle begins.

(2) After power-up, the Stratix V device holds nSTATUS low for the time of the POR delay.

(3) After power-up, before and during configuration, CONF_DONE is low.

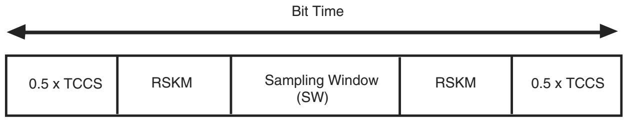
(4) Do not leave DCLK floating after configuration. You can drive it high or low, whichever is more convenient.

(5) DATA0 is available as a user I/O pin after configuration. The state of this pin depends on the dual-purpose pin settings in the **Device and Pins Option**.

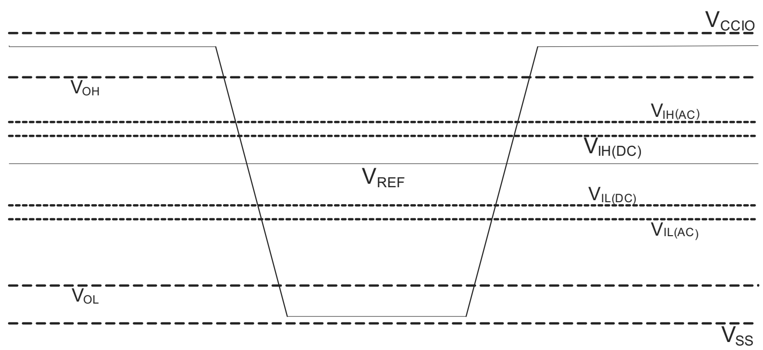
(6) To ensure a successful configuration, send the entire configuration data to the Stratix V device. CONF_DONE is released high after the Stratix V device receives all the configuration data successfully. After CONF_DONE goes high, send two additional falling edges on DCLK to begin initialization and enter user mode.

(7) After the option bit to enable the INIT_DONE pin is configured into the device, the INIT_DONE goes low.

Table 60. Glossary (Part 3 of 4)

<table>
<tr><th>Letter</th><th>Subject</th><th>Definitions</th></tr>
<tr><td rowspan="2">S</td><td>SW (sampling window)</td><td>Timing Diagram—the period of time during which the data must be valid in order to capture it correctly. The setup and hold times determine the ideal strobe position within the sampling window, as shown:

</td></tr>
<tr><td>Single-ended voltage referenced I/O standard</td><td>The JEDEC standard for SSTL and HSTL I/O defines both the AC and DC input signal values. The AC values indicate the voltage levels at which the receiver must meet its timing specifications. The DC values indicate the voltage levels at which the final logic state of the receiver is unambiguously defined. After the receiver input has crossed the AC value, the receiver changes to the new logic state.

The new logic state is then maintained as long as the input stays beyond the DC threshold. This approach is intended to provide predictable receiver timing in the presence of input waveform ringing:

Single-Ended Voltage Referenced I/O Standard

</td></tr>
<tr><td rowspan="7">T</td><td>t_C</td><td>High-speed receiver and transmitter input and output clock period.</td></tr>
<tr><td>TCCS (channel-to-channel-skew)</td><td>The timing difference between the fastest and slowest output edges, including t_{CO} variation and clock skew, across channels driven by the same PLL. The clock is included in the TCCS measurement (refer to the Timing Diagram figure under SW in this table).</td></tr>
<tr><td>t_{DUTY}</td><td>High-speed I/O block—Duty cycle on the high-speed transmitter output clock.

Timing Unit Interval (TUI)

The timing budget allowed for skew, propagation delays, and the data sampling window. (TUI = 1/(receiver input clock frequency multiplication factor) = t_C/w)</td></tr>
<tr><td>t_{FALL}</td><td>Signal high-to-low transition time (80-20%)</td></tr>
<tr><td>t_{INCCJ}</td><td>Cycle-to-cycle jitter tolerance on the PLL clock input.</td></tr>
<tr><td>t_{OUTPJ_IO}</td><td>Period jitter on the general purpose I/O driven by a PLL.</td></tr>
<tr><td>t_{OUTPJ_DC}</td><td>Period jitter on the dedicated clock output driven by a PLL.</td></tr>
<tr><td>t_{RISE}</td><td>Signal low-to-high transition time (20-80%)</td></tr>
<tr><td>U</td><td>—</td><td>—</td></tr>
</table>

Table 60. Glossary (Part 4 of 4)

Letter	Subject	Definitions
V	$V_{CM(DC)}$	DC common mode input voltage.
	V_{ICM}	Input common mode voltage—The common mode of the differential signal at the receiver.
	V_{ID}	Input differential voltage swing—The difference in voltage between the positive and complementary conductors of a differential transmission at the receiver.
	$V_{DIF(AC)}$	AC differential input voltage—Minimum AC input differential voltage required for switching.
	$V_{DIF(DC)}$	DC differential input voltage— Minimum DC input differential voltage required for switching.
	V_{IH}	Voltage input high—The minimum positive voltage applied to the input which is accepted by the device as a logic high.
	$V_{IH(AC)}$	High-level AC input voltage
	$V_{IH(DC)}$	High-level DC input voltage
	V_{IL}	Voltage input low—The maximum positive voltage applied to the input which is accepted by the device as a logic low.
	$V_{IL(AC)}$	Low-level AC input voltage
	$V_{IL(DC)}$	Low-level DC input voltage
	V_{OCM}	Output common mode voltage—The common mode of the differential signal at the transmitter.
	V_{OD}	Output differential voltage swing—The difference in voltage between the positive and complementary conductors of a differential transmission at the transmitter.
	V_{SWING}	Differential input voltage
	V_X	Input differential cross point voltage
	V_{OX}	Output differential cross point voltage
W	W	High-speed I/O block—clock boost factor
X Y Z	—	—