### Intel - 5SGXMA5H3F35I4 Datasheet





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#### **Applications of Embedded - FPGAs**

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

#### Details

Product Status	Obsolete
Number of LABs/CLBs	185000
Number of Logic Elements/Cells	490000
Total RAM Bits	46080000
Number of I/O	552
Number of Gates	-
Voltage - Supply	0.82V ~ 0.88V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	1152-BBGA, FCBGA
Supplier Device Package	1152-FBGA (35x35)
Purchase URL	https://www.e-xfl.com/product-detail/intel/5sgxma5h3f35i4

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### I/O Pin Leakage Current

Table 9 lists the Stratix V I/O pin leakage current specifications.

Table 9.	I/O Pin	Leakage	<b>Current for</b>	Stratix V	Devices (1)
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Symbol	Description	Conditions	Min	Тур	Max	Unit
I <sub>I</sub>	Input pin	$V_I = 0 V \text{ to } V_{CCIOMAX}$	-30	_	30	μA
I <sub>OZ</sub>	Tri-stated I/O pin	$V_0 = 0 V \text{ to } V_{\text{CCIOMAX}}$	-30		30	μA

### Note to Table 9:

(1) If  $V_0 = V_{CCI0}$  to  $V_{CCI0Max}$ , 100  $\mu$ A of leakage current per I/O is expected.

### **Bus Hold Specifications**

Table 10 lists the Stratix V device family bus hold specifications.

Table 10. Bus Hold Parameters for Stratix V Devices

							Va	CI0					
Parameter	Symbol	Conditions	ions 1.2 V		1.5 V		1.8 V		2.5 V		3.0 V		Unit
			Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Low sustaining current	I <sub>SUSL</sub>	V <sub>IN</sub> > V <sub>IL</sub> (maximum)	22.5	_	25.0	_	30.0	_	50.0	_	70.0	_	μA
High sustaining current	I <sub>SUSH</sub>	V <sub>IN</sub> < V <sub>IH</sub> (minimum)	-22.5		-25.0	_	-30.0	_	-50.0	_	-70.0		μA
Low overdrive current	I <sub>odl</sub>	$0V < V_{IN} < V_{CCIO}$		120		160		200	_	300		500	μA
High overdrive current	I <sub>odh</sub>	$0V < V_{IN} < V_{CCIO}$		-120		-160		-200		-300		-500	μΑ
Bus-hold trip point	V <sub>TRIP</sub>	_	0.45	0.95	0.50	1.00	0.68	1.07	0.70	1.70	0.80	2.00	۷

### **On-Chip Termination (OCT) Specifications**

If you enable OCT calibration, calibration is automatically performed at power-up for I/Os connected to the calibration block. Table 11 lists the Stratix V OCT termination calibration accuracy specifications.

Table 11. OCT Calibration Accuracy Specifications for Stratix V Devices <sup>(1)</sup> (Part 1 of 2)

			Calibration Accuracy					
Symbol	Description	Conditions	C1	C2,12	C3,I3, I3YY	C4,14	Unit	
25- $Ω$ R <sub>S</sub>	Internal series termination with calibration (25- $\Omega$ setting)	V <sub>CCI0</sub> = 3.0, 2.5, 1.8, 1.5, 1.2 V	±15	±15	±15	±15	%	

1/0 Standard		V <sub>ccio</sub> (V)			V <sub>REF</sub> (V)			V <sub>TT</sub> (V)	
i/O Stanuaru	Min	Тур	Max	Min	Тур	Max	Min	Тур	Max
SSTL-2 Class I, II	2.375	2.5	2.625	0.49 * V <sub>CCI0</sub> 0.5 * V <sub>CCI0</sub>		0.51 * V <sub>CCIO</sub>	V <sub>REF</sub> – 0.04	V <sub>REF</sub>	V <sub>REF</sub> + 0.04
SSTL-18 Class I, II	1.71	1.8	1.89	0.833 0.9		0.969	V <sub>REF</sub> – 0.04	V <sub>REF</sub>	V <sub>REF</sub> + 0.04
SSTL-15 Class I, II	1.425	1.5	1.575	0.49 * V <sub>CCIO</sub>	0.5 * V <sub>CCIO</sub>	0.51 * V <sub>CCIO</sub>	0.49 * V <sub>CCI0</sub>	0.5 * VCCIO	0.51 * V <sub>CCIO</sub>
SSTL-135 Class I, II	1.283	1.35	1.418	0.49 * V <sub>CCIO</sub>	0.5 * V <sub>CCIO</sub>	0.51 * V <sub>CCIO</sub>	0.49 * V <sub>CCIO</sub>	0.5 * V <sub>CCIO</sub>	0.51 * V <sub>CCIO</sub>
SSTL-125 Class I, II	1.19	1.25	1.26	0.49 * V <sub>CCIO</sub>	0.5 * V <sub>CCIO</sub>	0.51 * V <sub>CCIO</sub>	0.49 * V <sub>CCIO</sub>	0.5 * VCCIO	0.51 * V <sub>CCIO</sub>
SSTL-12 Class I, II	1.14	1.20	1.26	0.49 * V <sub>CCIO</sub>	0.5 * V <sub>CCIO</sub>	0.51 * V <sub>CCIO</sub>	0.49 * V <sub>CCIO</sub>	0.5 * VCCIO	0.51 * V <sub>CCIO</sub>
HSTL-18 Class I, II	1.71	1.8	1.89	0.85	0.9	0.95	_	V <sub>CCI0</sub> /2	_
HSTL-15 Class I, II	1.425	1.5	1.575	0.68	0.75	0.9	_	V <sub>CCI0</sub> /2	_
HSTL-12 Class I, II	1.14	1.2	1.26	0.47 * V <sub>CCIO</sub>	0.5 * V <sub>CCIO</sub>	0.53 * V <sub>CCIO</sub>	_	V <sub>CCI0</sub> /2	_
HSUL-12	1.14	1.2	1.3	0.49 * V <sub>CCIO</sub>	0.5 * V <sub>CCIO</sub>	0.51 * V <sub>CCIO</sub>	_		

Table 18. Single-Ended SSTL, HSTL, and HSUL I/O Reference Voltage Specifications for Stratix V Devi	ces
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Table 19.	Single-Ended SSTL	, HSTL, and HSUL I/	/O Standards Signal S	<b>Specifications for</b>	Stratix V Devices	(Part 1 of 2)
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1/0 Standard	V <sub>IL(DI</sub>	<sub>c)</sub> (V)	V <sub>IH(D</sub>	<sub>c)</sub> (V)	V <sub>IL(AC)</sub> (V)	V <sub>IH(AC)</sub> (V)	V <sub>ol</sub> (V)	V <sub>oh</sub> (V)	I (mA)	I <sub>oh</sub>
i/o Stanuaru	Min	Max	Min	Max	Max	Min	Max	Min	I <sub>ol</sub> (IIIA)	(mÄ)
SSTL-2 Class I	-0.3	V <sub>REF</sub> – 0.15	V <sub>REF</sub> + 0.15	V <sub>CCI0</sub> + 0.3	V <sub>REF</sub> – 0.31	V <sub>REF</sub> + 0.31	V <sub>TT</sub> – 0.608	V <sub>TT</sub> + 0.608	8.1	-8.1
SSTL-2 Class II	-0.3	V <sub>REF</sub> – 0.15	V <sub>REF</sub> + 0.15	V <sub>CCI0</sub> + 0.3	V <sub>REF</sub> – 0.31	V <sub>REF</sub> + 0.31	V <sub>TT</sub> – 0.81	V <sub>TT</sub> + 0.81	16.2	-16.2
SSTL-18 Class I	-0.3	V <sub>REF</sub> – 0.125	V <sub>REF</sub> + 0.125	V <sub>CCI0</sub> + 0.3	V <sub>REF</sub> – 0.25	V <sub>REF</sub> + 0.25	V <sub>TT</sub> – 0.603	V <sub>TT</sub> + 0.603	6.7	-6.7
SSTL-18 Class II	-0.3	V <sub>REF</sub> – 0.125	V <sub>REF</sub> + 0.125	V <sub>CCI0</sub> + 0.3	V <sub>REF</sub> – 0.25	V <sub>REF</sub> + 0.25	0.28	V <sub>CCI0</sub> – 0.28	13.4	-13.4
SSTL-15 Class I	_	V <sub>REF</sub> – 0.1	V <sub>REF</sub> + 0.1	_	V <sub>REF</sub> – 0.175	V <sub>REF</sub> + 0.175	0.2 * V <sub>CCI0</sub>	0.8 * V <sub>CCI0</sub>	8	-8
SSTL-15 Class II	_	V <sub>REF</sub> – 0.1	V <sub>REF</sub> + 0.1	_	V <sub>REF</sub> – 0.175	V <sub>REF</sub> + 0.175	0.2 * V <sub>CCI0</sub>	0.8 * V <sub>CCI0</sub>	16	-16
SSTL-135 Class I, II	_	V <sub>REF</sub> – 0.09	V <sub>REF</sub> + 0.09	—	V <sub>REF</sub> – 0.16	V <sub>REF</sub> + 0.16	0.2 * V <sub>CCI0</sub>	0.8 * V <sub>CCI0</sub>	—	_
SSTL-125 Class I, II		V <sub>REF</sub> – 0.85	V <sub>REF</sub> + 0.85	_	V <sub>REF</sub> – 0.15	V <sub>REF</sub> - V <sub>REF</sub> + 0.15		0.8 * V <sub>CCI0</sub>		
SSTL-12 Class I, II	_	V <sub>REF</sub> – 0.1	V <sub>REF</sub> + 0.1	_	V <sub>REF</sub> – 0.15	V <sub>REF</sub> - V <sub>REF</sub> + 0.15		0.8 * V <sub>CCI0</sub>	_	

I/O		V <sub>ccio</sub> (V)		V <sub>DIF(DC)</sub> (V)		V <sub>X(AC)</sub> (V)				V <sub>CM(DC)</sub> (V	V <sub>DIF(AC)</sub> (V)		
Standard	Min	Тур	Max	Min	Max	Min	Тур	Max	Min	Тур	Max	Min	Max
HSTL-12 Class I, II	1.14	1.2	1.26	0.16	V <sub>CCI0</sub> + 0.3	_	0.5* V <sub>CCI0</sub>	_	0.4* V <sub>CCIO</sub>	0.5* V <sub>CCIO</sub>	0.6* V <sub>CCI0</sub>	0.3	V <sub>CCI0</sub> + 0.48
HSUL-12	1.14	1.2	1.3	0.26	0.26	0.5*V <sub>CCI0</sub> - 0.12	0.5* V <sub>CCI0</sub>	0.5*V <sub>CCI0</sub> + 0.12	0.4* V <sub>CCIO</sub>	0.5* V <sub>CCIO</sub>	0.6* V <sub>CCIO</sub>	0.44	0.44

### Table 21. Differential HSTL and HSUL I/O Standards for Stratix V Devices (Part 2 of 2)

### Table 22. Differential I/O Standard Specifications for Stratix V Devices (7)

I/O	Vc	<sub>cio</sub> (V)	(10)	V <sub>ID</sub> (mV) <sup>(8)</sup>			V <sub>ICM(DC)</sub> (V)			V <sub>OD</sub> (V) <sup>(6)</sup>			V <sub>OCM</sub> (V) <sup>(6)</sup>		
Standard	Min	Тур	Max	Min	Condition	Max	Min	Condition	Max	Min	Тур	Max	Min	Тур	Max
PCML	Trar	nsmitte	er, receiv transmi	ver, and itter, rec	input referer ceiver, and re	nce cloo eference	ck pins e clock	of the high-s I/O pin speci	peed tra fications	nsceiver , refer to	rs use o Table	the PC e 23 on	ML I/O s page 18	standard 3.	. For
2.5 V	2 375	25	2 625	100	V <sub>CM</sub> =	_	0.05	D <sub>MAX</sub> ≤ 700 Mbps	1.8	0.247	_	0.6	1.125	1.25	1.375
LVDS <sup>(1)</sup>	2.575	2.0	2.025	100	1.25 V	_	1.05	D <sub>MAX</sub> > 700 Mbps	1.55	0.247	_	0.6	1.125	1.25	1.375
BLVDS (5)	2.375	2.5	2.625	100	_	—	_	_	_	_	_	—	_	—	
RSDS (HIO) <sup>(2)</sup>	2.375	2.5	2.625	100	V <sub>CM</sub> = 1.25 V	_	0.3	_	1.4	0.1	0.2	0.6	0.5	1.2	1.4
Mini- LVDS (HIO) <sup>(3)</sup>	2.375	2.5	2.625	200	_	600	0.4	_	1.325	0.25	_	0.6	1	1.2	1.4
LVPECL (4	_	_	_	300	_		0.6	D <sub>MAX</sub> ≤ 700 Mbps	1.8	_	_	_	_	_	_
), (9)				300			1	D <sub>MAX</sub> > 700 Mbps	1.6						

Notes to Table 22:

(1) For optimized LVDS receiver performance, the receiver voltage input range must be between 1.0 V to 1.6 V for data rates above 700 Mbps, and 0 V to 1.85 V for data rates below 700 Mbps.

(2) For optimized RSDS receiver performance, the receiver voltage input range must be between 0.25 V to 1.45 V.

(3) For optimized Mini-LVDS receiver performance, the receiver voltage input range must be between 0.3 V to 1.425 V.

- (4) For optimized LVPECL receiver performance, the receiver voltage input range must be between 0.85 V to 1.75 V for data rate above 700 Mbps and 0.45 V to 1.95 V for data rate below 700 Mbps.
- (5) There are no fixed  $V_{ICM}$ ,  $V_{OD}$ , and  $V_{OCM}$  specifications for BLVDS. They depend on the system topology.
- (6) RL range:  $90 \le RL \le 110 \Omega$ .
- (7) The 1.4-V and 1.5-V PCML transceiver I/O standard specifications are described in "Transceiver Performance Specifications" on page 18.
- (8) The minimum VID value is applicable over the entire common mode range, VCM.
- (9) LVPECL is only supported on dedicated clock input pins.
- (10) Differential inputs are powered by VCCPD which requires 2.5 V.

## **Power Consumption**

Altera offers two ways to estimate power consumption for a design—the Excel-based Early Power Estimator and the Quartus<sup>®</sup> II PowerPlay Power Analyzer feature.

- You typically use the interactive Excel-based Early Power Estimator before designing the FPGA to get a magnitude estimate of the device power. The Quartus II PowerPlay Power Analyzer provides better quality estimates based on the specifics of the design after you complete place-and-route. The PowerPlay Power Analyzer can apply a combination of user-entered, simulation-derived, and estimated signal activities that, when combined with detailed circuit models, yields very accurate power estimates.
- **\*** For more information about power estimation tools, refer to the *PowerPlay Early Power Estimator User Guide* and the *PowerPlay Power Analysis* chapter in the *Quartus II Handbook*.

# **Switching Characteristics**

This section provides performance characteristics of the Stratix V core and periphery blocks.

These characteristics can be designated as Preliminary or Final.

- Preliminary characteristics are created using simulation results, process data, and other known parameters. The title of these tables show the designation as "Preliminary."
- Final numbers are based on actual silicon characterization and testing. The numbers reflect the actual performance of the device under worst-case silicon process, voltage, and junction temperature conditions. There are no designations on finalized tables.

## **Transceiver Performance Specifications**

This section describes transceiver performance specifications.

Table 23 lists the Stratix V GX and GS transceiver specifications.

Table 23.	Transceiver 3	Specifications	for Stratix	V GX	and GS	Devices	(1)	(Part 1	nf 7	۱
Table 20.	TIANSUCIACI	opeonitionationa	IUI UIIAIIA	I UA	anu uu	DEVICES	• •	(1 61 6 1		

Symbol/	Conditions	Tra	nsceive Grade	r Speed 1	Trai	nsceive Grade	r Speed 2	Trai	er Speed e 3	Unit					
Description		Min	Тур	Max	Min	Тур	Max	Min	Тур	Max					
Reference Clock															
Supported I/O	Dedicated reference clock pin	1.2-V	PCML,	1.4-V PCM	IL, 1.5-∖	/ PCML	, 2.5-V PCN HCSL	1L, Diffe	rential	LVPECL, L\	/DS, and				
Standards	RX reference clock pin		1.4-V PCML, 1.5-V PCML, 2.5-V PCML, LVPECL, and LVDS												
Input Reference Clock Frequency (CMU PLL) <sup>(8)</sup>	_	40		710	40	_	710	40	_	710	MHz				
Input Reference Clock Frequency (ATX PLL) <sup>(8)</sup>		100		710	100		710	100	_	710	MHz				
Rise time	Measure at ±60 mV of differential signal <sup>(26)</sup>			400	_		400			400	ns				
Fall time	Measure at ±60 mV of differential signal <sup>(26)</sup>		_	400	_		400			400	μs				
Duty cycle		45		55	45		55	45	—	55	%				
Spread-spectrum modulating clock frequency	PCI Express® (PCIe <sup>®</sup> )	30		33	30		33	30	_	33	kHz				

Symbol/	Conditions	Tra	nsceive Grade	r Speed 1	Trai	nsceive Grade	r Speed 2	Trai	Unit		
Description		Min	Тур	Max	Min	Тур	Max	Min	Тур	Max	
Spread-spectrum downspread	PCIe	_	0 to 0.5	_	_	0 to 0.5	_	_	0 to 0.5	_	%
On-chip termination resistors <sup>(21)</sup>	_	_	100		_	100		_	100		Ω
Absolute V <sub>MAX</sub> <sup>(5)</sup>	Dedicated reference clock pin	_	_	1.6	_	_	1.6	_	_	1.6	V
	RX reference clock pin	_		1.2		_	1.2			1.2	
Absolute V <sub>MIN</sub>	—	-0.4	-	_	-0.4	_		-0.4	—		V
Peak-to-peak differential input voltage	_	200	_	1600	200	_	1600	200		1600	mV
V <sub>ICM</sub> (AC	Dedicated reference clock pin	1050/	(1000/90	00/850 <sup>(2)</sup>	1050/	1000/9	00/850 <sup>(2)</sup>	1050/	1000/9	00/850 <sup>(2)</sup>	mV
coupled) (9	RX reference clock pin	1	.0/0.9/0	.85 (4)	1.	.0/0.9/0	.85 (4)	1.	.0/0.9/0	.85 <sup>(4)</sup>	V
V <sub>ICM</sub> (DC coupled)	HCSL I/O standard for PCIe reference clock	250		550	250		550	250	_	550	mV
	100 Hz	—	—	-70	—	—	-70	—	—	-70	dBc/Hz
Transmitter	1 kHz	—	—	-90	—	—	-90	—	—	-90	dBc/Hz
REFCLK Phase	10 kHz	—	—	-100	—	—	-100	—	—	-100	dBc/Hz
(622 MHz) <sup>(20)</sup>	100 kHz	—	—	-110	—	—	-110	—	—	-110	dBc/Hz
	≥1 MHz	—	—	-120		—	-120	—	—	-120	dBc/Hz
Transmitter REFCLK Phase Jitter (100 MHz) <sup>(17)</sup>	10 kHz to 1.5 MHz (PCIe)	_	_	3	_	_	3	_	_	3	ps (rms)
R <sub>REF</sub> (19)	_			_	1800 ±1%	_	_	180 0 ±1%	_	Ω	
Transceiver Clock	s										
fixedclk <b>clock</b> frequency	PCIe Receiver Detect		100 or 125			100 or 125		_	100 or 125		MHz

### Table 23. Transceiver Specifications for Stratix V GX and GS Devices <sup>(1)</sup> (Part 2 of 7)

Symbol/	Conditions	Trai	nsceive Grade	r Speed 1	Trai	nsceive Grade	r Speed 2	Trai	Unit		
Description		Min	Тур	Max	Min	Тур	Max	Min	Тур	Max	
	DC Gain Setting = 0		0	_	_	0	_	_	0	—	dB
	DC Gain Setting = 1	_	2		_	2	_	_	2	_	dB
Programmable DC gain	DC Gain Setting = 2	_	4	_	_	4	_	_	4	_	dB
DC Gain Setting = 3		_	6	_	_	6	_	_	6	_	dB
	DC Gain Setting = 4		8			8	—		8	_	dB
Transmitter		<u> </u>									
Supported I/O Standards	_				-	1.4-V ar	nd 1.5-V PC	ML			
Data rate (Standard PCS)	_	600	_	12200	600	_	12200	600	_	8500/ 10312.5 (24)	Mbps
Data rate (10G PCS)	_	600	600 — 14100 600 —		12500	600	_	8500/ 10312.5 (24)	Mbps		
	85-Ω setting	_	85 ± 20%	_	_	85 ± 20%	_	_	85 ± 20%	—	Ω
Differential on-	100-Ω setting	_	100 ± 20%	_	_	100 ± 20%	_	_	100 ± 20%	_	Ω
chip termination resistors	120-Ω setting		120 ± 20%	_		120 ± 20%	_		120 ± 20%	_	Ω
	150-Ω setting	_	150 ± 20%			150 ± 20%	_		150 ± 20%	_	Ω
V <sub>OCM</sub> (AC coupled)	0.65-V setting	_	650		_	650	_	_	650	—	mV
V <sub>OCM</sub> (DC coupled)	_	_	650	_	_	650		_	650	_	mV
Rise time <sup>(7)</sup>	20% to 80%	30	—	160	30	—	160	30	—	160	ps
Fall time <sup>(7)</sup>	80% to 20%	30		160	30		160	30	—	160	ps
Intra-differential pair skew	Tx V <sub>CM</sub> = 0.5 V and slew rate of 15 ps	_	_	15			15		_	15	ps
Intra-transceiver block transmitter channel-to- channel skew	x6 PMA bonded mode	_	_	120	_	_	120	_		120	ps

### Table 23. Transceiver Specifications for Stratix V GX and GS Devices <sup>(1)</sup> (Part 5 of 7)

Table 29 shows the  $V_{\text{OD}}$  settings for the GT channel.

Symbol	V <sub>OD</sub> Setting	V <sub>od</sub> Value (mV)
	0	0
	1	200
V., differential neak to neak typical $(1)$	2	400
The american hear to hear thicat to	3	600
	4	800
	5	1000

### Note:

(1) Refer to Figure 4.

Figure 4 shows the differential transmitter output waveform.





Figure 5 shows the Stratix V AC gain curves for GT channels.

Figure 5. AC Gain Curves for GT Channels

### Table 31. PLL Specifications for Stratix V Devices (Part 3 of 3)

Symbol	Parameter	Min	Тур	Max	Unit
f <sub>RES</sub>	Resolution of VCO frequency ( $f_{INPFD} = 100 \text{ MHz}$ )	390625	5.96	0.023	Hz

#### Notes to Table 31:

(1) This specification is limited in the Quartus II software by the I/O maximum frequency. The maximum I/O frequency is different for each I/O standard.

(2) This specification is limited by the lower of the two: I/O  $f_{MAX}$  or  $f_{OUT}$  of the PLL.

- (3) A high input jitter directly affects the PLL output jitter. To have low PLL output clock jitter, you must provide a clean clock source < 120 ps.
- (4)  $f_{REF}$  is fIN/N when N = 1.
- (5) Peak-to-peak jitter with a probability level of 10<sup>-12</sup> (14 sigma, 99.9999999974404% confidence level). The output jitter specification applies to the intrinsic jitter of the PLL, when an input jitter of 30 ps is applied. The external memory interface clock output jitter specifications use a different measurement method and are available in Table 44 on page 52.
- (6) The cascaded PLL specification is only applicable with the following condition: a. Upstream PLL: 0.59Mhz ≤ Upstream PLL BW < 1 MHz b. Downstream PLL: Downstream PLL BW > 2 MHz
- (7) High bandwidth PLL settings are not supported in external feedback mode.
- (8) The external memory interface clock output jitter specifications use a different measurement method, which is available in Table 42 on page 50.
- (9) The VCO frequency reported by the Quartus II software in the PLL Usage Summary section of the compilation report takes into consideration the VCO post-scale counter K value. Therefore, if the counter K has a value of 2, the frequency reported can be lower than the f<sub>VCO</sub> specification.
- (10) This specification only covers fractional PLL for low bandwidth. The  $f_{VCO}$  for fractional value range 0.05 0.95 must be  $\geq$  1000 MHz, while  $f_{VCO}$  for fractional value range 0.20 0.80 must be  $\geq$  1200 MHz.
- (11) This specification only covered fractional PLL for low bandwidth. The  $f_{VC0}$  for fractional value range 0.05-0.95 must be  $\geq$  1000 MHz.
- (12) This specification only covered fractional PLL for low bandwidth. The  $f_{VC0}$  for fractional value range 0.20-0.80 must be  $\geq$  1200 MHz.

### **DSP Block Specifications**

Table 32 lists the Stratix V DSP block performance specifications.

			F	Peformanc	e			
Mode	C1	C2, C2L	12, 12L	C3	13, 13L, 13YY	C4	14	Unit
		Modes ı	using one	DSP				
Three 9 x 9	600	600	600	480	480	420	420	MHz
One 18 x 18	600	600	600	480	480	420	400	MHz
Two partial 18 x 18 (or 16 x 16)	600	600	600	480	480	420	400	MHz
One 27 x 27	500	500	500	400	400	350	350	MHz
One 36 x 18	500	500	500	400	400	350	350	MHz
One sum of two 18 x 18(One sum of 2 16 x 16)	500	500	500	400	400	350	350	MHz
One sum of square	500	500	500	400	400	350	350	MHz
One 18 x 18 plus 36 (a x b) + c	500	500	500	400	400	350	350	MHz
		Modes u	sing two l	DSPs				
Three 18 x 18	500	500	500	400	400	350	350	MHz
One sum of four 18 x 18	475	475	475	380	380	300	300	MHz
One sum of two 27 x 27	465	465	450	380	380	300	290	MHz
One sum of two 36 x 18	475	475	475	380	380	300	300	MHz
One complex 18 x 18	500	500	500	400	400	350	350	MHz
One 36 x 36	475	475	475	380	380	300	300	MHz

### Table 32. Block Performance Specifications for Stratix V DSP Devices (Part 1 of 2)

Mode											
	C1	C2, C2L	12, 12L	C3	13, 13L, 13YY	C4	14	Unit			
		Modes us	ing Three	DSPs							
One complex 18 x 25	425	425	415	340	340	275	265	MHz			
Modes using Four DSPs											
One complex 27 x 27	465	465	465	380	380	300	290	MHz			

### Table 32. Block Performance Specifications for Stratix V DSP Devices (Part 2 of 2)

## **Memory Block Specifications**

Table 33 lists the Stratix V memory block specifications.

### Table 33. Memory Block Performance Specifications for Stratix V Devices <sup>(1), (2)</sup> (Part 1 of 2)

		Resour	ces Used	Performance								
Memory	Mode	ALUTS	Memory	C1	C2, C2L	C3	C4	12, 12L	13, 13L, 13YY	14	Unit	
	Single port, all supported widths	0	1	450	450	400	315	450	400	315	MHz	
	Simple dual-port, x32/x64 depth	0	1	450	450	400	315	450	400	315	MHz	
WILAD	Simple dual-port, x16 depth <sup>(3)</sup>	0	1	675	675	533	400	675	533	400	MHz	
	ROM, all supported widths	0	1	600	600	500	450	600	500	450	MHz	

## **Periphery Performance**

This section describes periphery performance, including high-speed I/O and external memory interface.

I/O performance supports several system interfaces, such as the **LVDS** high-speed I/O interface, external memory interface, and the **PCI/PCI-X** bus interface. General-purpose I/O standards such as 3.3-, 2.5-, 1.8-, and 1.5-**LVTTL/LVCMOS** are capable of a typical 167 MHz and 1.2-**LVCMOS** at 100 MHz interfacing frequency with a 10 pF load.

The actual achievable frequency depends on design- and system-specific factors. Ensure proper timing closure in your design and perform HSPICE/IBIS simulations based on your specific design and system setup to determine the maximum achievable frequency in your system.

### **High-Speed I/O Specification**

Table 36 lists high-speed I/O timing for Stratix V devices.

Table 36. High-Speed I/O Specifications for Stratix V Devices (1), (2) (Part 1 of 4)

Sumbol	Conditions		C1		C2, C2L, I2, I2L			C3, I3, I3L, I3YY				11		
Symbol	Conditions	Min	Тур	Max	Min	Тур	Max	Min	Тур	Max	Min	Тур	Max	
f <sub>HSCLK_in</sub> (input clock frequency) True Differential I/O Standards	Clock boost factor W = 1 to 40 $^{(4)}$	5	_	800	5		800	5		625	5		525	MHz
f <sub>HSCLK_in</sub> (input clock frequency) Single Ended I/O Standards <sup>(3)</sup>	Clock boost factor W = 1 to 40 $^{(4)}$	5		800	5		800	5		625	5		525	MHz
f <sub>HSCLK_in</sub> (input clock frequency) Single Ended I/O Standards	Clock boost factor W = 1 to 40 $^{(4)}$	5	_	520	5		520	5	_	420	5	_	420	MHz
f <sub>HSCLK_OUT</sub> (output clock frequency)	_	5	_	800	5	_	800	5	_	625 (5)	5	_	525 (5)	MHz

Svmbol	Conditions		C1		C2,	C2L, I	2, I2L	C3,	13, 131	., I3YY	C4,14			Unit
Symbol	Conditions	Min	Тур	Max	Min	Тур	Max	Min	Тур	Max	Min	Тур	Max	UIIIL
Transmitter														
	SERDES factor J = 3 to 10 <sup>(9)</sup> , <sup>(11)</sup> , <sup>(12)</sup> , <sup>(13)</sup> , <sup>(14)</sup> , <sup>(15)</sup> , <sup>(16)</sup>	(6)	_	1600	(6)	_	1434	(6)	_	1250	(6)	_	1050	Mbps
True Differential I/O Standards	SERDES factor J $\geq 4$ LVDS TX with DPA (12), (14), (15), (16)	(6)		1600	(6)		1600	(6)		1600	(6)	_	1250	Mbps
- f <sub>HSDR</sub> (data rate)	SERDES factor J = 2, uses DDR Registers	(6)	_	(7)	(6)	_	(7)	(6)	_	(7)	(6)		(7)	Mbps
	SERDES factor J = 1, uses SDR Register	(6)	_	(7)	(6)	_	(7)	(6)	_	(7)	(6)	_	(7)	Mbps
Emulated Differential I/O Standards with Three External Output Resistor Networks - f <sub>HSDR</sub> (data rate) <sup>(10)</sup>	SERDES factor J = 4 to 10 $(^{17})$	(6)		1100	(6)		1100	(6)		840	(6)		840	Mbps
t <sub>x Jitter</sub> - True Differential	Total Jitter for Data Rate 600 Mbps - 1.25 Gbps		_	160		_	160		_	160			160	ps
I/O Standards	Total Jitter for Data Rate < 600 Mbps	_	_	0.1			0.1			0.1		_	0.1	UI
t <sub>x Jitter</sub> - Emulated Differential I/O Standards	Total Jitter for Data Rate 600 Mbps - 1.25 Gbps	_	_	300	_	_	300	_	_	300	_		325	ps
with Three External Output Resistor Network	Total Jitter for Data Rate < 600 Mbps	_	_	0.2	_	_	0.2	_	_	0.2	_	_	0.25	UI

## Table 36. High-Speed I/O Specifications for Stratix V Devices (1), (2) (Part 2 of 4)

Figure 7 shows the dynamic phase alignment (DPA) lock time specifications with the DPA PLL calibration option enabled.

Figure 7. DPA Lock Time Specification with DPA PLL Calibration Enabled

rx_reset			
rx_dpa_locked			<u> </u>
			-

Table 37 lists the DPA lock time specifications for Stratix V devices.

Table 37. DPA Lock Time Specifications for Stratix V GX Devices Only (1), (2), (3)

Standard	Training Pattern	Number of Data Transitions in One Repetition of the Training Pattern	Number of Repetitions per 256 Data Transitions <sup>(4)</sup>	Maximum
SPI-4	00000000001111111111	2	128	640 data transitions
Parallel Rapid I/O	00001111	2	128	640 data transitions
Parallel Rapid I/O	10010000	4	64	640 data transitions
Miscellaneous	10101010	8	32	640 data transitions
	01010101	8	32	640 data transitions

#### Notes to Table 37:

(1) The DPA lock time is for one channel.

(2) One data transition is defined as a 0-to-1 or 1-to-0 transition.

(3) The DPA lock time stated in this table applies to both commercial and industrial grade.

(4) This is the number of repetitions for the stated training pattern to achieve the 256 data transitions.

Figure 8 shows the **LVDS** soft-clock data recovery (CDR)/DPA sinusoidal jitter tolerance specification for a data rate  $\geq$  1.25 Gbps. Table 38 lists the **LVDS** soft-CDR/DPA sinusoidal jitter tolerance specification for a data rate  $\geq$  1.25 Gbps.





Clock Network	Parameter	Symbol	C	1	C2, C2L	, 12, 12L	C3, I3 I3	8, <b>13L</b> , YY	C4	,14	Unit
		-	Min	Max	Min	Max	Min	Max	Min	Max	
PHY Clock	Clock period jitter	$t_{JIT(per)}$	-25	25	-25	25	-30	30	-35	35	ps
	Cycle-to-cycle period jitter	$t_{\rm JIT(cc)}$	-50	50	-50	50	-60	60	-70	70	ps
	Duty cycle jitter	$t_{JIT(duty)}$	-37.5	37.5	-37.5	37.5	-45	45	-56	56	ps

### Table 42. Memory Output Clock Jitter Specification for Stratix V Devices (1), (Part 2 of 2) (2), (3)

### Notes to Table 42:

(1) The clock jitter specification applies to the memory output clock pins generated using differential signal-splitter and DDIO circuits clocked by a PLL output routed on a PHY, regional, or global clock network as specified. Altera recommends using PHY clock networks whenever possible.

(2) The clock jitter specification applies to the memory output clock pins clocked by an integer PLL.

(3) The memory output clock jitter is applicable when an input jitter of 30 ps peak-to-peak is applied with bit error rate (BER) -12, equivalent to 14 sigma.

### **OCT Calibration Block Specifications**

Table 43 lists the OCT calibration block specifications for Stratix V devices.

### Table 43. OCT Calibration Block Specifications for Stratix V Devices

Symbol	Description	Min	Тур	Max	Unit
OCTUSRCLK	Clock required by the OCT calibration blocks	—	—	20	MHz
T <sub>OCTCAL</sub>	Number of OCTUSRCLK clock cycles required for OCT $\rm R_S/R_T$ calibration		1000	_	Cycles
T <sub>OCTSHIFT</sub>	Number of OCTUSRCLK clock cycles required for the OCT code to shift out	_	32	_	Cycles
T <sub>RS_RT</sub>	Time required between the dyn_term_ctrl and oe signal transitions in a bidirectional I/O buffer to dynamically switch between OCT $R_S$ and $R_T$ (Figure 10)		2.5		ns

Figure 10 shows the timing diagram for the oe and dyn\_term\_ctrl signals.

### Figure 10. Timing Diagram for oe and dyn\_term\_ctrl Signals



Symbol	Description	Min	Max	Unit
t <sub>JPH</sub>	JTAG port hold time	5	—	ns
t <sub>JPCO</sub>	JTAG port clock to output	—	11 <sup>(1)</sup>	ns
t <sub>JPZX</sub>	JTAG port high impedance to valid output	—	14 <sup>(1)</sup>	ns
t <sub>JPXZ</sub>	JTAG port valid output to high impedance	—	<b>14</b> <sup>(1)</sup>	ns

Table 46. JTAG Timing Parameters and Values for Stratix V Devices

Notes to Table 46:

(1) A 1 ns adder is required for each V<sub>CCI0</sub> voltage step down from 3.0 V. For example,  $t_{JPC0} = 12$  ns if V<sub>CCI0</sub> of the TDO I/O bank = 2.5 V, or 13 ns if it equals 1.8 V.

(2) The minimum TCK clock period is 167 ns if VCCBAT is within the range 1.2V-1.5V when you perform the volatile key programming.

## **Raw Binary File Size**

For the POR delay specification, refer to the "POR Delay Specification" section of the "Configuration, Design Security, and Remote System Upgrades in Stratix V Devices".

Table 47 lists the uncompressed raw binary file (.rbf) sizes for Stratix V devices.

Family	Device Package		Configuration .rbf Size (bits)	IOCSR .rbf Size (bits) <sup>(4), (5)</sup>	
	500742	H35, F40, F35 <sup>(2)</sup>	213,798,880	562,392	
	JOUNAS	H29, F35 <sup>(3)</sup>	137,598,880	564,504	
	5SGXA4	—	213,798,880	563,672	
	5SGXA5	—	269,979,008	562,392	
	5SGXA7	—	269,979,008	562,392	
Stratix V GX	5SGXA9	—	342,742,976	700,888	
	5SGXAB	—	342,742,976	700,888	
	5SGXB5	—	270,528,640	584,344	
	5SGXB6	—	270,528,640	584,344	
	5SGXB9	—	342,742,976	700,888	
	5SGXBB	—	342,742,976	700,888	
Stratix V CT	5SGTC5	—	269,979,008	562,392	
	5SGTC7	_	269,979,008	562,392	
	5SGSD3	—	137,598,880	564,504	
	590904	F1517	213,798,880	563,672	
Stratix V GS	J303D4		137,598,880	564,504	
	5SGSD5		213,798,880	563,672	
	5SGSD6		293,441,888	565,528	
	5SGSD8	—	293,441,888	565,528	

Table 47. Uncompressed .rbf Sizes for Stratix V Devices

## **Active Serial Configuration Timing**

Table 52 lists the DCLK frequency specification in the AS configuration scheme.

Fable 52.	DCLK Frequency	Specification in th	e AS Configuration	Scheme <sup>(1),</sup>	(2)
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Minimum	Typical	Maximum	Unit
5.3	7.9	12.5	MHz
10.6	15.7	25.0	MHz
21.3	31.4	50.0	MHz
42.6	62.9	100.0	MHz

#### Notes to Table 52:

(1) This applies to the DCLK frequency specification when using the internal oscillator as the configuration clock source.

(2) The AS multi-device configuration scheme does not support DCLK frequency of 100 MHz.

Figure 14 shows the single-device configuration setup for an AS ×1 mode.





#### Notes to Figure 14:

- (1) If you are using AS  $\times 4$  mode, this signal represents the AS\_DATA[3..0] and EPCQ sends in 4-bits of data for each DCLK cycle.
- (2) The initialization clock can be from internal oscillator or CLKUSR pin.
- (3) After the option bit to enable the INIT\_DONE pin is configured into the device, the INIT\_DONE goes low.

Table 53 lists the timing parameters for AS  $\times 1$  and AS  $\times 4$  configurations in Stratix V devices.

Table JS. As fining falancees for as $\times 1$ and as $\times 4$ configurations in straits V devices $(2, 2, 2, 3, 3, 3, 3, 3, 3, 3, 3, 3, 3, 3, 3, 3,$	Table 53.	AS Timing	<b>Parameters for AS</b>	$\times$ 1 and AS $\times$ 4 Confi	gurations in Stratix V	/ Devices <sup>(1), (2)</sup>	(Part 1 of 2)
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Symbol	Parameter	Minimum	Maximum	Units
t <sub>CO</sub>	DCLK falling edge to AS_DATA0/ASDO output	—	2	ns
t <sub>SU</sub>	Data setup time before falling edge on DCLK	1.5	_	ns
t <sub>H</sub>	Data hold time after falling edge on DCLK	0	_	ns

Parameter Available	Min	Fast	Model				Slow Model					
(1)	<sup>(1)</sup> Settings	<b>Offset</b> (2)	Industrial	Commercial	C1	C2	C3	C4	12	13, 13YY	14	Unit
D3	8	0	1.587	1.699	2.793	2.793	2.992	3.192	2.811	3.047	3.257	ns
D4	64	0	0.464	0.492	0.838	0.838	0.924	1.011	0.843	0.920	1.006	ns
D5	64	0	0.464	0.493	0.838	0.838	0.924	1.011	0.844	0.921	1.006	ns
D6	32	0	0.229	0.244	0.415	0.415	0.458	0.503	0.418	0.456	0.499	ns

Table 58.	IOE Pro	grammable De	lay for	Stratix V	V Devices	(Part 2 of 2	)
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#### Notes to Table 58:

(1) You can set this value in the Quartus II software by selecting D1, D2, D3, D5, and D6 in the Assignment Name column of Assignment Editor.

(2) Minimum offset does not include the intrinsic delay.

## **Programmable Output Buffer Delay**

Table 59 lists the delay chain settings that control the rising and falling edge delays of the output buffer. The default delay is 0 ps.

Symbol	Parameter	Typical	Unit
	Rising and/or falling edge delay	0 (default)	ps
Dauman		25	ps
DOUTBUF		50	ps
		75	ps

Note to Table 59:

(1) You can set the programmable output buffer delay in the Quartus II software by setting the Output Buffer Delay Control assignment to either positive, negative, or both edges, with the specific values stated here (in ps) for the Output Buffer Delay assignment.

# Glossary

Table 60 lists the glossary for this chapter.

Table 60. Glossary (Part 1 of 4)

Letter	Subject	Definitions	
Α			
В	—	—	
С			
D	—	_	
E	—	_	
F	f <sub>HSCLK</sub>	Left and right PLL input clock frequency.	
	f <sub>HSDR</sub>	High-speed I/O block—Maximum and minimum <b>LVDS</b> data transfer rate (f <sub>HSDR</sub> = 1/TUI), non-DPA.	
	f <sub>hsdrdpa</sub>	High-speed I/O block—Maximum and minimum <b>LVDS</b> data transfer rate (f <sub>HSDRDPA</sub> = 1/TUI), DPA.	

Table 60.	Glossary	(Part 3 of 4)
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Letter	Subject	Definitions		
	SW (sampling window)	Timing Diagram—the period of time during which the data must be valid in order to capture it correctly. The setup and hold times determine the ideal strobe position within the sampling window, as shown:         Bit Time         0.5 x TCCS       RSKM         Sampling Window       RSKM         0.5 x TCCS       RSKM		
S	Single-ended voltage referenced I/O standard	The JEDEC standard for <b>SSTL</b> and <b>HSTL</b> I/O defines both the AC and DC input signal values. The AC values indicate the voltage levels at which the receiver must meet its timing specifications. The DC values indicate the voltage levels at which the final logic state of the receiver is unambiguously defined. After the receiver input has crossed the AC value, the receiver changes to the new logic state. The new logic state is then maintained as long as the input stays beyond the DC threshold. This approach is intended to provide predictable receiver timing in the presence of input waveform ringing: <i>Single-Ended Voltage Referenced I/O Standard</i> 		
	t <sub>C</sub>	High-speed receiver and transmitter input and output clock period.		
	TCCS (channel- to-channel-skew)	The timing difference between the fastest and slowest output edges, including $t_{CO}$ variation and clock skew, across channels driven by the same PLL. The clock is included in the TCCS measurement (refer to the <i>Timing Diagram</i> figure under <b>SW</b> in this table).		
	touty	High-speed I/O block—Duty cycle on the high-speed transmitter output clock.		
т		<b>Timing Unit Interval (TUI)</b> The timing budget allowed for skew, propagation delays, and the data sampling window.		
		(TUI = 1/(receiver input clock frequency multiplication factor) = $t_c/w$ )		
	t <sub>FALL</sub>	Signal high-to-low transition time (80-20%)		
	t <sub>INCCJ</sub>	Cycle-to-cycle jitter tolerance on the PLL clock input.		
	t <sub>outpj_i0</sub>	Period jitter on the general purpose I/O driven by a PLL.		
	t <sub>outpj_dc</sub>	Period jitter on the dedicated clock output driven by a PLL.		
	t <sub>RISE</sub>	Signal low-to-high transition time (20-80%)		
U	—	_		

Letter	Subject	Definitions
	V <sub>CM(DC)</sub>	DC common mode input voltage.
	V <sub>ICM</sub>	Input common mode voltage—The common mode of the differential signal at the receiver.
	V <sub>ID</sub>	Input differential voltage swing—The difference in voltage between the positive and complementary conductors of a differential transmission at the receiver.
	V <sub>DIF(AC)</sub>	AC differential input voltage—Minimum AC input differential voltage required for switching.
	V <sub>DIF(DC)</sub>	DC differential input voltage— Minimum DC input differential voltage required for switching.
	V <sub>IH</sub>	Voltage input high—The minimum positive voltage applied to the input which is accepted by the device as a logic high.
	V <sub>IH(AC)</sub>	High-level AC input voltage
	V <sub>IH(DC)</sub>	High-level DC input voltage
V	V <sub>IL</sub>	Voltage input low—The maximum positive voltage applied to the input which is accepted by the device as a logic low.
	V <sub>IL(AC)</sub>	Low-level AC input voltage
	V <sub>IL(DC)</sub>	Low-level DC input voltage
	V <sub>OCM</sub>	Output common mode voltage—The common mode of the differential signal at the transmitter.
	V <sub>OD</sub>	Output differential voltage swing—The difference in voltage between the positive and complementary conductors of a differential transmission at the transmitter.
	V <sub>SWING</sub>	Differential input voltage
	V <sub>X</sub>	Input differential cross point voltage
	V <sub>OX</sub>	Output differential cross point voltage
W	W	High-speed I/O block—clock boost factor
X		
Y	—	—
Z		

### Table 60. Glossary (Part 4 of 4)