



Welcome to [E-XFL.COM](https://www.e-xfl.com)

Understanding [Embedded - FPGAs \(Field Programmable Gate Array\)](#)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Obsolete
Number of LABs/CLBs	185000
Number of Logic Elements/Cells	490000
Total RAM Bits	46080000
Number of I/O	696
Number of Gates	-
Voltage - Supply	0.87V ~ 0.93V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	1517-BBGA, FCBGA
Supplier Device Package	1517-FBGA (40x40)
Purchase URL	https://www.e-xfl.com/product-detail/intel/5sgxma5k1f40c2n

Table 7. Recommended Transceiver Power Supply Operating Conditions for Stratix V GX, GS, and GT Devices (Part 2 of 2)

Symbol	Description	Devices	Minimum ⁽⁴⁾	Typical	Maximum ⁽⁴⁾	Unit
V_{CCR_GXBR} (2)	Receiver analog power supply (right side)	GX, GS, GT	0.82	0.85	0.88	V
			0.87	0.90	0.93	
			0.97	1.0	1.03	
			1.03	1.05	1.07	
V_{CCR_GTBR}	Receiver analog power supply for GT channels (right side)	GT	1.02	1.05	1.08	V
V_{CCT_GXBL} (2)	Transmitter analog power supply (left side)	GX, GS, GT	0.82	0.85	0.88	V
			0.87	0.90	0.93	
			0.97	1.0	1.03	
			1.03	1.05	1.07	
V_{CCT_GXBR} (2)	Transmitter analog power supply (right side)	GX, GS, GT	0.82	0.85	0.88	V
			0.87	0.90	0.93	
			0.97	1.0	1.03	
			1.03	1.05	1.07	
V_{CCT_GTBR}	Transmitter analog power supply for GT channels (right side)	GT	1.02	1.05	1.08	V
V_{CCL_GTBR}	Transmitter clock network power supply	GT	1.02	1.05	1.08	V
V_{CCH_GXBL}	Transmitter output buffer power supply (left side)	GX, GS, GT	1.425	1.5	1.575	V
V_{CCH_GXBR}	Transmitter output buffer power supply (right side)	GX, GS, GT	1.425	1.5	1.575	V

Notes to Table 7:

- (1) This supply must be connected to 3.0 V if the CMU PLL, receiver CDR, or both, are configured at a base data rate > 6.5 Gbps. Up to 6.5 Gbps, you can connect this supply to either 3.0 V or 2.5 V.
- (2) Refer to Table 8 to select the correct power supply level for your design.
- (3) When using ATX PLLs, the supply must be 3.0 V.
- (4) This value describes the budget for the DC (static) power supply tolerance and does not include the dynamic tolerance requirements. Refer to the PDN tool for the additional budget for the dynamic tolerance requirements.

Table 19. Single-Ended SSTL, HSTL, and HSUL I/O Standards Signal Specifications for Stratix V Devices (Part 2 of 2)

I/O Standard	$V_{IL(DC)}$ (V)		$V_{IH(DC)}$ (V)		$V_{IL(AC)}$ (V)	$V_{IH(AC)}$ (V)	V_{OL} (V)	V_{OH} (V)	I_{ol} (mA)	I_{oh} (mA)
	Min	Max	Min	Max	Max	Min	Max	Min		
HSTL-18 Class I	—	$V_{REF} - 0.1$	$V_{REF} + 0.1$	—	$V_{REF} - 0.2$	$V_{REF} + 0.2$	0.4	$V_{CCIO} - 0.4$	8	-8
HSTL-18 Class II	—	$V_{REF} - 0.1$	$V_{REF} + 0.1$	—	$V_{REF} - 0.2$	$V_{REF} + 0.2$	0.4	$V_{CCIO} - 0.4$	16	-16
HSTL-15 Class I	—	$V_{REF} - 0.1$	$V_{REF} + 0.1$	—	$V_{REF} - 0.2$	$V_{REF} + 0.2$	0.4	$V_{CCIO} - 0.4$	8	-8
HSTL-15 Class II	—	$V_{REF} - 0.1$	$V_{REF} + 0.1$	—	$V_{REF} - 0.2$	$V_{REF} + 0.2$	0.4	$V_{CCIO} - 0.4$	16	-16
HSTL-12 Class I	-0.15	$V_{REF} - 0.08$	$V_{REF} + 0.08$	$V_{CCIO} + 0.15$	$V_{REF} - 0.15$	$V_{REF} + 0.15$	$0.25^* V_{CCIO}$	$0.75^* V_{CCIO}$	8	-8
HSTL-12 Class II	-0.15	$V_{REF} - 0.08$	$V_{REF} + 0.08$	$V_{CCIO} + 0.15$	$V_{REF} - 0.15$	$V_{REF} + 0.15$	$0.25^* V_{CCIO}$	$0.75^* V_{CCIO}$	16	-16
HSUL-12	—	$V_{REF} - 0.13$	$V_{REF} + 0.13$	—	$V_{REF} - 0.22$	$V_{REF} + 0.22$	$0.1^* V_{CCIO}$	$0.9^* V_{CCIO}$	—	—

Table 20. Differential SSTL I/O Standards for Stratix V Devices

I/O Standard	V_{CCIO} (V)			$V_{SWING(DC)}$ (V)		$V_{X(AC)}$ (V)			$V_{SWING(AC)}$ (V)	
	Min	Typ	Max	Min	Max	Min	Typ	Max	Min	Max
SSTL-2 Class I, II	2.375	2.5	2.625	0.3	$V_{CCIO} + 0.6$	$V_{CCIO}/2 - 0.2$	—	$V_{CCIO}/2 + 0.2$	0.62	$V_{CCIO} + 0.6$
SSTL-18 Class I, II	1.71	1.8	1.89	0.25	$V_{CCIO} + 0.6$	$V_{CCIO}/2 - 0.175$	—	$V_{CCIO}/2 + 0.175$	0.5	$V_{CCIO} + 0.6$
SSTL-15 Class I, II	1.425	1.5	1.575	0.2	(1)	$V_{CCIO}/2 - 0.15$	—	$V_{CCIO}/2 + 0.15$	0.35	—
SSTL-135 Class I, II	1.283	1.35	1.45	0.2	(1)	$V_{CCIO}/2 - 0.15$	$V_{CCIO}/2$	$V_{CCIO}/2 + 0.15$	$2(V_{IH(AC)} - V_{REF})$	$2(V_{IL(AC)} - V_{REF})$
SSTL-125 Class I, II	1.19	1.25	1.31	0.18	(1)	$V_{CCIO}/2 - 0.15$	$V_{CCIO}/2$	$V_{CCIO}/2 + 0.15$	$2(V_{IH(AC)} - V_{REF})$	—
SSTL-12 Class I, II	1.14	1.2	1.26	0.18	—	$V_{REF} - 0.15$	$V_{CCIO}/2$	$V_{REF} + 0.15$	-0.30	0.30

Note to Table 20:

(1) The maximum value for $V_{SWING(DC)}$ is not defined. However, each single-ended signal needs to be within the respective single-ended limits ($V_{IH(DC)}$ and $V_{IL(DC)}$).

Table 21. Differential HSTL and HSUL I/O Standards for Stratix V Devices (Part 1 of 2)

I/O Standard	V_{CCIO} (V)			$V_{DIF(DC)}$ (V)		$V_{X(AC)}$ (V)			$V_{CM(DC)}$ (V)			$V_{DIF(AC)}$ (V)	
	Min	Typ	Max	Min	Max	Min	Typ	Max	Min	Typ	Max	Min	Max
HSTL-18 Class I, II	1.71	1.8	1.89	0.2	—	0.78	—	1.12	0.78	—	1.12	0.4	—
HSTL-15 Class I, II	1.425	1.5	1.575	0.2	—	0.68	—	0.9	0.68	—	0.9	0.4	—

Table 21. Differential HSTL and HSUL I/O Standards for Stratix V Devices (Part 2 of 2)

I/O Standard	V_{CCIO} (V)			$V_{DIF(DC)}$ (V)		$V_{X(AC)}$ (V)			$V_{CM(DC)}$ (V)			$V_{DIF(AC)}$ (V)	
	Min	Typ	Max	Min	Max	Min	Typ	Max	Min	Typ	Max	Min	Max
HSTL-12 Class I, II	1.14	1.2	1.26	0.16	$V_{CCIO} + 0.3$	—	$0.5^* V_{CCIO}$	—	$0.4^* V_{CCIO}$	$0.5^* V_{CCIO}$	$0.6^* V_{CCIO}$	0.3	$V_{CCIO} + 0.48$
HSUL-12	1.14	1.2	1.3	0.26	0.26	$0.5^* V_{CCIO} - 0.12$	$0.5^* V_{CCIO}$	$0.5^* V_{CCIO} + 0.12$	$0.4^* V_{CCIO}$	$0.5^* V_{CCIO}$	$0.6^* V_{CCIO}$	0.44	0.44

Table 22. Differential I/O Standard Specifications for Stratix V Devices ⁽⁷⁾

I/O Standard	V_{CCIO} (V) ⁽¹⁰⁾			V_{ID} (mV) ⁽⁸⁾			$V_{ICM(DC)}$ (V)			V_{OD} (V) ⁽⁶⁾			V_{OCM} (V) ⁽⁶⁾		
	Min	Typ	Max	Min	Condition	Max	Min	Condition	Max	Min	Typ	Max	Min	Typ	Max
PCML	Transmitter, receiver, and input reference clock pins of the high-speed transceivers use the PCML I/O standard. For transmitter, receiver, and reference clock I/O pin specifications, refer to Table 23 on page 18.														
2.5 V LVDS ⁽¹⁾	2.375	2.5	2.625	100	$V_{CM} = 1.25$ V	—	0.05	$D_{MAX} \leq 700$ Mbps	1.8	0.247	—	0.6	1.125	1.25	1.375
						—	1.05	$D_{MAX} > 700$ Mbps	1.55	0.247	—	0.6	1.125	1.25	1.375
BLVDS ⁽⁵⁾	2.375	2.5	2.625	100	—	—	—	—	—	—	—	—	—	—	—
RSDS (HIO) ⁽²⁾	2.375	2.5	2.625	100	$V_{CM} = 1.25$ V	—	0.3	—	1.4	0.1	0.2	0.6	0.5	1.2	1.4
Mini-LVDS (HIO) ⁽³⁾	2.375	2.5	2.625	200	—	600	0.4	—	1.325	0.25	—	0.6	1	1.2	1.4
LVPECL ^{(4), (9)}	—	—	—	300	—	—	0.6	$D_{MAX} \leq 700$ Mbps	1.8	—	—	—	—	—	—
	—	—	—	300	—	—	1	$D_{MAX} > 700$ Mbps	1.6	—	—	—	—	—	—

Notes to Table 22:

- (1) For optimized LVDS receiver performance, the receiver voltage input range must be between 1.0 V to 1.6 V for data rates above 700 Mbps, and 0 V to 1.85 V for data rates below 700 Mbps.
- (2) For optimized RSDS receiver performance, the receiver voltage input range must be between 0.25 V to 1.45 V.
- (3) For optimized Mini-LVDS receiver performance, the receiver voltage input range must be between 0.3 V to 1.425 V.
- (4) For optimized LVPECL receiver performance, the receiver voltage input range must be between 0.85 V to 1.75 V for data rate above 700 Mbps and 0.45 V to 1.95 V for data rate below 700 Mbps.
- (5) There are no fixed V_{ICM} , V_{OD} , and V_{OCM} specifications for BLVDS. They depend on the system topology.
- (6) RL range: $90 \leq RL \leq 110 \Omega$.
- (7) The 1.4-V and 1.5-V PCML transceiver I/O standard specifications are described in "Transceiver Performance Specifications" on page 18.
- (8) The minimum V_{ID} value is applicable over the entire common mode range, V_{CM} .
- (9) LVPECL is only supported on dedicated clock input pins.
- (10) Differential inputs are powered by VCCPD which requires 2.5 V.

Power Consumption

Altera offers two ways to estimate power consumption for a design—the Excel-based Early Power Estimator and the Quartus® II PowerPlay Power Analyzer feature.

Table 23. Transceiver Specifications for Stratix V GX and GS Devices ⁽¹⁾ (Part 2 of 7)

Symbol/ Description	Conditions	Transceiver Speed Grade 1			Transceiver Speed Grade 2			Transceiver Speed Grade 3			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Spread-spectrum downspread	PCIe	—	0 to -0.5	—	—	0 to -0.5	—	—	0 to -0.5	—	%
On-chip termination resistors ⁽²¹⁾	—	—	100	—	—	100	—	—	100	—	Ω
Absolute V_{MAX} ⁽⁵⁾	Dedicated reference clock pin	—	—	1.6	—	—	1.6	—	—	1.6	V
	RX reference clock pin	—	—	1.2	—	—	1.2	—	—	1.2	
Absolute V_{MIN}	—	-0.4	—	—	-0.4	—	—	-0.4	—	—	V
Peak-to-peak differential input voltage	—	200	—	1600	200	—	1600	200	—	1600	mV
V_{ICM} (AC coupled) ⁽³⁾	Dedicated reference clock pin	1050/1000/900/850 ⁽²⁾			1050/1000/900/850 ⁽²⁾			1050/1000/900/850 ⁽²⁾			mV
	RX reference clock pin	1.0/0.9/0.85 ⁽⁴⁾			1.0/0.9/0.85 ⁽⁴⁾			1.0/0.9/0.85 ⁽⁴⁾			V
V_{ICM} (DC coupled)	HCSL I/O standard for PCIe reference clock	250	—	550	250	—	550	250	—	550	mV
Transmitter REFCLK Phase Noise (622 MHz) ⁽²⁰⁾	100 Hz	—	—	-70	—	—	-70	—	—	-70	dBc/Hz
	1 kHz	—	—	-90	—	—	-90	—	—	-90	dBc/Hz
	10 kHz	—	—	-100	—	—	-100	—	—	-100	dBc/Hz
	100 kHz	—	—	-110	—	—	-110	—	—	-110	dBc/Hz
	≥ 1 MHz	—	—	-120	—	—	-120	—	—	-120	dBc/Hz
Transmitter REFCLK Phase Jitter (100 MHz) ⁽¹⁷⁾	10 kHz to 1.5 MHz (PCIe)	—	—	3	—	—	3	—	—	3	ps (rms)
R_{REF} ⁽¹⁹⁾	—	—	1800 $\pm 1\%$	—	—	1800 $\pm 1\%$	—	—	1800 $\pm 1\%$	—	Ω
Transceiver Clocks											
fixedclk clock frequency	PCIe Receiver Detect	—	100 or 125	—	—	100 or 125	—	—	100 or 125	—	MHz

Table 28. Transceiver Specifications for Stratix V GT Devices (Part 2 of 5) ⁽¹⁾

Symbol/ Description	Conditions	Transceiver Speed Grade 2			Transceiver Speed Grade 3			Unit
		Min	Typ	Max	Min	Typ	Max	
Transmitter REFCLK Phase Noise (622 MHz) ⁽¹⁸⁾	100 Hz	—	—	-70	—	—	-70	dBc/Hz
	1 kHz	—	—	-90	—	—	-90	
	10 kHz	—	—	-100	—	—	-100	
	100 kHz	—	—	-110	—	—	-110	
	≥ 1 MHz	—	—	-120	—	—	-120	
Transmitter REFCLK Phase Jitter (100 MHz) ⁽¹⁵⁾	10 kHz to 1.5 MHz (PCIe)	—	—	3	—	—	3	ps (rms)
RREF ⁽¹⁷⁾	—	—	1800 ± 1%	—	—	1800 ± 1%	—	Ω
Transceiver Clocks								
fixedclk clock frequency	PCIe Receiver Detect	—	100 or 125	—	—	100 or 125	—	MHz
Reconfiguration clock (mgmt_clk_clk) frequency	—	100	—	125	100	—	125	MHz
Receiver								
Supported I/O Standards	—	1.4-V PCML, 1.5-V PCML, 2.5-V PCML, LVPECL, and LVDS						
Data rate (Standard PCS) ⁽²¹⁾	GX channels	600	—	8500	600	—	8500	Mbps
Data rate (10G PCS) ⁽²¹⁾	GX channels	600	—	12,500	600	—	12,500	Mbps
Data rate	GT channels	19,600	—	28,050	19,600	—	25,780	Mbps
Absolute V _{MAX} for a receiver pin ⁽³⁾	GT channels	—	—	1.2	—	—	1.2	V
Absolute V _{MIN} for a receiver pin	GT channels	-0.4	—	—	-0.4	—	—	V
Maximum peak-to-peak differential input voltage V _{ID} (diff p-p) before device configuration ⁽²⁰⁾	GT channels	—	—	1.6	—	—	1.6	V
	GX channels	⁽⁸⁾						
Maximum peak-to-peak differential input voltage V _{ID} (diff p-p) after device configuration ⁽¹⁶⁾ , ⁽²⁰⁾	GT channels V _{CCR_GTB} = 1.05 V (V _{ICM} = 0.65 V)	—	—	2.2	—	—	2.2	V
	GX channels	⁽⁸⁾						
Minimum differential eye opening at receiver serial input pins ⁽⁴⁾ , ⁽²⁰⁾	GT channels	200	—	—	200	—	—	mV
	GX channels	⁽⁸⁾						

Table 28. Transceiver Specifications for Stratix V GT Devices (Part 3 of 5) ⁽¹⁾

Symbol/ Description	Conditions	Transceiver Speed Grade 2			Transceiver Speed Grade 3			Unit
		Min	Typ	Max	Min	Typ	Max	
Differential on-chip termination resistors ⁽⁷⁾	GT channels	—	100	—	—	100	—	Ω
Differential on-chip termination resistors for GX channels ⁽¹⁹⁾	85- Ω setting	—	85 $\pm$ 30%	—	—	85 $\pm$ 30%	—	Ω
	100- Ω setting	—	100 $\pm$ 30%	—	—	100 $\pm$ 30%	—	Ω
	120- Ω setting	—	120 $\pm$ 30%	—	—	120 $\pm$ 30%	—	Ω
	150- Ω setting	—	150 $\pm$ 30%	—	—	150 $\pm$ 30%	—	Ω
V _{ICM} (AC coupled)	GT channels	—	650	—	—	650	—	mV
VICM (AC and DC coupled) for GX Channels	VCCR_GXB = 0.85 V or 0.9 V	—	600	—	—	600	—	mV
	VCCR_GXB = 1.0 V full bandwidth	—	700	—	—	700	—	mV
	VCCR_GXB = 1.0 V half bandwidth	—	750	—	—	750	—	mV
t _{LTR} ⁽⁹⁾	—	—	—	10	—	—	10	μ s
t _{LTD} ⁽¹⁰⁾	—	4	—	—	4	—	—	μ s
t _{LTD_manual} ⁽¹¹⁾	—	4	—	—	4	—	—	μ s
t _{LTR_LTD_manual} ⁽¹²⁾	—	15	—	—	15	—	—	μ s
Run Length	GT channels	—	—	72	—	—	72	CID
	GX channels	⁽⁸⁾						
CDR PPM	GT channels	—	—	1000	—	—	1000	$\pm$ PPM
	GX channels	⁽⁸⁾						
Programmable equalization (AC Gain) ⁽⁵⁾	GT channels	—	—	14	—	—	14	dB
	GX channels	⁽⁸⁾						
Programmable DC gain ⁽⁶⁾	GT channels	—	—	7.5	—	—	7.5	dB
	GX channels	⁽⁸⁾						
Differential on-chip termination resistors ⁽⁷⁾	GT channels	—	100	—	—	100	—	Ω
Transmitter								
Supported I/O Standards	—	1.4-V and 1.5-V PCML						
Data rate (Standard PCS)	GX channels	600	—	8500	600	—	8500	Mbps
Data rate (10G PCS)	GX channels	600	—	12,500	600	—	12,500	Mbps

Table 31. PLL Specifications for Stratix V Devices (Part 2 of 3)

Symbol	Parameter	Min	Typ	Max	Unit
t_{INCCJ} ^{(3), (4)}	Input clock cycle-to-cycle jitter ($f_{\text{REF}} \geq 100$ MHz)	—	—	0.15	UI (p-p)
	Input clock cycle-to-cycle jitter ($f_{\text{REF}} < 100$ MHz)	−750	—	+750	ps (p-p)
$t_{\text{OUTPJ_DC}}$ ⁽⁵⁾	Period Jitter for dedicated clock output ($f_{\text{OUT}} \geq 100$ MHz)	—	—	175 ⁽¹⁾	ps (p-p)
	Period Jitter for dedicated clock output ($f_{\text{OUT}} < 100$ MHz)	—	—	17.5 ⁽¹⁾	mUI (p-p)
$t_{\text{FOUTPJ_DC}}$ ⁽⁵⁾	Period Jitter for dedicated clock output in fractional PLL ($f_{\text{OUT}} \geq 100$ MHz)	—	—	250 ⁽¹¹⁾ , 175 ⁽¹²⁾	ps (p-p)
	Period Jitter for dedicated clock output in fractional PLL ($f_{\text{OUT}} < 100$ MHz)	—	—	25 ⁽¹¹⁾ , 17.5 ⁽¹²⁾	mUI (p-p)
$t_{\text{OUTCCJ_DC}}$ ⁽⁵⁾	Cycle-to-Cycle Jitter for a dedicated clock output ($f_{\text{OUT}} \geq 100$ MHz)	—	—	175	ps (p-p)
	Cycle-to-Cycle Jitter for a dedicated clock output ($f_{\text{OUT}} < 100$ MHz)	—	—	17.5	mUI (p-p)
$t_{\text{FOUTCCJ_DC}}$ ⁽⁵⁾	Cycle-to-cycle Jitter for a dedicated clock output in fractional PLL ($f_{\text{OUT}} \geq 100$ MHz)	—	—	250 ⁽¹¹⁾ , 175 ⁽¹²⁾	ps (p-p)
	Cycle-to-cycle Jitter for a dedicated clock output in fractional PLL ($f_{\text{OUT}} < 100$ MHz)+	—	—	25 ⁽¹¹⁾ , 17.5 ⁽¹²⁾	mUI (p-p)
$t_{\text{OUTPJ_IO}}$ ^{(5), (8)}	Period Jitter for a clock output on a regular I/O in integer PLL ($f_{\text{OUT}} \geq 100$ MHz)	—	—	600	ps (p-p)
	Period Jitter for a clock output on a regular I/O ($f_{\text{OUT}} < 100$ MHz)	—	—	60	mUI (p-p)
$t_{\text{FOUTPJ_IO}}$ ^{(5), (8), (11)}	Period Jitter for a clock output on a regular I/O in fractional PLL ($f_{\text{OUT}} \geq 100$ MHz)	—	—	600 ⁽¹⁰⁾	ps (p-p)
	Period Jitter for a clock output on a regular I/O in fractional PLL ($f_{\text{OUT}} < 100$ MHz)	—	—	60 ⁽¹⁰⁾	mUI (p-p)
$t_{\text{OUTCCJ_IO}}$ ^{(5), (8)}	Cycle-to-cycle Jitter for a clock output on a regular I/O in integer PLL ($f_{\text{OUT}} \geq 100$ MHz)	—	—	600	ps (p-p)
	Cycle-to-cycle Jitter for a clock output on a regular I/O in integer PLL ($f_{\text{OUT}} < 100$ MHz)	—	—	60 ⁽¹⁰⁾	mUI (p-p)
$t_{\text{FOUTCCJ_IO}}$ ^{(5), (8), (11)}	Cycle-to-cycle Jitter for a clock output on a regular I/O in fractional PLL ($f_{\text{OUT}} \geq 100$ MHz)	—	—	600 ⁽¹⁰⁾	ps (p-p)
	Cycle-to-cycle Jitter for a clock output on a regular I/O in fractional PLL ($f_{\text{OUT}} < 100$ MHz)	—	—	60	mUI (p-p)
$t_{\text{CASC_OUTPJ_DC}}$ ^{(5), (6)}	Period Jitter for a dedicated clock output in cascaded PLLs ($f_{\text{OUT}} \geq 100$ MHz)	—	—	175	ps (p-p)
	Period Jitter for a dedicated clock output in cascaded PLLs ($f_{\text{OUT}} < 100$ MHz)	—	—	17.5	mUI (p-p)
f_{DRIFT}	Frequency drift after PFDENA is disabled for a duration of 100 μ s	—	—	± 10	%
dK_{BIT}	Bit number of Delta Sigma Modulator (DSM)	8	24	32	Bits
K_{VALUE}	Numerator of Fraction	128	8388608	2147483648	—

Table 31. PLL Specifications for Stratix V Devices (Part 3 of 3)

Symbol	Parameter	Min	Typ	Max	Unit
f_{RES}	Resolution of VCO frequency ($f_{INPFD} = 100$ MHz)	390625	5.96	0.023	Hz

Notes to Table 31:

- (1) This specification is limited in the Quartus II software by the I/O maximum frequency. The maximum I/O frequency is different for each I/O standard.
- (2) This specification is limited by the lower of the two: I/O f_{MAX} or f_{OUT} of the PLL.
- (3) A high input jitter directly affects the PLL output jitter. To have low PLL output clock jitter, you must provide a clean clock source < 120 ps.
- (4) f_{REF} is f_{IN}/N when $N = 1$.
- (5) Peak-to-peak jitter with a probability level of 10^{-12} (14 sigma, 99.9999999974404% confidence level). The output jitter specification applies to the intrinsic jitter of the PLL, when an input jitter of 30 ps is applied. The external memory interface clock output jitter specifications use a different measurement method and are available in Table 44 on page 52.
- (6) The cascaded PLL specification is only applicable with the following condition:
 - a. Upstream PLL: $0.59\text{MHz} \leq \text{Upstream PLL BW} < 1$ MHz
 - b. Downstream PLL: Downstream PLL BW > 2 MHz
- (7) High bandwidth PLL settings are not supported in external feedback mode.
- (8) The external memory interface clock output jitter specifications use a different measurement method, which is available in Table 42 on page 50.
- (9) The VCO frequency reported by the Quartus II software in the PLL Usage Summary section of the compilation report takes into consideration the VCO post-scale counter K value. Therefore, if the counter K has a value of 2, the frequency reported can be lower than the f_{VCO} specification.
- (10) This specification only covers fractional PLL for low bandwidth. The f_{VCO} for fractional value range 0.05 - 0.95 must be ≥ 1000 MHz, while f_{VCO} for fractional value range 0.20 - 0.80 must be ≥ 1200 MHz.
- (11) This specification only covered fractional PLL for low bandwidth. The f_{VCO} for fractional value range 0.05-0.95 must be ≥ 1000 MHz.
- (12) This specification only covered fractional PLL for low bandwidth. The f_{VCO} for fractional value range 0.20-0.80 must be ≥ 1200 MHz.

DSP Block Specifications

Table 32 lists the Stratix V DSP block performance specifications.

Table 32. Block Performance Specifications for Stratix V DSP Devices (Part 1 of 2)

Mode	Peformance							Unit
	C1	C2, C2L	I2, I2L	C3	I3, I3L, I3YY	C4	I4	
Modes using one DSP								
Three 9 x 9	600	600	600	480	480	420	420	MHz
One 18 x 18	600	600	600	480	480	420	400	MHz
Two partial 18 x 18 (or 16 x 16)	600	600	600	480	480	420	400	MHz
One 27 x 27	500	500	500	400	400	350	350	MHz
One 36 x 18	500	500	500	400	400	350	350	MHz
One sum of two 18 x 18(One sum of 2 16 x 16)	500	500	500	400	400	350	350	MHz
One sum of square	500	500	500	400	400	350	350	MHz
One 18 x 18 plus 36 (a x b) + c	500	500	500	400	400	350	350	MHz
Modes using two DSPs								
Three 18 x 18	500	500	500	400	400	350	350	MHz
One sum of four 18 x 18	475	475	475	380	380	300	300	MHz
One sum of two 27 x 27	465	465	450	380	380	300	290	MHz
One sum of two 36 x 18	475	475	475	380	380	300	300	MHz
One complex 18 x 18	500	500	500	400	400	350	350	MHz
One 36 x 36	475	475	475	380	380	300	300	MHz

Table 33. Memory Block Performance Specifications for Stratix V Devices ^{(1), (2)} (Part 2 of 2)

Memory	Mode	Resources Used		Performance							Unit
		ALUTs	Memory	C1	C2, C2L	C3	C4	I2, I2L	I3, I3L, I3YY	I4	
M20K Block	Single-port, all supported widths	0	1	700	700	650	550	700	500	450	MHz
	Simple dual-port, all supported widths	0	1	700	700	650	550	700	500	450	MHz
	Simple dual-port with the read-during-write option set to Old Data , all supported widths	0	1	525	525	455	400	525	455	400	MHz
	Simple dual-port with ECC enabled, 512 × 32	0	1	450	450	400	350	450	400	350	MHz
	Simple dual-port with ECC and optional pipeline registers enabled, 512 × 32	0	1	600	600	500	450	600	500	450	MHz
	True dual port, all supported widths	0	1	700	700	650	550	700	500	450	MHz
	ROM, all supported widths	0	1	700	700	650	550	700	500	450	MHz

Notes to Table 33:

- (1) To achieve the maximum memory block performance, use a memory block clock that comes through global clock routing from an on-chip PLL set to **50%** output duty cycle. Use the Quartus II software to report timing for this and other memory block clocking schemes.
- (2) When you use the error detection cyclical redundancy check (CRC) feature, there is no degradation in F_{MAX}.
- (3) The F_{MAX} specification is only achievable with Fitter options, **MLAB Implementation In 16-Bit Deep Mode** enabled.

Temperature Sensing Diode Specifications

Table 34 lists the internal TSD specification.

Table 34. Internal Temperature Sensing Diode Specification

Temperature Range	Accuracy	Offset Calibrated Option	Sampling Rate	Conversion Time	Resolution	Minimum Resolution with no Missing Codes
–40°C to 100°C	±8°C	No	1 MHz, 500 KHz	< 100 ms	8 bits	8 bits

Table 35 lists the specifications for the Stratix V external temperature sensing diode.

Table 35. External Temperature Sensing Diode Specifications for Stratix V Devices

Description	Min	Typ	Max	Unit
I _{bias} , diode source current	8	—	200	μA
V _{bias} , voltage across diode	0.3	—	0.9	V
Series resistance	—	—	< 1	Ω
Diode ideality factor	1.006	1.008	1.010	—

Table 36. High-Speed I/O Specifications for Stratix V Devices ^{(1), (2)} (Part 2 of 4)

Symbol	Conditions	C1			C2, C2L, I2, I2L			C3, I3, I3L, I3YY			C4,I4			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Transmitter														
True Differential I/O Standards - f _{HSDR} (data rate)	SERDES factor J = 3 to 10 ^{(9), (11), (12), (13), (14), (15), (16)}	(6)	—	1600	(6)	—	1434	(6)	—	1250	(6)	—	1050	Mbps
	SERDES factor J ≥ 4 LVDS TX with DPA ^{(12), (14), (15), (16)}	(6)	—	1600	(6)	—	1600	(6)	—	1600	(6)	—	1250	Mbps
	SERDES factor J = 2, uses DDR Registers	(6)	—	(7)	(6)	—	(7)	(6)	—	(7)	(6)	—	(7)	Mbps
	SERDES factor J = 1, uses SDR Register	(6)	—	(7)	(6)	—	(7)	(6)	—	(7)	(6)	—	(7)	Mbps
Emulated Differential I/O Standards with Three External Output Resistor Networks - f _{HSDR} (data rate) ⁽¹⁰⁾	SERDES factor J = 4 to 10 ⁽¹⁷⁾	(6)	—	1100	(6)	—	1100	(6)	—	840	(6)	—	840	Mbps
t _{x Jitter} - True Differential I/O Standards	Total Jitter for Data Rate 600 Mbps - 1.25 Gbps	—	—	160	—	—	160	—	—	160	—	—	160	ps
	Total Jitter for Data Rate < 600 Mbps	—	—	0.1	—	—	0.1	—	—	0.1	—	—	0.1	UI
t _{x Jitter} - Emulated Differential I/O Standards with Three External Output Resistor Network	Total Jitter for Data Rate 600 Mbps - 1.25 Gbps	—	—	300	—	—	300	—	—	300	—	—	325	ps
	Total Jitter for Data Rate < 600 Mbps	—	—	0.2	—	—	0.2	—	—	0.2	—	—	0.25	UI

Table 42. Memory Output Clock Jitter Specification for Stratix V Devices ⁽¹⁾, (Part 2 of 2) ⁽²⁾, ⁽³⁾

Clock Network	Parameter	Symbol	C1		C2, C2L, I2, I2L		C3, I3, I3L, I3YY		C4,I4		Unit
			Min	Max	Min	Max	Min	Max	Min	Max	
PHY Clock	Clock period jitter	$t_{JIT(per)}$	-25	25	-25	25	-30	30	-35	35	ps
	Cycle-to-cycle period jitter	$t_{JIT(cc)}$	-50	50	-50	50	-60	60	-70	70	ps
	Duty cycle jitter	$t_{JIT(duty)}$	-37.5	37.5	-37.5	37.5	-45	45	-56	56	ps

Notes to Table 42:

- (1) The clock jitter specification applies to the memory output clock pins generated using differential signal-splitter and DDIO circuits clocked by a PLL output routed on a PHY, regional, or global clock network as specified. Altera recommends using PHY clock networks whenever possible.
- (2) The clock jitter specification applies to the memory output clock pins clocked by an integer PLL.
- (3) The memory output clock jitter is applicable when an input jitter of 30 ps peak-to-peak is applied with bit error rate (BER) -12, equivalent to 14 sigma.

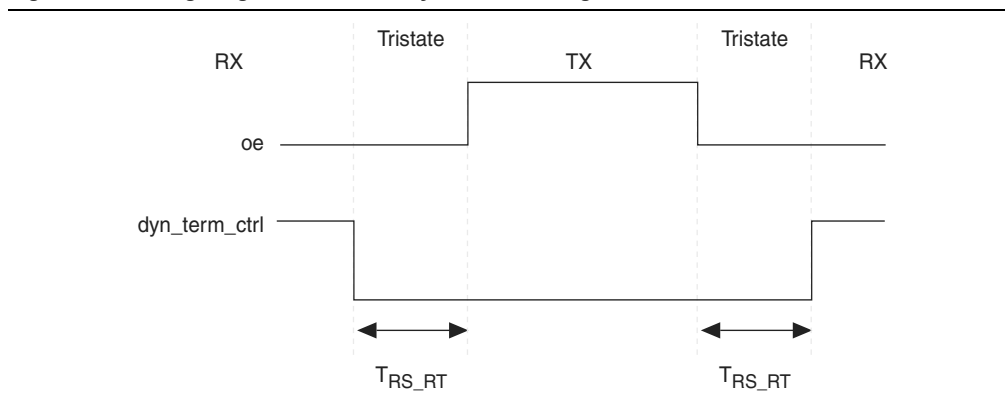
OCT Calibration Block Specifications

Table 43 lists the OCT calibration block specifications for Stratix V devices.

Table 43. OCT Calibration Block Specifications for Stratix V Devices

Symbol	Description	Min	Typ	Max	Unit
OCTUSRCLK	Clock required by the OCT calibration blocks	—	—	20	MHz
T_{OCTCAL}	Number of OCTUSRCLK clock cycles required for OCT R_S/R_T calibration	—	1000	—	Cycles
$T_{OCTSHIFT}$	Number of OCTUSRCLK clock cycles required for the OCT code to shift out	—	32	—	Cycles
T_{RS_RT}	Time required between the <code>dyn_term_ctrl</code> and <code>oe</code> signal transitions in a bidirectional I/O buffer to dynamically switch between OCT R_S and R_T (Figure 10)	—	2.5	—	ns

Figure 10 shows the timing diagram for the `oe` and `dyn_term_ctrl` signals.

Figure 10. Timing Diagram for `oe` and `dyn_term_ctrl` Signals

Duty Cycle Distortion (DCD) Specifications

Table 44 lists the worst-case DCD for Stratix V devices.

Table 44. Worst-Case DCD on Stratix V I/O Pins ⁽¹⁾

Symbol	C1		C2, C2L, I2, I2L		C3, I3, I3L, I3YY		C4, I4		Unit
	Min	Max	Min	Max	Min	Max	Min	Max	
Output Duty Cycle	45	55	45	55	45	55	45	55	%

Note to Table 44:

(1) The DCD numbers do not cover the core clock network.

Configuration Specification

POR Delay Specification

Power-on reset (POR) delay is defined as the delay between the time when all the power supplies monitored by the POR circuitry reach the minimum recommended operating voltage to the time when the nSTATUS is released high and your device is ready to begin configuration.



For more information about the POR delay, refer to the *Hot Socketing and Power-On Reset in Stratix V Devices* chapter.

Table 45 lists the fast and standard POR delay specification.

Table 45. Fast and Standard POR Delay Specification ⁽¹⁾

POR Delay	Minimum	Maximum
Fast	4 ms	12 ms
Standard	100 ms	300 ms

Note to Table 45:

(1) You can select the POR delay based on the MSEL settings as described in the MSEL Pin Settings section of the “Configuration, Design Security, and Remote System Upgrades in Stratix V Devices” chapter.

JTAG Configuration Specifications

Table 46 lists the JTAG timing parameters and values for Stratix V devices.

Table 46. JTAG Timing Parameters and Values for Stratix V Devices

Symbol	Description	Min	Max	Unit
t _{JCP}	TCK clock period ⁽²⁾	30	—	ns
t _{JCP}	TCK clock period ⁽²⁾	167	—	ns
t _{JCH}	TCK clock high time ⁽²⁾	14	—	ns
t _{JCL}	TCK clock low time ⁽²⁾	14	—	ns
t _{JPSU (TDI)}	TDI JTAG port setup time	2	—	ns
t _{JPSU (TMS)}	TMS JTAG port setup time	3	—	ns

Table 48. Minimum Configuration Time Estimation for Stratix V Devices

Variant	Member Code	Active Serial ⁽¹⁾			Fast Passive Parallel ⁽²⁾		
		Width	DCLK (MHz)	Min Config Time (s)	Width	DCLK (MHz)	Min Config Time (s)
GS	D3	4	100	0.344	32	100	0.043
	D4	4	100	0.534	32	100	0.067
		4	100	0.344	32	100	0.043
	D5	4	100	0.534	32	100	0.067
	D6	4	100	0.741	32	100	0.093
	D8	4	100	0.741	32	100	0.093
E	E9	4	100	0.857	32	100	0.107
	EB	4	100	0.857	32	100	0.107

Notes to Table 48:

(1) DCLK frequency of 100 MHz using external CLKUSR.

(2) Max FPGA FPP bandwidth may exceed bandwidth available from some external storage or control logic.

Fast Passive Parallel Configuration Timing

This section describes the fast passive parallel (FPP) configuration timing parameters for Stratix V devices.

DCLK-to-DATA[] Ratio for FPP Configuration

FPP configuration requires a different DCLK-to-DATA[] ratio when you enable the design security, decompression, or both features. Table 49 lists the DCLK-to-DATA[] ratio for each combination.

Table 49. DCLK-to-DATA[] Ratio ⁽¹⁾ (Part 1 of 2)

Configuration Scheme	Decompression	Design Security	DCLK-to-DATA[] Ratio
FPP ×8	Disabled	Disabled	1
	Disabled	Enabled	1
	Enabled	Disabled	2
	Enabled	Enabled	2
FPP ×16	Disabled	Disabled	1
	Disabled	Enabled	2
	Enabled	Disabled	4
	Enabled	Enabled	4

Table 50 lists the timing parameters for Stratix V devices for FPP configuration when the DCLK-to-DATA [] ratio is 1.

Table 50. FPP Timing Parameters for Stratix V Devices ⁽¹⁾

Symbol	Parameter	Minimum	Maximum	Units
t _{CF2CD}	nCONFIG low to CONF_DONE low	—	600	ns
t _{CF2ST0}	nCONFIG low to nSTATUS low	—	600	ns
t _{CFG}	nCONFIG low pulse width	2	—	μs
t _{STATUS}	nSTATUS low pulse width	268	1,506 ⁽²⁾	μs
t _{CF2ST1}	nCONFIG high to nSTATUS high	—	1,506 ⁽³⁾	μs
t _{CF2CK} ⁽⁶⁾	nCONFIG high to first rising edge on DCLK	1,506	—	μs
t _{ST2CK} ⁽⁶⁾	nSTATUS high to first rising edge of DCLK	2	—	μs
t _{DSU}	DATA [] setup time before rising edge on DCLK	5.5	—	ns
t _{DH}	DATA [] hold time after rising edge on DCLK	0	—	ns
t _{CH}	DCLK high time	$0.45 \times 1/f_{\text{MAX}}$	—	s
t _{CL}	DCLK low time	$0.45 \times 1/f_{\text{MAX}}$	—	s
t _{CLK}	DCLK period	$1/f_{\text{MAX}}$	—	s
f _{MAX}	DCLK frequency (FPP ×8/×16)	—	125	MHz
	DCLK frequency (FPP ×32)	—	100	MHz
t _{CD2UM}	CONF_DONE high to user mode ⁽⁴⁾	175	437	μs
t _{CD2CU}	CONF_DONE high to CLKUSR enabled	4 × maximum DCLK period	—	—
t _{CD2UMC}	CONF_DONE high to user mode with CLKUSR option on	t _{CD2CU} + (8576 × CLKUSR period) ⁽⁵⁾	—	—

Notes to Table 50:

- (1) Use these timing parameters when the decompression and design security features are disabled.
- (2) This value is applicable if you do not delay configuration by extending the nCONFIG or nSTATUS low pulse width.
- (3) This value is applicable if you do not delay configuration by externally holding the nSTATUS low.
- (4) The minimum and maximum numbers apply only if you chose the internal oscillator as the clock source for initializing the device.
- (5) To enable the CLKUSR pin as the initialization clock source and to obtain the maximum frequency specification on these pins, refer to the Initialization section of the “Configuration, Design Security, and Remote System Upgrades in Stratix V Devices” chapter.
- (6) If nSTATUS is monitored, follow the t_{ST2CK} specification. If nSTATUS is not monitored, follow the t_{CF2CK} specification.

FPP Configuration Timing when DCLK-to-DATA [] > 1

Figure 13 shows the timing waveform for FPP configuration when using a MAX II device, MAX V device, or microprocessor as an external host. This waveform shows timing when the DCLK-to-DATA [] ratio is more than 1.

Table 51 lists the timing parameters for Stratix V devices for FPP configuration when the DCLK-to-DATA [] ratio is more than 1.

Table 51. FPP Timing Parameters for Stratix V Devices When the DCLK-to-DATA[] Ratio is >1 ⁽¹⁾

Symbol	Parameter	Minimum	Maximum	Units
t_{CF2CD}	nCONFIG low to CONF_DONE low	—	600	ns
t_{CF2ST0}	nCONFIG low to nSTATUS low	—	600	ns
t_{CFG}	nCONFIG low pulse width	2	—	μ s
t_{STATUS}	nSTATUS low pulse width	268	1,506 ⁽²⁾	μ s
t_{CF2ST1}	nCONFIG high to nSTATUS high	—	1,506 ⁽²⁾	μ s
t_{CF2CK} ⁽⁵⁾	nCONFIG high to first rising edge on DCLK	1,506	—	μ s
t_{ST2CK} ⁽⁵⁾	nSTATUS high to first rising edge of DCLK	2	—	μ s
t_{DSU}	DATA [] setup time before rising edge on DCLK	5.5	—	ns
t_{DH}	DATA [] hold time after rising edge on DCLK	$N-1/f_{DCLK}$ ⁽⁵⁾	—	s
t_{CH}	DCLK high time	$0.45 \times 1/f_{MAX}$	—	s
t_{CL}	DCLK low time	$0.45 \times 1/f_{MAX}$	—	s
t_{CLK}	DCLK period	$1/f_{MAX}$	—	s
f_{MAX}	DCLK frequency (FPP $\times 8/\times 16$)	—	125	MHz
	DCLK frequency (FPP $\times 32$)	—	100	MHz
t_R	Input rise time	—	40	ns
t_F	Input fall time	—	40	ns
t_{CD2UM}	CONF_DONE high to user mode ⁽³⁾	175	437	μ s
t_{CD2CU}	CONF_DONE high to CLKUSR enabled	$4 \times$ maximum DCLK period	—	—
t_{CD2UMC}	CONF_DONE high to user mode with CLKUSR option on	$t_{CD2CU} + (8576 \times \text{CLKUSR period})$ ⁽⁴⁾	—	—

Notes to Table 51:

- (1) Use these timing parameters when you use the decompression and design security features.
- (2) You can obtain this value if you do not delay configuration by extending the nCONFIG or nSTATUS low pulse width.
- (3) The minimum and maximum numbers apply only if you use the internal oscillator as the clock source for initializing the device.
- (4) To enable the CLKUSR pin as the initialization clock source and to obtain the maximum frequency specification on these pins, refer to the Initialization section of the “Configuration, Design Security, and Remote System Upgrades in Stratix V Devices” chapter.
- (5) N is the DCLK-to-DATA ratio and f_{DCLK} is the DCLK frequency the system is operating.
- (6) If nSTATUS is monitored, follow the t_{ST2CK} specification. If nSTATUS is not monitored, follow the t_{CF2CK} specification.

Active Serial Configuration Timing

Table 52 lists the DCLK frequency specification in the AS configuration scheme.

Table 52. DCLK Frequency Specification in the AS Configuration Scheme ^{(1), (2)}

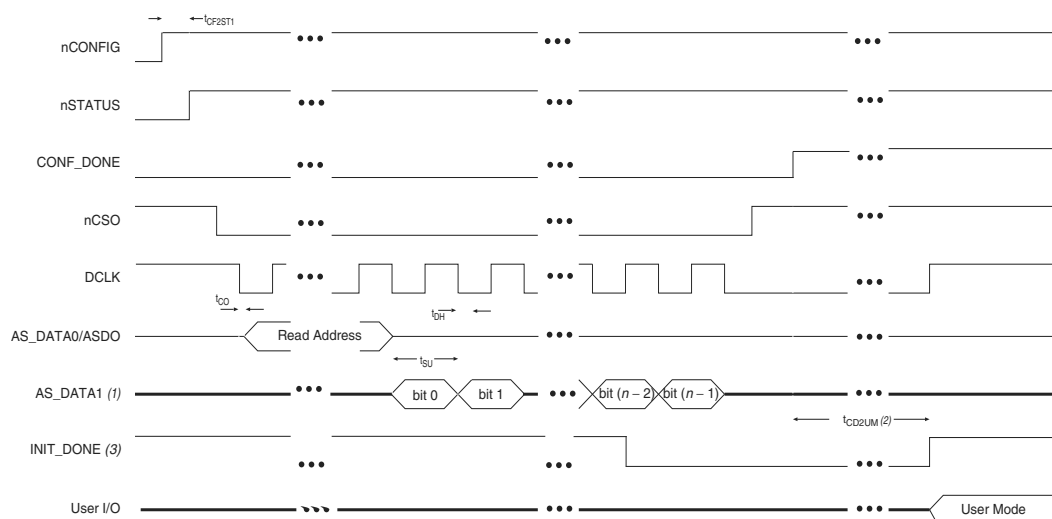
Minimum	Typical	Maximum	Unit
5.3	7.9	12.5	MHz
10.6	15.7	25.0	MHz
21.3	31.4	50.0	MHz
42.6	62.9	100.0	MHz

Notes to Table 52:

- (1) This applies to the DCLK frequency specification when using the internal oscillator as the configuration clock source.
- (2) The AS multi-device configuration scheme does not support DCLK frequency of 100 MHz.

Figure 14 shows the single-device configuration setup for an AS ×1 mode.

Figure 14. AS Configuration Timing



Notes to Figure 14:

- (1) If you are using AS ×4 mode, this signal represents the AS_DATA [3 : 0] and EPCQ sends in 4-bits of data for each DCLK cycle.
- (2) The initialization clock can be from internal oscillator or CLKUSR pin.
- (3) After the option bit to enable the INIT_DONE pin is configured into the device, the INIT_DONE goes low.

Table 53 lists the timing parameters for AS ×1 and AS ×4 configurations in Stratix V devices.

Table 53. AS Timing Parameters for AS ×1 and AS ×4 Configurations in Stratix V Devices ^{(1), (2)} (Part 1 of 2)

Symbol	Parameter	Minimum	Maximum	Units
t _{CO}	DCLK falling edge to AS_DATA0/ASDO output	—	2	ns
t _{SU}	Data setup time before falling edge on DCLK	1.5	—	ns
t _H	Data hold time after falling edge on DCLK	0	—	ns

Table 60. Glossary (Part 2 of 4)

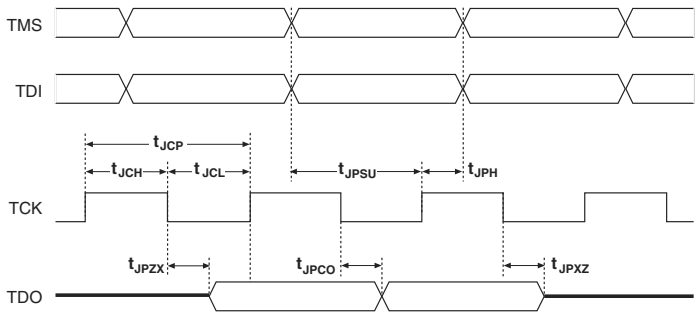
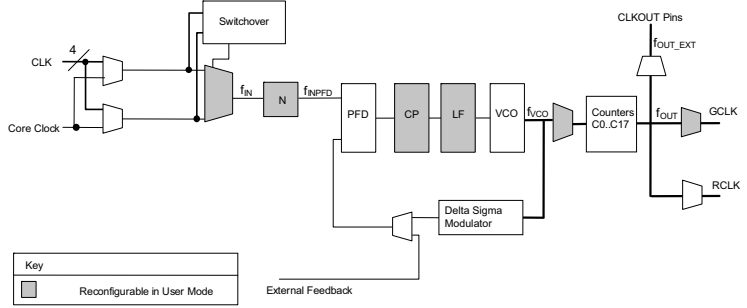
Letter	Subject	Definitions
G H I	—	—
J	JTAG Timing Specifications	High-speed I/O block—Deserialization factor (width of parallel data bus). JTAG Timing Specifications: 
K L M N O	—	—
P	PLL Specifications	Diagram of PLL Specifications ⁽¹⁾  Note: (1) Core Clock can only be fed by dedicated clock input pins or PLL outputs.
Q	—	—
R	R _L	Receiver differential input discrete resistor (external to the Stratix V device).

Table 60. Glossary (Part 4 of 4)

Letter	Subject	Definitions
V	V_{CM(DC)}	DC common mode input voltage.
	V_{ICM}	Input common mode voltage—The common mode of the differential signal at the receiver.
	V_{ID}	Input differential voltage swing—The difference in voltage between the positive and complementary conductors of a differential transmission at the receiver.
	V_{DIF(AC)}	AC differential input voltage—Minimum AC input differential voltage required for switching.
	V_{DIF(DC)}	DC differential input voltage— Minimum DC input differential voltage required for switching.
	V_{IH}	Voltage input high—The minimum positive voltage applied to the input which is accepted by the device as a logic high.
	V_{IH(AC)}	High-level AC input voltage
	V_{IH(DC)}	High-level DC input voltage
	V_{IL}	Voltage input low—The maximum positive voltage applied to the input which is accepted by the device as a logic low.
	V_{IL(AC)}	Low-level AC input voltage
	V_{IL(DC)}	Low-level DC input voltage
	V_{OCM}	Output common mode voltage—The common mode of the differential signal at the transmitter.
	V_{OD}	Output differential voltage swing—The difference in voltage between the positive and complementary conductors of a differential transmission at the transmitter.
	V_{SWING}	Differential input voltage
	V_X	Input differential cross point voltage
	V_{OX}	Output differential cross point voltage
W	W	High-speed I/O block—clock boost factor
X	—	—
Y		
Z		

Table 61. Document Revision History (Part 3 of 3)

Date	Version	Changes
May 2013	2.7	■ Updated Table 2, Table 6, Table 7, Table 20, Table 23, Table 27, Table 47, Table 60 ■ Added Table 24, Table 48 ■ Updated Figure 9, Figure 10, Figure 11, Figure 12
February 2013	2.6	■ Updated Table 7, Table 9, Table 20, Table 23, Table 27, Table 30, Table 31, Table 35, Table 46 ■ Updated “Maximum Allowed Overshoot and Undershoot Voltage”
December 2012	2.5	■ Updated Table 3, Table 6, Table 7, Table 8, Table 23, Table 24, Table 25, Table 27, Table 30, Table 32, Table 35 ■ Added Table 33 ■ Added “Fast Passive Parallel Configuration Timing” ■ Added “Active Serial Configuration Timing” ■ Added “Passive Serial Configuration Timing” ■ Added “Remote System Upgrades” ■ Added “User Watchdog Internal Circuitry Timing Specification” ■ Added “Initialization” ■ Added “Raw Binary File Size”
June 2012	2.4	■ Added Figure 1, Figure 2, and Figure 3. ■ Updated Table 1, Table 2, Table 3, Table 6, Table 11, Table 22, Table 23, Table 27, Table 29, Table 30, Table 31, Table 32, Table 35, Table 38, Table 39, Table 40, Table 41, Table 43, Table 56, and Table 59. ■ Various edits throughout to fix bugs. ■ Changed title of document to <i>Stratix V Device Datasheet</i>. ■ Removed document from the Stratix V handbook and made it a separate document.
February 2012	2.3	■ Updated Table 1–22, Table 1–29, Table 1–31, and Table 1–31.
December 2011	2.2	■ Added Table 2–31. ■ Updated Table 2–28 and Table 2–34.
November 2011	2.1	■ Added Table 2–2 and Table 2–21 and updated Table 2–5 with information about Stratix V GT devices. ■ Updated Table 2–11, Table 2–13, Table 2–20, and Table 2–25. ■ Various edits throughout to fix SPRs.
May 2011	2.0	■ Updated Table 2–4, Table 2–18, Table 2–19, Table 2–21, Table 2–22, Table 2–23, and Table 2–24. ■ Updated the “DQ Logic Block and Memory Output Clock Jitter Specifications” title. ■ Chapter moved to Volume 1. ■ Minor text edits.
December 2010	1.1	■ Updated Table 1–2, Table 1–4, Table 1–19, and Table 1–23. ■ Converted chapter to the new template. ■ Minor text edits.
July 2010	1.0	Initial release.

