E·XFL

Intel - 5SGXMA5K2F35C1N Datasheet



Welcome to <u>E-XFL.COM</u>

Understanding <u>Embedded - FPGAs (Field</u> <u>Programmable Gate Array)</u>

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Obsolete
Number of LABs/CLBs	185000
Number of Logic Elements/Cells	490000
Total RAM Bits	46080000
Number of I/O	432
Number of Gates	-
Voltage - Supply	0.87V ~ 0.93V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	1152-BBGA, FCBGA
Supplier Device Package	1152-FBGA (35x35)
Purchase URL	https://www.e-xfl.com/product-detail/intel/5sgxma5k2f35c1n

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

Symbol	Description	Devices	Minimum ⁽⁴⁾	Typical	Maximum ⁽⁴⁾	Unit
			0.82	0.85	0.88	
V _{CCR_GXBR}	Receiver analog power supply (right side)		0.87	0.90	0.93	v
(2)	neceiver analog power supply (right side)	ux, u3, u1	0.97	1.0	1.03	v
			1.03	1.05	1.07	
V _{CCR_GTBR}	Receiver analog power supply for GT channels (right side)	GT	1.02	1.05	1.08	V
			0.82	0.85	0.88	
V _{CCT GXBL}	Transmitter analog newer supply (left side)		0.87	0.90	0.93	V
(2)	Transmitter analog power supply (left side)	un, uo, ui	0.97	1.0	1.03	v
			1.03	1.05	1.07	
			0.82	0.85	0.88	
V _{CCT GXBB}	Transmitter engles action supply (right side)	GX, GS, GT	0.87	0.90	0.93	V
(2) _	Transmitter analog power supply (light side)		0.97	1.0	1.03	
			1.03	1.05	1.07	
V_{CCT_GTBR}	Transmitter analog power supply for GT channels (right side)	GT	1.02	1.05	1.08	V
V_{CCL_GTBR}	Transmitter clock network power supply	GT	1.02	1.05	1.08	V
V _{CCH_GXBL}	Transmitter output buffer power supply (left side)	GX, GS, GT	1.425	1.5	1.575	V
V _{CCH_GXBR}	Transmitter output buffer power supply (right side)	GX, GS, GT	1.425	1.5	1.575	V

Table 7.	Recommended Transceiver Power Supply Operating Conditions for Stratix V GX ,	GS , and GT Devices
(Part 2	of 2)	

Notes to Table 7:

(1) This supply must be connected to 3.0 V if the CMU PLL, receiver CDR, or both, are configured at a base data rate > 6.5 Gbps. Up to 6.5 Gbps, you can connect this supply to either 3.0 V or 2.5 V.

(2) Refer to Table 8 to select the correct power supply level for your design.

(3) When using ATX PLLs, the supply must be 3.0 V.

(4) This value describes the budget for the DC (static) power supply tolerance and does not include the dynamic tolerance requirements. Refer to the PDN tool for the additional budget for the dynamic tolerance requirements.

Table 8 shows the transceiver power supply voltage requirements for various conditions.

Table 8. Transceiver Power Supply Voltage Requirements

Conditions	Core Speed Grade	VCCR_GXB & VCCT_GXB ⁽²⁾	VCCA_GXB	VCCH_GXB	Unit
If BOTH of the following conditions are true:	A11	1.05			
■ Data rate > 10.3 Gbps.	All	1.00			
 DFE is used. 					
If ANY of the following conditions are true ⁽¹⁾ :			3.0		
 ATX PLL is used. 					
■ Data rate > 6.5Gbps.	All	1.0			
■ DFE (data rate ≤ 10.3 Gbps), AEQ, or EyeQ feature is used.				1.5	V
If ALL of the following	C1, C2, I2, and I3YY	0.90	2.5		
 ATX PLL is not used. 					
■ Data rate \leq 6.5Gbps.	C2L, C3, C4, I2L, I3, I3L, and I4	0.85	2.5		
 DFE, AEQ, and EyeQ are not used. 					

Notes to Table 8:

(1) Choose this power supply voltage requirement option if you plan to upgrade your design later with any of the listed conditions.

(2) If the VCCR_GXB and VCCT_GXB supplies are set to 1.0 V or 1.05 V, they cannot be shared with the VCC core supply. If the VCCR_GXB and VCCT_GXB are set to either 0.90 V or 0.85 V, they can be shared with the VCC core supply.

DC Characteristics

This section lists the supply current, I/O pin leakage current, input pin capacitance, on-chip termination tolerance, and hot socketing specifications.

Supply Current

Supply current is the current drawn from the respective power rails used for power budgeting. Use the Excel-based Early Power Estimator (EPE) to get supply current estimates for your design because these currents vary greatly with the resources you use.

For more information about power estimation tools, refer to the *PowerPlay Early Power Estimator User Guide* and the *PowerPlay Power Analysis* chapter in the *Quartus II Handbook*.

Internal Weak Pull-Up Resistor

Table 16 lists the weak pull-up resistor values for Stratix V devices.

Symbol	Description	V _{CCIO} Conditions (V) ⁽³⁾	Value ⁽⁴⁾	Unit
		3.0 ±5%	25	kΩ
Value of the I/O pin pull-up resistor before	2.5 ±5%	25	kΩ	
	Value of the I/O pin pull-up resistor before	1.8 ±5%	25	kΩ
R _{PU}	and during configuration, as well as user mode if you enable the programmable	1.5 ±5%	25	kΩ
	pull-up resistor option.	1.35 ±5%	25	kΩ
		1.25 ±5%	25	kΩ
		1.2 ±5%	25	kΩ

Table 16. Internal Weak Pull-Up Resistor for Stratix V Devices (1), (2)

Notes to Table 16:

(1) All I/O pins have an option to enable the weak pull-up resistor except the configuration, test, and JTAG pins.

(2) The internal weak pull-down feature is only available for the JTAG TCK pin. The typical value for this internal weak pull-down resistor is approximately 25 k Ω .

- (3) The pin pull-up resistance values may be lower if an external source drives the pin higher than V_{CCIO}.
- (4) These specifications are valid with a $\pm 10\%$ tolerance to cover changes over PVT.

I/O Standard Specifications

Table 17 through Table 22 list the input voltage (V_{IH} and V_{IL}), output voltage (V_{OH} and V_{OL}), and current drive characteristics (I_{OH} and I_{OL}) for various I/O standards supported by Stratix V devices. These tables also show the Stratix V device family I/O standard specifications. The V_{OL} and V_{OH} values are valid at the corresponding I_{OH} and I_{OL}, respectively.

For an explanation of the terms used in Table 17 through Table 22, refer to "Glossary" on page 65. For tolerance calculations across all SSTL and HSTL I/O standards, refer to Altera knowledge base solution rd07262012_486.

I/O		V _{ccio} (V)		VII	∟ (V)	VIH	(V)	V _{OL} (V)	V _{OH} (V)	I _{OL}	I _{oh}
Standard	Min	Тур	Max	Min	Max	Min	Max	Max	Min	(mA)	(mA)
LVTTL	2.85	3	3.15	-0.3	0.8	1.7	3.6	0.4	2.4	2	-2
LVCMOS	2.85	3	3.15	-0.3	0.8	1.7	3.6	0.2	$V_{CCIO} - 0.2$	0.1	-0.1
2.5 V	2.375	2.5	2.625	-0.3	0.7	1.7	3.6	0.4	2	1	-1
1.8 V	1.71	1.8	1.89	-0.3	0.35 * V _{CCIO}	0.65 * V _{CCIO}	V _{CCI0} + 0.3	0.45	V _{CCI0} – 0.45	2	-2
1.5 V	1.425	1.5	1.575	-0.3	0.35 * V _{CCI0}	0.65 * V _{CCI0}	V _{CCI0} + 0.3	0.25 * V _{CCIO}	0.75 * V _{CCIO}	2	-2
1.2 V	1.14	1.2	1.26	-0.3	0.35 * V _{CCI0}	0.65 * V _{CCI0}	V _{CCI0} + 0.3	0.25 * V _{CCIO}	0.75 * V _{CCIO}	2	-2

Table 17. Single-Ended I/O Standards for Stratix V Devices

Switching Characteristics

This section provides performance characteristics of the Stratix V core and periphery blocks.

These characteristics can be designated as Preliminary or Final.

- Preliminary characteristics are created using simulation results, process data, and other known parameters. The title of these tables show the designation as "Preliminary."
- Final numbers are based on actual silicon characterization and testing. The numbers reflect the actual performance of the device under worst-case silicon process, voltage, and junction temperature conditions. There are no designations on finalized tables.

Transceiver Performance Specifications

This section describes transceiver performance specifications.

Table 23 lists the Stratix V GX and GS transceiver specifications.

Table 23.	Transceiver 3	Specifications	for Stratix	V GX	and GS	Devices	(1)	(Part 1	nf 7	۱
Table 20.	TIANSUCIACI	opeonitionationa	IUI UIIAIIA	I UA	anu uu	DEVICES	• •	(1 61 6 1		

Symbol/	Conditions	Transceiver Speed Grade 1		r Speed 1	Transceiver Speed Grade 2			Transceiver Speed Grade 3			Unit		
Description		Min	Тур	Max	Min	Тур	Max	Min	Тур	Max			
Reference Clock													
Supported I/O	Dedicated reference clock pin	1.2-V	PCML,	1.4-V PCM	IL, 1.5-∖	/ PCML	, 2.5-V PCN HCSL	1L, Diffe	rential	LVPECL, L\	/DS, and		
Standards	RX reference clock pin		1.4-V PCML, 1.5-V PCML, 2.5-V PCML, LVPECL, and LVDS										
Input Reference Clock Frequency (CMU PLL) ⁽⁸⁾	_	40		710	40	_	710	40	_	710	MHz		
Input Reference Clock Frequency (ATX PLL) ⁽⁸⁾		100		710	100		710	100		710	MHz		
Rise time	Measure at ±60 mV of differential signal ⁽²⁶⁾			400	_		400			400	ns		
Fall time	Measure at ±60 mV of differential signal ⁽²⁶⁾		_	400	_		400			400	- ps		
Duty cycle		45		55	45		55	45	—	55	%		
Spread-spectrum modulating clock frequency	PCI Express® (PCIe [®])	30		33	30		33	30	_	33	kHz		

Symbol/	Conditions	Transceiver Speed Grade 1			Transceiver Speed Grade 2			Trai	Unit		
Description		Min	Тур	Max	Min	Тур	Max	Min	Тур	Max	
	85– Ω setting	_	85 ± 30%		_	85 ± 30%		—	85 ± 30%		Ω
Differential on-	100–Ω setting	_	100 ± 30%		_	100 ± 30%		_	100 ± 30%	_	Ω
chip termination resistors ⁽²¹⁾	120–Ω setting	_	120 ± 30%		_	120 ± 30%		_	120 ± 30%	_	Ω
	150-Ω setting	_	150 ± 30%		_	150 ± 30%	_	_	150 ± 30%	_	Ω
	V _{CCR_GXB} = 0.85 V or 0.9 V full bandwidth	_	600	_	_	600	_		600	_	mV
V _{ICM} (AC and DC	V _{CCR_GXB} = 0.85 V or 0.9 V half bandwidth		600	_		600	_		600	_	mV
(oupled)	V _{CCR_GXB} = 1.0 V/1.05 V full bandwidth	_	700	_	_	700	_	_	700	_	mV
	V _{CCR_GXB} = 1.0 V half bandwidth		750	_	_	750	_	_	750	_	mV
t _{LTR} ⁽¹¹⁾	—	_	_	10	_	—	10	_	—	10	μs
t _{LTD} ⁽¹²⁾	—	4	_		4	—		4	-	—	μs
t _{LTD_manual} ⁽¹³⁾	—	4			4	—		4	—	—	μs
t _{LTR_LTD_manual} ⁽¹⁴⁾	—	15	_		15	—		15	—	—	μs
Run Length		_		200	_	—	200	_	—	200	UI
Programmable equalization (AC Gain) ⁽¹⁰⁾	Full bandwidth (6.25 GHz) Half bandwidth (3.125 GHz)		_	16	_	_	16	_		16	dB

 Table 23. Transceiver Specifications for Stratix V GX and GS Devices ⁽¹⁾ (Part 4 of 7)

Symbol/	Conditions	Transceiver Speed Grade 2			S	Transceive peed Grade	r 3	Unit			
Description		Min	Тур	Max	Min	Тур	Max	ľ			
Reference Clock								1			
Supported I/O Standards	Dedicated reference clock pin	1.2-V PCN	IL, 1.4-V PC	ML, 1.5-V P(CML, 2.5-V I and HCSL	PCML, Diffe	rential LVPE	ECL, LVDS,			
otanuarus	RX reference clock pin		1.4-V PCML, 1.5-V PCML, 2.5-V PCML, LVPECL, and LVDS								
Input Reference Clock Frequency (CMU PLL) ⁽⁶⁾	_	40	_	710	40	_	710	MHz			
Input Reference Clock Frequency (ATX PLL) ⁽⁶⁾	_	100	_	710	100	_	710	MHz			
Rise time	20% to 80%	_		400	_	_	400				
Fall time	80% to 20%			400	—	_	400	ps			
Duty cycle	—	45	_	55	45	_	55	%			
Spread-spectrum modulating clock frequency	PCI Express (PCIe)	30	_	33	30	_	33	kHz			
Spread-spectrum downspread	PCle	_	0 to -0.5	_	_	0 to -0.5	_	%			
On-chip termination resistors ⁽¹⁹⁾	_	_	100	_	_	100	_	Ω			
Absolute V _{MAX} ⁽³⁾	Dedicated reference clock pin	_	_	1.6	_	_	1.6	V			
	RX reference clock pin	_	_	1.2	_	_	1.2				
Absolute V _{MIN}	—	-0.4		—	-0.4	—		V			
Peak-to-peak differential input voltage	_	200	_	1600	200	_	1600	mV			
V _{ICM} (AC coupled)	Dedicated reference clock pin		1050/1000 ^{(,}	2)	1	050/1000 (2)	mV			
	RX reference clock pin	1	.0/0.9/0.85 (22)	1.	0/0.9/0.85 ((22)	V			
V _{ICM} (DC coupled)	HCSL I/O standard for PCIe reference clock	250	_	550	250	_	550	mV			

Table 28. Transceiver Specifications for Stratix V GT Devices (Part 1 of 5)⁽¹⁾

Table 28. Transceiver Specifications for Stratix V GT Devices (Part 2 of 5)⁽¹⁾

Symbol/	Conditions	Transceiver Speed Grade 2			SI	Unit		
Description		Min	Тур	Max	Min	Тур	Max	
	100 Hz	—	—	-70			-70	
Transmitter REFCLK	1 kHz		_	-90	_	_	-90	
Phase Noise (622	10 kHz		—	-100	_		-100	dBc/Hz
MHz) ⁽¹⁸⁾	100 kHz			-110			-110	
	\geq 1 MHz	—	—	-120	_	_	-120	
Transmitter REFCLK Phase Jitter (100 MHz) ⁽¹⁵⁾	10 kHz to 1.5 MHz (PCle)	_	_	3		_	3	ps (rms)
RREF ⁽¹⁷⁾	_	_	1800 ± 1%	—	_	1800 ± 1%	_	Ω
Transceiver Clocks								
fixedclk clock frequency	PCIe Receiver Detect	_	100 or 125	_	_	100 or 125	_	MHz
Reconfiguration clock (mgmt_clk_clk) frequency	_	100	_	125	100	_	125	MHz
Receiver	•							
Supported I/O Standards	_		1.4-V PCML	., 1.5-V PCMI	L, 2.5-V PCI	VIL, LVPEC	L, and LVDS	6
Data rate (Standard PCS) ⁽²¹⁾	GX channels	600	_	8500	600	_	8500	Mbps
Data rate (10G PCS) ⁽²¹⁾	GX channels	600	_	12,500	600	_	12,500	Mbps
Data rate	GT channels	19,600	—	28,050	19,600		25,780	Mbps
Absolute V _{MAX} for a receiver pin ⁽³⁾	GT channels	_	_	1.2	_	_	1.2	V
Absolute V _{MIN} for a receiver pin	GT channels	-0.4	_	—	-0.4	_	_	V
Maximum peak-to-peak	GT channels	_		1.6	—	_	1.6	V
differential input voltage V _{ID} (diff p-p) before device configuration ⁽²⁰⁾	GX channels				(8)			
	GT channels							
Maximum peak-to-peak differential input voltage V_{ID} (diff p-p) after device	V _{CCR_GTB} = 1.05 V (V _{ICM} = 0.65 V)	_	_	2.2	_	—	2.2	V
	GX channels		1	1 1	(8)			1
Minimum differential	GT channels	200	_	—	200		_	mV
eye opening at receiver serial input pins ⁽⁴⁾ , ⁽²⁰⁾	GX channels			·	(8)			

Figure 4 shows the differential transmitter output waveform.





Figure 5 shows the Stratix V AC gain curves for GT channels.

Figure 5. AC Gain Curves for GT Channels

Table 31. PLL Specifications for Stratix V Devices (Part 3 of 3)

Symbol	Parameter	Min	Тур	Max	Unit
f _{RES}	Resolution of VCO frequency ($f_{INPFD} = 100 \text{ MHz}$)	390625	5.96	0.023	Hz

Notes to Table 31:

(1) This specification is limited in the Quartus II software by the I/O maximum frequency. The maximum I/O frequency is different for each I/O standard.

(2) This specification is limited by the lower of the two: I/O f_{MAX} or f_{OUT} of the PLL.

- (3) A high input jitter directly affects the PLL output jitter. To have low PLL output clock jitter, you must provide a clean clock source < 120 ps.
- (4) f_{REF} is fIN/N when N = 1.
- (5) Peak-to-peak jitter with a probability level of 10⁻¹² (14 sigma, 99.9999999974404% confidence level). The output jitter specification applies to the intrinsic jitter of the PLL, when an input jitter of 30 ps is applied. The external memory interface clock output jitter specifications use a different measurement method and are available in Table 44 on page 52.
- (6) The cascaded PLL specification is only applicable with the following condition: a. Upstream PLL: 0.59Mhz ≤ Upstream PLL BW < 1 MHz b. Downstream PLL: Downstream PLL BW > 2 MHz
- (7) High bandwidth PLL settings are not supported in external feedback mode.
- (8) The external memory interface clock output jitter specifications use a different measurement method, which is available in Table 42 on page 50.
- (9) The VCO frequency reported by the Quartus II software in the PLL Usage Summary section of the compilation report takes into consideration the VCO post-scale counter K value. Therefore, if the counter K has a value of 2, the frequency reported can be lower than the f_{VCO} specification.
- (10) This specification only covers fractional PLL for low bandwidth. The f_{VCO} for fractional value range 0.05 0.95 must be \geq 1000 MHz, while f_{VCO} for fractional value range 0.20 0.80 must be \geq 1200 MHz.
- (11) This specification only covered fractional PLL for low bandwidth. The f_{VC0} for fractional value range 0.05-0.95 must be \geq 1000 MHz.
- (12) This specification only covered fractional PLL for low bandwidth. The f_{VC0} for fractional value range 0.20-0.80 must be \geq 1200 MHz.

DSP Block Specifications

Table 32 lists the Stratix V DSP block performance specifications.

			F	Peformanc	e				
Mode	C1	C2, C2L	12, 12L	C3	13, 13L, 13YY	C4	14	Unit	
		Modes ı	using one	DSP					
Three 9 x 9	600	600	600	480	480	420	420	MHz	
One 18 x 18	600	600	600	480	480	420	400	MHz	
Two partial 18 x 18 (or 16 x 16)	600	600	600	480	480	420	400	MHz	
One 27 x 27	500	500	500	400	400	350	350	MHz	
One 36 x 18	500	500	500	400	400	350	350	MHz	
One sum of two 18 x 18(One sum of 2 16 x 16)	500	500	500	400	400	350	350	MHz	
One sum of square	500	500	500	400	400	350	350	MHz	
One 18 x 18 plus 36 (a x b) + c	500	500	500	400	400	350	350	MHz	
		Modes u	sing two l	DSPs					
Three 18 x 18	500	500	500	400	400	350	350	MHz	
One sum of four 18 x 18	475	475	475	380	380	300	300	MHz	
One sum of two 27 x 27	465	465	450	380	380	300	290	MHz	
One sum of two 36 x 18	475	475	475	380	380	300	300	MHz	
One complex 18 x 18	500	500	500	400	400	350	350	MHz	
One 36 x 36	475	475	475	380	380	300	300	MHz	

Table 32. Block Performance Specifications for Stratix V DSP Devices (Part 1 of 2)

Periphery Performance

This section describes periphery performance, including high-speed I/O and external memory interface.

I/O performance supports several system interfaces, such as the **LVDS** high-speed I/O interface, external memory interface, and the **PCI/PCI-X** bus interface. General-purpose I/O standards such as 3.3-, 2.5-, 1.8-, and 1.5-**LVTTL/LVCMOS** are capable of a typical 167 MHz and 1.2-**LVCMOS** at 100 MHz interfacing frequency with a 10 pF load.

The actual achievable frequency depends on design- and system-specific factors. Ensure proper timing closure in your design and perform HSPICE/IBIS simulations based on your specific design and system setup to determine the maximum achievable frequency in your system.

High-Speed I/O Specification

Table 36 lists high-speed I/O timing for Stratix V devices.

Table 36. High-Speed I/O Specifications for Stratix V Devices (1), (2) (Part 1 of 4)

	Sumbol	Conditions	C1		C2, C2L, I2, I2L		C3, I3, I3L, I3YY			C4,14			11		
	Symbol		Min	Тур	Max	Min	Тур	Max	Min	Тур	Max	Min	Тур	Max	UNIT
	f _{HSCLK_in} (input clock frequency) True Differential I/O Standards	Clock boost factor W = 1 to 40 $^{(4)}$	5	_	800	5		800	5		625	5		525	MHz
	f _{HSCLK_in} (input clock frequency) Single Ended I/O Standards ⁽³⁾	Clock boost factor W = 1 to 40 $^{(4)}$	5		800	5		800	5		625	5		525	MHz
	f _{HSCLK_in} (input clock frequency) Single Ended I/O Standards	Clock boost factor W = 1 to 40 $^{(4)}$	5	_	520	5		520	5	_	420	5	_	420	MHz
f _{HSCLK_OUT} (output clock frequency)		_	5	_	800	5	_	800	5	_	625 (5)	5	_	525 (5)	MHz

Duty Cycle Distortion (DCD) Specifications

Table 44 lists the worst-case DCD for Stratix V devices.

Table 44. Worst-Case DCD on Stratix V I/O Pins (1)

Symbol	C1		C2, C2L, I2, I2L		C3, I3, I3L, I3YY		C4,14		Unit	
	Min	Max	Min	Max	Min	Max	Min	Max		
Output Duty Cycle	45	55	45	55	45	55	45	55	%	

Note to Table 44:

(1) The DCD numbers do not cover the core clock network.

Configuration Specification

POR Delay Specification

Power-on reset (POR) delay is defined as the delay between the time when all the power supplies monitored by the POR circuitry reach the minimum recommended operating voltage to the time when the nSTATUS is released high and your device is ready to begin configuration.



For more information about the POR delay, refer to the *Hot Socketing and Power-On Reset in Stratix V Devices* chapter.

Table 45 lists the fast and standard POR delay specification.

Table 45. Fast and Standard POR Delay Specification (1)

POR Delay	Minimum	Maximum
Fast	4 ms	12 ms
Standard	100 ms	300 ms

Note to Table 45:

(1) You can select the POR delay based on the MSEL settings as described in the MSEL Pin Settings section of the "Configuration, Design Security, and Remote System Upgrades in Stratix V Devices" chapter.

JTAG Configuration Specifications

Table 46 lists the JTAG timing parameters and values for Stratix V devices.

Table 46. JTAG Timing Parameters and Values for Stratix V Devices

Symbol	Description	Min	Max	Unit
t _{JCP}	TCK clock period ⁽²⁾	30		ns
t _{JCP}	TCK clock period ⁽²⁾	167	—	ns
t _{JCH}	TCK clock high time ⁽²⁾	14	—	ns
t _{JCL}	TCK clock low time ⁽²⁾	14		ns
t _{JPSU (TDI)}	TDI JTAG port setup time	2	—	ns
t _{JPSU (TMS)}	TMS JTAG port setup time	3	_	ns

Symbol	Description	Min	Max	Unit
t _{JPH}	JTAG port hold time	5	—	ns
t _{JPCO}	JTAG port clock to output	—	11 ⁽¹⁾	ns
t _{JPZX}	JTAG port high impedance to valid output	—	14 ⁽¹⁾	ns
t _{JPXZ}	JTAG port valid output to high impedance	—	14 ⁽¹⁾	ns

Table 46. JTAG Timing Parameters and Values for Stratix V Devices

Notes to Table 46:

(1) A 1 ns adder is required for each V_{CCI0} voltage step down from 3.0 V. For example, $t_{JPC0} = 12$ ns if V_{CCI0} of the TDO I/O bank = 2.5 V, or 13 ns if it equals 1.8 V.

(2) The minimum TCK clock period is 167 ns if VCCBAT is within the range 1.2V-1.5V when you perform the volatile key programming.

Raw Binary File Size

For the POR delay specification, refer to the "POR Delay Specification" section of the "Configuration, Design Security, and Remote System Upgrades in Stratix V Devices".

Table 47 lists the uncompressed raw binary file (.rbf) sizes for Stratix V devices.

Family	Device	Package	Configuration .rbf Size (bits)	IOCSR .rbf Size (bits) ^{(4), (5)}	
	500742	H35, F40, F35 ⁽²⁾	213,798,880	562,392	
	JOUNAS	H29, F35 ⁽³⁾	137,598,880	564,504	
	5SGXA4	—	213,798,880	563,672	
	5SGXA5	—	269,979,008	562,392	
	5SGXA7	—	269,979,008	562,392	
Stratix V GX	5SGXA9	—	342,742,976	700,888	
	5SGXAB	—	342,742,976	700,888	
	5SGXB5	—	270,528,640	584,344	
	5SGXB6	—	270,528,640	584,344	
	5SGXB9	_	342,742,976	700,888	
	5SGXBB	—	342,742,976	700,888	
Stratix V CT	5SGTC5	—	269,979,008	562,392	
	5SGTC7	_	269,979,008	562,392	
	5SGSD3	—	137,598,880	564,504	
	590904	F1517	213,798,880	563,672	
Stratix V GS	J303D4		137,598,880	564,504	
	5SGSD5		213,798,880	563,672	
	5SGSD6		293,441,888	565,528	
	5SGSD8	—	293,441,888	565,528	

Table 47. Uncompressed .rbf Sizes for Stratix V Devices

	Member Code		Active Serial ⁽¹⁾)	Fast Passive Parallel ⁽²⁾				
Variant		Width	DCLK (MHz)	Min Config Time (s)	Width	DCLK (MHz)	Min Config Time (s)		
	D3	4	100	0.344	32	100	0.043		
00	D4	4	100	0.534	32	100	0.067		
		4	100	0.344	32	100	0.043		
03	D5	4	100	0.534	32	100	0.067		
	D6	4	100	0.741	32	100	0.093		
	D8	4	100	0.741	32	100	0.093		
F	E9	4	100	0.857	32	100	0.107		
Ľ	EB	4	100	0.857	32	100	0.107		

Table 48. Minimum Configuration Time Estimation for Stratix V Devices

Notes to Table 48:

(1) DCLK frequency of 100 MHz using external CLKUSR.

(2) Max FPGA FPP bandwidth may exceed bandwidth available from some external storage or control logic.

Fast Passive Parallel Configuration Timing

This section describes the fast passive parallel (FPP) configuration timing parameters for Stratix V devices.

DCLK-to-DATA[] Ratio for FPP Configuration

FPP configuration requires a different DCLK-to-DATA[]ratio when you enable the design security, decompression, or both features. Table 49 lists the DCLK-to-DATA[]ratio for each combination.

Configuration Scheme	Decompression	Design Security	DCLK-to-DATA[] Ratio
	Disabled	Disabled	1
	Disabled	Enabled	1
111 ×0	Enabled	Disabled	2
	Enabled	Enabled	2
	Disabled	Disabled	1
	Disabled	Enabled	2
FPP ×10	Enabled	Disabled	4
	Enabled	Enabled	4

 Table 49. DCLK-to-DATA[] Ratio ⁽¹⁾ (Part 1 of 2)

Table 51 lists the timing parameters for Stratix V devices for FPP configuration when the DCLK-to-DATA [] ratio is more than 1.

Table 51.	FPP Timing	Parameters f	or Stratix V	Devices When	the DCLK-te	o-DATA[] Ratio	is >1 (1)
			•••••••••••••••••••••••••••••••••••••••			• • • • • • • • • • • • • • • • • • •		

Symbol	Parameter	Minimum	Maximum	Units
t _{CF2CD}	nCONFIG low to CONF_DONE low	—	600	ns
t _{CF2ST0}	nCONFIG low to nSTATUS low	—	600	ns
t _{CFG}	nCONFIG low pulse width	2		μS
t _{STATUS}	nSTATUS low pulse width	268	1,506 ⁽²⁾	μS
t _{CF2ST1}	nCONFIG high to nSTATUS high	—	1,506 ⁽²⁾	μS
t _{CF2CK} (5)	nCONFIG high to first rising edge on DCLK	1,506		μS
t _{ST2CK} (5)	nSTATUS high to first rising edge of DCLK	2		μS
t _{DSU}	DATA [] setup time before rising edge on DCLK	5.5		ns
t _{DH}	DATA [] hold time after rising edge on DCLK	N-1/f _{DCLK} (5)		S
t _{CH}	DCLK high time	$0.45\times 1/f_{MAX}$		S
t _{CL}	DCLK low time	$0.45\times 1/f_{MAX}$		S
t _{CLK}	DCLK period	1/f _{MAX}		S
f	DCLK frequency (FPP ×8/×16)	—	125	MHz
IMAX	DCLK frequency (FPP ×32)	—	100	MHz
t _R	Input rise time	—	40	ns
t _F	Input fall time	—	40	ns
t _{CD2UM}	CONF_DONE high to user mode ⁽³⁾	175	437	μS
t _{CD2CU}	CONF_DONE high to CLKUSR enabled	4 × maximum DCLK period	_	_
t _{CD2UMC}	CONF_DONE high to user mode with CLKUSR option on	t _{CD2CU} + (8576 × CLKUSR period) ⁽⁴⁾	_	_

Notes to Table 51:

- (1) Use these timing parameters when you use the decompression and design security features.
- (2) You can obtain this value if you do not delay configuration by extending the nCONFIG or nSTATUS low pulse width.
- (3) The minimum and maximum numbers apply only if you use the internal oscillator as the clock source for initializing the device.
- (4) To enable the CLKUSR pin as the initialization clock source and to obtain the maximum frequency specification on these pins, refer to the Initialization section of the "Configuration, Design Security, and Remote System Upgrades in Stratix V Devices" chapter.
- (5) N is the DCLK-to-DATA ratio and f_{DCLK} is the DCLK frequency the system is operating.
- (6) If nSTATUS is monitored, follow the t_{ST2CK} specification. If nSTATUS is not monitored, follow the t_{CF2CK} specification.

Parameter (1)	Available Settings	le Min Offset (2)	Fast Model		Slow Model							
			Industrial	Commercial	C1	C2	C3	C4	12	13, 13YY	14	Unit
D3	8	0	1.587	1.699	2.793	2.793	2.992	3.192	2.811	3.047	3.257	ns
D4	64	0	0.464	0.492	0.838	0.838	0.924	1.011	0.843	0.920	1.006	ns
D5	64	0	0.464	0.493	0.838	0.838	0.924	1.011	0.844	0.921	1.006	ns
D6	32	0	0.229	0.244	0.415	0.415	0.458	0.503	0.418	0.456	0.499	ns

Table 58.	IOE Pro	grammable De	ay for	Stratix V	V Devices	(Part 2 of 2)
-----------	---------	--------------	--------	-----------	-----------	--------------	---

Notes to Table 58:

(1) You can set this value in the Quartus II software by selecting D1, D2, D3, D5, and D6 in the Assignment Name column of Assignment Editor.

(2) Minimum offset does not include the intrinsic delay.

Programmable Output Buffer Delay

Table 59 lists the delay chain settings that control the rising and falling edge delays of the output buffer. The default delay is 0 ps.

Symbol	Parameter	Typical	Unit
		0 (default)	ps
Dauman	Rising and/or falling edge delay	25	ps
DOUTBUF		50	ps
		75	ps

Note to Table 59:

(1) You can set the programmable output buffer delay in the Quartus II software by setting the Output Buffer Delay Control assignment to either positive, negative, or both edges, with the specific values stated here (in ps) for the Output Buffer Delay assignment.

Glossary

Table 60 lists the glossary for this chapter.

Table 60. Glossary (Part 1 of 4)

Letter	Subject	Definitions
Α		
В	—	—
С		
D	—	_
E	—	_
F	f _{HSCLK}	Left and right PLL input clock frequency.
	f _{HSDR}	High-speed I/O block—Maximum and minimum LVDS data transfer rate (f _{HSDR} = 1/TUI), non-DPA.
	f _{hsdrdpa}	High-speed I/O block—Maximum and minimum LVDS data transfer rate (f _{HSDRDPA} = 1/TUI), DPA.

Letter	Subject	Definitions
	V _{CM(DC)}	DC common mode input voltage.
	V _{ICM}	Input common mode voltage—The common mode of the differential signal at the receiver.
	V _{ID}	Input differential voltage swing—The difference in voltage between the positive and complementary conductors of a differential transmission at the receiver.
	V _{DIF(AC)}	AC differential input voltage—Minimum AC input differential voltage required for switching.
	V _{DIF(DC)}	DC differential input voltage— Minimum DC input differential voltage required for switching.
	V _{IH}	Voltage input high—The minimum positive voltage applied to the input which is accepted by the device as a logic high.
	V _{IH(AC)}	High-level AC input voltage
	V _{IH(DC)}	High-level DC input voltage
V	V _{IL}	Voltage input low—The maximum positive voltage applied to the input which is accepted by the device as a logic low.
	V _{IL(AC)}	Low-level AC input voltage
	V _{IL(DC)}	Low-level DC input voltage
	V _{OCM}	Output common mode voltage—The common mode of the differential signal at the transmitter.
	V _{OD}	Output differential voltage swing—The difference in voltage between the positive and complementary conductors of a differential transmission at the transmitter.
	V _{SWING}	Differential input voltage
	V _X	Input differential cross point voltage
	V _{OX}	Output differential cross point voltage
W	W	High-speed I/O block—clock boost factor
X		
Y	—	—
Z		

Table 60. Glossary (Part 4 of 4)

Document Revision History

Table 61 lists the revision history for this chapter.

 Table 61. Document Revision History (Part 1 of 3)

Date	Version	Changes	
June 2018	3.9	Added the "Stratix V Device Overshoot Duration" figure.	
April 2017	3.8	Added a footnote to the "High-Speed I/O Specifications for Stratix V Devices" table.	
		 Changed the minimum value for t_{CD2UMC} in the "PS Timing Parameters for Stratix V Devices" table. 	
		 Changed the condition for 100-Ω R_D in the "OCT Without Calibration Resistance Tolerance Specifications for Stratix V Devices" table. 	
		 Changed the minimum value for t_{CD2UMC} in the "AS Timing Parameters for AS '1 and AS '4 Configurations in Stratix V Devices" table 	
		 Changed the minimum value for t_{CD2UMC} in the "FPP Timing Parameters for Stratix V Devices When the DCLK-to-DATA[] Ratio is >1" table. 	
		 Changed the minimum value for t_{CD2UMC} in the "FPP Timing Parameters for Stratix V Devices When the DCLK-to-DATA[] Ratio is >1" table. 	
		 Changed the minimum number of clock cycles value in the "Initialization Clock Source Option and the Maximum Frequency" table. 	
June 2016	3.7	 Added the V_{ID} minimum specification for LVPECL in the "Differential I/O Standard Specifications for Stratix V Devices" table 	
June 2016		 Added the I_{OUT} specification to the "Absolute Maximum Ratings for Stratix V Devices" table. 	
December 2015	3.6	Added a footnote to the "High-Speed I/O Specifications for Stratix V Devices" table.	
December 2015	3.5	 Changed the transmitter, receiver, and ATX PLL data rate specifications in the "Transceiver Specifications for Stratix V GX and GS Devices" table. 	
		 Changed the configuration .rbf sizes in the "Uncompressed .rbf Sizes for Stratix V Devices" table. 	
	3.4	• Changed the data rate specification for transceiver speed grade 3 in the following tables:	
		 "Transceiver Specifications for Stratix V GX and GS Devices" 	
		 "Stratix V Standard PCS Approximate Maximum Date Rate" 	
		 "Stratix V 10G PCS Approximate Maximum Data Rate" 	
July 2015		 Changed the conditions for reference clock rise and fall time, and added a note to the "Transceiver Specifications for Stratix V GX and GS Devices" table. 	
		 Added a note to the "Minimum differential eye opening at receiver serial input pins" specification in the "Transceiver Specifications for Stratix V GX and GS Devices" table. 	
		 Changed the t_{c0} maximum value in the "AS Timing Parameters for AS '1 and AS '4 Configurations in Stratix V Devices" table. 	
		 Removed the CDR ppm tolerance specification from the "Transceiver Specifications for Stratix V GX and GS Devices" table. 	

Table 61. Document Revision History (Part 2 of 3)

Date	Version	Changes	
		 Added the I3YY speed grade and changed the data rates for the GX channel in Table 1. 	
		 Added the I3YY speed grade to the V_{CC} description in Table 6. 	
		 Added the I3YY speed grade to V_{CCHIP_L}, V_{CCHIP_R}, V_{CCHSSI_L}, and V_{CCHSSI_R} descriptions in Table 7. 	
		■ Added 240-Ω to Table 11.	
		Changed CDR PPM tolerance in Table 23.	
		 Added additional max data rate for fPLL in Table 23. 	
November 2014		 Added the I3YY speed grade and changed the data rates for transceiver speed grade 3 in Table 25. 	
		 Added the I3YY speed grade and changed the data rates for transceiver speed grade 3 in Table 26. 	
		 Changed CDR PPM tolerance in Table 28. 	
		 Added additional max data rate for fPLL in Table 28. 	
		 Changed the mode descriptions for MLAB and M20K in Table 33. 	
		 Changed the Max value of f_{HSCLK_OUT} for the C2, C2L, I2, I2L speed grades in Table 36. 	
	3.3	 Changed the frequency ranges for C1 and C2 in Table 39. 	
		 Changed the .rbf file sizes for 5SGSD6 and 5SGSD8 in Table 47. 	
		 Added note about nSTATUS to Table 50, Table 51, Table 54. 	
		 Changed the available settings in Table 58. 	
		 Changed the note in "Periphery Performance". 	
		 Updated the "I/O Standard Specifications" section. 	
		 Updated the "Raw Binary File Size" section. 	
		 Updated the receiver voltage input range in Table 22. 	
		 Updated the max frequency for the LVDS clock network in Table 36. 	
		■ Updated the DCLK note to Figure 11.	
		 Updated Table 23 VO_{CM} (DC Coupled) condition. 	
		Updated Table 6 and Table 7.	
		 Added the DCLK specification to Table 55. 	
		Updated the notes for Table 47.	
		 Updated the list of parameters for Table 56. 	
November 2013	3.2	Updated Table 28	
November 2013	3.1	Updated Table 33	
November 2013	3.0	Updated Table 23 and Table 28	
October 2013	2.9	 Updated the "Transceiver Characterization" section 	
		 Updated Table 3, Table 12, Table 14, Table 19, Table 20, Table 23, Table 24, Table 28, Table 30, Table 31, Table 32, Table 33, Table 36, Table 39, Table 40, Table 41, Table 42, Table 47, Table 53, Table 58, and Table 59 	
Uctober 2013	2.8	 Added Figure 1 and Figure 3 	
		 Added the "Transceiver Characterization" section 	
		 Removed all "Preliminary" designations. 	

 Table 61. Document Revision History (Part 3 of 3)

Date	Version	Changes
May 2013		■ Updated Table 2, Table 6, Table 7, Table 20, Table 23, Table 27, Table 47, Table 60
	2.7	Added Table 24, Table 48
		 Updated Figure 9, Figure 10, Figure 11, Figure 12
February 2013	26	 Updated Table 7, Table 9, Table 20, Table 23, Table 27, Table 30, Table 31, Table 35, Table 46
		Updated "Maximum Allowed Overshoot and Undershoot Voltage"
		 Updated Table 3, Table 6, Table 7, Table 8, Table 23, Table 24, Table 25, Table 27, Table 30, Table 32, Table 35
		Added Table 33
		 Added "Fast Passive Parallel Configuration Timing"
		 Added "Active Serial Configuration Timing"
December 2012	2.5	 Added "Passive Serial Configuration Timing"
		 Added "Remote System Upgrades"
		 Added "User Watchdog Internal Circuitry Timing Specification"
		Added "Initialization"
		Added "Raw Binary File Size"
	2.4	 Added Figure 1, Figure 2, and Figure 3.
June 2012		 Updated Table 1, Table 2, Table 3, Table 6, Table 11, Table 22, Table 23, Table 27, Table 29, Table 30, Table 31, Table 32, Table 35, Table 38, Table 39, Table 40, Table 41, Table 43, Table 56, and Table 59.
		 Various edits throughout to fix bugs.
		Changed title of document to <i>Stratix V Device Datasheet</i> .
		 Removed document from the Stratix V handbook and made it a separate document.
February 2012	2.3	■ Updated Table 1–22, Table 1–29, Table 1–31, and Table 1–31.
December 2011	2.2	■ Added Table 2–31.
December 2011		■ Updated Table 2–28 and Table 2–34.
	2.1	 Added Table 2–2 and Table 2–21 and updated Table 2–5 with information about Stratix V GT devices.
November 2011		 Updated Table 2–11, Table 2–13, Table 2–20, and Table 2–25.
		 Various edits throughout to fix SPRs.
	2.0	■ Updated Table 2–4, Table 2–18, Table 2–19, Table 2–21, Table 2–22, Table 2–23, and Table 2–24.
May 2011		 Updated the "DQ Logic Block and Memory Output Clock Jitter Specifications" title.
		Chapter moved to Volume 1.
		 Minor text edits.
	1.1	■ Updated Table 1–2, Table 1–4, Table 1–19, and Table 1–23.
December 2010		 Converted chapter to the new template.
		 Minor text edits.
July 2010	1.0	Initial release.