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Understanding [Embedded - FPGAs \(Field Programmable Gate Array\)](#)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

| | |
|--------------------------------|---|
| Product Status | Obsolete |
| Number of LABs/CLBs | 185000 |
| Number of Logic Elements/Cells | 490000 |
| Total RAM Bits | 46080000 |
| Number of I/O | 696 |
| Number of Gates | - |
| Voltage - Supply | 0.87V ~ 0.93V |
| Mounting Type | Surface Mount |
| Operating Temperature | 0°C ~ 85°C (TJ) |
| Package / Case | 1517-BBGA, FCBGA |
| Supplier Device Package | 1517-FBGA (40x40) |
| Purchase URL | https://www.e-xfl.com/product-detail/intel/5sgxma5k2f40c1n |

Table 1. Stratix V GX and GS Commercial and Industrial Speed Grade Offering ⁽¹⁾, ⁽²⁾, ⁽³⁾ (Part 2 of 2)

| Transceiver Speed Grade | Core Speed Grade | | | | | | | |
|--------------------------|------------------|---------|-----|-----|---------|---------|--------------------|-----|
| | C1 | C2, C2L | C3 | C4 | I2, I2L | I3, I3L | I3YY | I4 |
| 3 GX channel—8.5 Gbps | — | Yes | Yes | Yes | — | Yes | Yes ⁽⁴⁾ | Yes |

Notes to Table 1:

- (1) C = Commercial temperature grade; I = Industrial temperature grade.
 (2) Lower number refers to faster speed grade.
 (3) C2L, I2L, and I3L speed grades are for low-power devices.
 (4) I3YY speed grades can achieve up to 10.3125 Gbps.

Table 2 lists the industrial and commercial speed grades for the Stratix V GT devices.

Table 2. Stratix V GT Commercial and Industrial Speed Grade Offering ⁽¹⁾, ⁽²⁾

| Transceiver Speed Grade | Core Speed Grade | | | |
|--|------------------|-----|-----|-----|
| | C1 | C2 | I2 | I3 |
| 2 GX channel—12.5 Gbps GT channel—28.05 Gbps | Yes | Yes | — | — |
| 3 GX channel—12.5 Gbps GT channel—25.78 Gbps | Yes | Yes | Yes | Yes |

Notes to Table 2:

- (1) C = Commercial temperature grade; I = Industrial temperature grade.
 (2) Lower number refers to faster speed grade.

Absolute Maximum Ratings

Absolute maximum ratings define the maximum operating conditions for Stratix V devices. The values are based on experiments conducted with the devices and theoretical modeling of breakdown and damage mechanisms. The functional operation of the device is not implied for these conditions.



Conditions other than those listed in Table 3 may cause permanent damage to the device. Additionally, device operation at the absolute maximum ratings for extended periods of time may have adverse effects on the device.

Table 3. Absolute Maximum Ratings for Stratix V Devices (Part 1 of 2)

| Symbol | Description | Minimum | Maximum | Unit |
|---------------------|--|---------|---------|------|
| V _{CC} | Power supply for core voltage and periphery circuitry | −0.5 | 1.35 | V |
| V _{CCPT} | Power supply for programmable power technology | −0.5 | 1.8 | V |
| V _{CCPGM} | Power supply for configuration pins | −0.5 | 3.9 | V |
| V _{CC_AUX} | Auxiliary supply for the programmable power technology | −0.5 | 3.4 | V |
| V _{CCBAT} | Battery back-up power supply for design security volatile key register | −0.5 | 3.9 | V |
| V _{CCPD} | I/O pre-driver power supply | −0.5 | 3.9 | V |
| V _{CCIO} | I/O power supply | −0.5 | 3.9 | V |

Table 3. Absolute Maximum Ratings for Stratix V Devices (Part 2 of 2)

| Symbol | Description | Minimum | Maximum | Unit |
|-----------------------|--------------------------------|---------|---------|------|
| V _{CCD_FPLL} | PLL digital power supply | −0.5 | 1.8 | V |
| V _{CCA_FPLL} | PLL analog power supply | −0.5 | 3.4 | V |
| V _I | DC input voltage | −0.5 | 3.8 | V |
| T _J | Operating junction temperature | −55 | 125 | °C |
| T _{STG} | Storage temperature (No bias) | −65 | 150 | °C |
| I _{OUT} | DC output current per pin | −25 | 40 | mA |

Table 4 lists the absolute conditions for the transceiver power supply for Stratix V GX, GS, and GT devices.

Table 4. Transceiver Power Supply Absolute Conditions for Stratix V GX, GS, and GT Devices

| Symbol | Description | Devices | Minimum | Maximum | Unit |
|-----------------------|--|------------|---------|---------|------|
| V _{CCA_GXBL} | Transceiver channel PLL power supply (left side) | GX, GS, GT | −0.5 | 3.75 | V |
| V _{CCA_GXBR} | Transceiver channel PLL power supply (right side) | GX, GS | −0.5 | 3.75 | V |
| V _{CCA_GTBR} | Transceiver channel PLL power supply (right side) | GT | −0.5 | 3.75 | V |
| V _{CCHIP_L} | Transceiver hard IP power supply (left side) | GX, GS, GT | −0.5 | 1.35 | V |
| V _{CCHIP_R} | Transceiver hard IP power supply (right side) | GX, GS, GT | −0.5 | 1.35 | V |
| V _{CCHSSI_L} | Transceiver PCS power supply (left side) | GX, GS, GT | −0.5 | 1.35 | V |
| V _{CCHSSI_R} | Transceiver PCS power supply (right side) | GX, GS, GT | −0.5 | 1.35 | V |
| V _{CCR_GXBL} | Receiver analog power supply (left side) | GX, GS, GT | −0.5 | 1.35 | V |
| V _{CCR_GXBR} | Receiver analog power supply (right side) | GX, GS, GT | −0.5 | 1.35 | V |
| V _{CCR_GTBR} | Receiver analog power supply for GT channels (right side) | GT | −0.5 | 1.35 | V |
| V _{CCT_GXBL} | Transmitter analog power supply (left side) | GX, GS, GT | −0.5 | 1.35 | V |
| V _{CCT_GXBR} | Transmitter analog power supply (right side) | GX, GS, GT | −0.5 | 1.35 | V |
| V _{CCT_GTBR} | Transmitter analog power supply for GT channels (right side) | GT | −0.5 | 1.35 | V |
| V _{CCL_GTBR} | Transmitter clock network power supply (right side) | GT | −0.5 | 1.35 | V |
| V _{CCH_GXBL} | Transmitter output buffer power supply (left side) | GX, GS, GT | −0.5 | 1.8 | V |
| V _{CCH_GXBR} | Transmitter output buffer power supply (right side) | GX, GS, GT | −0.5 | 1.8 | V |

Maximum Allowed Overshoot and Undershoot Voltage

During transitions, input signals may overshoot to the voltage shown in Table 5 and undershoot to −2.0 V for input currents less than 100 mA and periods shorter than 20 ns.

Table 5 lists the maximum allowed input overshoot voltage and the duration of the overshoot voltage as a percentage of device lifetime. The maximum allowed overshoot duration is specified as a percentage of high time over the lifetime of the device. A DC signal is equivalent to 100% of the duty cycle. For example, a signal that overshoots to 3.95 V can be at 3.95 V for only ~21% over the lifetime of the device; for a device lifetime of 10 years, the overshoot duration amounts to ~2 years.

Table 5. Maximum Allowed Overshoot During Transitions

| Symbol | Description | Condition (V) | Overshoot Duration as % @ $T_J = 100^{\circ}\text{C}$ | Unit |
|------------|------------------|---------------|--|------|
| V_i (AC) | AC input voltage | 3.8 | 100 | % |
| | | 3.85 | 64 | % |
| | | 3.9 | 36 | % |
| | | 3.95 | 21 | % |
| | | 4 | 12 | % |
| | | 4.05 | 7 | % |
| | | 4.1 | 4 | % |
| | | 4.15 | 2 | % |
| | | 4.2 | 1 | % |

Figure 1. Stratix V Device Overshoot Duration

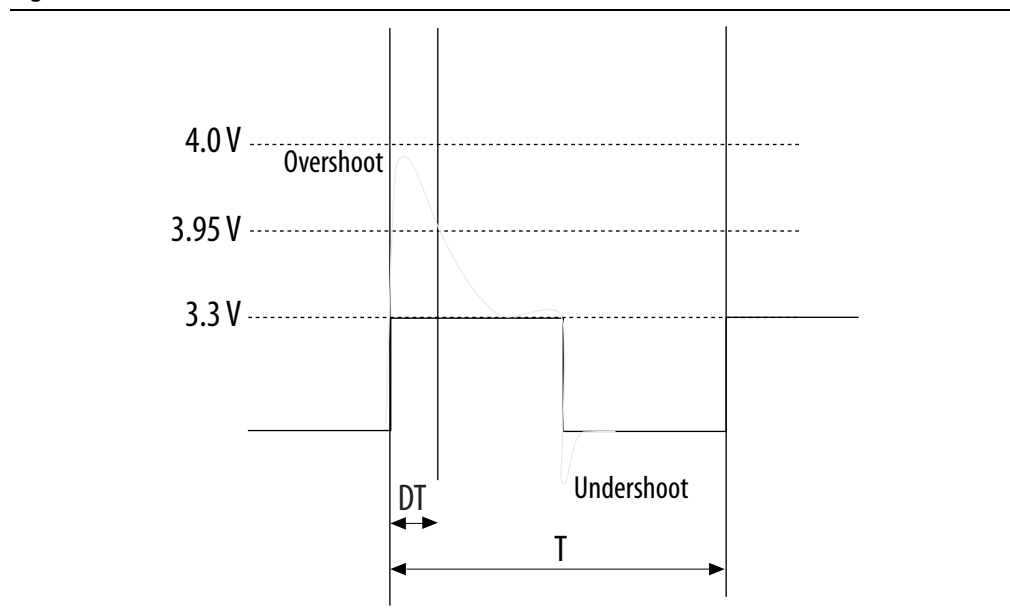


Table 8 shows the transceiver power supply voltage requirements for various conditions.

Table 8. Transceiver Power Supply Voltage Requirements

| Conditions | Core Speed Grade | VCCR_GXB & VCCT_GXB ⁽²⁾ | VCCA_GXB | VCCH_GXB | Unit |
|---|-----------------------------------|------------------------------------|----------|----------|------|
| If BOTH of the following conditions are true: <ul style="list-style-type: none"> ■ Data rate > 10.3 Gbps. ■ DFE is used. | All | 1.05 | 3.0 | 1.5 | V |
| If ANY of the following conditions are true ⁽¹⁾ : <ul style="list-style-type: none"> ■ ATX PLL is used. ■ Data rate > 6.5Gbps. ■ DFE (data rate ≤ 10.3 Gbps), AEQ, or EyeQ feature is used. | All | 1.0 | | | |
| If ALL of the following conditions are true: <ul style="list-style-type: none"> ■ ATX PLL is not used. ■ Data rate ≤ 6.5Gbps. ■ DFE, AEQ, and EyeQ are not used. | C1, C2, I2, and I3YY | 0.90 | 2.5 | | |
| | C2L, C3, C4, I2L, I3, I3L, and I4 | 0.85 | 2.5 | | |

Notes to Table 8:

- (1) Choose this power supply voltage requirement option if you plan to upgrade your design later with any of the listed conditions.
- (2) If the VCCR_GXB and VCCT_GXB supplies are set to 1.0 V or 1.05 V, they cannot be shared with the VCC core supply. If the VCCR_GXB and VCCT_GXB are set to either 0.90 V or 0.85 V, they can be shared with the VCC core supply.

DC Characteristics

This section lists the supply current, I/O pin leakage current, input pin capacitance, on-chip termination tolerance, and hot socketing specifications.

Supply Current

Supply current is the current drawn from the respective power rails used for power budgeting. Use the Excel-based Early Power Estimator (EPE) to get supply current estimates for your design because these currents vary greatly with the resources you use.



For more information about power estimation tools, refer to the *PowerPlay Early Power Estimator User Guide* and the *PowerPlay Power Analysis* chapter in the *Quartus II Handbook*.

I/O Pin Leakage Current

Table 9 lists the Stratix V I/O pin leakage current specifications.

Table 9. I/O Pin Leakage Current for Stratix V Devices ⁽¹⁾

| Symbol | Description | Conditions | Min | Typ | Max | Unit |
|----------|--------------------|-------------------------------------|-----|-----|-----|---------------|
| I_I | Input pin | $V_I = 0 \text{ V to } V_{CCIOMAX}$ | -30 | — | 30 | μA |
| I_{OZ} | Tri-stated I/O pin | $V_O = 0 \text{ V to } V_{CCIOMAX}$ | -30 | — | 30 | μA |

Note to Table 9:

(1) If $V_O = V_{CCIO}$ to $V_{CCIOMAX}$, 100 μA of leakage current per I/O is expected.

Bus Hold Specifications

Table 10 lists the Stratix V device family bus hold specifications.

Table 10. Bus Hold Parameters for Stratix V Devices

| Parameter | Symbol | Conditions | V _{CCIO} | | | | | | | | | | Unit |
|-------------------------|-------------------|--|-------------------|------|-------|------|-------|------|-------|------|-------|------|------|
| | | | 1.2 V | | 1.5 V | | 1.8 V | | 2.5 V | | 3.0 V | | |
| | | | Min | Max | Min | Max | Min | Max | Min | Max | Min | Max | |
| Low sustaining current | I _{SUSL} | V _{IN} > V _{IL} (maximum) | 22.5 | — | 25.0 | — | 30.0 | — | 50.0 | — | 70.0 | — | μA |
| High sustaining current | I _{SUSH} | V _{IN} < V _{IH} (minimum) | −22.5 | — | −25.0 | — | −30.0 | — | −50.0 | — | −70.0 | — | μA |
| Low overdrive current | I _{ODL} | 0V < V _{IN} < V _{CCIO} | — | 120 | — | 160 | — | 200 | — | 300 | — | 500 | μA |
| High overdrive current | I _{ODH} | 0V < V _{IN} < V _{CCIO} | — | −120 | — | −160 | — | −200 | — | −300 | — | −500 | μA |
| Bus-hold trip point | V _{TRIP} | — | 0.45 | 0.95 | 0.50 | 1.00 | 0.68 | 1.07 | 0.70 | 1.70 | 0.80 | 2.00 | V |

On-Chip Termination (OCT) Specifications

If you enable OCT calibration, calibration is automatically performed at power-up for I/Os connected to the calibration block. Table 11 lists the Stratix V OCT termination calibration accuracy specifications.

Table 11. OCT Calibration Accuracy Specifications for Stratix V Devices ⁽¹⁾ (Part 1 of 2)

| Symbol | Description | Conditions | Calibration Accuracy | | | | Unit |
|--------------------|---|--|----------------------|----------|----------------|----------|------|
| | | | C1 | C2,I2 | C3,I3, I3YY | C4,I4 | |
| 25- Ω R_S | Internal series termination with calibration (25- Ω setting) | $V_{CCIO} = 3.0, 2.5, 1.8, 1.5, 1.2 \text{ V}$ | ± 15 | ± 15 | ± 15 | ± 15 | % |

Table 11. OCT Calibration Accuracy Specifications for Stratix V Devices ⁽¹⁾ (Part 2 of 2)

| Symbol | Description | Conditions | Calibration Accuracy | | | | Unit |
|--|--|---|----------------------|------------|----------------|------------|------|
| | | | C1 | C2,I2 | C3,I3, I3YY | C4,I4 | |
| 50-Ω R _S | Internal series termination with calibration (50-Ω setting) | V _{CCIO} = 3.0, 2.5, 1.8, 1.5, 1.2 V | ±15 | ±15 | ±15 | ±15 | % |
| 34-Ω and 40-Ω R _S | Internal series termination with calibration (34-Ω and 40-Ω setting) | V _{CCIO} = 1.5, 1.35, 1.25, 1.2 V | ±15 | ±15 | ±15 | ±15 | % |
| 48-Ω, 60-Ω, 80-Ω, and 240-Ω R _S | Internal series termination with calibration (48-Ω, 60-Ω, 80-Ω, and 240-Ω setting) | V _{CCIO} = 1.2 V | ±15 | ±15 | ±15 | ±15 | % |
| 50-Ω R _T | Internal parallel termination with calibration (50-Ω setting) | V _{CCIO} = 2.5, 1.8, 1.5, 1.2 V | -10 to +40 | -10 to +40 | -10 to +40 | -10 to +40 | % |
| 20-Ω, 30-Ω, 40-Ω, 60-Ω, and 120-Ω R _T | Internal parallel termination with calibration (20-Ω, 30-Ω, 40-Ω, 60-Ω, and 120-Ω setting) | V _{CCIO} = 1.5, 1.35, 1.25 V | -10 to +40 | -10 to +40 | -10 to +40 | -10 to +40 | % |
| 60-Ω and 120-Ω R _T | Internal parallel termination with calibration (60-Ω and 120-Ω setting) | V _{CCIO} = 1.2 | -10 to +40 | -10 to +40 | -10 to +40 | -10 to +40 | % |
| 25-Ω R _{S_left_shift} | Internal left shift series termination with calibration (25-Ω R _{S_left_shift} setting) | V _{CCIO} = 3.0, 2.5, 1.8, 1.5, 1.2 V | ±15 | ±15 | ±15 | ±15 | % |

Note to Table 11:

(1) OCT calibration accuracy is valid at the time of calibration only.

Table 12 lists the Stratix V OCT without calibration resistance tolerance to PVT changes.

Table 12. OCT Without Calibration Resistance Tolerance Specifications for Stratix V Devices (Part 1 of 2)

| Symbol | Description | Conditions | Resistance Tolerance | | | | Unit |
|-----------------------------|--|-----------------------------------|----------------------|-------|-----------------|--------|------|
| | | | C1 | C2,I2 | C3, I3, I3YY | C4, I4 | |
| 25-Ω R, 50-Ω R _S | Internal series termination without calibration (25-Ω setting) | V _{CCIO} = 3.0 and 2.5 V | ±30 | ±30 | ±40 | ±40 | % |
| 25-Ω R _S | Internal series termination without calibration (25-Ω setting) | V _{CCIO} = 1.8 and 1.5 V | ±30 | ±30 | ±40 | ±40 | % |
| 25-Ω R _S | Internal series termination without calibration (25-Ω setting) | V _{CCIO} = 1.2 V | ±35 | ±35 | ±50 | ±50 | % |

Table 19. Single-Ended SSTL, HSTL, and HSUL I/O Standards Signal Specifications for Stratix V Devices (Part 2 of 2)

| I/O Standard | $V_{IL(DC)}$ (V) | | $V_{IH(DC)}$ (V) | | $V_{IL(AC)}$ (V) | $V_{IH(AC)}$ (V) | V_{OL} (V) | V_{OH} (V) | I_{ol} (mA) | I_{oh} (mA) |
|------------------|------------------|------------------|------------------|-------------------|------------------|------------------|-------------------|-------------------|---------------|---------------|
| | Min | Max | Min | Max | Max | Min | Max | Min | | |
| HSTL-18 Class I | — | $V_{REF} - 0.1$ | $V_{REF} + 0.1$ | — | $V_{REF} - 0.2$ | $V_{REF} + 0.2$ | 0.4 | $V_{CCIO} - 0.4$ | 8 | -8 |
| HSTL-18 Class II | — | $V_{REF} - 0.1$ | $V_{REF} + 0.1$ | — | $V_{REF} - 0.2$ | $V_{REF} + 0.2$ | 0.4 | $V_{CCIO} - 0.4$ | 16 | -16 |
| HSTL-15 Class I | — | $V_{REF} - 0.1$ | $V_{REF} + 0.1$ | — | $V_{REF} - 0.2$ | $V_{REF} + 0.2$ | 0.4 | $V_{CCIO} - 0.4$ | 8 | -8 |
| HSTL-15 Class II | — | $V_{REF} - 0.1$ | $V_{REF} + 0.1$ | — | $V_{REF} - 0.2$ | $V_{REF} + 0.2$ | 0.4 | $V_{CCIO} - 0.4$ | 16 | -16 |
| HSTL-12 Class I | -0.15 | $V_{REF} - 0.08$ | $V_{REF} + 0.08$ | $V_{CCIO} + 0.15$ | $V_{REF} - 0.15$ | $V_{REF} + 0.15$ | $0.25^* V_{CCIO}$ | $0.75^* V_{CCIO}$ | 8 | -8 |
| HSTL-12 Class II | -0.15 | $V_{REF} - 0.08$ | $V_{REF} + 0.08$ | $V_{CCIO} + 0.15$ | $V_{REF} - 0.15$ | $V_{REF} + 0.15$ | $0.25^* V_{CCIO}$ | $0.75^* V_{CCIO}$ | 16 | -16 |
| HSUL-12 | — | $V_{REF} - 0.13$ | $V_{REF} + 0.13$ | — | $V_{REF} - 0.22$ | $V_{REF} + 0.22$ | $0.1^* V_{CCIO}$ | $0.9^* V_{CCIO}$ | — | — |

Table 20. Differential SSTL I/O Standards for Stratix V Devices

| I/O Standard | V_{CCIO} (V) | | | $V_{SWING(DC)}$ (V) | | $V_{X(AC)}$ (V) | | | $V_{SWING(AC)}$ (V) | |
|----------------------|----------------|------|-------|---------------------|------------------|----------------------|--------------|----------------------|---------------------------|---------------------------|
| | Min | Typ | Max | Min | Max | Min | Typ | Max | Min | Max |
| SSTL-2 Class I, II | 2.375 | 2.5 | 2.625 | 0.3 | $V_{CCIO} + 0.6$ | $V_{CCIO}/2 - 0.2$ | — | $V_{CCIO}/2 + 0.2$ | 0.62 | $V_{CCIO} + 0.6$ |
| SSTL-18 Class I, II | 1.71 | 1.8 | 1.89 | 0.25 | $V_{CCIO} + 0.6$ | $V_{CCIO}/2 - 0.175$ | — | $V_{CCIO}/2 + 0.175$ | 0.5 | $V_{CCIO} + 0.6$ |
| SSTL-15 Class I, II | 1.425 | 1.5 | 1.575 | 0.2 | (1) | $V_{CCIO}/2 - 0.15$ | — | $V_{CCIO}/2 + 0.15$ | 0.35 | — |
| SSTL-135 Class I, II | 1.283 | 1.35 | 1.45 | 0.2 | (1) | $V_{CCIO}/2 - 0.15$ | $V_{CCIO}/2$ | $V_{CCIO}/2 + 0.15$ | $2(V_{IH(AC)} - V_{REF})$ | $2(V_{IL(AC)} - V_{REF})$ |
| SSTL-125 Class I, II | 1.19 | 1.25 | 1.31 | 0.18 | (1) | $V_{CCIO}/2 - 0.15$ | $V_{CCIO}/2$ | $V_{CCIO}/2 + 0.15$ | $2(V_{IH(AC)} - V_{REF})$ | — |
| SSTL-12 Class I, II | 1.14 | 1.2 | 1.26 | 0.18 | — | $V_{REF} - 0.15$ | $V_{CCIO}/2$ | $V_{REF} + 0.15$ | -0.30 | 0.30 |

Note to Table 20:

(1) The maximum value for $V_{SWING(DC)}$ is not defined. However, each single-ended signal needs to be within the respective single-ended limits ($V_{IH(DC)}$ and $V_{IL(DC)}$).

Table 21. Differential HSTL and HSUL I/O Standards for Stratix V Devices (Part 1 of 2)

| I/O Standard | V_{CCIO} (V) | | | $V_{DIF(DC)}$ (V) | | $V_{X(AC)}$ (V) | | | $V_{CM(DC)}$ (V) | | | $V_{DIF(AC)}$ (V) | |
|---------------------|----------------|-----|-------|-------------------|-----|-----------------|-----|------|------------------|-----|------|-------------------|-----|
| | Min | Typ | Max | Min | Max | Min | Typ | Max | Min | Typ | Max | Min | Max |
| HSTL-18 Class I, II | 1.71 | 1.8 | 1.89 | 0.2 | — | 0.78 | — | 1.12 | 0.78 | — | 1.12 | 0.4 | — |
| HSTL-15 Class I, II | 1.425 | 1.5 | 1.575 | 0.2 | — | 0.68 | — | 0.9 | 0.68 | — | 0.9 | 0.4 | — |

Switching Characteristics

This section provides performance characteristics of the Stratix V core and periphery blocks.

These characteristics can be designated as Preliminary or Final.

- Preliminary characteristics are created using simulation results, process data, and other known parameters. The title of these tables show the designation as “Preliminary.”
- Final numbers are based on actual silicon characterization and testing. The numbers reflect the actual performance of the device under worst-case silicon process, voltage, and junction temperature conditions. There are no designations on finalized tables.

Transceiver Performance Specifications

This section describes transceiver performance specifications.

Table 23 lists the Stratix V GX and GS transceiver specifications.

Table 23. Transceiver Specifications for Stratix V GX and GS Devices ⁽¹⁾ (Part 1 of 7)

| Symbol/ Description | Conditions | Transceiver Speed Grade 1 | | | Transceiver Speed Grade 2 | | | Transceiver Speed Grade 3 | | | Unit |
|--|---|---|-----|-----|------------------------------|-----|-----|------------------------------|-----|-----|------|
| | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| Reference Clock | | | | | | | | | | | |
| Supported I/O Standards | Dedicated reference clock pin | 1.2-V PCML, 1.4-V PCML, 1.5-V PCML, 2.5-V PCML, Differential LVPECL, LVDS, and HCSL | | | | | | | | | |
| | RX reference clock pin | 1.4-V PCML, 1.5-V PCML, 2.5-V PCML, LVPECL, and LVDS | | | | | | | | | |
| Input Reference Clock Frequency (CMU PLL) ⁽⁸⁾ | — | 40 | — | 710 | 40 | — | 710 | 40 | — | 710 | MHz |
| Input Reference Clock Frequency (ATX PLL) ⁽⁸⁾ | — | 100 | — | 710 | 100 | — | 710 | 100 | — | 710 | MHz |
| Rise time | Measure at ±60 mV of differential signal ⁽²⁶⁾ | — | — | 400 | — | — | 400 | — | — | 400 | ps |
| Fall time | Measure at ±60 mV of differential signal ⁽²⁶⁾ | — | — | 400 | — | — | 400 | — | — | 400 | |
| Duty cycle | — | 45 | — | 55 | 45 | — | 55 | 45 | — | 55 | % |
| Spread-spectrum modulating clock frequency | PCI Express® (PCIe®) | 30 | — | 33 | 30 | — | 33 | 30 | — | 33 | kHz |

Table 23. Transceiver Specifications for Stratix V GX and GS Devices ⁽¹⁾ (Part 6 of 7)

| Symbol/ Description | Conditions | Transceiver Speed Grade 1 | | | Transceiver Speed Grade 2 | | | Transceiver Speed Grade 3 | | | Unit |
|---|--|------------------------------|-----|-------------------------------|------------------------------|-----|-------------------------------|------------------------------|-----|-------------------------------------|------|
| | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| Inter-transceiver block transmitter channel-to- channel skew | xN PMA bonded mode | — | — | 500 | — | — | 500 | — | — | 500 | ps |
| CMU PLL | | | | | | | | | | | |
| Supported Data Range | — | 600 | — | 12500 | 600 | — | 12500 | 600 | — | 8500/ 10312.5 ⁽²⁴⁾ | Mbps |
| t _{pll_powerdown} ⁽¹⁵⁾ | — | 1 | — | — | 1 | — | — | 1 | — | — | μs |
| t _{pll_lock} ⁽¹⁶⁾ | — | — | — | 10 | — | — | 10 | — | — | 10 | μs |
| ATX PLL | | | | | | | | | | | |
| Supported Data Rate Range | VCO post-divider L=2 | 8000 | — | 14100 | 8000 | — | 12500 | 8000 | — | 8500/ 10312.5 ⁽²⁴⁾ | Mbps |
| | L=4 | 4000 | — | 7050 | 4000 | — | 6600 | 4000 | — | 6600 | Mbps |
| | L=8 | 2000 | — | 3525 | 2000 | — | 3300 | 2000 | — | 3300 | Mbps |
| | L=8, Local/Central Clock Divider =2 | 1000 | — | 1762.5 | 1000 | — | 1762.5 | 1000 | — | 1762.5 | Mbps |
| t _{pll_powerdown} ⁽¹⁵⁾ | — | 1 | — | — | 1 | — | — | 1 | — | — | μs |
| t _{pll_lock} ⁽¹⁶⁾ | — | — | — | 10 | — | — | 10 | — | — | 10 | μs |
| fPLL | | | | | | | | | | | |
| Supported Data Range | — | 600 | — | 3250/ 3125 ⁽²⁵⁾ | 600 | — | 3250/ 3125 ⁽²⁵⁾ | 600 | — | 3250/ 3125 ⁽²⁵⁾ | Mbps |
| t _{pll_powerdown} ⁽¹⁵⁾ | — | 1 | — | — | 1 | — | — | 1 | — | — | μs |

Table 26 shows the approximate maximum data rate using the 10G PCS.

Table 26. Stratix V 10G PCS Approximate Maximum Data Rate ⁽¹⁾

| Mode ⁽²⁾ | Transceiver Speed Grade | PMA Width | 64 | 40 | 40 | 40 | 32 | 32 |
|---------------------|-------------------------|---------------------------------------|--------------|-------|-------|------|----------|-------|
| | | PCS Width | 64 | 66/67 | 50 | 40 | 64/66/67 | 32 |
| FIFO or Register | 1 | C1, C2, C2L, I2, I2L core speed grade | 14.1 | 14.1 | 10.69 | 14.1 | 13.6 | 13.6 |
| | 2 | C1, C2, C2L, I2, I2L core speed grade | 12.5 | 12.5 | 10.69 | 12.5 | 12.5 | 12.5 |
| | | C3, I3, I3L core speed grade | 12.5 | 12.5 | 10.69 | 12.5 | 10.88 | 10.88 |
| | 3 | C1, C2, C2L, I2, I2L core speed grade | 8.5 Gbps | | | | | |
| | | C3, I3, I3L core speed grade | | | | | | |
| | | C4, I4 core speed grade | | | | | | |
| | | I3YY core speed grade | 10.3125 Gbps | | | | | |

Notes to Table 26:

- (1) The maximum data rate is in Gbps.
- (2) The Phase Compensation FIFO can be configured in FIFO mode or register mode. In the FIFO mode, the pointers are not fixed, and the latency can vary. In the register mode the pointers are fixed for low latency.

Table 27 shows the V_{OD} settings for the GX channel.

Table 27. Typical V_{OD} Setting for GX Channel, TX Termination = 100 Ω ⁽²⁾

| Symbol | V_{OD} Setting | V_{OD} Value (mV) | V_{OD} Setting | V_{OD} Value (mV) |
|---|------------------|---------------------|------------------|---------------------|
| V_{OD} differential peak to peak typical ⁽³⁾ | 0 ⁽¹⁾ | 0 | 32 | 640 |
| | 1 ⁽¹⁾ | 20 | 33 | 660 |
| | 2 ⁽¹⁾ | 40 | 34 | 680 |
| | 3 ⁽¹⁾ | 60 | 35 | 700 |
| | 4 ⁽¹⁾ | 80 | 36 | 720 |
| | 5 ⁽¹⁾ | 100 | 37 | 740 |
| | 6 | 120 | 38 | 760 |
| | 7 | 140 | 39 | 780 |
| | 8 | 160 | 40 | 800 |
| | 9 | 180 | 41 | 820 |
| | 10 | 200 | 42 | 840 |
| | 11 | 220 | 43 | 860 |
| | 12 | 240 | 44 | 880 |
| | 13 | 260 | 45 | 900 |
| | 14 | 280 | 46 | 920 |
| | 15 | 300 | 47 | 940 |
| | 16 | 320 | 48 | 960 |
| | 17 | 340 | 49 | 980 |
| | 18 | 360 | 50 | 1000 |
| | 19 | 380 | 51 | 1020 |
| | 20 | 400 | 52 | 1040 |
| | 21 | 420 | 53 | 1060 |
| | 22 | 440 | 54 | 1080 |
| | 23 | 460 | 55 | 1100 |
| | 24 | 480 | 56 | 1120 |
| | 25 | 500 | 57 | 1140 |
| | 26 | 520 | 58 | 1160 |
| | 27 | 540 | 59 | 1180 |
| | 28 | 560 | 60 | 1200 |
| | 29 | 580 | 61 | 1220 |
| | 30 | 600 | 62 | 1240 |
| | 31 | 620 | 63 | 1260 |

Note to Table 27:

- (1) If TX termination resistance = 100 Ω , this VOD setting is illegal.
- (2) The tolerance is +/-20% for all VOD settings except for settings 2 and below.
- (3) Refer to Figure 2.

Table 28. Transceiver Specifications for Stratix V GT Devices (Part 2 of 5) ⁽¹⁾

| Symbol/ Description | Conditions | Transceiver Speed Grade 2 | | | Transceiver Speed Grade 3 | | | Unit |
|---|---|--|---------------|--------|------------------------------|---------------|--------|----------|
| | | Min | Typ | Max | Min | Typ | Max | |
| Transmitter REFCLK Phase Noise (622 MHz) ⁽¹⁸⁾ | 100 Hz | — | — | -70 | — | — | -70 | dBc/Hz |
| | 1 kHz | — | — | -90 | — | — | -90 | |
| | 10 kHz | — | — | -100 | — | — | -100 | |
| | 100 kHz | — | — | -110 | — | — | -110 | |
| | ≥ 1 MHz | — | — | -120 | — | — | -120 | |
| Transmitter REFCLK Phase Jitter (100 MHz) ⁽¹⁵⁾ | 10 kHz to 1.5 MHz (PCIe) | — | — | 3 | — | — | 3 | ps (rms) |
| RREF ⁽¹⁷⁾ | — | — | 1800 ± 1% | — | — | 1800 ± 1% | — | Ω |
| Transceiver Clocks | | | | | | | | |
| fixedclk clock frequency | PCIe Receiver Detect | — | 100 or 125 | — | — | 100 or 125 | — | MHz |
| Reconfiguration clock (mgmt_clk_clk) frequency | — | 100 | — | 125 | 100 | — | 125 | MHz |
| Receiver | | | | | | | | |
| Supported I/O Standards | — | 1.4-V PCML, 1.5-V PCML, 2.5-V PCML, LVPECL, and LVDS | | | | | | |
| Data rate (Standard PCS) ⁽²¹⁾ | GX channels | 600 | — | 8500 | 600 | — | 8500 | Mbps |
| Data rate (10G PCS) ⁽²¹⁾ | GX channels | 600 | — | 12,500 | 600 | — | 12,500 | Mbps |
| Data rate | GT channels | 19,600 | — | 28,050 | 19,600 | — | 25,780 | Mbps |
| Absolute V _{MAX} for a receiver pin ⁽³⁾ | GT channels | — | — | 1.2 | — | — | 1.2 | V |
| Absolute V _{MIN} for a receiver pin | GT channels | -0.4 | — | — | -0.4 | — | — | V |
| Maximum peak-to-peak differential input voltage V _{ID} (diff p-p) before device configuration ⁽²⁰⁾ | GT channels | — | — | 1.6 | — | — | 1.6 | V |
| | GX channels | ⁽⁸⁾ | | | | | | |
| Maximum peak-to-peak differential input voltage V _{ID} (diff p-p) after device configuration ⁽¹⁶⁾ , ⁽²⁰⁾ | GT channels V _{CCR_GTB} = 1.05 V (V _{ICM} = 0.65 V) | — | — | 2.2 | — | — | 2.2 | V |
| | GX channels | ⁽⁸⁾ | | | | | | |
| Minimum differential eye opening at receiver serial input pins ⁽⁴⁾ , ⁽²⁰⁾ | GT channels | 200 | — | — | 200 | — | — | mV |
| | GX channels | ⁽⁸⁾ | | | | | | |

Table 28. Transceiver Specifications for Stratix V GT Devices (Part 5 of 5) ⁽¹⁾

| Symbol/ Description | Conditions | Transceiver Speed Grade 2 | | | Transceiver Speed Grade 3 | | | Unit |
|---------------------------------|------------|------------------------------|-----|-----|------------------------------|-----|-----|------|
| | | Min | Typ | Max | Min | Typ | Max | |
| t_{pll_lock} ⁽¹⁴⁾ | — | — | — | 10 | — | — | 10 | μs |

Notes to Table 28:

- (1) Speed grades shown refer to the PMA Speed Grade in the device ordering code. The maximum data rate could be restricted by the Core/PCS speed grade. Contact your Altera Sales Representative for the maximum data rate specifications in each speed grade combination offered. For more information about device ordering codes, refer to the *Stratix V Device Overview*.
- (2) The reference clock common mode voltage is equal to the VCCR_GXB power supply level.
- (3) The device cannot tolerate prolonged operation at this absolute maximum.
- (4) The differential eye opening specification at the receiver input pins assumes that receiver equalization is disabled. If you enable receiver equalization, the receiver circuitry can tolerate a lower minimum eye opening, depending on the equalization level.
- (5) Refer to Figure 5 for the GT channel AC gain curves. The total effective AC gain is the AC gain minus the DC gain.
- (6) Refer to Figure 6 for the GT channel DC gain curves.
- (7) CFP2 optical modules require the host interface to have the receiver data pins differentially terminated with 100 Ω. The internal OCT feature is available after the Stratix V FPGA configuration is completed. Altera recommends that FPGA configuration is completed before inserting the optical module. Otherwise, minimize unnecessary removal and insertion with unconfigured devices.
- (8) Specifications for this parameter are the same as for Stratix V GX and GS devices. See Table 23 for specifications.
- (9) t_{LTR} is the time required for the receive CDR to lock to the input reference clock frequency after coming out of reset.
- (10) t_{LTD} is time required for the receiver CDR to start recovering valid data after the $rx_is_lockedto\ data$ signal goes high.
- (11) t_{LTD_manual} is the time required for the receiver CDR to start recovering valid data after the $rx_is_lockedto\ data$ signal goes high when the CDR is functioning in the manual mode.
- (12) $t_{LTR_LTD_manual}$ is the time the receiver CDR must be kept in lock to reference (LTR) mode after the $rx_is_lockedto\ ref$ signal goes high when the CDR is functioning in the manual mode.
- (13) $tp11_powerdown$ is the PLL powerdown minimum pulse width.
- (14) $tp11_lock$ is the time required for the transmitter CMU/ATX PLL to lock to the input reference clock frequency after coming out of reset.
- (15) To calculate the REFCLK rms phase jitter requirement for PCIe at reference clock frequencies other than 100 MHz, use the following formula:
REFCLK rms phase jitter at f(MHz) = REFCLK rms phase jitter at 100 MHz × 100/f.
- (16) The maximum peak to peak differential input voltage V_{ID} after device configuration is equal to $4 \times (\text{absolute } V_{MAX} \text{ for receiver pin} - V_{ICM})$.
- (17) For ES devices, RREF is 2000 Ω ±1%.
- (18) To calculate the REFCLK phase noise requirement at frequencies other than 622 MHz, use the following formula: REFCLK phase noise at f(MHz) = REFCLK phase noise at 622 MHz + 20*log(f/622).
- (19) SFP/+ optical modules require the host interface to have RD+/- differentially terminated with 100 Ω. The internal OCT feature is available after the Stratix V FPGA configuration is completed. Altera recommends that FPGA configuration is completed before inserting the optical module. Otherwise, minimize unnecessary removal and insertion with unconfigured devices.
- (20) Refer to Figure 4.
- (21) For oversampling design to support data rates less than the minimum specification, the CDR needs to be in LTR mode only.
- (22) This supply follows VCCR_GXB for both GX and GT channels.
- (23) When you use fPLL as a TXPLL of the transceiver.

Table 29 shows the V_{OD} settings for the GT channel.

Table 29. Typical V_{OD} Setting for GT Channel, TX Termination = 100 Ω

| Symbol | V_{OD} Setting | V_{OD} Value (mV) |
|---|------------------|---------------------|
| V_{OD} differential peak to peak typical ⁽¹⁾ | 0 | 0 |
| | 1 | 200 |
| | 2 | 400 |
| | 3 | 600 |
| | 4 | 800 |
| | 5 | 1000 |

Note:

(1) Refer to Figure 4.

- XFI
- ASI
- HiGig/HiGig+
- HiGig2/HiGig2+
- Serial Data Converter (SDC)
- GPON
- SDI
- SONET
- Fibre Channel (FC)
- PCIe
- QPI
- SFF-8431

Download the Stratix V Characterization Report Tool to view the characterization report summary for these protocols.

Core Performance Specifications

This section describes the clock tree, phase-locked loop (PLL), digital signal processing (DSP), memory blocks, configuration, and JTAG specifications.

Clock Tree Specifications

Table 30 lists the clock tree specifications for Stratix V devices.

Table 30. Clock Tree Performance for Stratix V Devices ⁽¹⁾

| Symbol | Performance | | | Unit |
|---------------------------|--------------------------|-----------------------|--------|------|
| | C1, C2, C2L, I2, and I2L | C3, I3, I3L, and I3YY | C4, I4 | |
| Global and Regional Clock | 717 | 650 | 580 | MHz |
| Periphery Clock | 550 | 500 | 500 | MHz |

Note to Table 30:

(1) The Stratix V ES devices are limited to 600 MHz core clock tree performance.

PLL Specifications

Table 31 lists the Stratix V PLL specifications when operating in both the commercial junction temperature range (0° to 85°C) and the industrial junction temperature range (–40° to 100°C).

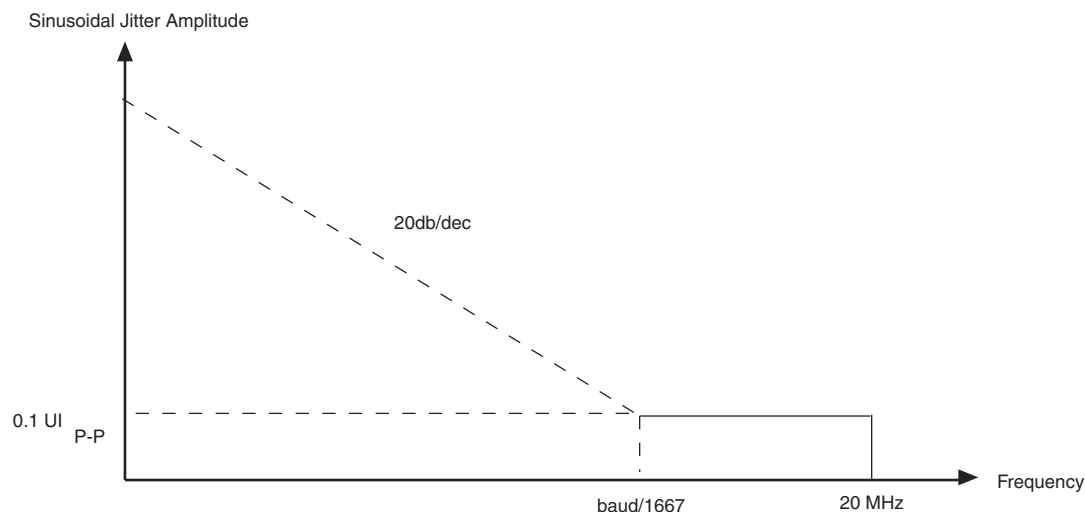
Table 31. PLL Specifications for Stratix V Devices (Part 1 of 3)

| Symbol | Parameter | Min | Typ | Max | Unit |
|--------------------------|--|-----|-----|--------------------|------|
| f_{IN} | Input clock frequency (C1, C2, C2L, I2, and I2L speed grades) | 5 | — | 800 ⁽¹⁾ | MHz |
| | Input clock frequency (C3, I3, I3L, and I3YY speed grades) | 5 | — | 800 ⁽¹⁾ | MHz |
| | Input clock frequency (C4, I4 speed grades) | 5 | — | 650 ⁽¹⁾ | MHz |
| f_{INPFD} | Input frequency to the PFD | 5 | — | 325 | MHz |
| f_{FINPFD} | Fractional Input clock frequency to the PFD | 50 | — | 160 | MHz |
| f_{VCO} ⁽⁹⁾ | PLL VCO operating range (C1, C2, C2L, I2, I2L speed grades) | 600 | — | 1600 | MHz |
| | PLL VCO operating range (C3, I3, I3L, I3YY speed grades) | 600 | — | 1600 | MHz |
| | PLL VCO operating range (C4, I4 speed grades) | 600 | — | 1300 | MHz |
| $t_{EINDUTY}$ | Input clock or external feedback clock input duty cycle | 40 | — | 60 | % |
| f_{OUT} | Output frequency for an internal global or regional clock (C1, C2, C2L, I2, I2L speed grades) | — | — | 717 ⁽²⁾ | MHz |
| | Output frequency for an internal global or regional clock (C3, I3, I3L speed grades) | — | — | 650 ⁽²⁾ | MHz |
| | Output frequency for an internal global or regional clock (C4, I4 speed grades) | — | — | 580 ⁽²⁾ | MHz |
| f_{OUT_EXT} | Output frequency for an external clock output (C1, C2, C2L, I2, I2L speed grades) | — | — | 800 ⁽²⁾ | MHz |
| | Output frequency for an external clock output (C3, I3, I3L speed grades) | — | — | 667 ⁽²⁾ | MHz |
| | Output frequency for an external clock output (C4, I4 speed grades) | — | — | 553 ⁽²⁾ | MHz |
| $t_{OUTDUTY}$ | Duty cycle for a dedicated external clock output (when set to 50%) | 45 | 50 | 55 | % |
| t_{FCOMP} | External feedback clock compensation time | — | — | 10 | ns |
| $f_{DYCONFIGCLK}$ | Dynamic Configuration Clock used for <code>mgmt_clk</code> and <code>scanclk</code> | — | — | 100 | MHz |
| t_{LOCK} | Time required to lock from the end-of-device configuration or deassertion of <code>areset</code> | — | — | 1 | ms |
| t_{DLOCK} | Time required to lock dynamically (after switchover or reconfiguring any non-post-scale counters/delays) | — | — | 1 | ms |
| f_{CLBW} | PLL closed-loop low bandwidth | — | 0.3 | — | MHz |
| | PLL closed-loop medium bandwidth | — | 1.5 | — | MHz |
| | PLL closed-loop high bandwidth ⁽⁷⁾ | — | 4 | — | MHz |
| t_{PLL_PSERR} | Accuracy of PLL phase shift | — | — | ±50 | ps |
| t_{ARESET} | Minimum pulse width on the <code>areset</code> signal | 10 | — | — | ns |

Table 38. LVDS Soft-CDR/DPA Sinusoidal Jitter Mask Values for a Data Rate ≥ 1.25 Gbps

| Jitter Frequency (Hz) | | Sinusoidal Jitter (UI) |
|-----------------------|------------|------------------------|
| F1 | 10,000 | 25.000 |
| F2 | 17,565 | 25.000 |
| F3 | 1,493,000 | 0.350 |
| F4 | 50,000,000 | 0.350 |

Figure 9 shows the LVDS soft-CDR/DPA sinusoidal jitter tolerance specification for a data rate < 1.25 Gbps.

Figure 9. LVDS Soft-CDR/DPA Sinusoidal Jitter Tolerance Specification for a Data Rate < 1.25 Gbps

DLL Range, DQS Logic Block, and Memory Output Clock Jitter Specifications

Table 39 lists the DLL range specification for Stratix V devices. The DLL is always in 8-tap mode in Stratix V devices.

Table 39. DLL Range Specifications for Stratix V Devices ⁽¹⁾

| C1 | C2, C2L, I2, I2L | C3, I3, I3L, I3YY | C4,I4 | Unit |
|---------|------------------|-------------------|---------|------|
| 300-933 | 300-933 | 300-890 | 300-890 | MHz |

Note to Table 39:

- (1) Stratix V devices support memory interface frequencies lower than 300 MHz, although the reference clock that feeds the DLL must be at least 300 MHz. To support interfaces below 300 MHz, multiply the reference clock feeding the DLL to ensure the frequency is within the supported range of the DLL.

Table 40 lists the DQS phase offset delay per stage for Stratix V devices.

Table 40. DQS Phase Offset Delay Per Setting for Stratix V Devices ^{(1), (2)} (Part 1 of 2)

| Speed Grade | Min | Max | Unit |
|------------------|-----|-----|------|
| C1 | 8 | 14 | ps |
| C2, C2L, I2, I2L | 8 | 14 | ps |
| C3,I3, I3L, I3YY | 8 | 15 | ps |

Table 48. Minimum Configuration Time Estimation for Stratix V Devices

| Variant | Member Code | Active Serial ⁽¹⁾ | | | Fast Passive Parallel ⁽²⁾ | | |
|---------|-------------|------------------------------|------------|---------------------|--------------------------------------|------------|---------------------|
| | | Width | DCLK (MHz) | Min Config Time (s) | Width | DCLK (MHz) | Min Config Time (s) |
| GS | D3 | 4 | 100 | 0.344 | 32 | 100 | 0.043 |
| | D4 | 4 | 100 | 0.534 | 32 | 100 | 0.067 |
| | | 4 | 100 | 0.344 | 32 | 100 | 0.043 |
| | D5 | 4 | 100 | 0.534 | 32 | 100 | 0.067 |
| | D6 | 4 | 100 | 0.741 | 32 | 100 | 0.093 |
| | D8 | 4 | 100 | 0.741 | 32 | 100 | 0.093 |
| E | E9 | 4 | 100 | 0.857 | 32 | 100 | 0.107 |
| | EB | 4 | 100 | 0.857 | 32 | 100 | 0.107 |

Notes to Table 48:

(1) DCLK frequency of 100 MHz using external CLKUSR.

(2) Max FPGA FPP bandwidth may exceed bandwidth available from some external storage or control logic.

Fast Passive Parallel Configuration Timing

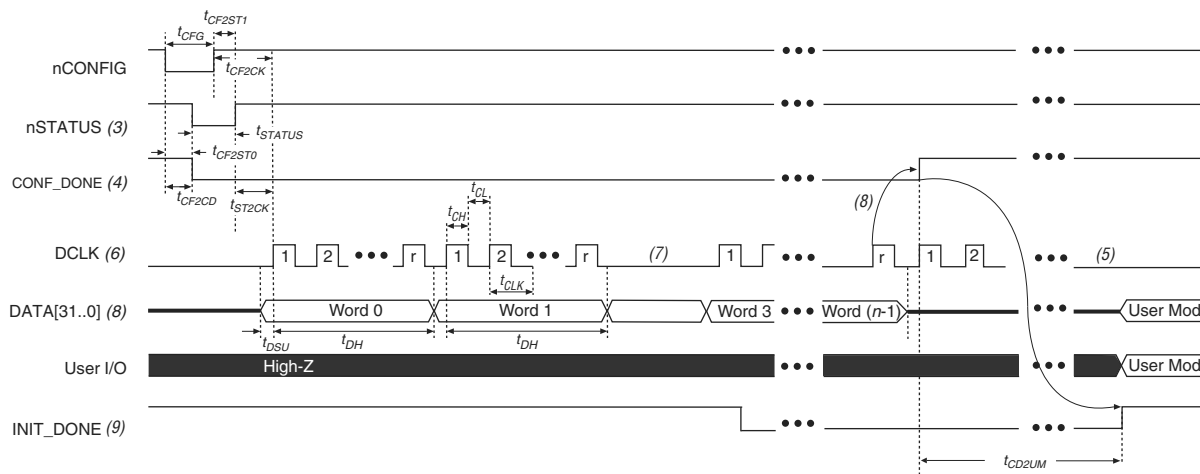
This section describes the fast passive parallel (FPP) configuration timing parameters for Stratix V devices.

DCLK-to-DATA[] Ratio for FPP Configuration

FPP configuration requires a different DCLK-to-DATA [] ratio when you enable the design security, decompression, or both features. Table 49 lists the DCLK-to-DATA [] ratio for each combination.

Table 49. DCLK-to-DATA[] Ratio ⁽¹⁾ (Part 1 of 2)

| Configuration Scheme | Decompression | Design Security | DCLK-to-DATA[] Ratio |
|----------------------|---------------|-----------------|----------------------|
| FPP ×8 | Disabled | Disabled | 1 |
| | Disabled | Enabled | 1 |
| | Enabled | Disabled | 2 |
| | Enabled | Enabled | 2 |
| FPP ×16 | Disabled | Disabled | 1 |
| | Disabled | Enabled | 2 |
| | Enabled | Disabled | 4 |
| | Enabled | Enabled | 4 |

Figure 13. FPP Configuration Timing Waveform When the DCLK-to-DATA[] Ratio is >1 (1), (2)**Notes to Figure 13:**

- (1) Use this timing waveform and parameters when the DCLK-to-DATA[] ratio is >1. To find out the DCLK-to-DATA[] ratio for your system, refer to Table 49 on page 55.
- (2) The beginning of this waveform shows the device in user mode. In user mode, nCONFIG, nSTATUS, and CONF_DONE are at logic high levels. When nCONFIG is pulled low, a reconfiguration cycle begins.
- (3) After power-up, the Stratix V device holds nSTATUS low for the time as specified by the POR delay.
- (4) After power-up, before and during configuration, CONF_DONE is low.
- (5) Do not leave DCLK floating after configuration. You can drive it high or low, whichever is more convenient.
- (6) "r" denotes the DCLK-to-DATA[] ratio. For the DCLK-to-DATA[] ratio based on the decompression and the design security feature enable settings, refer to Table 49 on page 55.
- (7) If needed, pause DCLK by holding it low. When DCLK restarts, the external host must provide data on the DATA[31..0] pins prior to sending the first DCLK rising edge.
- (8) To ensure a successful configuration, send the entire configuration data to the Stratix V device. CONF_DONE is released high after the Stratix V device receives all the configuration data successfully. After CONF_DONE goes high, send two additional falling edges on DCLK to begin initialization and enter user mode.
- (9) After the option bit to enable the INIT_DONE pin is configured into the device, the INIT_DONE goes low.

Document Revision History

Table 61 lists the revision history for this chapter.

Table 61. Document Revision History (Part 1 of 3)

| Date | Version | Changes |
|---------------|---------|---|
| June 2018 | 3.9 | <ul style="list-style-type: none"> Added the “Stratix V Device Overshoot Duration” figure. |
| April 2017 | 3.8 | <ul style="list-style-type: none"> Added a footnote to the “High-Speed I/O Specifications for Stratix V Devices” table. Changed the minimum value for t_{CD2UMC} in the “PS Timing Parameters for Stratix V Devices” table. Changed the condition for $100\text{-}\Omega$ R_D in the “OCT Without Calibration Resistance Tolerance Specifications for Stratix V Devices” table. Changed the minimum value for t_{CD2UMC} in the “AS Timing Parameters for AS ‘1 and AS ‘4 Configurations in Stratix V Devices” table Changed the minimum value for t_{CD2UMC} in the “FPP Timing Parameters for Stratix V Devices When the DCLK-to-DATA[] Ratio is >1” table. Changed the minimum value for t_{CD2UMC} in the “FPP Timing Parameters for Stratix V Devices When the DCLK-to-DATA[] Ratio is >1” table. Changed the minimum number of clock cycles value in the “Initialization Clock Source Option and the Maximum Frequency” table. |
| June 2016 | 3.7 | <ul style="list-style-type: none"> Added the V_{ID} minimum specification for LVPECL in the “Differential I/O Standard Specifications for Stratix V Devices” table Added the I_{OUT} specification to the “Absolute Maximum Ratings for Stratix V Devices” table. |
| December 2015 | 3.6 | <ul style="list-style-type: none"> Added a footnote to the “High-Speed I/O Specifications for Stratix V Devices” table. |
| December 2015 | 3.5 | <ul style="list-style-type: none"> Changed the transmitter, receiver, and ATX PLL data rate specifications in the “Transceiver Specifications for Stratix V GX and GS Devices” table. Changed the configuration .rbf sizes in the “Uncompressed .rbf Sizes for Stratix V Devices” table. |
| July 2015 | 3.4 | <ul style="list-style-type: none"> Changed the data rate specification for transceiver speed grade 3 in the following tables: <ul style="list-style-type: none"> “Transceiver Specifications for Stratix V GX and GS Devices” “Stratix V Standard PCS Approximate Maximum Date Rate” “Stratix V 10G PCS Approximate Maximum Data Rate” Changed the conditions for reference clock rise and fall time, and added a note to the “Transceiver Specifications for Stratix V GX and GS Devices” table. Added a note to the “Minimum differential eye opening at receiver serial input pins” specification in the “Transceiver Specifications for Stratix V GX and GS Devices” table. Changed the t_{CO} maximum value in the “AS Timing Parameters for AS ‘1 and AS ‘4 Configurations in Stratix V Devices” table. Removed the CDR ppm tolerance specification from the “Transceiver Specifications for Stratix V GX and GS Devices” table. |