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Understanding [Embedded - FPGAs \(Field Programmable Gate Array\)](#)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

| | |
|--------------------------------|---|
| Product Status | Obsolete |
| Number of LABs/CLBs | 185000 |
| Number of Logic Elements/Cells | 490000 |
| Total RAM Bits | 46080000 |
| Number of I/O | 696 |
| Number of Gates | - |
| Voltage - Supply | 0.82V ~ 0.88V |
| Mounting Type | Surface Mount |
| Operating Temperature | -40°C ~ 100°C (TJ) |
| Package / Case | 1517-BBGA, FCBGA |
| Supplier Device Package | 1517-FBGA (40x40) |
| Purchase URL | https://www.e-xfl.com/product-detail/intel/5sgxma5k3f40i4n |

Recommended Operating Conditions

This section lists the functional operating limits for the AC and DC parameters for Stratix V devices. Table 6 lists the steady-state voltage and current values expected from Stratix V devices. Power supply ramps must all be strictly monotonic, without plateaus.

Table 6. Recommended Operating Conditions for Stratix V Devices (Part 1 of 2)

| Symbol | Description | Condition | Min ⁽⁴⁾ | Typ | Max ⁽⁴⁾ | Unit |
|-----------------------------------|---|------------|--------------------|------|--------------------|------|
| V _{CC} | Core voltage and periphery circuitry power supply (C1, C2, I2, and I3YY speed grades) | — | 0.87 | 0.9 | 0.93 | V |
| | Core voltage and periphery circuitry power supply (C2L, C3, C4, I2L, I3, I3L, and I4 speed grades) ⁽³⁾ | — | 0.82 | 0.85 | 0.88 | V |
| V _{CCPT} | Power supply for programmable power technology | — | 1.45 | 1.50 | 1.55 | V |
| V _{CC_AUX} | Auxiliary supply for the programmable power technology | — | 2.375 | 2.5 | 2.625 | V |
| V _{CCPD} ⁽¹⁾ | I/O pre-driver (3.0 V) power supply | — | 2.85 | 3.0 | 3.15 | V |
| | I/O pre-driver (2.5 V) power supply | — | 2.375 | 2.5 | 2.625 | V |
| V _{CCIO} | I/O buffers (3.0 V) power supply | — | 2.85 | 3.0 | 3.15 | V |
| | I/O buffers (2.5 V) power supply | — | 2.375 | 2.5 | 2.625 | V |
| | I/O buffers (1.8 V) power supply | — | 1.71 | 1.8 | 1.89 | V |
| | I/O buffers (1.5 V) power supply | — | 1.425 | 1.5 | 1.575 | V |
| | I/O buffers (1.35 V) power supply | — | 1.283 | 1.35 | 1.45 | V |
| | I/O buffers (1.25 V) power supply | — | 1.19 | 1.25 | 1.31 | V |
| | I/O buffers (1.2 V) power supply | — | 1.14 | 1.2 | 1.26 | V |
| V _{CCPGM} | Configuration pins (3.0 V) power supply | — | 2.85 | 3.0 | 3.15 | V |
| | Configuration pins (2.5 V) power supply | — | 2.375 | 2.5 | 2.625 | V |
| | Configuration pins (1.8 V) power supply | — | 1.71 | 1.8 | 1.89 | V |
| V _{CCA_FPLL} | PLL analog voltage regulator power supply | — | 2.375 | 2.5 | 2.625 | V |
| V _{CCD_FPLL} | PLL digital voltage regulator power supply | — | 1.45 | 1.5 | 1.55 | V |
| V _{CCBAT} ⁽²⁾ | Battery back-up power supply (For design security volatile key register) | — | 1.2 | — | 3.0 | V |
| V _I | DC input voltage | — | −0.5 | — | 3.6 | V |
| V _O | Output voltage | — | 0 | — | V _{CCIO} | V |
| T _J | Operating junction temperature | Commercial | 0 | — | 85 | °C |
| | | Industrial | −40 | — | 100 | °C |

Table 7. Recommended Transceiver Power Supply Operating Conditions for Stratix V GX, GS, and GT Devices (Part 2 of 2)

| Symbol | Description | Devices | Minimum ⁽⁴⁾ | Typical | Maximum ⁽⁴⁾ | Unit |
|------------------------|--|------------|------------------------|---------|------------------------|------|
| V_{CCR_GXBR} (2) | Receiver analog power supply (right side) | GX, GS, GT | 0.82 | 0.85 | 0.88 | V |
| | | | 0.87 | 0.90 | 0.93 | |
| | | | 0.97 | 1.0 | 1.03 | |
| | | | 1.03 | 1.05 | 1.07 | |
| V_{CCR_GTBR} | Receiver analog power supply for GT channels (right side) | GT | 1.02 | 1.05 | 1.08 | V |
| V_{CCT_GXBL} (2) | Transmitter analog power supply (left side) | GX, GS, GT | 0.82 | 0.85 | 0.88 | V |
| | | | 0.87 | 0.90 | 0.93 | |
| | | | 0.97 | 1.0 | 1.03 | |
| | | | 1.03 | 1.05 | 1.07 | |
| V_{CCT_GXBR} (2) | Transmitter analog power supply (right side) | GX, GS, GT | 0.82 | 0.85 | 0.88 | V |
| | | | 0.87 | 0.90 | 0.93 | |
| | | | 0.97 | 1.0 | 1.03 | |
| | | | 1.03 | 1.05 | 1.07 | |
| V_{CCT_GTBR} | Transmitter analog power supply for GT channels (right side) | GT | 1.02 | 1.05 | 1.08 | V |
| V_{CCL_GTBR} | Transmitter clock network power supply | GT | 1.02 | 1.05 | 1.08 | V |
| V_{CCH_GXBL} | Transmitter output buffer power supply (left side) | GX, GS, GT | 1.425 | 1.5 | 1.575 | V |
| V_{CCH_GXBR} | Transmitter output buffer power supply (right side) | GX, GS, GT | 1.425 | 1.5 | 1.575 | V |

Notes to Table 7:

- (1) This supply must be connected to 3.0 V if the CMU PLL, receiver CDR, or both, are configured at a base data rate > 6.5 Gbps. Up to 6.5 Gbps, you can connect this supply to either 3.0 V or 2.5 V.
- (2) Refer to Table 8 to select the correct power supply level for your design.
- (3) When using ATX PLLs, the supply must be 3.0 V.
- (4) This value describes the budget for the DC (static) power supply tolerance and does not include the dynamic tolerance requirements. Refer to the PDN tool for the additional budget for the dynamic tolerance requirements.

I/O Pin Leakage Current

Table 9 lists the Stratix V I/O pin leakage current specifications.

Table 9. I/O Pin Leakage Current for Stratix V Devices ⁽¹⁾

| Symbol | Description | Conditions | Min | Typ | Max | Unit |
|----------|--------------------|--|-----|-----|-----|---------------|
| I_I | Input pin | $V_I = 0 \text{ V to } V_{CCIO\text{MAX}}$ | -30 | — | 30 | μA |
| I_{OZ} | Tri-stated I/O pin | $V_O = 0 \text{ V to } V_{CCIO\text{MAX}}$ | -30 | — | 30 | μA |

Note to Table 9:

(1) If $V_O = V_{CCIO}$ to $V_{CCIO\text{MAX}}$, 100 μA of leakage current per I/O is expected.

Bus Hold Specifications

Table 10 lists the Stratix V device family bus hold specifications.

Table 10. Bus Hold Parameters for Stratix V Devices

| Parameter | Symbol | Conditions | V _{CCIO} | | | | | | | | | | Unit |
|-------------------------|-------------------|--|-------------------|------|-------|------|-------|------|-------|------|-------|------|------|
| | | | 1.2 V | | 1.5 V | | 1.8 V | | 2.5 V | | 3.0 V | | |
| | | | Min | Max | Min | Max | Min | Max | Min | Max | Min | Max | |
| Low sustaining current | I _{SUSL} | V _{IN} > V _{IL} (maximum) | 22.5 | — | 25.0 | — | 30.0 | — | 50.0 | — | 70.0 | — | μA |
| High sustaining current | I _{SUSH} | V _{IN} < V _{IH} (minimum) | −22.5 | — | −25.0 | — | −30.0 | — | −50.0 | — | −70.0 | — | μA |
| Low overdrive current | I _{ODL} | 0V < V _{IN} < V _{CCIO} | — | 120 | — | 160 | — | 200 | — | 300 | — | 500 | μA |
| High overdrive current | I _{ODH} | 0V < V _{IN} < V _{CCIO} | — | −120 | — | −160 | — | −200 | — | −300 | — | −500 | μA |
| Bus-hold trip point | V _{TRIP} | — | 0.45 | 0.95 | 0.50 | 1.00 | 0.68 | 1.07 | 0.70 | 1.70 | 0.80 | 2.00 | V |

On-Chip Termination (OCT) Specifications

If you enable OCT calibration, calibration is automatically performed at power-up for I/Os connected to the calibration block. Table 11 lists the Stratix V OCT termination calibration accuracy specifications.

Table 11. OCT Calibration Accuracy Specifications for Stratix V Devices ⁽¹⁾ (Part 1 of 2)

| Symbol | Description | Conditions | Calibration Accuracy | | | | Unit |
|--------------------|---|---|----------------------|----------|----------------|----------|------|
| | | | C1 | C2,I2 | C3,I3, I3YY | C4,I4 | |
| 25- Ω R_S | Internal series termination with calibration (25- Ω setting) | $V_{\text{CCIO}} = 3.0, 2.5, 1.8, 1.5, 1.2 \text{ V}$ | ± 15 | ± 15 | ± 15 | ± 15 | % |

Internal Weak Pull-Up Resistor

Table 16 lists the weak pull-up resistor values for Stratix V devices.

Table 16. Internal Weak Pull-Up Resistor for Stratix V Devices ^{(1), (2)}

| Symbol | Description | V _{CCIO} Conditions (V) ⁽³⁾ | Value ⁽⁴⁾ | Unit |
|-----------------|---|---|----------------------|------|
| R _{PU} | Value of the I/O pin pull-up resistor before and during configuration, as well as user mode if you enable the programmable pull-up resistor option. | 3.0 ±5% | 25 | kΩ |
| | | 2.5 ±5% | 25 | kΩ |
| | | 1.8 ±5% | 25 | kΩ |
| | | 1.5 ±5% | 25 | kΩ |
| | | 1.35 ±5% | 25 | kΩ |
| | | 1.25 ±5% | 25 | kΩ |
| | | 1.2 ±5% | 25 | kΩ |

Notes to Table 16:

- (1) All I/O pins have an option to enable the weak pull-up resistor except the configuration, test, and JTAG pins.
- (2) The internal weak pull-down feature is only available for the JTAG TCK pin. The typical value for this internal weak pull-down resistor is approximately 25 kΩ.
- (3) The pin pull-up resistance values may be lower if an external source drives the pin higher than V_{CCIO}.
- (4) These specifications are valid with a ±10% tolerance to cover changes over PVT.

I/O Standard Specifications

Table 17 through Table 22 list the input voltage (V_{IH} and V_{IL}), output voltage (V_{OH} and V_{OL}), and current drive characteristics (I_{OH} and I_{OL}) for various I/O standards supported by Stratix V devices. These tables also show the Stratix V device family I/O standard specifications. The V_{OL} and V_{OH} values are valid at the corresponding I_{OH} and I_{OL}, respectively.

For an explanation of the terms used in Table 17 through Table 22, refer to “Glossary” on page 65. For tolerance calculations across all SSTL and HSTL I/O standards, refer to Altera knowledge base solution rd07262012_486.

Table 17. Single-Ended I/O Standards for Stratix V Devices

| I/O Standard | V _{CCIO} (V) | | | V _{IL} (V) | | V _{IH} (V) | | V _{OL} (V) | V _{OH} (V) | I _{OL} (mA) | I _{OH} (mA) |
|--------------|-----------------------|-----|-------|---------------------|-----------------------------|-----------------------------|-------------------------|-----------------------------|-----------------------------|----------------------|----------------------|
| | Min | Typ | Max | Min | Max | Min | Max | Max | Min | | |
| LVTTTL | 2.85 | 3 | 3.15 | −0.3 | 0.8 | 1.7 | 3.6 | 0.4 | 2.4 | 2 | −2 |
| LVC MOS | 2.85 | 3 | 3.15 | −0.3 | 0.8 | 1.7 | 3.6 | 0.2 | V _{CCIO} − 0.2 | 0.1 | −0.1 |
| 2.5 V | 2.375 | 2.5 | 2.625 | −0.3 | 0.7 | 1.7 | 3.6 | 0.4 | 2 | 1 | −1 |
| 1.8 V | 1.71 | 1.8 | 1.89 | −0.3 | 0.35 * V _{CCIO} | 0.65 * V _{CCIO} | V _{CCIO} + 0.3 | 0.45 | V _{CCIO} − 0.45 | 2 | −2 |
| 1.5 V | 1.425 | 1.5 | 1.575 | −0.3 | 0.35 * V _{CCIO} | 0.65 * V _{CCIO} | V _{CCIO} + 0.3 | 0.25 * V _{CCIO} | 0.75 * V _{CCIO} | 2 | −2 |
| 1.2 V | 1.14 | 1.2 | 1.26 | −0.3 | 0.35 * V _{CCIO} | 0.65 * V _{CCIO} | V _{CCIO} + 0.3 | 0.25 * V _{CCIO} | 0.75 * V _{CCIO} | 2 | −2 |

Table 25 shows the approximate maximum data rate using the standard PCS.

Table 25. Stratix V Standard PCS Approximate Maximum Date Rate ⁽¹⁾, ⁽³⁾

| Mode ⁽²⁾ | Transceiver Speed Grade | PMA Width | 20 | 20 | 16 | 16 | 10 | 10 | 8 | 8 |
|---------------------|-------------------------|---------------------------------------|---------|---------|---------|---------|-----|-----|------|------|
| | | PCS/Core Width | 40 | 20 | 32 | 16 | 20 | 10 | 16 | 8 |
| FIFO | 1 | C1, C2, C2L, I2, I2L core speed grade | 12.2 | 11.4 | 9.76 | 9.12 | 6.5 | 5.8 | 5.2 | 4.72 |
| | 2 | C1, C2, C2L, I2, I2L core speed grade | 12.2 | 11.4 | 9.76 | 9.12 | 6.5 | 5.8 | 5.2 | 4.72 |
| | | C3, I3, I3L core speed grade | 9.8 | 9.0 | 7.84 | 7.2 | 5.3 | 4.7 | 4.24 | 3.76 |
| | 3 | C1, C2, C2L, I2, I2L core speed grade | 8.5 | 8.5 | 8.5 | 8.5 | 6.5 | 5.8 | 5.2 | 4.72 |
| | | I3YY core speed grade | 10.3125 | 10.3125 | 7.84 | 7.2 | 5.3 | 4.7 | 4.24 | 3.76 |
| | | C3, I3, I3L core speed grade | 8.5 | 8.5 | 7.84 | 7.2 | 5.3 | 4.7 | 4.24 | 3.76 |
| | | C4, I4 core speed grade | 8.5 | 8.2 | 7.04 | 6.56 | 4.8 | 4.2 | 3.84 | 3.44 |
| Register | 1 | C1, C2, C2L, I2, I2L core speed grade | 12.2 | 11.4 | 9.76 | 9.12 | 6.1 | 5.7 | 4.88 | 4.56 |
| | 2 | C1, C2, C2L, I2, I2L core speed grade | 12.2 | 11.4 | 9.76 | 9.12 | 6.1 | 5.7 | 4.88 | 4.56 |
| | | C3, I3, I3L core speed grade | 9.8 | 9.0 | 7.92 | 7.2 | 4.9 | 4.5 | 3.96 | 3.6 |
| | 3 | C1, C2, C2L, I2, I2L core speed grade | 10.3125 | 10.3125 | 10.3125 | 10.3125 | 6.1 | 5.7 | 4.88 | 4.56 |
| | | I3YY core speed grade | 10.3125 | 10.3125 | 7.92 | 7.2 | 4.9 | 4.5 | 3.96 | 3.6 |
| | | C3, I3, I3L core speed grade | 8.5 | 8.5 | 7.92 | 7.2 | 4.9 | 4.5 | 3.96 | 3.6 |
| | | C4, I4 core speed grade | 8.5 | 8.2 | 7.04 | 6.56 | 4.4 | 4.1 | 3.52 | 3.28 |

Notes to Table 25:

- (1) The maximum data rate is in Gbps.
- (2) The Phase Compensation FIFO can be configured in FIFO mode or register mode. In the FIFO mode, the pointers are not fixed, and the latency can vary. In the register mode the pointers are fixed for low latency.
- (3) The maximum data rate is also constrained by the transceiver speed grade. Refer to Table 1 for the transceiver speed grade.

Table 28. Transceiver Specifications for Stratix V GT Devices (Part 4 of 5) ⁽¹⁾

| Symbol/ Description | Conditions | Transceiver Speed Grade 2 | | | Transceiver Speed Grade 3 | | | Unit |
|--|--|------------------------------|-----|--------------------------------|------------------------------|-----|--------------------------------|------|
| | | Min | Typ | Max | Min | Typ | Max | |
| Data rate | GT channels | 19,600 | — | 28,050 | 19,600 | — | 25,780 | Mbps |
| Differential on-chip termination resistors | GT channels | — | 100 | — | — | 100 | — | Ω |
| | GX channels | (8) | | | | | | |
| V _{OCM} (AC coupled) | GT channels | — | 500 | — | — | 500 | — | mV |
| | GX channels | (8) | | | | | | |
| Rise/Fall time | GT channels | — | 15 | — | — | 15 | — | ps |
| | GX channels | (8) | | | | | | |
| Intra-differential pair skew | GX channels | (8) | | | | | | |
| Intra-transceiver block transmitter channel-to- channel skew | GX channels | (8) | | | | | | |
| Inter-transceiver block transmitter channel-to- channel skew | GX channels | (8) | | | | | | |
| CMU PLL | | | | | | | | |
| Supported Data Range | — | 600 | — | 12500 | 600 | — | 8500 | Mbps |
| t _{pll_powerdown} ⁽¹³⁾ | — | 1 | — | — | 1 | — | — | μs |
| t _{pll_lock} ⁽¹⁴⁾ | — | — | — | 10 | — | — | 10 | μs |
| ATX PLL | | | | | | | | |
| Supported Data Rate Range for GX Channels | VCO post- divider L=2 | 8000 | — | 12500 | 8000 | — | 8500 | Mbps |
| | L=4 | 4000 | — | 6600 | 4000 | — | 6600 | Mbps |
| | L=8 | 2000 | — | 3300 | 2000 | — | 3300 | Mbps |
| | L=8, Local/Central Clock Divider =2 | 1000 | — | 1762.5 | 1000 | — | 1762.5 | Mbps |
| Supported Data Rate Range for GT Channels | VCO post- divider L=2 | 9800 | — | 14025 | 9800 | — | 12890 | Mbps |
| t _{pll_powerdown} ⁽¹³⁾ | — | 1 | — | — | 1 | — | — | μs |
| t _{pll_lock} ⁽¹⁴⁾ | — | — | — | 10 | — | — | 10 | μs |
| fPLL | | | | | | | | |
| Supported Data Range | — | 600 | — | 3250/ 3.125 ⁽²³⁾ | 600 | — | 3250/ 3.125 ⁽²³⁾ | Mbps |
| t _{pll_powerdown} ⁽¹³⁾ | — | 1 | — | — | 1 | — | — | μs |

Table 28. Transceiver Specifications for Stratix V GT Devices (Part 5 of 5) ⁽¹⁾

| Symbol/ Description | Conditions | Transceiver Speed Grade 2 | | | Transceiver Speed Grade 3 | | | Unit |
|---------------------------------|------------|------------------------------|-----|-----|------------------------------|-----|-----|------|
| | | Min | Typ | Max | Min | Typ | Max | |
| t_{pll_lock} ⁽¹⁴⁾ | — | — | — | 10 | — | — | 10 | μs |

Notes to Table 28:

- (1) Speed grades shown refer to the PMA Speed Grade in the device ordering code. The maximum data rate could be restricted by the Core/PCS speed grade. Contact your Altera Sales Representative for the maximum data rate specifications in each speed grade combination offered. For more information about device ordering codes, refer to the *Stratix V Device Overview*.
- (2) The reference clock common mode voltage is equal to the VCCR_GXB power supply level.
- (3) The device cannot tolerate prolonged operation at this absolute maximum.
- (4) The differential eye opening specification at the receiver input pins assumes that receiver equalization is disabled. If you enable receiver equalization, the receiver circuitry can tolerate a lower minimum eye opening, depending on the equalization level.
- (5) Refer to Figure 5 for the GT channel AC gain curves. The total effective AC gain is the AC gain minus the DC gain.
- (6) Refer to Figure 6 for the GT channel DC gain curves.
- (7) CFP2 optical modules require the host interface to have the receiver data pins differentially terminated with 100 Ω. The internal OCT feature is available after the Stratix V FPGA configuration is completed. Altera recommends that FPGA configuration is completed before inserting the optical module. Otherwise, minimize unnecessary removal and insertion with unconfigured devices.
- (8) Specifications for this parameter are the same as for Stratix V GX and GS devices. See Table 23 for specifications.
- (9) t_{LTR} is the time required for the receive CDR to lock to the input reference clock frequency after coming out of reset.
- (10) t_{LTD} is time required for the receiver CDR to start recovering valid data after the $rx_is_lockedto\ data$ signal goes high.
- (11) t_{LTD_manual} is the time required for the receiver CDR to start recovering valid data after the $rx_is_lockedto\ data$ signal goes high when the CDR is functioning in the manual mode.
- (12) $t_{LTR_LTD_manual}$ is the time the receiver CDR must be kept in lock to reference (LTR) mode after the $rx_is_lockedto\ ref$ signal goes high when the CDR is functioning in the manual mode.
- (13) $tp11_powerdown$ is the PLL powerdown minimum pulse width.
- (14) $tp11_lock$ is the time required for the transmitter CMU/ATX PLL to lock to the input reference clock frequency after coming out of reset.
- (15) To calculate the REFCLK rms phase jitter requirement for PCIe at reference clock frequencies other than 100 MHz, use the following formula:
REFCLK rms phase jitter at f(MHz) = REFCLK rms phase jitter at 100 MHz × 100/f.
- (16) The maximum peak to peak differential input voltage V_{ID} after device configuration is equal to $4 \times (\text{absolute } V_{MAX} \text{ for receiver pin} - V_{ICM})$.
- (17) For ES devices, RREF is 2000 Ω ±1%.
- (18) To calculate the REFCLK phase noise requirement at frequencies other than 622 MHz, use the following formula: REFCLK phase noise at f(MHz) = REFCLK phase noise at 622 MHz + 20*log(f/622).
- (19) SFP/+ optical modules require the host interface to have RD+/- differentially terminated with 100 Ω. The internal OCT feature is available after the Stratix V FPGA configuration is completed. Altera recommends that FPGA configuration is completed before inserting the optical module. Otherwise, minimize unnecessary removal and insertion with unconfigured devices.
- (20) Refer to Figure 4.
- (21) For oversampling design to support data rates less than the minimum specification, the CDR needs to be in LTR mode only.
- (22) This supply follows VCCR_GXB for both GX and GT channels.
- (23) When you use fPLL as a TXPLL of the transceiver.

Table 29 shows the V_{OD} settings for the GT channel.

Table 29. Typical V_{OD} Setting for GT Channel, TX Termination = 100 Ω

| Symbol | V_{OD} Setting | V_{OD} Value (mV) |
|---|------------------|---------------------|
| V_{OD} differential peak to peak typical ⁽¹⁾ | 0 | 0 |
| | 1 | 200 |
| | 2 | 400 |
| | 3 | 600 |
| | 4 | 800 |
| | 5 | 1000 |

Note:

(1) Refer to Figure 4.

Table 31. PLL Specifications for Stratix V Devices (Part 2 of 3)

| Symbol | Parameter | Min | Typ | Max | Unit |
|--|--|------|---------|--|-----------|
| t_{INCCJ} ^{(3), (4)} | Input clock cycle-to-cycle jitter ($f_{\text{REF}} \geq 100$ MHz) | — | — | 0.15 | UI (p-p) |
| | Input clock cycle-to-cycle jitter ($f_{\text{REF}} < 100$ MHz) | −750 | — | +750 | ps (p-p) |
| $t_{\text{OUTPJ_DC}}$ ⁽⁵⁾ | Period Jitter for dedicated clock output ($f_{\text{OUT}} \geq 100$ MHz) | — | — | 175 ⁽¹⁾ | ps (p-p) |
| | Period Jitter for dedicated clock output ($f_{\text{OUT}} < 100$ MHz) | — | — | 17.5 ⁽¹⁾ | mUI (p-p) |
| $t_{\text{FOUTPJ_DC}}$ ⁽⁵⁾ | Period Jitter for dedicated clock output in fractional PLL ($f_{\text{OUT}} \geq 100$ MHz) | — | — | 250 ⁽¹¹⁾ , 175 ⁽¹²⁾ | ps (p-p) |
| | Period Jitter for dedicated clock output in fractional PLL ($f_{\text{OUT}} < 100$ MHz) | — | — | 25 ⁽¹¹⁾ , 17.5 ⁽¹²⁾ | mUI (p-p) |
| $t_{\text{OUTCCJ_DC}}$ ⁽⁵⁾ | Cycle-to-Cycle Jitter for a dedicated clock output ($f_{\text{OUT}} \geq 100$ MHz) | — | — | 175 | ps (p-p) |
| | Cycle-to-Cycle Jitter for a dedicated clock output ($f_{\text{OUT}} < 100$ MHz) | — | — | 17.5 | mUI (p-p) |
| $t_{\text{FOUTCCJ_DC}}$ ⁽⁵⁾ | Cycle-to-cycle Jitter for a dedicated clock output in fractional PLL ($f_{\text{OUT}} \geq 100$ MHz) | — | — | 250 ⁽¹¹⁾ , 175 ⁽¹²⁾ | ps (p-p) |
| | Cycle-to-cycle Jitter for a dedicated clock output in fractional PLL ($f_{\text{OUT}} < 100$ MHz)+ | — | — | 25 ⁽¹¹⁾ , 17.5 ⁽¹²⁾ | mUI (p-p) |
| $t_{\text{OUTPJ_IO}}$ ^{(5), (8)} | Period Jitter for a clock output on a regular I/O in integer PLL ($f_{\text{OUT}} \geq 100$ MHz) | — | — | 600 | ps (p-p) |
| | Period Jitter for a clock output on a regular I/O ($f_{\text{OUT}} < 100$ MHz) | — | — | 60 | mUI (p-p) |
| $t_{\text{FOUTPJ_IO}}$ ^{(5), (8), (11)} | Period Jitter for a clock output on a regular I/O in fractional PLL ($f_{\text{OUT}} \geq 100$ MHz) | — | — | 600 ⁽¹⁰⁾ | ps (p-p) |
| | Period Jitter for a clock output on a regular I/O in fractional PLL ($f_{\text{OUT}} < 100$ MHz) | — | — | 60 ⁽¹⁰⁾ | mUI (p-p) |
| $t_{\text{OUTCCJ_IO}}$ ^{(5), (8)} | Cycle-to-cycle Jitter for a clock output on a regular I/O in integer PLL ($f_{\text{OUT}} \geq 100$ MHz) | — | — | 600 | ps (p-p) |
| | Cycle-to-cycle Jitter for a clock output on a regular I/O in integer PLL ($f_{\text{OUT}} < 100$ MHz) | — | — | 60 ⁽¹⁰⁾ | mUI (p-p) |
| $t_{\text{FOUTCCJ_IO}}$ ^{(5), (8), (11)} | Cycle-to-cycle Jitter for a clock output on a regular I/O in fractional PLL ($f_{\text{OUT}} \geq 100$ MHz) | — | — | 600 ⁽¹⁰⁾ | ps (p-p) |
| | Cycle-to-cycle Jitter for a clock output on a regular I/O in fractional PLL ($f_{\text{OUT}} < 100$ MHz) | — | — | 60 | mUI (p-p) |
| $t_{\text{CASC_OUTPJ_DC}}$ ^{(5), (6)} | Period Jitter for a dedicated clock output in cascaded PLLs ($f_{\text{OUT}} \geq 100$ MHz) | — | — | 175 | ps (p-p) |
| | Period Jitter for a dedicated clock output in cascaded PLLs ($f_{\text{OUT}} < 100$ MHz) | — | — | 17.5 | mUI (p-p) |
| f_{DRIFT} | Frequency drift after PFDENA is disabled for a duration of 100 μ s | — | — | ± 10 | % |
| dK_{BIT} | Bit number of Delta Sigma Modulator (DSM) | 8 | 24 | 32 | Bits |
| K_{VALUE} | Numerator of Fraction | 128 | 8388608 | 2147483648 | — |

Table 33. Memory Block Performance Specifications for Stratix V Devices ^{(1), (2)} (Part 2 of 2)

| Memory | Mode | Resources Used | | Performance | | | | | | | Unit |
|------------|--|----------------|--------|-------------|---------|-----|-----|---------|---------------|-----|------|
| | | ALUTs | Memory | C1 | C2, C2L | C3 | C4 | I2, I2L | I3, I3L, I3YY | I4 | |
| M20K Block | Single-port, all supported widths | 0 | 1 | 700 | 700 | 650 | 550 | 700 | 500 | 450 | MHz |
| | Simple dual-port, all supported widths | 0 | 1 | 700 | 700 | 650 | 550 | 700 | 500 | 450 | MHz |
| | Simple dual-port with the read-during-write option set to Old Data , all supported widths | 0 | 1 | 525 | 525 | 455 | 400 | 525 | 455 | 400 | MHz |
| | Simple dual-port with ECC enabled, 512 × 32 | 0 | 1 | 450 | 450 | 400 | 350 | 450 | 400 | 350 | MHz |
| | Simple dual-port with ECC and optional pipeline registers enabled, 512 × 32 | 0 | 1 | 600 | 600 | 500 | 450 | 600 | 500 | 450 | MHz |
| | True dual port, all supported widths | 0 | 1 | 700 | 700 | 650 | 550 | 700 | 500 | 450 | MHz |
| | ROM, all supported widths | 0 | 1 | 700 | 700 | 650 | 550 | 700 | 500 | 450 | MHz |

Notes to Table 33:

- (1) To achieve the maximum memory block performance, use a memory block clock that comes through global clock routing from an on-chip PLL set to **50%** output duty cycle. Use the Quartus II software to report timing for this and other memory block clocking schemes.
- (2) When you use the error detection cyclical redundancy check (CRC) feature, there is no degradation in F_{MAX}.
- (3) The F_{MAX} specification is only achievable with Fitter options, **MLAB Implementation In 16-Bit Deep Mode** enabled.

Temperature Sensing Diode Specifications

Table 34 lists the internal TSD specification.

Table 34. Internal Temperature Sensing Diode Specification

| Temperature Range | Accuracy | Offset Calibrated Option | Sampling Rate | Conversion Time | Resolution | Minimum Resolution with no Missing Codes |
|-------------------|----------|--------------------------|----------------|-----------------|------------|--|
| –40°C to 100°C | ±8°C | No | 1 MHz, 500 KHz | < 100 ms | 8 bits | 8 bits |

Table 35 lists the specifications for the Stratix V external temperature sensing diode.

Table 35. External Temperature Sensing Diode Specifications for Stratix V Devices

| Description | Min | Typ | Max | Unit |
|--|-------|-------|-------|------|
| I _{bias} , diode source current | 8 | — | 200 | μA |
| V _{bias} , voltage across diode | 0.3 | — | 0.9 | V |
| Series resistance | — | — | < 1 | Ω |
| Diode ideality factor | 1.006 | 1.008 | 1.010 | — |

Table 36. High-Speed I/O Specifications for Stratix V Devices ^{(1), (2)} (Part 2 of 4)

| Symbol | Conditions | C1 | | | C2, C2L, I2, I2L | | | C3, I3, I3L, I3YY | | | C4,I4 | | | Unit |
|--|---|-----|-----|------|------------------|-----|------|-------------------|-----|------|-------|-----|------|------|
| | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| Transmitter | | | | | | | | | | | | | | |
| True Differential I/O Standards - f _{HSDR} (data rate) | SERDES factor J = 3 to 10 ^{(9), (11), (12), (13), (14), (15), (16)} | (6) | — | 1600 | (6) | — | 1434 | (6) | — | 1250 | (6) | — | 1050 | Mbps |
| | SERDES factor J ≥ 4 LVDS TX with DPA ^{(12), (14), (15), (16)} | (6) | — | 1600 | (6) | — | 1600 | (6) | — | 1600 | (6) | — | 1250 | Mbps |
| | SERDES factor J = 2, uses DDR Registers | (6) | — | (7) | (6) | — | (7) | (6) | — | (7) | (6) | — | (7) | Mbps |
| | SERDES factor J = 1, uses SDR Register | (6) | — | (7) | (6) | — | (7) | (6) | — | (7) | (6) | — | (7) | Mbps |
| Emulated Differential I/O Standards with Three External Output Resistor Networks - f _{HSDR} (data rate) ⁽¹⁰⁾ | SERDES factor J = 4 to 10 ⁽¹⁷⁾ | (6) | — | 1100 | (6) | — | 1100 | (6) | — | 840 | (6) | — | 840 | Mbps |
| t _{x Jitter} - True Differential I/O Standards | Total Jitter for Data Rate 600 Mbps - 1.25 Gbps | — | — | 160 | — | — | 160 | — | — | 160 | — | — | 160 | ps |
| | Total Jitter for Data Rate < 600 Mbps | — | — | 0.1 | — | — | 0.1 | — | — | 0.1 | — | — | 0.1 | UI |
| t _{x Jitter} - Emulated Differential I/O Standards with Three External Output Resistor Network | Total Jitter for Data Rate 600 Mbps - 1.25 Gbps | — | — | 300 | — | — | 300 | — | — | 300 | — | — | 325 | ps |
| | Total Jitter for Data Rate < 600 Mbps | — | — | 0.2 | — | — | 0.2 | — | — | 0.2 | — | — | 0.25 | UI |

Table 36. High-Speed I/O Specifications for Stratix V Devices ^{(1), (2)} (Part 3 of 4)

| Symbol | Conditions | C1 | | | C2, C2L, I2, I2L | | | C3, I3, I3L, I3YY | | | C4, I4 | | | Unit |
|--|---|----------------|-----|----------------|------------------|-----|----------------|-------------------|-----|----------------|----------------|-----|----------------|------|
| | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| t_{DUTY} | Transmitter output clock duty cycle for both True and Emulated Differential I/O Standards | 45 | 50 | 55 | 45 | 50 | 55 | 45 | 50 | 55 | 45 | 50 | 55 | % |
| t_{RISE} & t_{FALL} | True Differential I/O Standards | — | — | 160 | — | — | 160 | — | — | 200 | — | — | 200 | ps |
| | Emulated Differential I/O Standards with three external output resistor networks | — | — | 250 | — | — | 250 | — | — | 250 | — | — | 300 | ps |
| TCCS | True Differential I/O Standards | — | — | 150 | — | — | 150 | — | — | 150 | — | — | 150 | ps |
| | Emulated Differential I/O Standards | — | — | 300 | — | — | 300 | — | — | 300 | — | — | 300 | ps |
| Receiver | | | | | | | | | | | | | | |
| True Differential I/O Standards - f_{HSDRDP} (data rate) | SERDES factor J = 3 to 10 ^{(11), (12), (13), (14), (15), (16)} | 150 | — | 1434 | 150 | — | 1434 | 150 | — | 1250 | 150 | — | 1050 | Mbps |
| | SERDES factor J ≥ 4 | 150 | — | 1600 | 150 | — | 1600 | 150 | — | 1600 | 150 | — | 1250 | Mbps |
| | LVDS RX with DPA ^{(12), (14), (15), (16)} | 150 | — | 1600 | 150 | — | 1600 | 150 | — | 1600 | 150 | — | 1250 | Mbps |
| | SERDES factor J = 2, uses DDR Registers | ⁽⁶⁾ | — | ⁽⁷⁾ | ⁽⁶⁾ | — | ⁽⁷⁾ | ⁽⁶⁾ | — | ⁽⁷⁾ | ⁽⁶⁾ | — | ⁽⁷⁾ | Mbps |
| | SERDES factor J = 1, uses SDR Register | ⁽⁶⁾ | — | ⁽⁷⁾ | ⁽⁶⁾ | — | ⁽⁷⁾ | ⁽⁶⁾ | — | ⁽⁷⁾ | ⁽⁶⁾ | — | ⁽⁷⁾ | Mbps |

Figure 7 shows the dynamic phase alignment (DPA) lock time specifications with the DPA PLL calibration option enabled.

Figure 7. DPA Lock Time Specification with DPA PLL Calibration Enabled



Table 37 lists the DPA lock time specifications for Stratix V devices.

Table 37. DPA Lock Time Specifications for Stratix V GX Devices Only ^{(1), (2), (3)}

| Standard | Training Pattern | Number of Data Transitions in One Repetition of the Training Pattern | Number of Repetitions per 256 Data Transitions ⁽⁴⁾ | Maximum |
|--------------------|----------------------|--|---|----------------------|
| SPI-4 | 00000000001111111111 | 2 | 128 | 640 data transitions |
| Parallel Rapid I/O | 00001111 | 2 | 128 | 640 data transitions |
| | 10010000 | 4 | 64 | 640 data transitions |
| Miscellaneous | 10101010 | 8 | 32 | 640 data transitions |
| | 01010101 | 8 | 32 | 640 data transitions |

Notes to Table 37:

- (1) The DPA lock time is for one channel.
- (2) One data transition is defined as a 0-to-1 or 1-to-0 transition.
- (3) The DPA lock time stated in this table applies to both commercial and industrial grade.
- (4) This is the number of repetitions for the stated training pattern to achieve the 256 data transitions.

Figure 8 shows the LVDS soft-clock data recovery (CDR)/DPA sinusoidal jitter tolerance specification for a data rate ≥ 1.25 Gbps. Table 38 lists the LVDS soft-CDR/DPA sinusoidal jitter tolerance specification for a data rate ≥ 1.25 Gbps.

Figure 8. LVDS Soft-CDR/DPA Sinusoidal Jitter Tolerance Specification for a Data Rate ≥ 1.25 Gbps



Table 46. JTAG Timing Parameters and Values for Stratix V Devices

| Symbol | Description | Min | Max | Unit |
|------------|--|-----|-------------------|------|
| t_{JPH} | JTAG port hold time | 5 | — | ns |
| t_{JPCO} | JTAG port clock to output | — | 11 ⁽¹⁾ | ns |
| t_{JPZX} | JTAG port high impedance to valid output | — | 14 ⁽¹⁾ | ns |
| t_{JPXZ} | JTAG port valid output to high impedance | — | 14 ⁽¹⁾ | ns |

Notes to Table 46:

- (1) A 1 ns adder is required for each V_{CCIO} voltage step down from 3.0 V. For example, t_{JPCO} = 12 ns if V_{CCIO} of the TDO I/O bank = 2.5 V, or 13 ns if it equals 1.8 V.
- (2) The minimum TCK clock period is 167 ns if VCCBAT is within the range 1.2V-1.5V when you perform the volatile key programming.

Raw Binary File Size

For the POR delay specification, refer to the “POR Delay Specification” section of the “Configuration, Design Security, and Remote System Upgrades in Stratix V Devices”.

Table 47 lists the uncompressed raw binary file (.rbf) sizes for Stratix V devices.

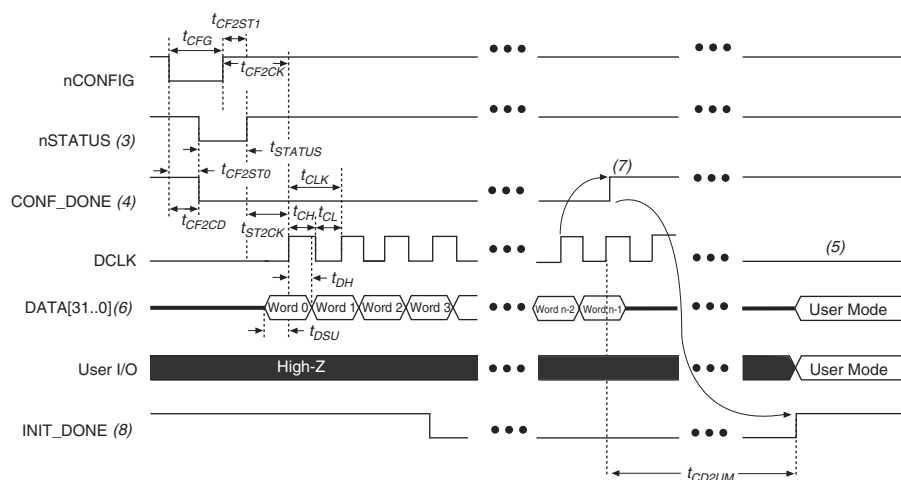
Table 47. Uncompressed .rbf Sizes for Stratix V Devices

| Family | Device | Package | Configuration .rbf Size (bits) | IOCSR .rbf Size (bits) ^{(4), (5)} |
|--------------|--------|------------------------------|--------------------------------|--|
| Stratix V GX | 5SGXA3 | H35, F40, F35 ⁽²⁾ | 213,798,880 | 562,392 |
| | | H29, F35 ⁽³⁾ | 137,598,880 | 564,504 |
| | 5SGXA4 | — | 213,798,880 | 563,672 |
| | 5SGXA5 | — | 269,979,008 | 562,392 |
| | 5SGXA7 | — | 269,979,008 | 562,392 |
| | 5SGXA9 | — | 342,742,976 | 700,888 |
| | 5SGXAB | — | 342,742,976 | 700,888 |
| | 5SGXB5 | — | 270,528,640 | 584,344 |
| | 5SGXB6 | — | 270,528,640 | 584,344 |
| | 5SGXB9 | — | 342,742,976 | 700,888 |
| | 5SGXBB | — | 342,742,976 | 700,888 |
| Stratix V GT | 5SGTC5 | — | 269,979,008 | 562,392 |
| | 5SGTC7 | — | 269,979,008 | 562,392 |
| Stratix V GS | 5SGSD3 | — | 137,598,880 | 564,504 |
| | 5SGSD4 | F1517 | 213,798,880 | 563,672 |
| | | — | 137,598,880 | 564,504 |
| | 5SGSD5 | — | 213,798,880 | 563,672 |
| | 5SGSD6 | — | 293,441,888 | 565,528 |
| | 5SGSD8 | — | 293,441,888 | 565,528 |

FPP Configuration Timing when DCLK-to-DATA [] = 1

Figure 12 shows the timing waveform for FPP configuration when using a MAX II or MAX V device as an external host. This waveform shows timing when the DCLK-to-DATA [] ratio is 1.

Figure 12. FPP Configuration Timing Waveform When the DCLK-to-DATA[] Ratio is 1 ^{(1), (2)}



Notes to Figure 12:

- (1) Use this timing waveform when the DCLK-to-DATA [] ratio is 1.
- (2) The beginning of this waveform shows the device in user mode. In user mode, nCONFIG, nSTATUS, and CONF_DONE are at logic-high levels. When nCONFIG is pulled low, a reconfiguration cycle begins.
- (3) After power-up, the Stratix V device holds nSTATUS low for the time of the POR delay.
- (4) After power-up, before and during configuration, CONF_DONE is low.
- (5) Do not leave DCLK floating after configuration. DCLK is ignored after configuration is complete. It can toggle high or low if required.
- (6) For FPP $\times 16$, use DATA [15..0]. For FPP $\times 8$, use DATA [7..0]. DATA [31..0] are available as a user I/O pin after configuration. The state of this pin depends on the dual-purpose pin settings.
- (7) To ensure a successful configuration, send the entire configuration data to the Stratix V device. CONF_DONE is released high when the Stratix V device receives all the configuration data successfully. After CONF_DONE goes high, send two additional falling edges on DCLK to begin initialization and enter user mode.
- (8) After the option bit to enable the INIT_DONE pin is configured into the device, the INIT_DONE goes low.

Active Serial Configuration Timing

Table 52 lists the DCLK frequency specification in the AS configuration scheme.

Table 52. DCLK Frequency Specification in the AS Configuration Scheme ^{(1), (2)}

| Minimum | Typical | Maximum | Unit |
|---------|---------|---------|------|
| 5.3 | 7.9 | 12.5 | MHz |
| 10.6 | 15.7 | 25.0 | MHz |
| 21.3 | 31.4 | 50.0 | MHz |
| 42.6 | 62.9 | 100.0 | MHz |

Notes to Table 52:

- (1) This applies to the DCLK frequency specification when using the internal oscillator as the configuration clock source.
- (2) The AS multi-device configuration scheme does not support DCLK frequency of 100 MHz.

Figure 14 shows the single-device configuration setup for an AS ×1 mode.

Figure 14. AS Configuration Timing



Notes to Figure 14:

- (1) If you are using AS ×4 mode, this signal represents the AS_DATA [3 : 0] and EPCQ sends in 4-bits of data for each DCLK cycle.
- (2) The initialization clock can be from internal oscillator or CLKUSR pin.
- (3) After the option bit to enable the INIT_DONE pin is configured into the device, the INIT_DONE goes low.

Table 53 lists the timing parameters for AS ×1 and AS ×4 configurations in Stratix V devices.

Table 53. AS Timing Parameters for AS ×1 and AS ×4 Configurations in Stratix V Devices ^{(1), (2)} (Part 1 of 2)

| Symbol | Parameter | Minimum | Maximum | Units |
|-----------------|---|---------|---------|-------|
| t _{CO} | DCLK falling edge to AS_DATA0/ASDO output | — | 2 | ns |
| t _{SU} | Data setup time before falling edge on DCLK | 1.5 | — | ns |
| t _H | Data hold time after falling edge on DCLK | 0 | — | ns |

Table 53. AS Timing Parameters for AS ×1 and AS ×4 Configurations in Stratix V Devices ^{(1), (2)} (Part 2 of 2)

| Symbol | Parameter | Minimum | Maximum | Units |
|--------------|---|--|---------|-------|
| t_{CD2UM} | CONF_DONE high to user mode ⁽³⁾ | 175 | 437 | μs |
| t_{CD2CU} | CONF_DONE high to CLKUSR enabled | 4 × maximum DCLK period | — | — |
| t_{CD2UMC} | CONF_DONE high to user mode with CLKUSR option on | $t_{CD2CU} + (8576 \times \text{CLKUSR period})$ | — | — |

Notes to Table 53:

- (1) The minimum and maximum numbers apply only if you choose the internal oscillator as the clock source for initializing the device.
- (2) t_{CF2CD} , t_{CF2ST0} , t_{CFG} , t_{STATUS} , and t_{CF2ST1} timing parameters are identical to the timing parameters for PS mode listed in Table 54 on page 63.
- (3) To enable the CLKUSR pin as the initialization clock source and to obtain the maximum frequency specification on this pin, refer to the Initialization section of the “Configuration, Design Security, and Remote System Upgrades in Stratix V Devices” chapter.

Passive Serial Configuration Timing

Figure 15 shows the timing waveform for a passive serial (PS) configuration when using a MAX II device, MAX V device, or microprocessor as an external host.

Figure 15. PS Configuration Timing Waveform ⁽¹⁾**Notes to Figure 15:**

- (1) The beginning of this waveform shows the device in user mode. In user mode, nCONFIG, nSTATUS, and CONF_DONE are at logic high levels. When nCONFIG is pulled low, a reconfiguration cycle begins.
- (2) After power-up, the Stratix V device holds nSTATUS low for the time of the POR delay.
- (3) After power-up, before and during configuration, CONF_DONE is low.
- (4) Do not leave DCLK floating after configuration. You can drive it high or low, whichever is more convenient.
- (5) DATA0 is available as a user I/O pin after configuration. The state of this pin depends on the dual-purpose pin settings in the **Device and Pins Option**.
- (6) To ensure a successful configuration, send the entire configuration data to the Stratix V device. CONF_DONE is released high after the Stratix V device receives all the configuration data successfully. After CONF_DONE goes high, send two additional falling edges on DCLK to begin initialization and enter user mode.
- (7) After the option bit to enable the INIT_DONE pin is configured into the device, the INIT_DONE goes low.

Remote System Upgrades

Table 56 lists the timing parameter specifications for the remote system upgrade circuitry.

Table 56. Remote System Upgrade Circuitry Timing Specifications

| Parameter | Minimum | Maximum | Unit |
|--------------------------|---------|---------|------|
| $t_{RU_nCONFIG}^{(1)}$ | 250 | — | ns |
| $t_{RU_nRSTIMER}^{(2)}$ | 250 | — | ns |

Notes to Table 56:

- (1) This is equivalent to strobing the reconfiguration input of the ALTREMOTE_UPDATE megafunction high for the minimum timing specification. For more information, refer to the Remote System Upgrade State Machine section of the “Configuration, Design Security, and Remote System Upgrades in Stratix V Devices” chapter.
- (2) This is equivalent to strobing the reset_timer input of the ALTREMOTE_UPDATE megafunction high for the minimum timing specification. For more information, refer to the User Watchdog Timer section of the “Configuration, Design Security, and Remote System Upgrades in Stratix V Devices” chapter.

User Watchdog Internal Circuitry Timing Specification

Table 57 lists the operating range of the 12.5-MHz internal oscillator.

Table 57. 12.5-MHz Internal Oscillator Specifications

| Minimum | Typical | Maximum | Units |
|---------|---------|---------|-------|
| 5.3 | 7.9 | 12.5 | MHz |

I/O Timing

Altera offers two ways to determine I/O timing—the Excel-based I/O Timing and the Quartus II Timing Analyzer.

Excel-based I/O timing provides pin timing performance for each device density and speed grade. The data is typically used prior to designing the FPGA to get an estimate of the timing budget as part of the link timing analysis. The Quartus II Timing Analyzer provides a more accurate and precise I/O timing data based on the specifics of the design after you complete place-and-route.



You can download the Excel-based I/O Timing spreadsheet from the Stratix V Devices Documentation web page.

Programmable IOE Delay

Table 58 lists the Stratix V IOE programmable delay settings.

Table 58. IOE Programmable Delay for Stratix V Devices (Part 1 of 2)

| Parameter (1) | Available Settings | Min Offset (2) | Fast Model | | Slow Model | | | | | | | |
|------------------|-----------------------|----------------------|------------|------------|------------|-------|-------|-------|-------|-------------|-------|------|
| | | | Industrial | Commercial | C1 | C2 | C3 | C4 | I2 | I3, I3YY | I4 | Unit |
| D1 | 64 | 0 | 0.464 | 0.493 | 0.838 | 0.838 | 0.924 | 1.011 | 0.844 | 0.921 | 1.006 | ns |
| D2 | 32 | 0 | 0.230 | 0.244 | 0.415 | 0.415 | 0.459 | 0.503 | 0.417 | 0.456 | 0.500 | ns |

Table 58. IOE Programmable Delay for Stratix V Devices (Part 2 of 2)

| Parameter (1) | Available Settings | Min Offset (2) | Fast Model | | Slow Model | | | | | | | |
|------------------|-----------------------|----------------------|------------|------------|------------|-------|-------|-------|-------|-------------|-------|------|
| | | | Industrial | Commercial | C1 | C2 | C3 | C4 | I2 | I3, I3YY | I4 | Unit |
| D3 | 8 | 0 | 1.587 | 1.699 | 2.793 | 2.793 | 2.992 | 3.192 | 2.811 | 3.047 | 3.257 | ns |
| D4 | 64 | 0 | 0.464 | 0.492 | 0.838 | 0.838 | 0.924 | 1.011 | 0.843 | 0.920 | 1.006 | ns |
| D5 | 64 | 0 | 0.464 | 0.493 | 0.838 | 0.838 | 0.924 | 1.011 | 0.844 | 0.921 | 1.006 | ns |
| D6 | 32 | 0 | 0.229 | 0.244 | 0.415 | 0.415 | 0.458 | 0.503 | 0.418 | 0.456 | 0.499 | ns |

Notes to Table 58:

- (1) You can set this value in the Quartus II software by selecting **D1**, **D2**, **D3**, **D5**, and **D6** in the **Assignment Name** column of **Assignment Editor**.
- (2) Minimum offset does not include the intrinsic delay.

Programmable Output Buffer Delay

Table 59 lists the delay chain settings that control the rising and falling edge delays of the output buffer. The default delay is 0 ps.

Table 59. Programmable Output Buffer Delay for Stratix V Devices (1)

| Symbol | Parameter | Typical | Unit |
|---------------------|----------------------------------|-------------|------|
| D _{OUTBUF} | Rising and/or falling edge delay | 0 (default) | ps |
| | | 25 | ps |
| | | 50 | ps |
| | | 75 | ps |

Note to Table 59:

- (1) You can set the programmable output buffer delay in the Quartus II software by setting the **Output Buffer Delay Control** assignment to either positive, negative, or both edges, with the specific values stated here (in ps) for the **Output Buffer Delay** assignment.

Glossary

Table 60 lists the glossary for this chapter.

Table 60. Glossary (Part 1 of 4)

| Letter | Subject | Definitions |
|--------|----------------------|---|
| A | — | — |
| B | | |
| C | | |
| D | — | — |
| E | — | — |
| F | f _{HCLK} | Left and right PLL input clock frequency. |
| | f _{HSDR} | High-speed I/O block—Maximum and minimum LVDS data transfer rate (f _{HSDR} = 1/TUI), non-DPA. |
| | f _{HSDRDPA} | High-speed I/O block—Maximum and minimum LVDS data transfer rate (f _{HSDRDPA} = 1/TUI), DPA. |

